Hardware-Aware Energy Efficiency Optimization in Wireless Communications Using a Gearbox-PHY

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***Abstract*— Current wireless networks prioritize spectral efficiency, however, energy efficiency has become crucial due to environmental, monetary, and device design considerations. The recently proposed Gearbox physical layer (PHY) approach dynamically switches between modulation schemes including corresponding transceiver front ends to optimize energy efficiency considering spectral availability and required data rates. The contribution of this work is the prediction of the energy-saving potential of a Gearbox-PHY with flexible front ends for linear amplitude modulation considering the power consumption of the analog front end, variable bandwidth usage, and transmission with sleep phases. Our results indicate that a Gearbox-PHY promises significant energy savings.**

***Index Terms*— Adaptive physical layer, wireless networks, hardware power consumption.**

I. Introduction

CURRENT cellular networks cover an extensive range of services with divergent requirements, spanning from rate-intensive high-resolution video streaming to low-rate communications, as seen in 4G narrowband Internet of Things (IoT) or 5G sensor communications. Despite this diversity, a common analog front end with limited configurability is employed across these applications, leading to suboptimal energy efficiency. While adaptive modulation and coding can increase energy efficiency by reducing transmit power [1], it solely changes the digital domain, leaving the shared analog radio front end untouched. However, considering the wide range of requirements for the radio front end, even in the same frequency range, the approach of a single front end that fits all services poses significant challenges in optimizing the power consumption. Nonetheless, despite these challenges, wireless network design has been predominantly centered on elevating the spectral efficiency and peak data rate, as seen in 5G specifications and ongoing 6G discussions.

The Gearbox-Physical Layer (Gearbox-PHY) concept [2] addresses the limitations of using a single analog front end by dynamically switching between multiple modulation schemes and corresponding parallel analog front ends, referred to as gears, while turning off unused front end components. This allows to supply the user with the required data rate and to maximize energy efficiency.

For instance, in cases involving low data rates and ample spectral availability, impulse radio-based transmission [3] promises a higher energy efficiency compared to conventional orthogonal frequency division multiplexing (OFDM) schemes with quadrature amplitude modulation (QAM), albeit the latter excels in delivering high data rates with high spectral efficiencies. Especially with the inclusion of the sub-THz band in cellular networks, spectrum availability may no longer be critical, enabling a shift from spectral to energy efficiency.

Implementing a Gearbox-PHY introduces the need for parallel hardware and additional control plane efforts to orchestrate the switching between gears, leading to increased manufacturing and development costs. However, similar to the approach of accepting increased silicon area for enhanced energy efficiency in CMOS digital circuits [4], a Gearbox-PHY accepts additional hardware and increased bandwidth for improved energy efficiency in wireless communications.

Assessing the balance between increased energy efficiency and added hardware expenses is vital. In this regard, this study aims to estimate the potential energy efficiency gains achievable with a Gearbox-PHY, a problem not previously considered as the concept has only emerged recently [2]. As such, this study represents a first attempt to assess its potential based on linear amplitude modulation. While the concept is not restricted to linear modulation schemes, this work aims to establish a conservative baseline. For this purpose, we compare data transmission in a point-to-point single-input single-output (SISO) system between a flexible Gearbox-PHY architecture, capable of switching between different gears, and a standard static single-gear architecture. Our evaluation focuses on linear amplitude modulation and takes into account lower bounds on the hardware power consumption, variable bandwidth usage, and the ability to transmit with sleep phases, i.e., operating in a duty-cycled mode. This holistic and general approach goes beyond existing works. Regarding the hardware power consumption, we consider the digital-to-analog converter (DAC), the power amplifier (PA), the low noise amplifier (LNA), the analog-to-digital converter (ADC), the mixers, and the local oscillators (LOs). Digital signal processing power consumption, which is reasonably assumed to be rate-dependent and approximately identical for all gears [5], is not considered here.

A similar analysis, although with a different scope and different modeling assumptions, was performed in [5], where

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the energy per bit is minimized for a given minimum target area spectral efficiency, i.e., $\mathrm{bit/s/Hz/m^2}$, while optimizing over hardware parameters like the ADC resolution and the PA backoff. In contrast, our approach maintains a fixed data rate, as opposed to a fixed spectral efficiency, enabling us to optimize energy efficiency over bandwidth usage, aligning with the Gearbox-PHY concept. Another relevant analysis in this area is presented in [6], where the optimal number of ADC bits for multi-antenna systems is covered.

This letter is structured as follows. In Section II, we formulate the optimization problem used to minimize the energy consumption, while models describing the hardware energy consumption are subsequently described in Section III. Afterwards, the solution of the optimization problem is discussed in Section IV, leading to concluding remarks in Section V.

II. Optimization Problem

To estimate the possible energy savings of a Gearbox-PHY, we consider a communications scenario, where a fixed amount of data Q needs to be transmitted within a maximum time $T_{\max}$ in a point-to-point SISO scenario. This implicitly defines the effective rate of transmission $R_{\text{eff}} = Q/T_{\max}$. We also consider the possibility of a transmission with an actual transmit time T smaller than $T_{\max}$ and, thus, a duty-cycled mode of operation, leading to the relative transmission time $\gamma = T/T_{\max} \leq 1$. To estimate the energy consumption we consider the power consumption of the hardware in the radio front end consisting of DAC, mixers, LOs, PA, LNA, and ADC. As we want to compare different gears with corresponding radio front ends, we do not consider the power consumption of the digital hardware, e.g., the power consumption due to channel decoding, as it is mainly dependent on the data rate, which is a given quantity in our setting, and the channel conditions [5]. As in practical systems, the transmit power P_{T} is subject to a maximum transmit power constraint, i.e., $P_{\mathrm{T}} \leq P_{\max}$.

Regarding the duty-cycled mode of operation, after the data transmission is completed the transmitter enters a sleep mode, while the receiver switches to an idle mode as it has to continuously monitor for incoming data. In these modes, their energy consumption reduces to a fraction of the values observed during transmission, specifically denoted as ϵ_{Tx} for the transmitter and ϵ_{Rx} for the receiver, where $\epsilon_{\mathrm{Rx}} \gg \epsilon_{\mathrm{Tx}}$. This enables to understand if it is preferable to use the entire transmission time $T_{\max}$ or alternatively to reduce the transmission time T while requiring higher spectral efficiencies or a larger bandwidth. We further assume the transmission to be performed in a band with carrier frequency f_c. We constrain the usable bandwidth B to a fraction η of the carrier frequency. Overall, the optimization problem can be formally stated as

$$\min_{B,\gamma,P_{\mathrm{T}},\text{gear}} \mathcal{E}_{\text{bit}} = \frac{(\gamma + \epsilon_{\mathrm{Tx}}(1-\gamma))P_{\mathrm{Tx}} + (\gamma + \epsilon_{\mathrm{Rx}}(1-\gamma))P_{\mathrm{Rx}}}{R_{\text{eff}}} \tag{1a}$$

$$\text{s. t.} \quad R_{\text{eff}} = \gamma\, B\, S \tag{1b}$$

$$0 \leq P_{\mathrm{T}} \leq P_{\max} \tag{1c}$$

$$0 \leq T \leq T_{\max} \tag{1d}$$

$$0 \leq B \leq \eta f_c, \tag{1e}$$

where $\mathcal{E}_{\text{bit}}$ denotes the energy consumed per communicated bit, P_{Tx} and P_{Rx} are the power consumption during transmission of the transmitter and the receiver, respectively, and S denotes the spectral efficiency. Note that the minimization in (1) also governs the gear switching by choosing the gear that minimizes the energy consumption. In the following section, each gear is modeled to have a distinct hardware power consumption, i.e., P_{Tx} and P_{Rx}, and spectral efficiency.

III. System Model

A. Hardware Power Consumption

Distinct modulation schemes, each capable of achieving different spectral efficiencies, exhibit unique hardware requirements resulting in different hardware power consumptions. For instance, single carrier 1024-QAM requires high resolution ADCs to enable the detection of all symbols, while quadrature phase shift keying (QPSK) can work with low resolution ADCs. However, the modulation scheme not only governs the requirements on the ADC but also on the PA due to different peak-to-average power ratios (PAPR) and different linearity requirements. While the modulation scheme heavily influences the ADC and the PA, a comprehensive estimate of the energy consumption requires the evaluation of the power consumption of all major components in the radio front end.

1) Analog-to-Digital Converter: To assess the hardware power consumption of the ADCs, we utilize the survey [7] evaluating the Walden figure-of-merit (FOM) [8] given as

$$FOM_{\mathrm{W}} = \frac{P_{\mathrm{ADC}}}{f_{\mathrm{s}} 2^{ENOB}}, \tag{2}$$

where $ENOB$ describes the amplitude resolution in terms of the effective number of bits and f_{s} is the sampling frequency. The FOM_{W} is given in units of Joules per conversion step, where one conversion step refers to one threshold comparison.

We approximate the effective number of bits $ENOB$ by the nominal number of bits b_{ADC}, i.e., the number of ADC output leads. Moreover, we assume Nyquist rate sampling, i.e., we assume the sampling frequency f_{s} to correspond to the double-sided bandwidth B. The survey [7] gives an *envelope*, i.e., an empirically found approximate lower bound, for the FOM_{W} as

$$FOM_{\mathrm{W}} \geq 0.67 \cdot 10^{-15} \sqrt{1 + \left(\frac{B}{560\,\mathrm{MHz}}\right)^2}\ \mathrm{J/conv\text{-}step}. \tag{3}$$

Using (2), (3), $B = f_s$, and $ENOB \approx b_{\mathrm{ADC}}$, we get the following pessimistic lower bound on the ADC power consumption

$$P_{\mathrm{ADC}} \gtrapprox 0.67 \cdot 10^{-15}\mathrm{Ws}\ 2^{b_{\mathrm{ADC}}} B \sqrt{1 + \left(\frac{B}{f_b}\right)^2}, \tag{4}$$

with $f_b = 560\,\mathrm{MHz}$. As we assume a complex baseband transmission, both the in-phase and quadrature components require one ADC, resulting in a total of two ADCs.

2) Power Amplifier: Models for PAs usually lack generic equations for the power consumption due to its dependency on the specific implementation and technology. Hence, we refer to the PA survey [9] to find an empirical lower bound on the PA power consumption P_{PA}. An important metric for PAs is the power added efficiency (PAE) defined as

$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{PA}}}, \tag{5}$$

where P_{in} represents the PA's input signal power, P_{out} denotes its output signal power, and P_{PA} is the power consumed by the

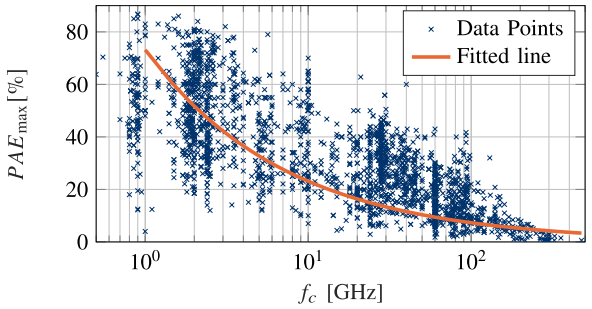


Fig. 1. Maximum PAE over carrier frequency f_c of PAs listed in [9]. Fit: $PAE_{\max} = 0.732\,(f_c/(1\,\text{GHz}))^{-0.5}$.

PA. The maximum PAE for various architectures and carrier frequencies f_c is covered in [9]. To find a relation between the PAE and the carrier frequency, we plot the maximum PAE $PAE_{\max}$ over the carrier frequency in Fig. 1 together with a fitted non-negative function obtained via linear regression with L1-regularization to enforce a *simple* fit.

Due to its specific PAPR and linearity requirements, every modulation scheme requires a specific backoff from the point of maximum efficiency of the PA to limit distortions due to PA non-linearity. However, to establish a lower bound on the PA power consumption we assume the PA to operate at the point of maximum efficiency, i.e., we assume the PAPR to be 1.

Since the output power of the PA P_{out} is generally much larger than the input power P_{in} and as we assume the output power of the PA to be equal to the transmit power, i.e., $P_{\text{out}} \approx P_{\text{T}}$, we lower-bound the PA power consumption as

$$P_{\text{PA}} \approx \frac{P_{\text{T}}}{PAE} \geq \frac{P_{\text{T}}}{PAE_{\max}}. \tag{6}$$

Using the fit in Fig. 1 and (6), we arrive at the following approximation for a lower bound on the PA power consumption

$$P_{\text{PA}} \gtrapprox 4.32 \cdot 10^{-5}\text{Hz}^{-0.5} P_{\text{T}} \sqrt{f_c}. \tag{7}$$

3) Low Noise Amplifier: For the LNA, which amplifies the receive signal, we assume that the gain is reasonably high and that the effects of non-linear distortions are negligible. As such, we model the power consumption of the LNA as in [5] using a bandwidth dependent FOM, i.e.,

$$FOM_{\text{LNA}} = \frac{G_{\text{LNA}} B N_0}{(N_{\text{LNA}} - 1) P_{\text{LNA}}}, \tag{8}$$

where G_{LNA} is the LNA gain, N_{LNA} is the LNA noise figure, N_0 is the noise power spectral density, and P_{LNA} is the power consumed by the LNA.

4) Digital-to-Analog Converter: When assuming a binary-weighted current-steering DAC, an approximation for the DAC power consumption, also used in [10], is given in [11] as

$$P_{\text{DAC}} = \underbrace{1.5 \cdot 10^{-5} (2^{b_{\text{DAC}}} - 1)\,\text{W}}_{\text{static}} + \underbrace{9 \cdot 10^{-12} b_{\text{DAC}} B\,\text{Ws}}_{\text{dynamic}}, \tag{9}$$

where b_{DAC} is the number of DAC input bits. One DAC each is required for the in-phase and quadrature components.

5) Up- and Down-Conversion: For up- and down-conversion an LO and a mixer are required at the transmitter and the receiver. For the mixer we focus on active CMOS implementations, which are covered in [12]. The LO is assumed to consist of a core oscillator, an I/Q-generator and a driver amplifier. As there are no general expressions for the power consumption of the mixer and the LO in the literature, we model these components based on measurements found in the available literature summarized in the following table.

f_c	2.4 GHz	28 GHz	60 GHz
P_{Mix}	1.57 mW [13]	8.4 mW [14]	17 mW[15]
P_{LO}	6 mW [16]	26.9 mW [17]	60 mW [18]

6) Hardware Power Model: Combining the power consumption of all considered hardware components leads to the following expressions for the hardware power consumption at the transmitter P_{Tx} and the receiver P_{Rx} for the optimization in (1)

$$P_{\text{Tx}} = 2P_{\text{DAC}} + P_{\text{LO}} + P_{\text{Mix}} + P_{\text{PA}} \tag{10a}$$

$$P_{\text{Rx}} = P_{\text{LNA}} + P_{\text{LO}} + P_{\text{Mix}} + 2P_{\text{ADC}}. \tag{10b}$$

B. Spectral Efficiency

To link the spectral efficiency to the hardware power consumption, we express the spectral efficiency of linear modulation schemes based on the ADC resolution b_{ADC}, as high spectral efficiencies require a high ADC resolution. Thus, b_{ADC} represents the modulation scheme, also referred to as gear.

The impact of the ADC resolution on the spectral efficiency is modeled as quantization noise. Further, as we are considering non-ideal components, the receiver increases the noise level by a noise factor F. With the Shannon-Hartley theorem considering an additive white Gaussian noise (AWGN) channel the achievable spectral efficiency is, thus, approximated as

$$S \approx \log_2\left(1 + \frac{P_{\text{R}}}{F N_0 B + \sigma_q^2}\right), \tag{11}$$

where P_{R} is the average receive power and σ_q^2 is the variance of the quantization noise.

Regarding the quantization, we consider uniform scalar mid-rise quantizers for the in-phase and quadrature components of the signal. For tractable evaluations the quantization noise and the ADC input signal need to be independent, which is the case for dithered quantizers if their input signal does not exceed their dynamic range and if they have a triangularly distributed dither [19]. For the in-phase and quadrature components the quantization noise can be modeled as white noise with variance $\sigma_q^2/2 = \Delta^2/4$ and quantization step size $\Delta = 2\phi/2^{b_{\text{ADC}}}$ [19], where ϕ is the one-sided dynamic range and b_{ADC} is the resolution for each ADC. Moreover, we choose the one-sided dynamic range ϕ of each ADC to be equal to a multiple κ of the variance of its input signal, i.e., $\phi = \sqrt{\kappa(P_{\text{R}} + F N_0 B)/2}$. For Nyquist rate sampling and a complex baseband transmission, the highest possible spectral efficiency for ADCs with b_{ADC} output bits each for the in-phase and quadrature components is $2b_{\text{ADC}}\,\text{bit/s/Hz}$. Thus, the expression for the spectral efficiency in (11) can be refined by choosing κ such that (11) saturates at $2b_{\text{ADC}}\,\text{bit/s/Hz}$, which implies $\kappa = \frac{1}{1-2^{-2b_{\text{ADC}}}} \approx 1$. This yields an ADC dynamic range of roughly one standard deviation of the input signal. As such we do not meet the condition of a negligible overload probability, thus not fulfilling the initial assumptions. However, compared to the achievable spectral efficiency of QAM in combination with hard demapping, as an example for a spectrally efficient linear amplitude modulation, the relative mismatch of (11)

is lower than 7% for $b_{\mathrm{ADC}} \geq 3$ (not shown here), which is sufficient considering the approximations and estimations made regarding the hardware power consumption.

Moreover, due to the saturation of the spectral efficiency at $2b_{\mathrm{ADC}}$ bit/s/Hz, it is not meaningful to consider a DAC resolution smaller than b_{ADC}. Hence, we choose $b_{\mathrm{DAC}} = b_{\mathrm{ADC}} = b$.

With (11), $\kappa \approx 1$, and $b = b_{\mathrm{ADC}} = b_{\mathrm{DAC}} \geq 3$ the achievable spectral efficiency can be approximated as

$$S \approx \log_2\left(1 + \frac{2^{2b}}{FN_0B\frac{1}{P_{\mathrm{R}}}(2^{2b}+1)+1}\right). \tag{12}$$

C. Path Loss

It is important to consider the frequency-dependent path loss. Since statistical path loss models, e.g., the Okumura-Hata model [20], are limited in terms of the frequency ranges they cover, we employ the well-known standard path loss model

$$L = \frac{P_{\mathrm{T}}}{P_{\mathrm{R}}} = \frac{1}{D_{\mathrm{R}}D_{\mathrm{T}}}\left(\frac{4\pi d}{\lambda}\right)^{\beta}, \tag{13}$$

where d represents the distance between the transmitter and the receiver, $\beta > 0$ is the path loss exponent (usually $2 \leq \beta \leq 4$ for outdoor environments), $\lambda = \frac{c}{f_c}$ denotes the wavelength with the speed of light c, and D_{T} and D_{R} represent the antenna gains of the transmit and the receive antenna, respectively.

IV. System Parameter Optimization

By substituting (13) into (12), the transmit power is given as

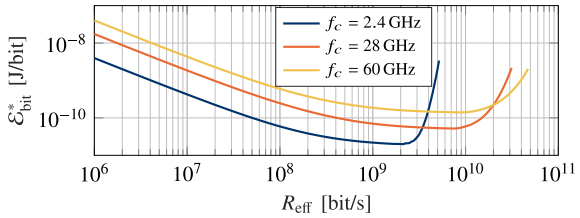
$$P_{\mathrm{T}} \approx \frac{FN_0BL(2^{2b}+1)(2^S-1)}{2^{2b}-2^S+1}. \tag{14}$$

Utilizing (14) and (1b) necessitates $\gamma B > R_{\mathrm{eff}}/\log_2(2^{2b}+1)$ to ensure $P_{\mathrm{T}} \geq 0$. Due to (14), the transmit power P_{T} is no longer an optimization parameter. Further, as the *gear* is represented by the ADC and DAC resolution b, (1a) reduces to

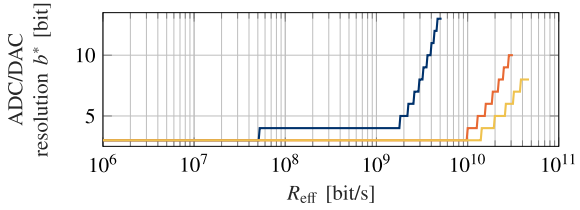
$$\min_{B,\gamma,b} \mathcal{E}_{\mathrm{bit}} = \frac{(\gamma+\epsilon_{\mathrm{Tx}}(1-\gamma))P_{\mathrm{Tx}}+(\gamma+\epsilon_{\mathrm{Rx}}(1-\gamma))P_{\mathrm{Rx}}}{R_{\mathrm{eff}}}. \tag{15}$$

Note that in our model all hardware components exhibit a direct or indirect dependence on the bandwidth B with the exception of the LO, the mixer, and the static part of the DAC. By switching between different gears, the Gearbox-PHY essentially increases energy efficiency at the price of increased bandwidth. Consequently, the optimization over the bandwidth B significantly impacts the power consumption of the DAC, the PA, the LNA, and the ADC, while the LO and the mixer are only affected by the optimization over the duty cycle γ.

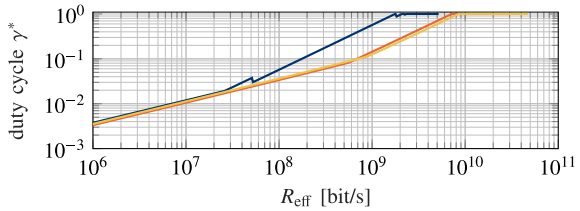
As there is no analytical solution of the optimization problem in (15) with the constraints (1b)-(1e), we resort to numerical optimization. To compare the energy-saving potential of a Gearbox-PHY, i.e., switching between different modulation schemes and radio front ends, to the currently implemented approach of utilizing a single highly spectral-efficient gear, we compare the result of the optimization over b, γ, and B with the results of optimizing over B and γ for a fixed $b = b_{\mathrm{fix}}$. Here we choose b_{fix} to align with the optimal ADC/DAC resolution at the highest rates deliverable for the considered system parameters and bands,



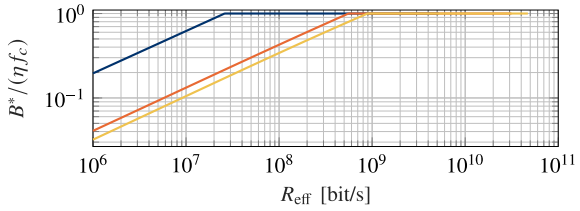
(a) Minimum energy per bit $\mathcal{E}^*_{\mathrm{bit}}$



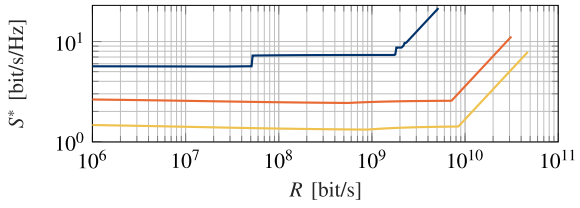
(b) Optimal number of ADC/DAC bits per I/Q component b^*



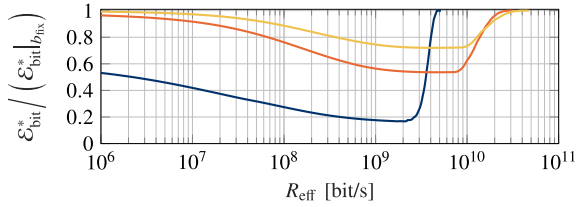
(c) Optimal duty cycle γ^*



(d) Optimal bandwidth B relative to available bandwidth ηf_c



(e) Optimal spectral efficiency S^*



(f) Minimum energy of Gearbox-PHY relative to single-gear approach

Fig. 2. Solution of (15) with (1b)-(1e) compared to conventional system and corresponding ADC resolution b^*, duty cycle γ^*, system bandwidth B^*, and spectral efficiency S^*; for the single-gear approach in (f): $b_{\mathrm{fix}} = 13$ bit for $f_c = 2.4$ GHz, $b_{\mathrm{fix}} = 10$ bit for $f_c = 28$ GHz, and $b_{\mathrm{fix}} = 8$ bit for $f_c = 60$ GHz; path loss exponent $\beta = 2$, distance $d = 20$ m, antenna gain $D_{\mathrm{R}} = D_{\mathrm{T}} = 6$ dB, maximum transmit power $P_{\max} = 10$ W, maximum relative bandwidth $\eta = 0.1$, Tx sleep factor $\epsilon_{\mathrm{Tx}} = 0.01$, Rx idle factor $\epsilon_{\mathrm{Rx}} = 0.5$, receiver noise factor $F = 10$, $G_{\mathrm{LNA}} = 15$ dB [21], $N_{\mathrm{LNA}} = 5$ dB [21], $FOM_{\mathrm{LNA}} = 10^{-7}$ [5].

i.e., we choose $b_{\text{fix}} = 13\,\text{bit}$ for $f_c = 2.4\,\text{GHz}$, $b_{\text{fix}} = 10\,\text{bit}$ for $f_c = 28\,\text{GHz}$, and $b_{\text{fix}} = 8\,\text{bit}$ for $f_c = 60\,\text{GHz}$. The relative bandwidth in current 5G-NR bands is typically around 5% but can also be above 10% (C-band). Thus, we choose $B/f_c \leq \eta = 0.1$ for the numerical results.

Fig. 2 shows the solution of (15) with (1b)-(1e), i.e., the minimum energy per bit $\mathcal{E}^*_{\text{bit}}$, as well as the optimal parameters, i.e., the optimal ADC and DAC resolution b^*, the optimal duty cycle γ^*, the optimal bandwidth B^* relative to the available bandwidth ηf_c, the resulting spectral efficiency S^*, and the energy consumption ratio of the Gearbox-PHY approach relative to a single-gear approach with a fixed ADC/DAC resolution b_{fix}. Note, the curves end at a certain R_{eff} due to the transmit power constraint $P_{\max}$, and the maximum deliverable data rate increases with higher carrier frequencies f_c as more bandwidth is available.

As expected, with increasing R_{eff} the ADC resolution b increases, where a change in b corresponds to a gear switch. Interestingly, the minimum energy per bit $\mathcal{E}^*_{\text{bit}}$ is not a monotonically increasing function of R_{eff}, as the hardware components with constant power consumption dominate the overall power consumption at low rates and their power consumption cannot be reduced with a low bandwidth B. Thus, as can be seen from Fig. 2c, for low data rate requirements it is beneficial to reduce the duty cycle γ as well. Fig. 2e depicts the resulting spectral efficiencies and emphasizes that high spectral efficiencies are only required for peak data rates or low spectral availability.

The relative energy consumption of a Gearbox-PHY approach compared to a conventional single-gear approach is displayed in Fig. 2f. For low rates the energy consumption is dominated by the components with constant power consumption, thus, the gains are smaller than for higher R_{eff}. When increasing the data rate R_{eff} to around $10^9\,\text{bit/s}$, the Gearbox-PHY approach offers the highest energy savings depending on the considered band. However, when moving to even higher data rates the system switches to higher ADC/DAC resolutions b to meet the increasing data rate demands until it reaches the b_{fix} of the single gear approach, not providing any energy efficiency gains. Note that the relative energy efficiency gains in Fig. 2f strongly depend on the b_{fix} used for comparison, which are different for the considered carrier frequencies f_c.

Although we consider Gaussian input distributions, we assume a PAPR of 1 for all gears, which underestimates the energy efficiency gains, particularly as modulation schemes with high spectral efficiency often exibit a high PAPR, degrading the PA efficiency. Additionally, by focusing solely on linear amplitude modulation, our approach excludes unconventional schemes like impulse radio, which promises high energy efficiency, especially at low data rates. However, optimizing a system with these modulation schemes does not allow for general expressions and, thus, makes it difficult to understand general relationships.

V. Conclusion

In the present study we evaluated the energy saving potential achieved by the hardware adaptivity of a Gearbox-PHY depending on data rate requirements and spectral availability. The evaluation is based on lower bounds and approximations of the DAC, the PA, the LNA, and the ADC power consumption, as well as literature-based measurement values for the LO and mixer. Our calculations indicate that significant energy savings are possible. Note that these findings provide a conservative estimate of the possible energy efficiency gains, as we consider linear modulation schemes and do not account for unconventional approaches like impulse radio, which may offer even higher energy efficiencies at low rates.

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