An Energy-Efficient Bridge-to-Digital Converter for Implantable Pressure Monitoring Systems

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***Abstract*—This paper presents an energy-efficient, duty-cycled, and spinning excitation bridge-to-digital converter (BDC) designed for implantable pressure sensing systems. The circuit provides the measure of the pulmonary artery pressure that is particularly relevant for the monitoring of heart failure and pulmonary hypertension patients. The BDC is made of a piezoresistive pressure sensor and a readout integrated circuit (IC) that comprises an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). The proposed design spins both the bridge excitation and the ADC's sampling input voltages simultaneously and exploits duty cycling to reduce the static power consumption of the bridge sensor and IA while cancelling the IA's offset and 1/f noise at the same time. The readout IC has been designed and fabricated in a standard 180-nm CMOS process and achieves 8.4 effective number of bits (ENOB) at 1 kHz sampling rate while drawing 0.53 μA current from a 1.2 V supply. The BDC, built with the readout IC and a differential pressure sensor having 5 kΩ bridge resistances, achieves 0.44 mmHg resolution in a 270 mmHg pressure range at 1 ms conversion time. The current consumption of the bridge sensor by employing duty cycling is reduced by 99.8% thus becoming 0.39 μA from a 1.2 V supply. The total conversion energy of the pressure sensing system is 1.1 nJ, and achieves a figure-of-merit (FoM) of 3.3 pJ/conversion, which both represent the state of the art.**

***Index Terms*—Bridge-to-digital converter (BDC), CCIA, energy-efficient, medical implantable device, offset compensation, pressure sensor, readout IC, SAR ADC.**

I. Introduction

HEART failure (HF) continues to be the leading cause of death, disability, and healthcare cost in the 21st century [1]–[3]. HF is a severe clinical syndrome that occurs when the heart is incapable to pump sufficient blood to meet the needs of the body [1]. It is estimated to affect more than 64 million individuals worldwide and would further increase due to ageing population [4]. The specific characteristic of HF is a high incidence of hospital admission and readmission. Notably, HF causes the highest rate of rehospitalization when compared with all other medical conditions [2]. In addition, pulmonary hypertension (PH) is a serious condition when there is abnormally high blood pressure in the arteries that supply the lungs. It has become an increasingly common global health issue and has a strong relation with HF secondary to left heart systolic and diastolic dysfunction. The PH prevalence is about 1% of the global population, and increases up to 10% in people older than 65 years [5]. Despite being relatively underestimated, PH is one of the major causes of disability worldwide [3]. HF and PH usually require extended and recurrent hospital stays. This situation significantly decreases the quality of life of millions of patients while resulting in a substantial economic burden to the patients and health care systems. Both cardiac diseases, HF and PH, are diagnosed by monitoring the patient's heart activity, particularly, the pulmonary arterial pressure (PAP).

Dealing with the pandemic of HF and PH requires accurate PAP monitoring. Noninvasive telemedical systems have failed to reduce hospitalization rates since they cannot accurately measure pressure [2]. Thus, implantable PAP monitoring systems have become the focus of tracking HF and PH patients. Implantable devices are receiving growing attention in several fields, including medical diagnostics, clinical therapy, and personal healthcare. Furthermore, they can provide accurate measurements and make remote monitoring of patients possible [6]. PH is defined by a mean PAP of 20 mmHg or more at rest [7], and direct measurement of this PAP with an implantable system is important to improve the pressure measurement accuracy. The continuous (24/7) and accurate monitoring of the heart activity is crucial to adapt treatments based on how patients react to the prescribed medicines and to decrease the repeated hospital admissions. A state-of-the-art implantable hemodynamic monitoring device is the CardioMEMS HF System [8]. By providing accurate PAP measurements during the CHAMPION trial, it showed a 37% reduction in the relative risk of HF hospitalizations and a significant improvement in the quality of life of HF patients [2]. CardioMEMS HF is a passive system consisting of a capacitive pressure sensor and an inductor. Pressure applied to the capacitive sensor leads to a characteristic shift in the

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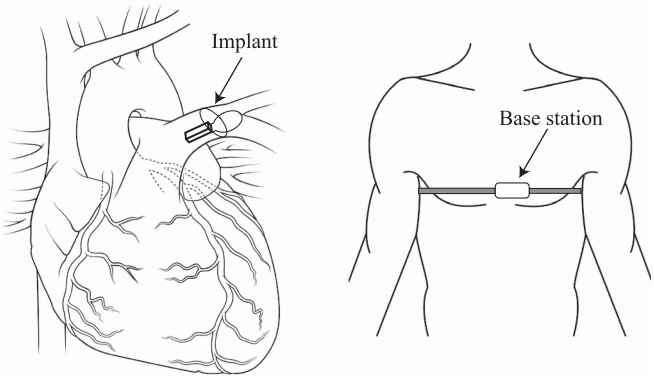

Fig. 1. (a) Conceptual view of a remotely powered deep implant placed in the pulmonary artery (PA) of HF patients for accurate and long-term PA pressure monitoring. (b) Conceptual view of the external base station for the wireless power and data transfer.

resonant frequency, and by applying electromagnetic signals from an external station, this data is transferred to the external base station.

An alternative method to monitor the pulmonary arterial pressure is the measure provided by an implantable active system. The PAP can be accurately measured by a remotely powered, deeply implanted device consisting of a pressure sensor and a readout integrated circuit (IC), which comprises a sensor interface and communication blocks. Fig. 1(a) reports the conceptual view of a deep implant placed in a branch of the pulmonary artery (PA). A solution for the wireless power transfer and data communication with the deep implant, places an external base station over the position of the unit implanted in the heart. Fig. 1(b) shows an example of a placement for the external base station. Implantable sensor nodes should have low power consumption and small size. Several pressure monitoring systems for implantable and wearable medical devices have been reported in the literature [9]–[13]. Miniaturized pressure sensors, implemented as micro-electromechanical systems (MEMS), use capacitive or resistive devices. Capacitive sensors grant low energy consumption and low temperature drift, however, they suffer from non-linearity of the output response [14]. Piezoresistive sensors configured in a Wheatstone bridge are an effective solution, and are widely used to measure pressure, temperature, and humidity, thanks to their small size and high accuracy [11]–[13], [15]–[18]. However, those sensors are power-hungry due to low bridge resistances.

Fig. 2 shows a conventional bridge sensor readout, known as the bridge-to-digital converter (BDC). It consists of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). In conventional BDCs, the top excitation voltage (V_{EXT}) of the bridge is connected to a DC biasing voltage while the bottom excitation (V_{EXB}) is grounded. In addition, the IA should have low noise, low offset, and low power consumption to accurately and energy-efficiently amplify the bridge sensor's output so as to utilize the full input range of the succeeding ADC. The bridge measurement can achieve

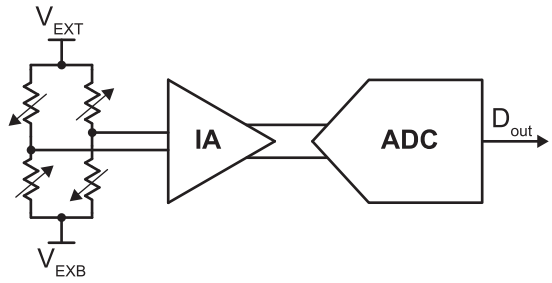

Fig. 2. Conventional bridge-to-digital converter (BDC).

high resolution and accuracy, but the bridge itself tends to be the most power-hungry block of the analog front-end. The excitation energy consumption of the bridge sensor is higher than the interface circuit's conversion energy because of low bridge resistances, thus limiting the full system's energy efficiency [17]. Recent works, such as [12], [15], [16], [18], have used duty cycling of the bridge in order to reduce its energy consumption.

Apart from the bridge sensor, a low-noise and low-power readout IC is required to achieve an energy-efficient BDC. Several techniques such as auto-zeroing, correlated double sampling, and chopping have been generally used for noise and offset cancellation [19]. The IA usually determines the energy efficiency of the readout circuit since the main noise contribution arises from its input stage. The input stage dominates the current consumption of the readout to achieve low noise. The chopper-stabilized capacitively-coupled IA (CCIA) delivers the best performance in accuracy and energy efficiency. Moreover, its input capacitors block common-mode (CM) input voltages, allowing to supply the bridge and the readout circuit at different voltage levels. However, the chopper stabilization generates a large ripple at the output; an additional circuitry such as a ripple reduction loop is needed to eliminate this drawback [20]. This solution, however, increases the energy consumption, chip area, and design complexity of the system.

This paper presents an energy-efficient BDC for implantable pressure sensing systems, specifically designed for PAP monitoring. The proposed technique applies duty cycling to the bridge sensor, while spinning its excitation voltage simultaneously. The sensor's excitation energy consumption is reduced by a factor of 640 times. This system avoids complex IAs that foresee offset-reduction techniques or need calibration. A novel spinning method applied to the bridge sensor and capacitive digital-to-analog converter (DAC) of the successive-approximation-register (SAR) ADC simultaneously suppresses the 1/f noise and offset. The IA is also duty-cycled to decrease its power consumption by a factor of 427 times. This novel architecture enables to achieve very low energy consumption in the bridge sensor and readout circuit at the same time and makes the bridge sensor suitable for implantable medical devices.

The organization of the paper is the following. Section II describes the working principle of the proposed duty-cycled and spinning excitation BDC, whereas the system and implementation details are presented in Section III. Section IV reports the experimental results and Section V provides the conclusion.

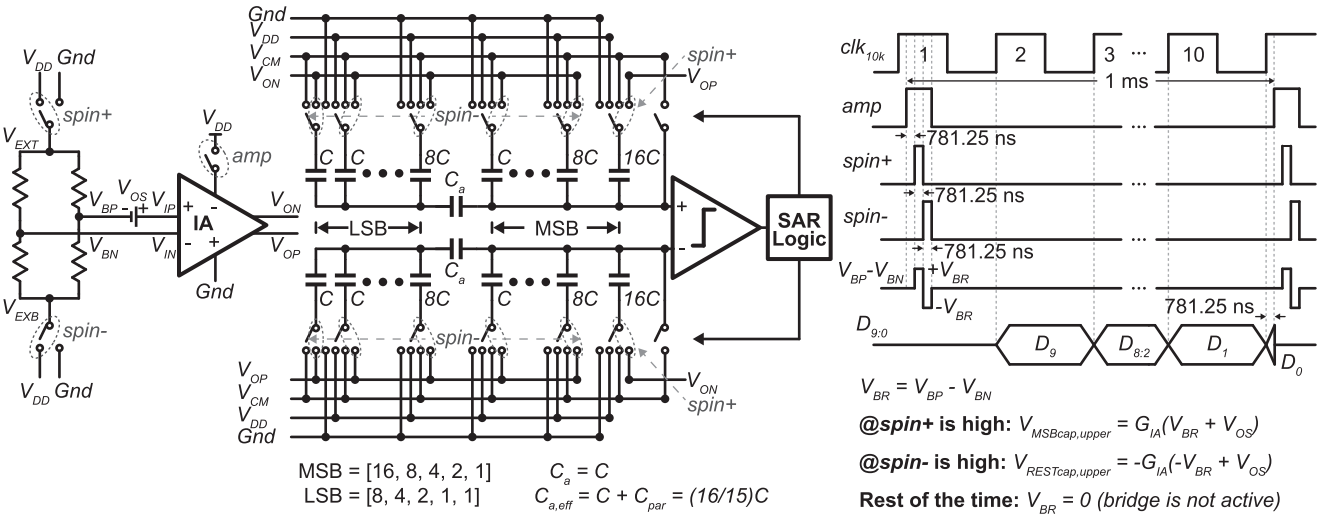

Fig. 3. Circuit diagram of the highly duty-cycled and spinning excitation BDC and its timing diagram.

II. Duty-Cycled and Spinning Excitation Bridge-to-Digital Converter (BDC)

The proposed BDC consists of a duty-cycled and spinning excitation bridge sensor, a duty-cycled IA, and a spinning SAR ADC. Fig. 3 shows the circuit diagram. The spinning and duty cycling operation uses switches controlled by amp, $spin+$, and $spin-$ signals. The switches controlled by $spin+$ and $spin-$ signals simultaneously spin both the bridge excitation ($V_{\rm EXT}$, $V_{\rm EXB}$) and the capacitive DAC's sampling inputs ($V_{\rm OP}$, $V_{\rm ON}$). These switches reverse the supply connections of the bridge so that during one phase, the bridge's output is $+V_{\rm BR}$, and during the other phase, the output is equal and opposite, $-V_{\rm BR}$. The duty-cycled IA is active when amp signal is high.

The excitation switches of the bridge sensor operate like the modulation switches of the chopping technique as they reverse the signal at the output. The IA amplifies the modulated signal and the low-frequency spurs made by the IA offset and the 1/f noise component. Indeed, the amplification of the IA offset ($V_{\rm OS}$) and the 1/f noise component also make the IA's output. Instead of using a demodulating chopper for cancelling the low-frequency spurs, the circuit implements the following scheme. During the first spin, half of the positive DAC array charges to $V_{\rm OP}$ while half of the negative DAC array charges to $V_{\rm ON}$. When the bridge excitation reverses, the second half of the positive DAC array charges to $V_{\rm ON}$, and the second half of the negative DAC array charges to $V_{\rm OP}$. The bridge is 640 times duty-cycled in 1 ms conversion time, and $spin+$ and $spin-$ are high for 781.25 ns. Since the time seperation of the two spinning phase is less than 800 ns and the estimated 1/f noise corner is 20 kHz, there is a strong correlation between 1/f noise components sampled on the two halves of the DAC array. As a result, the total charge on the capacitive DAC arrays depends only on the bridge signal and compensates for the 1/f noise and offset [21].

The method not only avoids a second chopper but also eliminates the offset contribution directly without the need of using a digital filter used to remove the spur components caused by the square wave modulation of the offset and the 1/f noise at the chopping frequency. The mismatch between the two halves of the capacitive arrays may lead to a residual offset. Still, this error is minimal if the circuit uses relatively large unity capacitors in the DAC array. It becomes negligible when it is less than the step resolved by the SAR ADC.

The timing diagram reported in Fig. 3 describes the working principle of this novel topology in detail. The bridge sensor and the IA are not active at the beginning of a conversion cycle. Then, the IA is powered up starting from the rising edge of the amp signal, 781.25 ns ahead of the activation of the bridge. After that, $spin+$ is high for 781.25 ns to connect the top excitation voltage ($V_{\rm EXT}$) of the bridge to $V_{\rm DD}$ while the bottom excitation voltage ($V_{\rm EXB}$) goes to ground for generating the bridge output $+V_{\rm BR}$. In order to avoid a short circuit in the bridge, the $spin+$ becomes low before $spin-$ rises, and then $spin-$ is high for another 781.25 ns for generating the bridge output $-V_{\rm BR}$. The bridge is active for only 1.5625 μs when $spin+$ or $spin-$ is high, and the IA is active for 2.3437 μs out of 1 ms conversion time when amp is high. Therefore, the energy consumptions of the bridge and the IA result respectively 640 and 427 times less than an equivalent static DC biasing.

When $spin+$ is high, the MSB capacitor ($16\,C$) of the DAC positive array is charged to $V_{\rm OP}$, while the DAC negative array's MSB capacitor ($16\,C$) is charged to $V_{\rm ON}$. All the other DAC capacitors remain floating during $spin+$ high. When $spin-$ is high, the remaining capacitors of the DAC positive array, which are equivalent to $16\,C$, are charged to $V_{\rm ON}$ while the MSB capacitor is floating. Similarly, $V_{\rm OP}$ charges the remaining capacitors of the DAC negative array, and the MSB capacitor is floating. As a result, the total charges in the positive and negative DAC arrays depend only on the two phases of the bridge signal ($+V_{\rm BR}$ and $-V_{\rm BR}$) [21]. The operation acts a correlated double sampling over the IA offset and compensates for it since the MSB capacitor and the remaining capacitors' array are equal.

III. System and Implementation Details

The proposed BDC requires low energy consumption to be remotely powered and a tiny volume to be implanted in the body. As depicted in Fig. 3, it consists of a piezoresistive pressure sensor, an IA, and a succeeding SAR ADC. The following sections provide detailed descriptions of the system design, IA, and SAR ADC.

A. System Design

Patients are considered at risk for HF hospitalization if their pressures are higher than 35 mmHg for systolic, 20 mmHg for diastolic, and 25 mmHg for mean PAP [2], and PH is defined by a mean PAP of 20 mmHg or more at rest [7]. So as to cover high-pressure limits, the pressure range of the system is selected to be from 0 to 135 mmHg. Since the atmospheric pressure decreases with increasing altitude, an additional margin in the negative pressure is also required. Thus, the overall pressure range with respect to the reference pressure (1 atm = 760 mmHg) is chosen to be from −135 to +135 mmHg, enabling calibration of the BDC with respect to the ambient pressure. For accurate PAP monitoring, the pressure resolution is higher than 0.5 mmHg. The system's bandwidth ranges from 0 to 450 Hz to precisely detect fast peaks of systolic and diastolic pressure changes.

Bridge sensors usually generate low-amplitude signals (millivolt range); a typical readout circuit uses an IA before the ADC. Highly duty-cycled bridge sensor requires higher bandwidth, thus increasing the power consumption of the IA. Lower duty cycle could decrease the IA's power dissipation, however, it would not be sufficient to keep the bridge's average power consumption lower than 1 μW. As a solution, the IA is also duty-cycled. The clock input frequency is 1.28 MHz and the highest possible duty cycle with the used clock is 1/640. The bandwidth and settling time requirements of the IA suggest a more prudent duty cycle of 1/427. Thus, the bridge sensor and the IA are duty-cycled by 640 and 427 times, respectively.

A circuit solution that allows an accurate amplification of the bridge sensor's output uses two IA stages, which are capacitively-coupled. The first stage ensures low-noise operation whereas a programmable capacitive feedback network defines the gain of the second stage for exploiting the ADC full input range. The variable gain also enables tuning of the IA input range for different bridge sensors and avoids the saturation of the output of the IA caused by the bridge offset. For ensuring a pressure resolution of at least 0.5 mmHg and a bandwidth of 450 Hz, the system uses a 10-bit SAR ADC with a sampling rate of 1 kilo-samples-per-second (kS/s). A spinning control logic generates the necessary control signals for the system. As shown in Fig. 4, it consists of a conventional D flip-flop-based clock divider and a set of shift registers. The clock input frequency is 1.28 MHz, and its value is because of a future wireless powering and communication by ultrasound, with the clock signal recovered from the acoustic waves. As Fig. 1 depicts, an external base station placed on the patient's skin transmits ultrasound signals at 1.28 MHz for wireless powering, communication, and clock generation. The logic block uses the 1.28 MHz input clock to generate amp, $spin+$, $spin-$, and two clock signals at 1 kHz and 10 kHz.

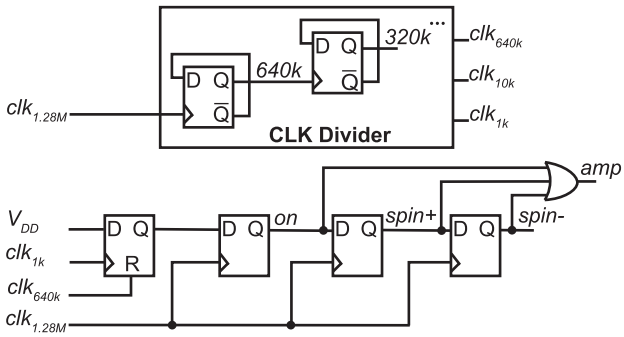

Fig. 4. Simplified circuit diagram of the spinning control logic.

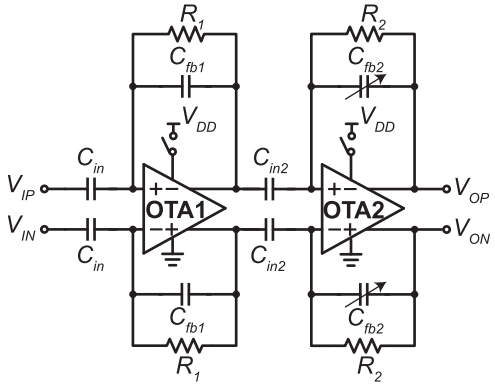

Fig. 5. Circuit diagram of the capacitively-coupled IA consisting of two gain stages.

B. Capacitively-Coupled Instrumentation Amplifier (CCIA)

As mentioned, a CCIA offers the best performance in terms of both accuracy and energy efficiency [20]. A programmable capacitive feedback network defines the gain of the CCIA within the gain range 29 V/V - 72 V/V, thus maximizing the dynamic range of the ADC. Fig. 5 shows the distribution of the gain along two stages to optimize the area and power consumption. A single-stage implementation would require larger capacitors and larger bandwidth. Since the bridge sensor is 640 times duty-cycled in a 1 ms conversion time and active only for 1.5625 μs, the bandwidth of the CCIA is about 1 MHz, properly handling the high-frequency input components. The high bandwidth of the IA imposes a large static current affecting the energy efficiency of the BDC. However, the 427 times duty cycling makes the circuit active only for 2.3437 μs in 1 ms conversion time.

The first stage amplifier is critical because of the stringent noise and power consumption request. As Fig. 5 shows, its mid-band gain depends on the capacitive ratio $C_{\rm in}/C_{\rm fb1}$: Its setting is 9 V/V. The used $C_{\rm in}$ is 1 pF, a relatively large value that decreases the input-referred noise and limits the error caused by parasitic terms. The value of R_1 needed for the input biasing of the operational amplifier must be high. Its implementation uses pseudo-resistances based on MOS transistors in

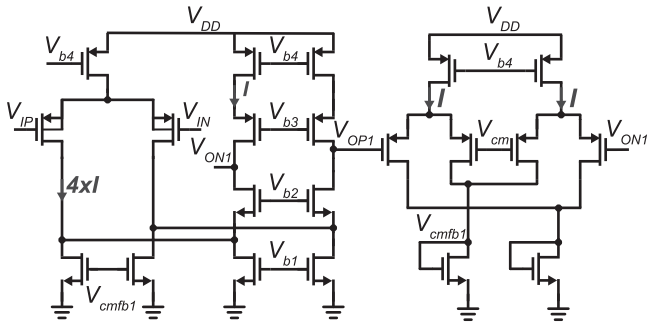

Fig. 6. Schematic of the folded-cascode amplifier (OTA1) with its CMFB circuit.

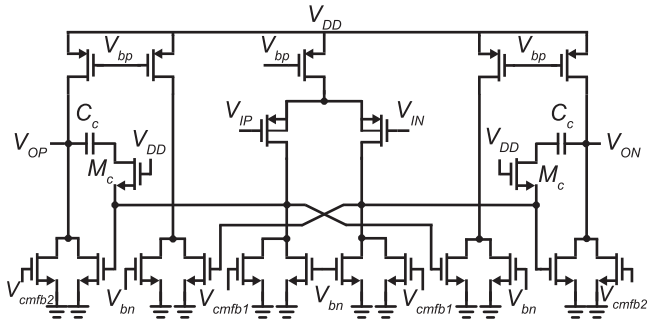

Fig. 7. Schematic of the two-stage Miller amplifier with class AB output stage (OTA2).

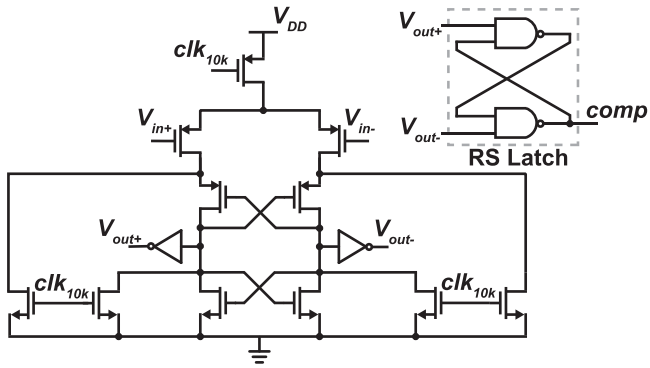

Fig. 8. Schematic of the StrongARM latch followed by an RS latch.

the sub-threshold region. They occupy a considerably smaller area than equivalent physical resistors. The high-gain OTA1 is a folded-cascode amplifier with a PMOS input pair biased in weak inversion. Fig. 6 shows the schematic of OTA1 including its CM feedback (CMFB) circuit. The CMFB circuit employs two differential pairs [22] to set the output CM voltage. The currents in the folded branches and CMFB circuit's branches are a factor of four smaller than the main current to improve the overall noise efficiency.

The gain of the second stage is variable to maximize the signal at the input of the ADC. The capacitive ratio $C_{\rm in2}/C_{\rm fb2}$ makes the gain of the second stage, depicted in Fig. 5. Two configuration bits set the feedback capacitors ($C_{\rm fb2}$) for the four gain settings 3.2, 4, 5.3, and 8 V/V. Like in the first stage, the stage uses relatively large feedback capacitors for high gain linearity and sets the DC biases of the stage with high-value pseudo-resistors (R_2). The OTA2 schematic, shown in Fig. 7, is a two-stage Miller OTA with a class AB output stage [23], a solution that ensures high linearity and high output swing. The circuit uses the Miller compensation made by the capacitor $C_{\rm c}$ and $M_{\rm c}$, which performs as a resistor. The output stage is an AB scheme that also increases the effective transconductance of the stage by using about half the current of a corresponding class A scheme [23]. OTA2 uses two separate CMFB circuits for setting the CM voltages of its first and second stages. The first stage uses an amplifier with two differential pairs [22] similar to OTA1, the second stage faces the large swing of the differential output with a resistive divider, and an amplifier [24]. Corner and Monte Carlo simulations verify that the CMFB circuits are stable in any conditions. The CMFB phase margin is at worst 46° for OTA1, and higher than 72° for both stages of OTA2. The supply voltage is 1.2 V, and the CM settings are 0.6 V to ensure a maximum signal amplitude.

C. SAR ADC

A 10-bit 1 kS/s SAR ADC digitizes the amplified signals (Fig. 3). A low-power dynamic comparator, capacitive DAC arrays, and a synchronous SAR control logic, consisting of a set of shift registers and bit registers [25], make the SAR ADC. The fully-differential architecture suppresses the supply noise and obtains a good CM noise rejection.

Fig. 8 shows the schematic of the StrongARM latch comparator followed by an RS latch [26]. The static offset of the comparator does not affect the linearity of the ADC. The comparator noise and kickback charge are the main design parameters. They should be lower than ADC's quantization error, which is 677 $\mu{\rm V}_{\rm rms}$ for the 10-bit differential mode SAR ADC having 1.2 V reference voltage. Post-layout transient noise simulations result in an input-referred noise variation $\sigma_{n,in} =$ 145 $\mu{\rm V}_{\rm rms}$. Both the $3\sigma_{n,in}$ and kickback noise are lower than the quantization error.

The capacitive DAC array adopts the ${\rm V}_{\rm CM}$-based switching technique to decrease the switching power [25]. In addition, the use of the split capacitor method employing an attenuation capacitor instead of the full binary-weighted arrays decreases total capacitance, benefitting power, and area. A 3σ design in the selected technology imposes a unit capacitance (C) higher than 17.2 fF. This design uses a relatively larger value ($C =$ 76.8 fF) to make the parasitic of the interconnection metal lines negligible [21], and is implemented by Metal-Insulator-Metal (MIM) capacitors. In a split capacitor DAC, the attenuation capacitor ($C_{\rm a}$) must be $(16/15)C$, a value not suitable for capacitor matching because it is not unity. Thus, this design uses a unity capacitance for $C_{\rm a}$ and adjust the layout of the top-to-bottom parasitic ($C_{\rm par}$) of $C_{\rm a}$ in a way to achieve an effective capacitance ($C_{\rm a,eff}$) of $16/15\,C \approx 81.9$ fF.

The sampling action in the DAC happens when $spin+$ or $spin-$ is high and lasts only 1.5625 μs. The fast sampling of the capacitive DAC permits a high duty cycle of both bridge sensor and IA.

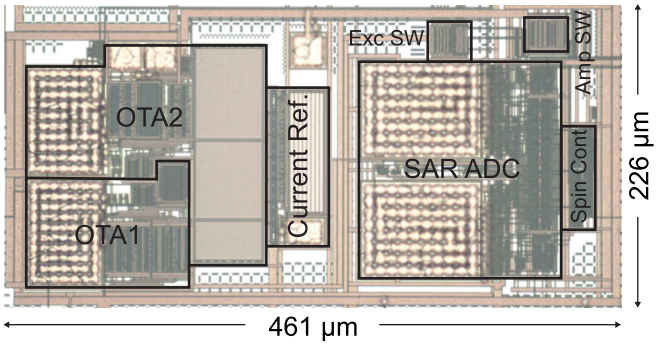

Fig. 9. Die micrograph of the BDC ASIC fabricated in a standard 180-nm CMOS process.

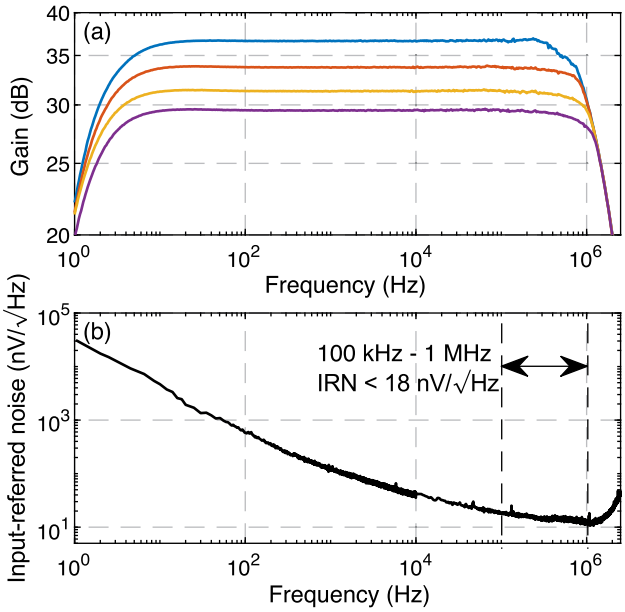

Fig. 10. (a) Capacitively-coupled IA's measured frequency response for different gain configurations and (b) input-referred noise (IRN) spectrum.

IV. Measurement Results

The BDC application-spesific IC (ASIC), designed and fabricated in a 180-nm standard CMOS technology, has an active area of 0.1 mm^2, as shown in Fig. 9. Experimental measures verified the performances of the BDC readout IC and the entire pressure sensing system. The following sections report the results.

A. Electrical Measurements

A first characterization separately measured the CCIA and SAR ADC in the implemented bridge-to-digital interface. Fig. 10(a) shows the closed-loop frequency response of the CCIA for different gain configurations. The gain changes in the range of 29.2 dB (29 V/V) to 37.1 dB (72 V/V) by trimming the 2-bit controlled feedback capacitors (C_{fb2}) for tuning the input range of the CCIA from $\pm$6.6 mV to $\pm$16.5 mV at 1.2 V supply voltage. Fig. 10(b) shows the CCIA's input-referred noise spectrum lower than 18 nV/$\sqrt{\text{Hz}}$ in the bandwidth from

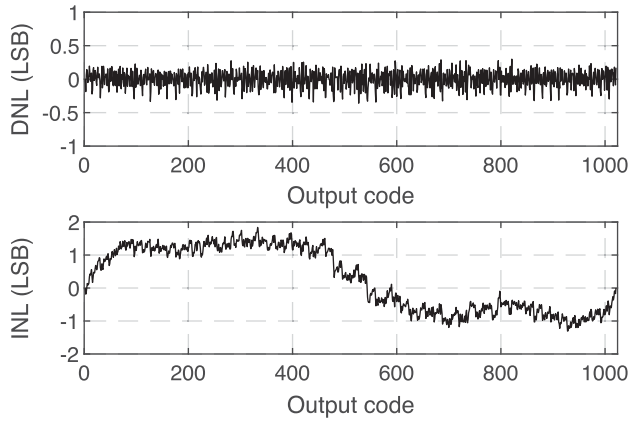

Fig. 11. Measured DNL and INL.

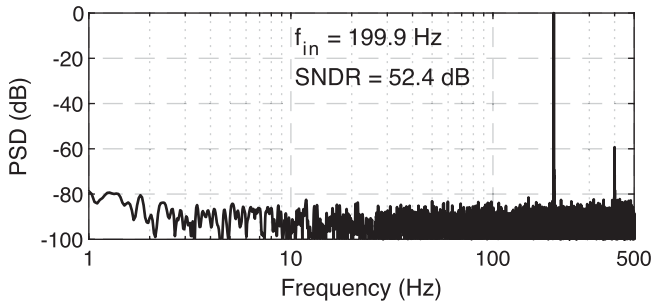

Fig. 12. Measured output spectrum of the BDC.

100 kHz to 1 MHz. The excitation switches of the bridge sensor up-modulate the bridge output at a frequency range and the selected bandwidth. The CCIA draws 217 μA static current from a 1.2 V supply, but thanks to the duty cycling, the average current consumption is 0.51 μA.

The supply voltage of the SAR ADC is 1.2 V and the sampling rate is 1 kS/s. At 199.9 Hz input frequency, the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 57 dB and 66.5 dB, respectively. It shows a negligible drop of performance over the entire bandwidth. At 1 kS/s sampling rate, the peak differential non-linearity (DNL) and integral non-linearity (INL) are +0.3/ –0.36 LSB and +1.8/ –1.3 LSB, respectively (Fig. 11). The SAR ADC consumes 19 nW and achieves a figure-of-merit (FoM = Power/2^{ENOB}*f_s) of 32.3 fJ/conversion [21].

Fig. 12 shows the measured output spectrum of the complete bridge-to-digital readout. At 199.9 Hz input frequency, the BDC achieves an SNDR of 52.4 dB, and the resultant effective number of bits (ENOB) is 8.4. The LSB for the minimum input is 39.1 μV, while the input-referred noise over the 100 kHz to 1 MHz range is about 18 μV, less than half LSB for the minimum input. Fig. 13 shows the measured SNDR values at different input amplitudes. The variable gain operation improves the SNDR for small amplitudes and the BDC achieves a dynamic range of 55.6 dB. The total current consumption of the ASIC is 9.48 μA from a 1.2 V supply. The current reference circuit consumes 8.4 μA since it is not duty-cycled, and the spinning control logic

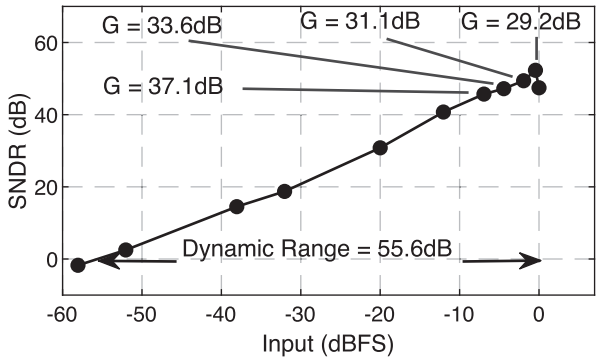

Fig. 13. SNDR vs. input amplitude of the BDC at $f_{in} = 199.9$ Hz.

TABLE I
PERFORMANCE SUMMARY

Technology (nm)	180
Supply Voltage (V)	1.2
Capacitively-Coupled IA	
Gain (V/V)	29, 36, 48, 72
Bandwidth (MHz)	1
Input Range (mV)	±6.6 to ±16.5
Input-referred noise (nV/$\sqrt{}$Hz)	18[a]
Average Power Consumption (nW)	636
SAR ADC	
Sampling Rate (kS/s)	1
SNDR and SFDR (dB)	57, 66.5
DNL and INL (LSB)	+0.3/-0.36, +1.8/-1.3
Power Consumption (nW)	19
Walden FOM (fJ/conversion)	32.3
Full System BDC with Bridge Sensor	
Pressure Range (mmHg)	270
Resolution (mmHg)	0.44
ENOB	8.4
Conversion Energy (nJ/conversion)	1.1[b]

[a] In a bandwidth from 100 kHz to 1 MHz.
[b] Current reference circuit and spinning control logic were not considered.

consumes 560 nA because it includes a clock divider circuit from 1.28 MHz to 1 kHz. If the current consumptions of the reference circuit and spinning control logic are not considered, the BDC ASIC draws 0.53 μA current from a 1.2 V supply and consumes 0.63 nJ energy in 1 ms conversion time.

B. System Measurements

The bridge-to-digital readout ASIC mounting two different pressure sensors verified the functionality of the BDC. The demo uses small size pressure sensors to match the miniature requests of the system for possible body implantation.

The initial use of an absolute pressure sensor (MS761) [27] revealed that the reverse biasing of the bridge sensor leads to a high leakage current. The sensing elements in the bridge sensors are diffused resistances, and the substrate can short to the positive

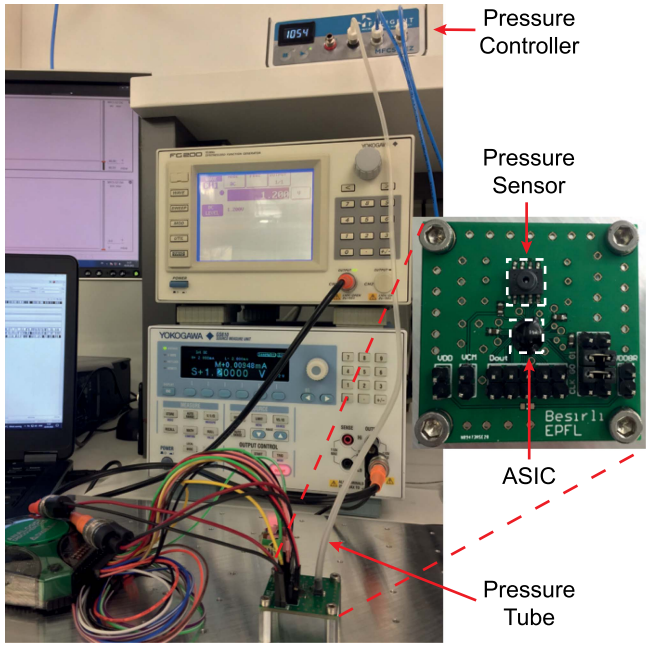

Fig. 14. Experimental setup for pressure measurements of the BDC.

supply of the bridge in some MEMS pressure sensors. In such sensors, the voltage applied to the top excitation must always be higher than the bottom excitation voltage. Our spinning topology does not work because of the excitation pad's connection to the substrate of the MEMS. In MS761, there is an additional pad for the epitaxial layer, but it is connected to the pad of the positive excitation voltage. To solve the leakage problem, we broke the connection between these two pads to connect the epitaxial layer to 1.2 V, while the excitation voltage of the bridge spins. The solution avoids reverse biasing and eliminates the current leakage issue.

A further functionality test of the BDC used a differential pressure sensor. The difficulty in measuring the differential pressure with a sensor die (SM30D) [28] forced to use its packaged version (SM5G) [29] with an operating pressure range of 0 to 5 PSI (0 to 258.6 mmHg). The substrate of SM5G also connects the top excitation voltage, and there is no additional pad for substrate connection for a substrate and excitation voltage separation. For an acceptable leakage current, the measures with the SM5G sensor use a maximum current on the bridge limited to 300 μA by the DC power supply. However, it is expected that the implanted system will separate the substrate and the excitation voltage of the MEMS sensor.

Fig. 14 shows the experimental setup used for the system pressure measurements. A pressure controller (Fluigent MFCS-EZ) generates stable pressure steps. The local pressure network in the laboratory provides pressurized nitrogen for creating positive pressure and tunes the input pressure value via a pneumatic regulator. A vacuum pump connected to the pressure controller generates the negative pressure. Conventional instruments bias the ASIC, provide an input clock at 1.28 MHz, accurately measure the current consumption, and read out the digital output.

TABLE II
STATE-OF-THE-ART BDCs

	IEEE Sens. J.'14 [12]	TBCAS'15 [13]	VLSI'17 [15]	ISSCC'18 [16]	JSSC'19 [17]	IEEE Sens. J.'20 [18]	**This work**
Technology (nm)	90	350	180	180	180	350	**180**
ASIC Supply Voltage (V)	1	3.3	1.8	1.2, 3.6	1.8	1.8	**1.2**
ASIC Supply Current (μA)	19.5[a]	60.6[a]	33.9[a]	0.38@3.6V 0.06@1.2V[a]	1200	328.6	**0.53**[a]
Bridge Voltage (V)	1	3.3	1.8	3.6	5	1.8	**1.2**
Bridge Resistance (kΩ)	12	8.25 - 16.5[b]	1	6	3.7	5	**5**
Bridge Current (μA)	83.3	60.6 - 121.2	102.8	0.13	1351	1.4	**0.39**
Conversion (Conv.) Time (ms)	0.096	0.8	1	1	0.5	0.27	**1**
Conv. Energy without Bridge (nJ/conv.)	1.87	160	61	1.4	1080	159.7	**0.63**
Conv. Energy with Bridge (nJ/conv.)	5	320 - 480	246	1.9	4458	160.4	**1.1**
ENOB	7.03	7.2	9.7	7.9[b]	15.4[b]	9.13	**8.4**
FoM[c] (pJ/conv.)	38.3	2176 - 3265	296	8.0	103.1	286.3	**3.3**

[a]Only sensor interface current (Power management, clock generators, and current references were excluded).
[b]Estimated from given data.
[c]FoM = (Conv. Energy with Bridge)/2^{ENOB}.

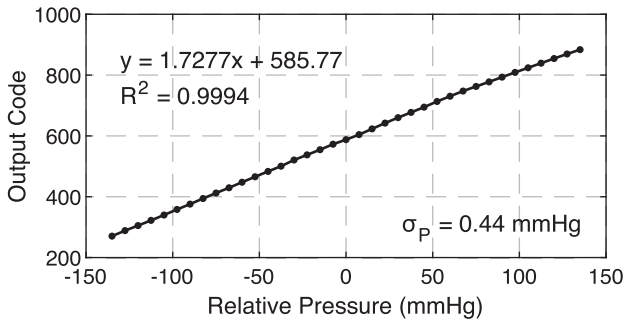

Fig. 15. Measured decimated output of the BDC with swept pressure from -135 mmHg to +135 mmHg with respect to the ambient pressure.

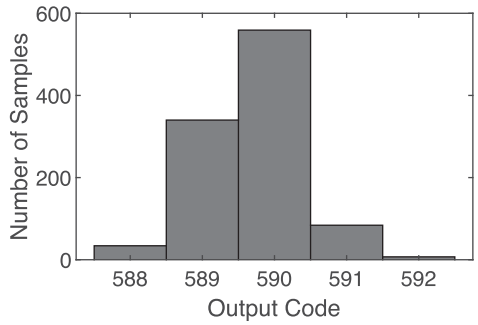

Fig. 16. Histogram of decimated output at zero pressure input for 1024 samples.

As shown in Fig. 15, the output of the BDC with SM5G differential pressure sensor linearly increases from 270 to 884, corresponding to 0.44 mmHg resolution with 1 ms conversion time. Table I summarises the overall system performance of the BDC. Fig. 16 shows the histogram of the output code for 1024 samples when the relative pressure is zero. It demonstrates an accuracy of 3 LSB equal to 1.32 mmHg. The pressure sensor having 5 kΩ bridge resistances draws 390 nA current and consumes 0.47 nJ excitation energy per conversion.

Table II compares this work with the state-of-the-art. The total BDC consumed energy is 1.1 nJ per conversion for an ENOB of 8.4. The figure-of-merit (FoM = (Conv. Energy)/2^{ENOB}) is 3.3 pJ/conversion, the state-of-the-art performance in terms of energy efficiency.

V. CONCLUSION

This paper describes the design, fabrication and test of an energy-efficient bridge-to-digital converter specifically tailored for implantable pressure monitoring systems. The design exploits the duty cycling of the bridge sensor for cancelling the IA offset at the same time. The 1/f noise and offset of the IA are inherently suppressed by designing a spinning method simultaneously applied to the bridge and capacitive DAC of the SAR ADC. The method avoids using digital filters for the cancellation of the spurs, that in a conventional chopper amplifier derive from the offset and 1/f modulation. The BDC interface, fabricated in a standard 180-nm CMOS technology, achieves 8.4 ENOB at 1 kS/s sampling rate. The highly duty-cycled CCIA enables the BDC readout to only draw 0.53 μA average current from the 1.2 V supply. The testing of the BDC readout used absolute and differential piezoresistive pressure sensors. The BDC with the differential pressure sensor achieves a resolution of 0.44 mmHg in a pressure range of -135 to +135 mmHg. The figure-of-merit of the pressure sensing system is 3.3 pJ/conversion for a total conversion energy of 1.1 nJ, which are state-of-the-art performances. The results make the system suitable for deeply implanted devices that continuously monitor the PAP of HF and PH patients.

In future work, ultrasound will establish wireless powering and communication. The future implant consists of the ASIC, pressure sensor, and an ultrasound transducer packaged using advanced glass technology. It will be in-vitro tested by using

a setup simulating the arterial blood flow and containing a pulmonary artery from a domestic pig.

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