On-Chip Sinusoidal Signal Generators for Electrical Impedance Spectroscopy: Methodological Review

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***Abstract*—This paper reviews architectures and circuit implementations of on-chip sinusoidal signal generators (SSGs) for electrical impedance spectroscopy (EIS) applications. In recent years, there have been increasing interests in on-chip EIS systems, which measure a target material's impedance spectrum over a frequency range. The on-chip implementation allows EIS systems to have low power and small form factor, enabling various biomedical applications. One of the key building blocks of on-chip EIS systems is on-chip SSG, which determines the frequency range and the analysis precision of the whole EIS system. On-chip SSGs are generally required to have high linearity, wide frequency range, and high power and area efficiency. They are typically composed of three stages in general: waveform generation, linearity enhancement, and current injection. First, a sinusoidal waveform should be generated in SSGs. The generated waveform's frequency should be accurately adjustable over a wide range. The firstly generated waveform may not be perfectly linear, including unwanted harmonics. In the following linearity-enhancement step, these harmonics are attenuated by using filters typically. As the linearity of the waveform is improved, the precision of the EIS system gets ensured. Lastly, the filtered voltage waveform is now converted to a current by a current driver. Then, the current sinusoidal signal is injected into the target impedance. This review discusses the principles, advantages, and disadvantages of various techniques applied to each step in state-of-the-art on-chip SSGs. In addition, state-of-the-art designs are compared and summarized.**

***Index Terms*—Bioimpedance, current driver, current injection, impedance measurement, linearity enhancement, sinusoidal waveform generation, spurious-free dynamic range, total harmonic distortion.**

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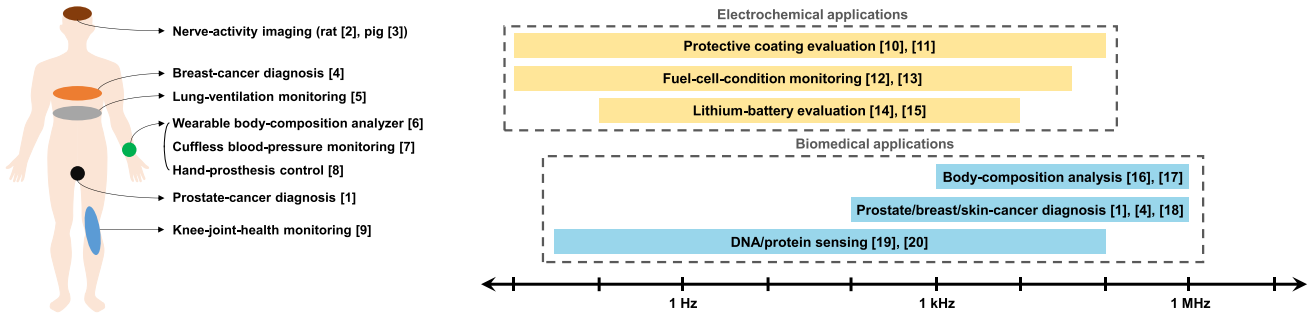
I. Introduction

IMPEDANCE of biomedical tissues (or bioimpedance) provides with valuable information about the target biomedical material. The bioimpedance of a tissue is a property related to the electrical current flow through the tissue and its ability to store electrical charges, indicating tissue architectures such as cellular size, cellular density, cellular spacing, and the constituents of the extracellular matrix [1]. As a result, the bioimpedance has been widely used as a marker in various medical applications to monitor physiological status, as shown in Fig. 1(a) [1]–[9].

Since the bioimpedance is strongly dependent on the frequency, electrical impedance spectroscopy (EIS), in which the target impedance is measured over a range of frequency, is one of popular techniques not only in biomedical but also in electrochemical fields. It has been widely used for characterizing materials, devices, biological tissues, and so on, as shown in Fig. 1(b) [1], [4], [10]–[20]. In particular, as portable EIS devices are required for some applications, such as wearable body-composition analysis, wearable cancer diagnosis, and other internet-of-thing (IoT) applications, there have been great interests in on-chip EIS systems implemented in the form of integrated circuits (ICs). One of the representative examples of this trend is body-composition analyzers. These analyzers were too large, heavy, and expensive to use personally in the early days of commercialization. However, they have become smaller, lighter, and cheaper. In recent years, even wearable versions of devices, such as smart watches and wrist bands, have emerged as a market trend. These wearable devices should be designed with a small form factor and low power consumption for user convenience and long operating time. On-chip implementation of EIS systems is typically inevitable for such wearable devices.

In EIS, the impedance spectrum can be obtained by two methods: (1) wide-band-signal excitation and (2) single-tone excitation. When a wide-band signal is delivered to the target material, demodulation of the signal obtained from the target material can result in impedance information for a wide band or multiple frequencies at once [21]. Such wide-band signals include white noise [22], chirp [21], [23], maximum length sequences (MLS) [21], differential maximum length sequence (DMLS) [21], and multiple-sine signals [23]. On the contrary, when a single-tone signal is delivered to the target material, the impedance spectrum can be obtained by measuring the impedance for the particular frequency at a time [24], [25]. And then, by repeating the measurements at different frequencies, the impedance spectrum can



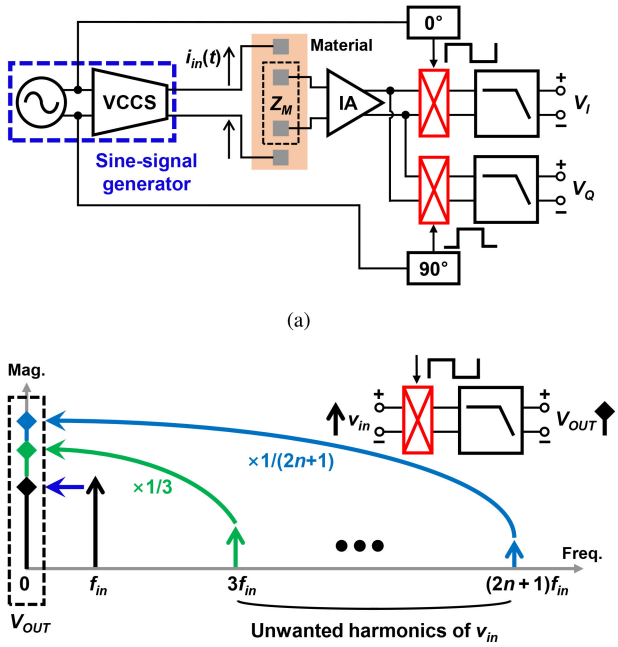
(a) (b)

Fig. 1. (a) Biomedical applications of impedance measurement and (b) applications of electrical impedance spectroscopy and their required frequency ranges.

be obtained. As such, the wide-band-signal excitation method can obtain the impedance spectrum with a shorter measurement time compared to the method using single-tone stimulus. At the sacrifice of the measurement speed, the single-tone stimulus can achieve a higher signal-to-noise ratio (SNR) than the method using wide-band-signal stimulus [21]. In the single-tone excitation method, the signal power is all concentrated at the single tone, leading to a better measurement sensitivity. As shown, there is a trade-off between measurement speed and sensitivity in EIS systems. The single-tone excitation is suitable for applications that require high sensitivity. Some wearable applications require very small resolution from 1 to 100 $m\Omega_{RMS}$ [21]. In addition, the single-tone excitation method is known to be easier to implement on-chip and has better accuracy [26], [27]. Moreover, widely used commercial impedance analyzer ICs (Texas Instruments AFE4300 and Analog Devices AD5933) also use the single-tone excitation method, and much more numerous researches have focused on achieving better performances with the single-tone excitation method than the wide-band excitation methods.

Fig. 2(a) shows a general block diagram of widely used on-chip EIS systems based on the single-tone stimulus method [28]–[30]. A sinusoidal signal generator (SSG) injects a sinusoidal current signal into the target material, and a demodulator extracts the real and imaginary parts of the target impedance by quadrature mixing with the in-phase and quadrature-phase (90°-shifted) signals. In another way, a sinusoidal voltage signal can be applied to the target material [31]–[37], but the current-injection method is more common due to the safety issue, especially in biomedical applications. The SSG is one of the key building blocks in on-chip EIS systems because its frequency range and linearity determine the frequency range and precision of the whole EIS system. Since many applications require a wide frequency range over three decades, as shown in Fig. 1, the SSG should have a wide frequency range. When an on-chip EIS system should support several applications, the required frequency range of the SSG should be wider. In order to know the effect of the linearity on the precision of the whole system, we should review the mixing process of general on-chip EIS systems in more detail.

Fig. 2(b) illustrates the down-conversion by the chopper in the frequency spectrum to show the effect of the SSG's linearity to the final impedance results. Since linear multipliers typically consume very large power [29], choppers, which consist of



(a) (b)

Fig. 2. (a) Block diagram of general on-chip EIS systems. (b) Error caused by the signal harmonic folding at the frequency mixing stage in the demodulator.

switches only, have been adopted widely for the quadrature multiplications due to their simplicity and low power consumption. The fundamental tone of the input signal at $f_{\rm in}$ is demodulated and down-converted to DC by multiplication with the demodulation clock signal at the same fundamental frequency. Although the chopper also generates another high-frequency tone at $2f_{\rm in}$, the following low-pass filter (LPF) removes this tone. However, when the input signals have odd-order harmonics, the chopper causes errors in the final result due to the odd-order harmonics of the chopper clock. The odd-order harmonics of the input signal are also down-converted to DC by the multiplications with the corresponding odd-order harmonics of the clock signal. The filters after choppers cannot prevent this harmonic-folding error since the folding happens at the mixing stage. To avoid this harmonic-folding error, the SSG should generate a sinusoidal signal with high linearity by suppressing the harmonics as much as possible.

TABLE I
KEY PERFORMANCE PARAMETERS OF REPRESENTATIVE ON-CHIP SSGS FOR THREE DIFFERENT EIS APPLICATIONS

	Implantable EIS system [38]	Wearable EIS system [28]	Miniature EIS instrum. [24]
Frequency [Hz]	20k	0.1k – 100k	40m – 40k
SFDR [dB]	65.2	59.0	63.0
THD [%]	0.088	0.2	< 0.1
Power [W]	6.2μ	N. R[a]	N. R
Area [mm^2]	0.059	0.74[b]	0.64

[a]Not reported, but total EIS system consumes 53.4 mW.
[b]Estimated area.

Table I shows main performance parameters of on-chip SSGs for the following three applications: implantable EIS systems, wearable EIS systems, and miniature EIS instruments. To minimize the harmonic-folding errors in the impedance measurement, high spurious-free dynamic range (SFDR) and low total harmonic distortion (THD) are needed for all the applications. In many systems, a SFDR of higher than 60 dB and a THD of less than 0.2% have been achieved. For implantable EIS systems, the power consumption should be low. For example, for ensuring the life time of pacemaker over 10 years, the power consumption of the EIS system is required to be less than 10 μW [39]. To save the power consumption, implantable EIS systems often support one or a few particular frequencies only at low frequency like the one shown in Table I [38]. In contrast, many wearable EIS systems support a wider frequency range thanks to their higher power budget. As reported in [21], a total power consumption is recommended to be less than 500 μW. Miniature EIS instruments are much less restricted by the power consumption, so they can more easily widen the frequency range for supporting various applications. For example, the EIS system in [24], which is for electrochemical applications, is designed to support a wide frequency range of six decades from 40 mHz to 40 kHz. Besides, some EIS systems for biomedical applications are designed to support high frequencies as 10 MHz [30].

There are several reviews on impedance measurement systems [21], [40]–[43], but they do not provide an in-depth discussion on the architectures and implementation of on-chip SSGs. To fill the gaps, this paper reviews various design techniques in the implementation of on-chip SSGs on the basis of four performance metrics: frequency range, linearity, power consumption, and chip area. On-chip SSGs typically consist of three stages to achieve improved performance metrics: waveform generation, linearity enhancement, and current injection. First, SSGs generate a sinusoidal waveform at a frequency. And the frequency should be easily and accurately controlled over a wide frequency range. Because the generated waveform is not perfect and includes unwanted harmonics, the harmonics should be attenuated further by using filters in the SSG before delivering the sinusoidal signal to the target material. By improving the linearity of the SSG, the harmonics-folding error, which occurs at the mixing stage of demodulator, can be reduced. Lastly, the voltage waveform should be converted to a current signal and injected into the target.

Each of these stages will be reviewed in the remainder of this paper, which is organized as follows. Section II introduces overall architecture of on-chip SSGs. Sections III, IV, and V review widely used circuits and techniques for waveform generation, linearity enhancement, and current injection, respectively. Section VI concludes the paper with a performance summary of state-of-the-art designs.

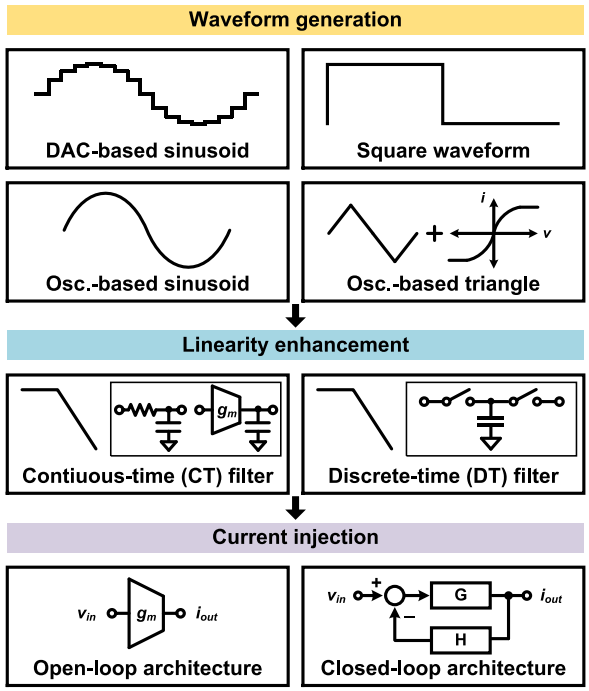


Fig. 3. Three main stages of on-chip SSGs and representative techniques for each stage.

II. OVERALL ARCHITECTURE

Fig. 3 shows three major stages of on-chip SSGs and representative methods of each stage: waveform generation, linearity enhancement, and current injection. Each stage is briefly introduced in this section.

A. Waveform Generation

First, on-chip SSGs should generate a base waveform. Various waveform generation methods have been demonstrated for on-chip SSGs: digital-to-analog converter (DAC)-based sinusoid, square waveform, oscillator-based sinusoid, and oscillator-based triangle. The methods based on discrete-time (DT) signals, including the DAC-based sinusoid and the square waveform, are widely used because their fundamental frequency can be easily and accurately controlled by their digital clock frequency. The DAC-based sinusoid is typically generated by a multi-bit-resolution DAC with oversampling. The higher the bit DAC's resolution and oversampling ratio (OSR), the clearer the sinusoidal waveform is generated with smaller harmonics. In contrast, the square waveform can be generated by a simple one-bit DAC, which can be implemented with digital blocks only, with no need for oversampling. While the generation of this square waveform requires much simpler hardware and a lower-speed clock, the DAC-based sinusoid is much better than

the square waveform in terms of linearity due to its multi-bit resolution and oversampling.

As alternatives to these discrete methods, sinusoidal waveforms can be generated by using oscillators without any DAC or oversampling. Two types of oscillators have been demonstrated. The first-type oscillators directly generate a sinusoidal signal while the second type, which involves a simpler structure, generates a triangular waveform. This triangular waveform is converted to a sinusoidal signal by a waveform shaper based on the non-linear V-I characteristics of a CMOS differential pair. These oscillator-based signals may achieve better linearity than the DAC-based sinusoids using low OSR and low-resolution DAC. However, frequency control of the oscillator is more difficult than that of DT signals because the oscillation frequency is determined by the oscillator's constituents, which are prone to change by PVT variations. The process variation can cause just a static error in the output frequency, which can be calibrated before the measurement if a reference frequency is given. However, it is still more difficult and complex to precisely control the oscillator's frequency over a wide range than the DT methods based on a clock frequency. In addition, it is difficult for oscillators to achieve a wide frequency range as more than three decades at a given area and power. It is because large-sized passive components are required for generating low-frequency signals, and large power is required for generating high-frequency signals.

B. Linearity Enhancement

After the waveform generation stage, the signal may still have unwanted harmonics. Depending on the linearity requirements, these harmonics should be attenuated further. While filters can be used to attenuate the harmonics of continuous-time (CT) signals generated by oscillators, they are more widely used to attenuate the harmonics of signals generated by DT-based methods. The 50%-duty square waveform has large odd-order harmonics, which is expressed as follows:

$$I_{\mathrm{in}}(t) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin(n \times 2\pi f_{SG} t)}{n} \tag{1}$$

where f_{SG} is the fundamental frequency of the signal. The third-order harmonic tone is –9 dBc, which is considered very large for most cases. Odd-order harmonics of the DAC-based sinusoid are smaller than those of the square waveform [44], [45], but they need to be attenuated further for high linearity in many cases.

SSGs have adopted two types of filters: CT and DT filters. The CT low-pass filters (LPFs), which is usually made of RC components and g_m stages, are suitable for attenuating high-order harmonics but not for attenuating low-order harmonics. Note that the error caused by low-order harmonics is larger than that caused by high-order harmonics, as shown in Fig. 2(b). Thus, low-order harmonics of the CT LPF's input signal should be already sufficiently suppressed, or the CT LPF should have high-order attenuation characteristics. Besides, in view of physical implementation, CT LPFs require very small g_m and/or very large-sized passive components when the EIS system analyzes the material at low frequencies.

In contrast, DT filters, which are based on switched-capacitor circuits, can support low frequencies easily without large-sized passive components. DT filters can easily control the cut-off frequency by changing the sampling frequency, thereby easily achieving low and wide f_{SG} ranges. Compared to CT LPFs, the DT filters can attenuate low-order harmonics further by using their nulls located at harmonics and/or high-order roll-off.

C. Current Injection

The generated sinusoidal waveform should be delivered to the target impedance. The delivery can be made in voltage or current. A more detailed comparison between these two methods is well presented in the literature [31], [32]. The voltage-excitation method can support higher f_{SG} than the current-injection method in general. The current injection is limited at high frequencies because it is hard to maintain the output impedance at high frequencies due to the output and parasitic capacitances. The current injection is preferred to the voltage excitation in most biomedical applications because it can more effectively prevent the target tissue from damages by unwanted high currents that may happen in the voltage excitation. This safety issue can be prevented by a current limiting resistor in the voltage-excitation method. But, additional read-out circuits are typically required to measure the actual current flowing through the target material. In addition, as the target impedance increases, the flowing current decreases. Then, the magnitude of resulting voltage signal from the target material decreases, degrading the sensitivity of the impedance measurement circuit. In other words, the current injection method is easier to obtain a larger signal magnitude than the voltage excitation method. As such, to avoid the tissue damage while obtaining the maximized signal magnitude, the current injection is preferred to the voltage excitation in most biomedical applications. Since most filters are implemented in the voltage domain, a current driver is needed to convert the voltage signal to current, which can be safely injected into the target material.

There are two important parameters in the implementation of current drivers: output impedance and linearity. The current driver should have a high output impedance to provide a constant current amplitude regardless of the target impedance. In addition, this large output impedance has to be maintained over a wide frequency range to provide a constant current over the entire frequency range. Finally, SSGs should inject the current without degrading the linearity of the sinusoidal signal generated by the waveform generation and linearity enhancement stages.

There are two main architectures of the current drivers in general: open-loop and closed-loop architectures. The open-loop architecture injects the current without feedback, thereby achieving simpler hardware complexity and a wider bandwidth with a given power consumption than the closed-loop ones. In contrast, the closed-loop architecture injects the current with feedback so that it can improve the output impedance and linearity and obtain more reliable transconductance compared to the open-loop ones. Since various current driver circuits are well reviewed in the literature [40], [41], representative and basic structures are briefly reviewed in Section V.

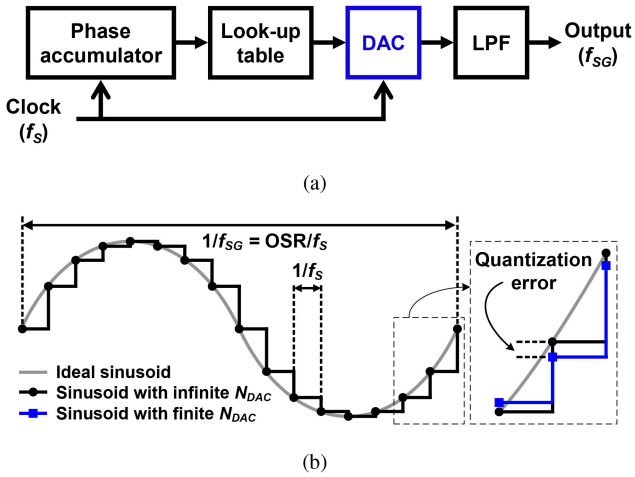


Fig. 4. (a) Block diagram of direct digital synthesizer for generating DAC-based sinusoid [46] and (b) an example DAC-based sinusoid when OSR $=$ 16. f_{SG} is the frequency of the generated sinusoidal waveform, and f_S is the sampling frequency. OSR $= f_S/f_{SG}$.

III. Waveform Generation

This section reviews four representative waveform-generation methods adopted in SSGs. For each waveform, basic characteristics and various circuit techniques that can improve the overall performance of the on-chip EIS system are discussed. Some techniques verified in off-chip designs are also included if they are applicable to on-chip designs.

A. DAC-Based Sinusoid

For the generation of DAC-based sinusoids, direct digital synthesizers (DDSs) are widely used in on-chip EIS systems [35], [36], [39], [47], [48]. Fig. 4(a) shows a block diagram of the most basic DDS architecture [46]. Fig. 4(b) shows an example DAC-based sinusoid when OSR $= f_{SG}/f_S = 16$. f_{SG} is the output sinusoid frequency, and f_S is the sampling frequency. As the DAC-based sinusoid gets closer to the ideal sinusoid, its harmonics are typically more suppressed. As the OSR increases, more samples reconstruct one sinusoidal period of f_{SG}. Then, the resulting DAC-based sinusoid becomes closer to the ideal sinusoid with smaller harmonics. Note that DDSs usually operate with a fixed f_S. Thus, as f_{SG} increases with a fixed f_S, the OSR decreases, thereby increasing the harmonics and degrading the linearity. As shown in the inset of Fig. 4(b), deviation of the DAC value from the ideal sinusoid, which is defined as the quantization error, is also a dominant parameter in determining the magnitudes of harmonics. As the number of the quantization levels (N_{DAC}) increases (the DAC's resolution increases), the quantization error gets smaller. To sum up, the DAC-based sinusoid becomes closer to the ideal single-tone sinusoid with better linearity as the OSR and/or N_{DAC} increase.

In order to characterize the effect of N_{DAC} and OSR on the linearity in more detail, a commercial impedance analyzer IC (Texas Instruments AFE4300) is used for the following tests. This IC includes a 6-bit 1-MSps DAC to generate DAC-based sinusoids. Using this IC, two sinusoidal waveforms are generated with OSR or 16 and 32. The corresponding f_{SG} is 62.5 kHz and 31.25 kHz, respectively. Fig. 5 shows simulated harmonic magnitudes of the sinusoidal signals. By the sampling theorem, the sampling harmonics are generated at $k \cdot f_S \pm f_{SG}$ where k is an integer number and f_S is the sampling frequency. Each of these tones' magnitude can be found by using the following transfer function:

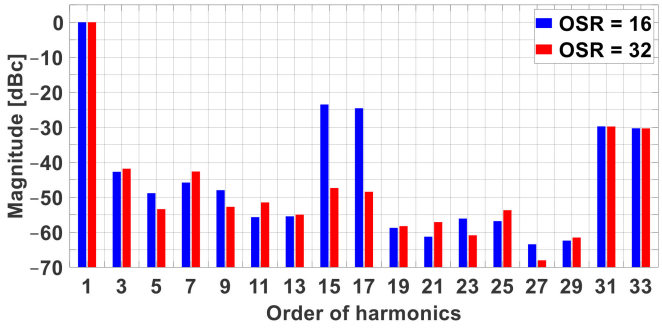


Fig. 5. Simulated harmonic magnitudes of a sinusoid generated by a 6-bit DAC with an OSR of 16 and 32.

$$|H_{sinc}(f)| = \left| \frac{\sin(\pi \cdot f \cdot f_S)}{\pi \cdot f \cdot f_S} \right|. \tag{2}$$

Among the harmonics for the DAC-based sinusoid with OSR of 16, the 15th, 17th, 31st, and 33th harmonics are generated by the sampling operation, and their magnitudes are determined by (2). Similarly, for OSR $=$ 32, the 31st and 33th harmonics are attributed to the sampling operation. Other harmonics are generated by the DAC's finite resolution.

The linearity of DAC-based sinusoids can be quantitatively evaluated by the signal's SFDR and THD. SFDR is defined as the power ratio of the fundamental signal to the largest harmonic signal. As shown in Fig. 5, the OSR exerts much more influence on the SFDR than N_{DAC} does because the largest harmonic is determined by the OSR. Therefore, another quantitative metric considering all other harmonics is required to evaluate the effect of the finite N_{DAC} on the linearity of DAC-based sinusoids. One of such metrics is THD, which is defined as the ratio of the sum of the power of all the harmonics to the power of the fundamental tone. It is useful to show the effect of the finite resolution because THD takes all the harmonics within the frequency range of interest into account. The DAC's finite resolution causes quantization errors between the DAC output signal and the perfect sinusoid, as shown in Fig. 4(b). When the DAC generates a sinusoid signal based on an look-up table (LUT), the quantization errors generate harmonics, not white noise, due to its deterministic characteristic.

Especially, since lower order harmonics cause much larger errors in EIS systems (Fig. 2(b)), it is also necessary to analyze THD considering low-order harmonics only up to ith-order (THD$_i$) excluding the sampling harmonics. THD$_i$ can be calculated from SQR$_i$, which is the signal to the quantization noise power (SQR) when the quantization noise power is calculated over a frequency range from 0 to $i \cdot f_{SG}$. Then, THD$_i$ equals –SQR$_i$ in the dB scale and 1/SQR$_i$ in the linear scale. When the DAC utilizes the full scale of the DAC to generate the DAC-based

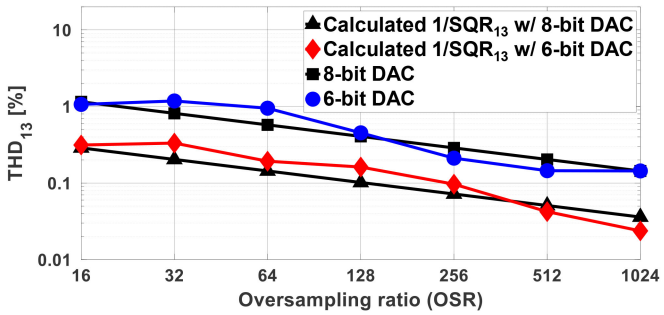


Fig. 6. THD_{13} versus OSR for 8- and 6-bit DAC cases in comparison with the calculated $1/\text{SQR}_{13}$.

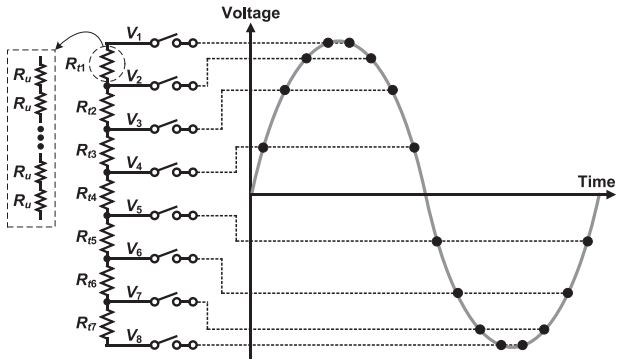


Fig. 7. Operation principle of a sinusoidally tapped resistor DAC for sinusoidal waveform generation. The resistor chain with only eight taps is demonstrated for simplicity. In [51], [52], 33 taps with 1000 unit resistors were used.

sinusoid, SQR_i is expressed as follows [49]:

$$\text{SQR}_i\ [\text{dB}] = 1.76 + 6.02N_{DAC} + 10\log\left(\frac{\text{OSR}}{i}\right) \tag{3}$$

where $\text{OSR} - 1 > i$. As the OSR increases, the power of quantization noise over the specific frequency range from 0 to $i \cdot f_{SG}$ decreases because the noise power spectral density decreases. As a result, SQR_i depends on not only N_{DAC} but also the OSR. Note that (3) does not include the sampling harmonics. When $i \geq \text{OSR} - 1$, the sampling harmonics are included within the frequency range of interest, and (3) does not hold. But, for $\text{OSR} - 1 > i$, (3) is useful to quantitatively evaluate the effect of low-order harmonics on the linearity. Fig. 6 shows the calculated $1/\text{SQR}_{13}$ and simulated THD_{13} for N_{DAC} of 6 and 8 when the DAC utilizes the full scale of DAC. When a 50%-duty square waveform is injected into the target material instead of a single-tone sinusoidal signal, the summed error caused by the harmonics from the 5th to 13th of the square waveform is also significant compared with that caused by the 3rd harmonic [50]. Thus, $i = 13$ is chosen here. Since the order of the sampling harmonic is higher than 13 for OSRs higher than 16, THD_{13} is well-matched with the calculated $1/\text{SQR}_{13}$. THD_{13} decreases as either N_{DAC} or OSR increases.

To sum up, the SFDR is a useful parameter showing the linearity of DAC-based sinusoid when the OSR is the dominant parameter on the linearity, i.e., N_{DAC} is high enough. In contrast, THD_i is more informative when the quantization error is the dominant parameter on the linearity due to a high enough OSR.

The linearity of a DAC-based sinusoid can be improved by increasing the OSR as shown in Fig. 6. However, as the OSR increases, the hardware gets more complex, and the power consumption increases. More specifically, the number of the sampling points per one sinusoid period increases, requiring a larger memory to store a larger LUT [52]. To reduce the LUT size, adaptive quantizing techniques according to the signal scale can be used [53]–[58]. For example, in [53]–[57], when the current level at a certain sampling point is less than 2/3 of the peak current of the sinusoid, the quantization level is rounded off to the nearest multiple of two of the unit current cell. As a result, the hardware complexity, including the LUT size, is reduced while keeping the low order harmonics less than the magnitude of the 63th harmonic, which is the main harmonic caused by the sampling operation. Similarly in [58], the linearity is further improved by a finer rounded-off. Although the complexity caused by high OSR can be mitigated to some extent by these methods [53]–[58], the maximum f_{SG} is still limited by the required high clock speed for such high OSR.

In addition to the OSR, N_{DAC}, the DAC's resolution, is another dominant parameter in determining magnitudes of the low-order harmonics. As shown in Fig. 6, the linearity is improved by increasing N_{DAC}. But, at the same time, the required switch control logic of the DAC gets more complex and larger [52]. This results in an increase of the required silicon area occupying the switches and routing lines [52]. In order to reduce the complexity while keeping a target N_{DAC}, a sinusoidally tapped resistor DAC (RDAC) with a fixed OSR can be used [52]. Fig. 7 briefly describes its overall operation concept. It consists of a resistor chain, which is sinusoidally rationed, and switches. The resistor chain is shown with only eight taps here for simplicity. Note that the OSR is fixed here when f_{SG} is varied. The switches are just connected to the taps corresponding to each phase while the amplitude corresponding to each phase is fixed. Although this DAC still uses as many unit resistors corresponding to its N_{DAC} as DACs of DDS, this DAC eliminates the need of connecting switches to all the unit resistors, thereby reducing the number of switches greatly. As shown in Fig. 7, the number of switches is reduced from $1 + 2^{N_{DAC}}$ to 8 only. The number of switches can be minimized to 0.5OSR.

As shown above, the smaller the OSR is, the lower the complexity of the switching logic and routing lines are required. As the OSR and the number of taps decrease, however, the burden of the following LPF can be increased in many cases to meet a certain linearity target. When the OSR is decreased, the order of the sampling harmonics also gets lower, and their magnitudes get higher according to (2). Consequently, the following LPF is required to have higher attenuation characteristics. Moreover, the cut-off frequency of LPF should be lowered when f_{SG} decreases. It is hard to implement an LPF that has both a low cut-off frequency and high attenuation characteristic with a small area. Thus, it is important to optimize the OSR and the number of taps. For instance, in [51], [52], a DAC with 33 taps with OSR of 64 and a second-order g_m-C filter are adopted to generate a single-ended DAC-based sinusoid. Its routing area is decreased

by 87% compared to that of an alternative with 256 taps without an LPF [52]. The g_m-C filter is chosen because a low cut-off frequency can be implemented with a small area by utilizing a small g_m. Due to its hardware simplicity, the DAC structure shown in Fig. 7 has been widely adopted in the waveform stage of various on-chip SSGs with OSR from 8 to 32 [59]–[63].

To reduce the burden of LPF, a linear interpolation technique is proposed for a sinusoidally 65-tapped DAC [63]. It employs one additional fine DAC, which interpolates rapidly between two voltage levels that are generated by the main DAC. As the fine DAC's bit resolution improves, the resulting transfer function becomes closer to the square function of (2) [64]. Although the interpolation attenuates the sampling harmonics further, the fine voltage levels should be generated very quickly. Inevitably, the required clock speed of the interpolation DAC is higher than that of typical DAC-based SSGs without interpolation. To address this issue, chain delay lines are used for the interpolation [64]. It can attenuate the sampling harmonics without increasing the required clock speed.

Besides, in order to reduce both unit components and switching logics, DAC-based sinusoids with a small N_{DAC} and a small OSR have been employed in spite of their large harmonics [38], [44], [45], [50], [65]–[67]. For instance, $N_{DAC} = 3$ [44], [45] and 20 unit cells [65] are adopted with OSR $= 16$. Although the complexity and area can be reduced thanks to the reduced N_{DAC} and OSR, these waveforms need sufficiently steep filtering to attenuate not only the sampling harmonics but also the low-order harmonics. Implementation of filters is reviewed in detail in Section IV.

As an alternative technique to generate these DAC-based sinusoids with low N_{DAC}, delta-sigma modulation (DSM) has been adopted in SSGs [38], [66], [67]. DSM with oversampling reduces the in-band quantization noise by shifting it to the out-band. The shaped out-band noise can be more easily filtered out by an LPF. While an EIS system adopting a single-bit DSM without an explicit LPF is verified using external instruments and board-level design [68], [69], on-chip SSGs based on DSM typically include an LPF to achieve high linearity [38], [66], [67]. A simple RC LPF [66] and a 2nd-order g_m-C LPF [38] are adopted for attenuating the fast-moving out-band noises, finally generating a cleaner sinusoidal signal. In other way, an FIR-filter-embedded DAC is demonstrated to attenuate the remaining harmonics further while reducing the analog LPF's area [67]. In some works, higher-order multiple-bit DSMs are used to improve the linearity of the output sinusoids instead of using single-bit first-order DSMs. The higher N_{DAC} and the order of DSM are, the lower the in-band quantization noise becomes. In [38], a capacitor DAC with N_{DAC} of three and a 3rd-order DSM are used. In addition, a pseudo-random number generator (PRNG), which feeds random values to the digital input signal of the DSM, is adopted for removing the periodicity of the signal generated DSM, thereby spreading the power of harmonics over a frequency range. In summary, by utilizing DSMs in SSGs, better linearity can be achieved. In addition, they need a very low N_{DAC}, thereby reducing the DAC-related hardware complexity. However, it is difficult to increase f_{SG} due to high OSR when the system clock speed is limited. For example, in [67], the maximum f_{SG} is 20 kHz only with f_S of 2 MHz due to its oversampling.

To adopt a low N_{DAC} without employing DSM or LPF, a technique to control the transition timings of a DAC with three levels only, i.e., +1, 0, and –1, is proposed [50]. Among the harmonics less than the 10th order, the 5th-order harmonic of the injected signal is suppressed by controlling the transition times between the three levels. In addition, the demodulation signal in the EIS demodulator is also generated with these three levels, now with different transition timings so that the signal's 3rd and 9th-order harmonics are suppressed. Only the 7th-order harmonic remains as an error source among the harmonics less than the 10th order during the demodulation. With this technique, the errors caused by the low-order harmonics are effectively reduced with three voltage levels only. However, it still needs a very fast clock speed ($30 f_{SG}$) to accurately control the transition times between the levels.

B. Square Waveform

The square waveform, which is basically a digital clock, is another widely used base waveform in on-chip SSGs due to its simple implementation and low required clock speed. Especially, the 50%-duty-cycle-ratio square waveform has been widely adopted as the base waveform because its even-order harmonics are ideally zero and practically very low. However, it includes significantly large odd-order harmonics. When the 50%-duty square waveform is solely used as the injection signal for the general on-chip EIS system shown in Fig. 2(a), odd-order harmonics of the 50%-duty square waveform are folded to the final output, resulting in significant errors. There are several on-chip EIS systems that can accept such errors while targeting low power consumption and simple hardware implementation [70]–[72]. But, most on-chip EIS systems have adopted the square waveform with the following additional techniques to avoid the folded errors: linearity enhancement techniques [24], [73], use of one more down-conversion stage in the demodulator [74]–[80], or error cancellation algorithms [29], [81].

The most straightforward way to adopt the 50%-duty square waveform in on-chip EIS systems is to use some linearity enhancement techniques in the following stage. Filters can attenuate the harmonics of the square waveform. Because the largest harmonic is the 3rd-order harmonic, which is too close to the fundamental tone, a very steep characteristic is required for the filter. Another approach is to add one more down-conversion stage in the demodulator. This additional stage down-converts the input signal from f_{SG} to an intermediate frequency (IF). By this down-conversion and quadrature demodulation, the harmonics are not folded onto the IF. Then, the second down-conversion is performed from the IF to DC. The remaining down-converted harmonics generated during the two-step down-conversion can be attenuated more easily. More details of the demodulator are well-reviewed in [21]. Finally, simple error-cancellation algorithms, which are based on the fact that the magnitudes of the square waveform's harmonics are known, are demonstrated [29], [81].

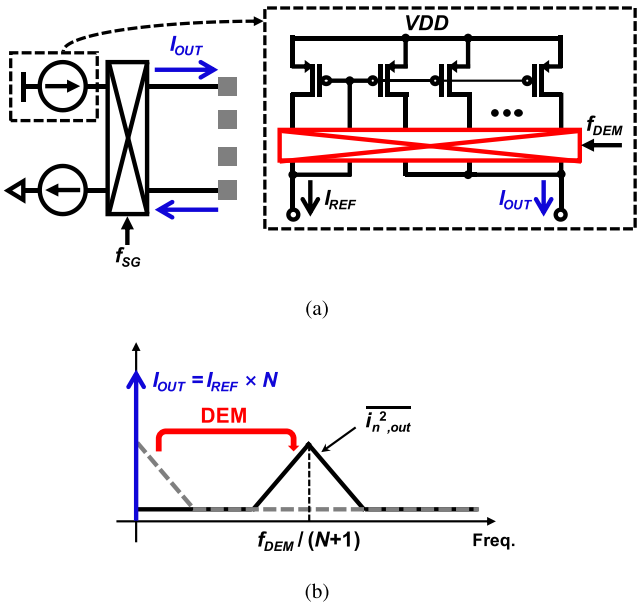


Fig. 8. (a) A square waveform generator based on a single-bit current DAC whose current source employs a dynamic element matching (DEM) technique. (b) Noise characteristics of the square waveform generator with DEM.

In terms of implementation, a single-bit DAC can generate the square waveform. Like DAC-based sinusoids, the square waveform can be generated by resistor-, capacitor-, or current-DACs. Among them, the current DAC has been widely adopted for injecting the square-waveform current directly to the target impedance [70]–[72], [74]–[80]. The SSG's hardware complexity can be greatly reduced by directly injecting the current into the target material without an additional current driver.

Fig. 8(a) shows an example of a single-bit current DAC. It is composed of a sinking current source, a sourcing current source, and a chopper. The chopper operating at f_{SG} multiplexes the two current sources to generate the square waveform. $1/f$ noise of the current sources often becomes the bottleneck limiting the measurement sensitivity of the on-chip EIS system for monitoring bioimpedance activities, such as respiration and body fluid change, which ranges less than 10 Hz [76], [77]. The DEM can be adopted to mitigate the $1/f$ noise, improving the noise performance of the on-chip EIS system. The unit transistors in each current source are swapped sequentially at the DEM frequency f_{DEM}. Then, $1/f$ noise of the transistors is up-converted to $f_{DEM}/(N+1)$, as shown in Fig. 8(b). N is the current gain of the current mirror. Since the $1/f$ noise is now far from f_{SG}, it can be more easily attenuated by using filters in the demodulator. But, the DEM cannot mitigate the noise from I_{REF}. To address this issue, a correlated noise cancellation technique is proposed and applied to an EIS demoulator [78].

Together with $1/f$ noise, it is also important to reduce the mismatch between the source and sink current sources in order to prevent the second-order harmonic [70]. The mismatch can be easily mitigated by adopting $N = 1$ with $f_{DEM} = 2f_{SG}$ (Fig. 8) [70], [74]. However, in this case, since the $1/f$ noise is also up-converted to f_{SG}, the noise cannot be mitigated. Thus, the square waveform generator in [76] adopts $N = 5$ to mitigate the $1/f$ noise while maintaining good matching characteristics. Here each current source has less than 1% current variation over their target PVT corners.

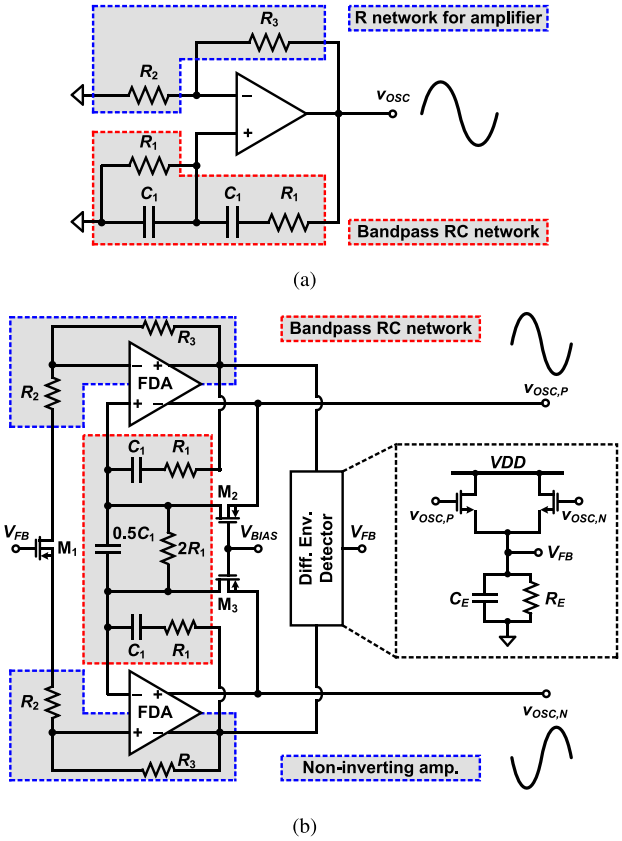


Fig. 9. Two sinusoidal oscillators based on Wien-bridge architecture: (a) a single-ended design [82], [83] and (b) a fully differential design [5], [28].

C. Oscillator-Based Sinusoidal Waveform

When on-chip EIS systems should support high f_{SG} with a limited system-clock frequency, the SSGs using oscillators, which do not require oversampling or DAC, can be a good alternative. Moreover, they do not require an LUT, which occupies a large area for a large memory size [52], [84]. Two types of oscillators have been adopted in on-chip EIS systems: RC-controlled and g_m-C-controlled structures.

RC-controlled structures, which are based on the Wien-bridge architecture, have been adopted in on-chip EIS systems that target f_{SG} less than 200 kHz [5], [28], [84]–[86]. Fig. 9(a) shows an example single-ended oscillator based on the Wien-bridge architecture [82], [83]. This oscillator is composed of an operational amplifier, a band-pass RC feedback network, and an R network. The RC feedback network forms a positive feedback loop with the amplifier, making the circuit oscillate. The R network forms negative feedback with the amplifier, amplifying the oscillating signal. The total loop gain of this oscillator in Fig. 9(a), $T(\omega)$, is expressed as follows:

$$T(\omega) = \frac{1 + \frac{R_3}{R_2}}{3 + j\left(\omega R_1 C_1 - \frac{1}{\omega R_1 C_1}\right)}. \tag{4}$$

It oscillates at the frequency when $|T(\omega)| \geq 1$ and $\angle T(\omega) = 0$. Therefore, when $1 + R_3/R_2$, which is the gain of the non-inverting amplifier, equals three, the oscillation frequency of the Wien-bridge architecture ($f_{OSC,WIEN}$) is expressed as follows:

$$f_{OSC,WIEN} = \frac{1}{2\pi R_1 C_1}. \tag{5}$$

Fig. 9(b) shows a block diagram of an example fully differential sinusoidal oscillator using Wien bridge for on-chip EIS systems [5], [28]. The fully differential design is adopted to suppress the even-order harmonics [85]. The band-pass RC feedback network and the two non-inverting amplifiers based on fully differential amplifiers (FDAs) induce an oscillation at $f_{OSC,WIEN}$. In [5], a differential envelope detector restrains the output swing by controlling the oscillator's loop gain. The envelope detector senses the amplitude of the output differential signals, and the sensed amplitude (V_{FB}) is fed to the gate of M_1 so that the gains of non-inverting amplifiers are adjusted. Then, the loop gain is changed accordingly, as shown in (4). In general, the initial gain of the non-inverting amplifiers is set to be greater than three to satisfy the oscillation condition. After starting an oscillation, the loop gain is lowered to stabilize the output swing within the linear output ranges of the FDAs while keeping the oscillation. Here the output swing is set to 200 mV and the 3rd-order harmonic of the output is less than –60 dBc [5]. Without the amplitude-control loop, this SSG has a 3rd-order harmonic of –42 dBc [85]. Although the oscillator shown in Fig. 9(b) achieves high linearity, the envelope detector requires a large-sized capacitor, which is too large to be integrated on-chip. An 1.8-nF off-chip capacitor is used with an 8-MΩ on-chip resistor, consuming a large area [28]. In order to avoid off-chip components, back-to-back diodes are connected in parallel to the feedback resistors in a replacement of the differential envelope detector and M_1 [86]. Diodes can be integrated inside the chip, but the THD of the oscillator is higher than –60 dBc.

These oscillators generate a sinusoidal signal without oversampling or DAC so that their achievable highest f_{SG} does not depend on the system clock speed. This makes the oscillator-based architectures more attractive than the DAC-based SSGs when it is required to generate sinusoids of high f_{SG} with low system-clock speed. However, these oscillators are not suitable for supporting a wide f_{SG} range. As shown in (5), the oscillation frequency is inversely proportional to the area of the passive components. Thus, the lowest f_{SG} is strictly limited by the die area. Furthermore, the highest f_{SG} is limited by the gain-bandwidth product (GBW) of the amplifiers. The linearity of these oscillators is dependent on the quality (Q) factor of the band-pass filter [86], [87]. Since the Q factor is strongly dependent on the gain of amplifier [84], a large GBW is required to obtain high linearity in the high-frequency region. For example, the FDAs in [84] has 80-MHz GBW to support f_{SG} up to 76 kHz with 2.38% THD. Similarly in [86], the amplifier has 10-MHz GBW to support f_{SG} of 100 kHz with THD of less than 1%. As the GBW is required to be about 100 times higher than the target f_{SG}, the maximum f_{SG} is limited by the achievable GBW in a given power budget.

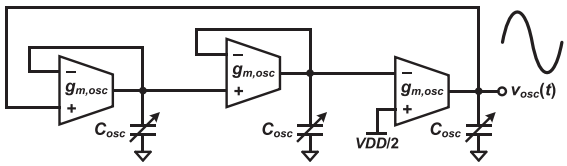


Fig. 10. An example g_m-C sinusoidal oscillator [89].

In addition, precise control of f_{SG} is much more difficult for the oscillator-based SSGs than other methods. In the oscillator-based SSGs, $f_{OSC,WIEN}$ is determined by the resistor and capacitor values, which are susceptible to process and temperature variations. Moreover, $f_{OSC,WIEN}$ is also dependent on the GBW of the amplifier [82], [83]. Note that the GBW can be varied not only by the process and temperature but also by the supply voltage. Thus, f_{SG} of these types of oscillators is prone to change by PVT variations. Although a technique combining two types of resistors, which have temperature coefficients of opposite signs, is employed in this type of oscillator to reduce the temperature dependency [88], it would still be challenging to obtain f_{SG} precisely due to other variations.

The g_m-C sinusoidal oscillator shown in Fig. 10 is used for an on-chip EIS system which supports a frequency range from 6.3 MHz to 22.6 MHz [89]. The output sinusoidal voltage ($v_{osc}(t)$) is expressed as follows [89]:

$$v_{osc}(t) = \frac{I_{SS}}{g_{m,osc}} \sin\left(\frac{g_{m,osc}}{2\pi C_L} t\right) \tag{6}$$

where $g_{m,osc}$ and C_L are g_m and the load capacitance of the g_m cell, respectively, and I_{SS} is the bias current. Since $g_{m,osc}$ is changed by both the frequency and the amplitude, C_L is controlled to sweep the oscillation frequency. Similar to the RC-controlled SSC structures, the g_m-C structure is also hard to achieve wide f_{SG} range and control f_{SG} precisely. The maximum f_{SG} is limited by both the maximum achievable $g_{m,osc}$ and the bandwidth of the transconductor. Particularly, this structure is considered hard to be adopted in on-chip EIS systems supporting low f_{SG} because of the large size of the required capacitor and the difficulty in obtaining a small and precise g_m. g_m and the capacitance are also prone to change by PVT variations.

D. Oscillator-Based Triangular Waveform

There are many practical difficulties in designing an oscillator that directly generates a sinusoidal waveform over a wide frequency range [90]. In particular, the linearity of the sinusoidal oscillators largely depends on the performance of the amplifiers in the oscillators, and a significantly large GBW is required, limiting the maximum f_{SG} with a given power budget. To address these issues, techniques based on triangular waveform generation have been proposed to reduce the burden of the oscillator itself, as shown in Fig. 11(a) and (b). Instead of generating a high-linearity sinusoidal signal, a low-linearity triangular waveform is generated first by a relaxation oscillator. Then, the following waveform shaper converts the triangle signal to a sinusoidal signal by using its transfer function, as shown in Fig. 11(b).

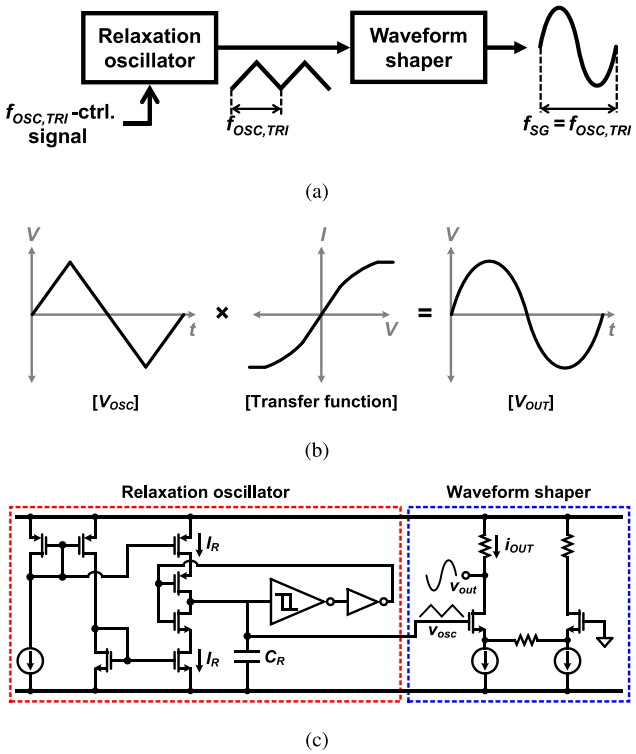


Fig. 11. (a) The block diagram of SSGs based on oscillator-based triangular waveform [90]–[92], (b) an operation principle of the waveform shaper [92], [93], and (c) a schematic of the SSG based on oscillator-based triangular waveform for EIS [92].

Various waveform shaper designs have been proposed to obtain a transfer function generating the output as close as the sinusoidal waveform [94]. Their waveform shaping is based on [94]: a polynomial approximation of $x(1-x^2)/(1+x^2)$ [95], [96], Taylor series expansion with low-order terms [90]–[93], [97], a sum of hypertangent functions [94], [98], [99], or a sum of parabolically spaced exponential functions [100].

Fig. 11(c) shows a schematic of an SSG using a relaxation oscillator for triangular waveform generation [92]. The frequency of the triangular waveform ($f_{OSC,TRI}$) is expressed as follows:

$$f_{OSC,TRI} = \frac{I_R}{2C_R(V_{ST,H} - V_{ST,L})} \tag{7}$$

where $V_{ST,H}$ and $V_{ST,L}$ are the upper and lower threshold voltages, respectively. $f_{OSC,TRI}$ can be controlled by adjusting I_R, C_R, and $V_{ST,H} - V_{ST,L}$. Since $V_{ST,H} - V_{ST,L}$ determines not only $f_{OSC,TRI}$ but also the amplitude of the triangular waveform, $V_{ST,H} - V_{ST,L}$ is mainly used for setting the amplitude of the triangular waveform, which determines the amplitude of the output signal. As shown in Fig. 11(b), the peak of the triangular waveform should be slightly saturated by the transfer function for obtaining the sinusoidal signal. Since the source degeneration resistor of the waveform shaper shown in Fig. 11(c) determines the saturation points, it should be properly determined by the target amplitude.

Compared to the DAC-based SSGs, the SSGs based on the triangular waveform have the same advantages as the SSGs based on sinusoidal oscillators. This method generates a sinusoidal signal without oversampling or DAC. Therefore, it is more suitable than the DAC-based SSGs when it is required to support high f_{SG} with low system clock speed. However, like the sinusoidal oscillator-based method, this method based on the triangular waveform is not suitable for supporting wide f_{SG} range and controlling f_{SG} precisely. The relaxation oscillator and the waveform shaper can easily support several MHz ranges. Therefore, the SSGs based on the triangular waveform are more suitable to support high f_{SG} than the SSGs based on sinusoidal oscillators. Yet, the lowest f_{SG} is strictly limited by die area because $f_{OSC,TRI}$ is inversely proportional to the capacitance as shown in (7). In addition, compared to the DAC-based SSGs, the precise control of f_{SG} is also more difficult for the SSGs based on the triangular waveform because $f_{OSC,TRI}$ is determined by the capacitance, resistance, and threshold voltages, which are vulnerable to PVT variations.

The on-chip SSG in [92] achieves 0.41%-THD when $f_{SG} = 1$ MHz. This THD is very close to the THD in [97], which is implemented using discrete MOS transistors, and even higher than f_{SG} achieved by sinusoidal oscillators in [5] and [28]. However, according to the simulations results in [92], the THD strongly depends on the circuit parameters such as the size of input pairs and the magnitude of current sources in the waveform shaper. The 0.41%-THD is obtained when input pairs are operated in the moderate inversion region, but the THD is degraded to 1.59% when the input pairs are operated in the weak inversion region. Moreover, in order to achieve high linearity by setting appropriate saturation points of the triangular waveform, all the circuit parameters should be set very carefully in consideration of PVT variations.

The SSG in [101] also adopts a triangular waveform as its starting waveform. This SSG uses a bandpass filter for attenuating the harmonics instead of a waveform shaper. By appropriately setting the parameters of the filter, i.e., order, bandwidth, filters can be more effective in the linearity enhancement compared to waveform shapers. Note that odd-order harmonics of the triangular waveform are lower than those of the 50%-duty square waveform. Adopting the triangular waveform makes the requirements of the filter more relaxed or improves the linearity when the same filter is adopted. Although ring oscillators have not been used in SSGs, they could be a good alternative. They also have much simpler hardware than the sinusoidal oscillators. And, they do not use an amplifier. However, the output of ring oscillators is typically similar to a square waveform.

E. Trade-Offs and Summary

DAC-based sinusoids can achieve high linearity by increasing the OSR and/or N_{DAC}. However, there is a trade-off between the OSR and f_{SG} range. With a given clock speed in the system, the maximum f_{SG} is limited by the clock speed:

$$f_{SG,\max} \leq \frac{f_{CLK}}{OSR} \tag{8}$$

where $f_{SG,\max}$ is the maximum f_{SG} that can be obtained with the given clock speed f_{CLK} and OSR. When f_{SG} is required to be higher for a given clock speed, the OSR should be reduced. It

makes the resulting sinusoidal output to have a higher sampling harmonics at lower frequencies, demanding a steeper filter. This trade-off is typically not a major issue in implantable and wearable EIS systems that support f_{SG} of less than several hundred kHz. For example, when a sinusoidal signal at f_{SG} of 200 kHz is required in implantable or wearable systems, an OSR of 100 can be achieved with a 20-MHz clock, which can be easily available. On the contrary, when the f_{SG} range needs to be high as several tens of MHz, this trade-off needs to be taken care of. In this case, a much higher clock speed is required, such as several hundreds MHz or higher, increasing the overall power consumption. Alternatively, the OSR should be lowered, requiring a steeper harmonic filtering.

DAC-based sinusoids have another trade-off between N_{DAC} and the area. As N_{DAC} increases, number of the unit components and switching logics increase, resulting in an increase of the required silicon area. Some optimization techniques, such as the method using DSM and the sinusoidally tapped DAC, have been demonstrated for reducing the area while maintaining the linearity. The DSM-based method can achieve a high area efficiency. However, it requires a high OSR, so its maximum supporting f_{SG} is limited by the reference clock speed. In contrast, the sinusoidally tapped DAC can be implemented with a lower OSR between 8 and 64. Thus, this method can support a high f_{SG} range up to several MHz for miniature EIS instruments. However, both of these methods require an LPF, so their minimum supporting f_{SG} is limited by the minimum achievable cut-off frequency of the following LPF.

The 50%-duty square waveform does not have the two trade-offs of DAC-based sinusoids since it is designed by a single-bit DAC and can be operated with a low-speed clock. Yet, when a sinusoidal signal is generated from the square waveform after filtering, the frequency range, power, linearity, and area are strongly dependent on the performance of the filter. Therefore, some on-chip EIS systems directly use the square waveform without filtering. Particularly, for wearable EIS systems [76]–[79], the 50%-duty square waveform has been widely used with a demodulator using one more down-conversion stage and an intermediate frequency. This method using an additional down-conversion can reduce the harmonic folding errors compared to the direct conversion to DC.

Sinusoidal oscillators have a trade-off between the maximum supporting f_{SG} and power consumption due to the requirement of high GBW of the amplifiers. Their lowest supporting f_{SG} is limited by the area because its oscillation frequency is determined by the passive components. The lower the oscillation frequency, the larger the required area for the components. Therefore, these oscillator-based SSGs have been used in wearable EIS systems covering a f_{SG} range that is neither too high nor too low, such as from 0.1 kHz to 200 kHz [5], [28], [84], [85]. Moreover, they can support only a few frequencies within the frequency range because the frequency is controlled by changing the component value. For example, the oscillator in [28] only supports four frequencies within the f_{SG} range from 0.1 kHz to 100 kHz. Triangular-waveform-based relaxation oscillators can relax the trade-off between the maximum supporting f_{SG} and power consumption to some extent by avoiding the use of high-GBW amplifiers. However, when the waveform shaper is used in triangular-waveform-based relaxation oscillators, the linearity is greatly susceptible to the PVT variations. When the triangular waveform is converted to a sinusoidal signal by a filter, the filter specification can be more relaxed than the case using the square waveform as the starting waveform.

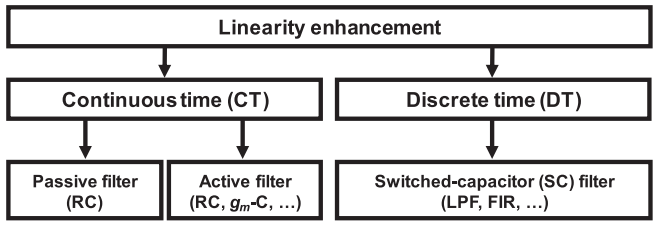


Fig. 12. Categorization of linearity enhancement techniques using filters in on-chip EIS systems.

IV. Linearity Enhancement

Some of the base waveforms like DAC-based sinusoids with low N_{DAC} and the 50%-duty square waveform are not highly linear intrinsically, including unwanted harmonics. These unwanted harmonics are likely to be folded onto the final impedance measurement result during the impedance demodulation process, causing significant errors in the result, as shown in Fig. 2(b). Hence, these harmonics should be further attenuated for more precise EIS systems.

The linearity of the SSG output waveform can be enhanced typically by filters, which can attenuate the unwanted frequency tones. They have been widely adopted to attenuate the harmonics of DAC-based sinusoids and the 50%-duty square waveform, but they can also be used to further attenuate the harmonics of the waveforms generated by oscillators [101].

Fig. 12 shows an overall categorization of filters employed in the linearity enhancement stage of on-chip SSGs. They can be largely divided into two types of filters: CT and DT filters. CT filters can be further categorized into two types: passive and active filters. Among passive filters, RC filters are widely employed in many designs because inductors are difficult to be integrated on-chip due to their large size. Active filters, including active RC and g_m-C filters, have been adopted to control various circuit parameters more easily, such as the gain, the type of frequency response, and Q factor. In general, attenuation of CT LPFs gets smaller as the frequency decreases, so it is difficult for them to attenuate low-order harmonics. Moreover, when the EIS system needs to support a low f_{SG}, the CT LPF requires a very small g_m and/or very large-sized passive components.

In order to improve the attenuation of low-order harmonics and offer low cut-off frequencies without large-sized passive components, DT filters based on switched-capacitor (SC) circuits have been employed in SSGs. DT filters can easily control the cut-off frequency by changing the sampling frequency, thereby easily achieving low and wide f_{SG} ranges. The low-order harmonics can be attenuated further by using the nulls located at the low-order harmonics and/or their high-order roll-off.

The following subsections review various CT and DT filters adopted in on-chip SSGs more in detail. For each filter type, basic characteristics and various circuit techniques that can improve the SFDR or THD of on-chip SSGs are discussed.

A. Linearity Enhancement in CT Domain

CT filters have been widely adopted in on-chip SSGs [35], [36], [38], [39], [44], [45], [47], [51], [52], [59], [62], [63], [73], [101], [102]. The most simple but fundamental CT filter is passive RC LPFs. RLC or RL filters can be used for SSGs in the board-level design, but these filters are not suitable for on-chip implementation because inductors typically require to occupy a very large chip area. A passive RC LPF is adopted in [45]. Two first-order RC LPFs are cascaded to attain a sufficient degree of attenuation of the harmonics. An unit-gain buffer can be optionally used for ensuring that the response is not affected by the preceding circuit. The resistances and capacitances can be varied for changing the bandwidth of the LPF. In [45], this filter is used to suppress the sampling harmonics of the DT signal with a constant OSR of 16. Here f_{SG} is varied from 1 kHz to 2.048 MHz, so the location of the largest sampling harmonic is changed from 15 kHz to 30.72 MHz. Attenuation of this harmonic over such a wide range can be done by changing the cut-off frequency of the LPF according to f_{SG}. In contrast, a constant f_S can be used with a high OSR while covering a range of f_{SG} as in [35]. Then, the sampling harmonics are located near the fixed f_S, so the cutoff frequency of the LPF can be fixed.

Although passive RC filters typically involve simpler implementation, active RC filters have been chosen over passive filters in several cases [47], [62]. Active RC filters can have additional gain and higher Q factor compared to passive ones. A larger output amplitude can be obtained through the additional gain, and the harmonic can be more attenuated through the high Q factor.

As an example, Fig. 13(a) shows a second-order active RC LPF adopted in [47]. The filter consists of two first-order LPFs. Although the frequency response of this active RC LPF can be implemented similarly by using passive LPFs, this active RC LPF can offer a large signal gain. The SSG, which adopts an 8-bit DAC and this active RC filter, attenuates all the unwanted harmonics less than –58 dBc [47].

Fig. 13(b) shows another 2nd-order active RC LPF, which is called Tomas biquad LPF [103]. The biquad LPF can adjust the quality factor (Q factor), bandwidth, and gain. The Q factor of the biquad LPF is expressed as follows:

$$Q = \frac{R_T}{\sqrt{R_2 C_2}} \sqrt{\frac{C_1}{C_2}}. \tag{9}$$

Here R_T can be used to change the Q factor while the other values are used for setting the bandwidth and gain. A constant gain in the pass-band region near the cut-off frequency of LPF ($f_{C,LPF}$) can be achieved by setting the Q factor higher than that of its passive equivalent. When $f_{C,LPF}$ of each 1st-order LPF in Fig. 13(a) is set to f_{SG}, the output sinusoidal signal is attenuated by 6 dB. Therefore, $f_{C,LPF}$ must be higher than f_{SG} to avoid such amplitude degradation. For example, in [45],

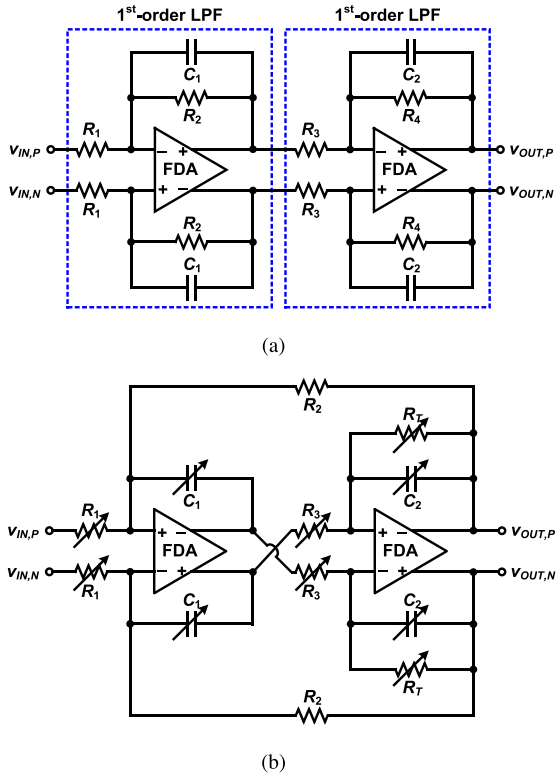


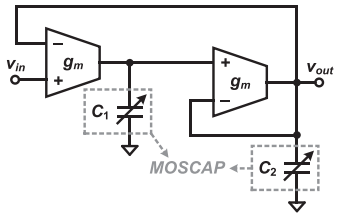
Fig. 13. Example active RC filters: (a) a 2nd-order active RC LPF for an on-chip SSG [47] and (b) a 2nd-order Tomas biquad RC LPF [103].

$f_{C,LPF}$ is chosen as $2.5 \times f_{SG}$ to reduce the degradation. On the contrary, $f_{C,LPF}$ of the biquad LPF can be reduced thanks to the constant pass-band by the improved Q factor. Consequently, this structure can achieve better attenuation of the harmonics by locating $f_{C,LPF}$ close to f_{SG}. To prevent an overshoot near the $f_{C,LPF}$, the Q factor should be appropriately set to about 1. When Q factor equals 1, the resulting overshoot is 0.69 dB.

Both passive and active RC filters cannot offer a low $f_{C,LPF}$ easily because $f_{C,LPF}$ of RC filters is inversely proportional to the resistance and capacitance. Bulky resistors and capacitors, which occupy larger areas, are needed to implement a low f_{SG}. For example, 3-Mohm resistors and 153.6-pF capacitors are used to generate f_{SG} of 1 kHz in [45]. Note that some EIS applications require generating sinusoidal waveforms of very low frequency (below 1 kHz), as shown in Fig. 1(b). It is not practically possible for passive or active RC filters to support cutoffs lying in such a low-frequency range due to large-sized passive components, which require to occupy a prohibitively large die area. The minimum f_{SG} of the SSG adopting a passive RC LPF is 1 kHz in [45] and that of SSG adopting the active RC LPF is 15.625 kHz in [47].

Alternatively, active g_m-C filters have been adopted for decreasing the minimum f_{SG} with small die area [38], [39], [44], [51], [52], [59], [73], [101], [102]. Fig. 14 shows a 2nd-order biquad g_m-C LPF, which is adopted in [52]. $f_{C,LPF}$ of this g_m-C LPF is expressed as follows:

$$f_{C,LPF} = \frac{1}{2\pi} \sqrt{\frac{g_m}{C_1 C_2}}. \tag{10}$$



Cutoff freq. (Hz)	g_m (S)	C_1 (F)	C_2 (F)
250	9n	7.5p	3.7p
2k	60n	5.0p	2.5p
20k	600n	5.0p	2.5p
200k	600n	0.5p	0.25p

Fig. 14. A 2nd-order biquad g_m-C LPF adopted in [52].

A low $f_{C,LPF}$ can be implemented by lowering g_m without the need for bulky resistors and capacitors. The minimum achieved $f_{C,LPF}$ here is 250 Hz, which is much smaller than that of [45], [47]. Moreover, $f_{C,LPF}$ of g_m-C filters can be adjusted by tuning g_m, which can be more easily controllable than passive components. g_m-C filters typically occupy a smaller area than the equivalent RC filters for a given order and $f_{C,LPF}$. However, in general, the linearity of g_m-C filters is poorer than that of active RC filters [104]–[106], and thus g_m cells should be carefully designed not to degrade the linearity of the output.

When CT filters are employed for a waveform whose low-order harmonics are more dominant, the required order gets higher. High-order CT filters need more active circuits and passive components, which result in higher power and area consumption, respectively. For example, in [73], to generate a sinusoidal signal with THD $= 1.40\%$ and SFDR $= 36.67$ dB from the 50%-duty square waveform, a high-order g_m-C filter which consists of 12 g_m cells and 6 capacitors is required. Similarly in [102], a high-order CT filter, which cascades seven g_m-C integrators coupled with high-pass filters between the stages, is adopted to achieve THD of –51 dBc and SFDR of 51 dB from the 50%-duty square waveform.

Due to such hardware and power overhead of higher-order CT filters, the 1st-order and 2nd-order CT filters have been more widely used in on-chip SSGs for EIS systems [38], [39], [44], [45], [47], [51], [52], [59], [62], [63], [101]. They occupy less die area and do not consume a lot of power. However, they are not suitable for attenuating low-order harmonics, and thus they have been mainly employed along with DT starting waveforms, of which low-order harmonics are already suppressed by a high-complexity DAC with high $N_{DAC} \geq 6$ [39], [47], [63] or a large number of unit cells [51], [52], [59], [62]. In addition, DSMs in the waveform generation stage [38], [66], [67] or FIR filters in front of the CT LPF [44], [45] have also been employed for the same purpose. Similarly, a second-order CT filter has been adopted to generate a sinusoidal signal from a triangular waveform, which has smaller low-order harmonics compared to the 50%-duty square waveform [101]. In applications using other waveform generation techniques, additional types of filters have also been used along with low-order CT filters. In such scenarios, the CT filters mainly serve the purpose of attenuating the higher harmonics, which are caused by the sampling operation in DAC-based sinusoids.

Besides, CT filters have two main disadvantages. First, their frequency responses are vulnerable to PVT variations. $f_{C,LPF}$ of RC filters is determined by the absolute values of the resistance and capacitance. The capacitance is vulnerable to the process variations, and the resistance is vulnerable to the process and temperature variations. In the case of the g_m-C filters, $f_{C,LPF}$ is determined by g_m and the capacitance. g_m is very vulnerable to PVT variations. As a result, it is difficult for RC and g_m-C filters to obtain a precise $f_{C,LPF}$. To improve the preciseness, a calibration scheme is required [107]. Second, their low $f_{C,LPF}$ range is limited by the area occupied by passive components, especially capacitors. Although there is a method that reduces the chip area by adopting an extremely low g_m of 9 nS and a MOS capacitor [51], [52], these make the filter more susceptible to PVT variations.

B. Linearity Enhancement in DT Domain

DT filters have been adopted for controlling $f_{C,LPF}$ precisely, supporting low f_{SG} ranges, and/or achieving high attenuation of low-order harmonics. Since DT filters are a sampled-data system, its frequency response can be controlled simply by changing f_S. Note that f_S can be easily adjusted by digital circuits like dividers with off-chip PVT-tolerant frequency generators, such as crystal oscillators. As such, $f_{C,LPF}$ of DT filters can be precisely adjusted regardless of PVT variations. In addition, low $f_{C,LPF}$ can be obtained by just reducing f_S without increasing the sizes of passive components. Therefore, the area is not one of the main factors that limit the lowest f_{SG} in DT filters. Moreover, unlike CT filters adopted in on-chip SSGs, DT filters can attenuate low-order harmonics more effectively by implementing high-order roll-off characteristic [24] or using inherent nulls of FIR functions [44], [45]. The remaining part describes how to obtain high-order roll-off and FIR response in the DT domain and use them in the linearity enhancement in SSGs, respectively.

1) Techniques Using High-Order Roll-Off of DT Filters: Large-sized equivalent inductance and capacitance can be implemented by SC integrators with small-size capacitors only, thus allowing a high-order filter with low $f_{C,LPF}$ to be integrated on-chip. As a result, an SSG that adopts a simple waveform and supports a wide f_{SG} range can be implemented. Here is an implementation example [24]. By implementing a 5th-order Chebyshev type-I frequency response in the DT domain, even the 50%-duty square waveform, which is the simplest waveform among the starting waveforms of on-chip SSGs, can be adopted. Because this SSG adopts the 50%-duty square waveform, $f_{C,LPF}$ should be adjusted according to f_{SG} over the wide frequency range of six decades. Moreover, the filter should attenuate the low-order harmonics sufficiently. Attenuations of 41 dBc and 51 dBc are required to reduce the 3rd-order harmonic of the 50%-duty square waveform to less than 50 dBc and 60 dBc, respectively. A DT filter based on SC integrators can be adopted for achieving such high attenuation of low-order harmonics with wide $f_{C,LPF}$ range. Such DT filters can be implemented using equivalent LC ladders. Fig. 15(a) shows an LC-ladder-based 5th-order Chebyshev type-I LPF with 1-Hz corner frequency and 0.5-dB pass-band ripple [24]. Although LC values are scaled down as $f_{C,LPF}$ increases, the values are still too large to be implemented on-chip. Moreover, it is difficult to accurately change the inductances and capacitances

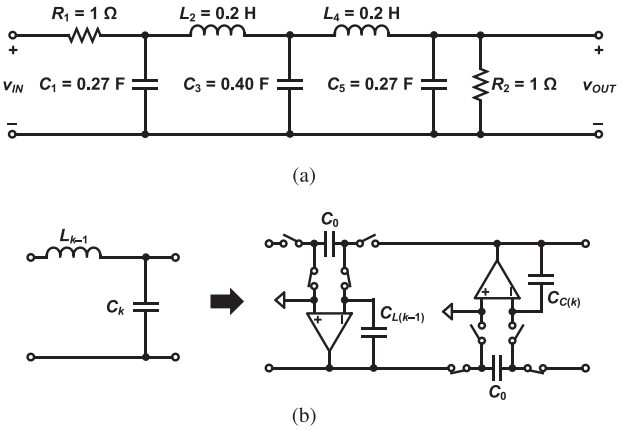


Fig. 15. (a) The 5th-order Chebyshev type-I LPF using LC ladders with 1-Hz $f_{C,LPF}$ and 0.5-dB pass-band ripple [24] and (b) implementation method of a LC pair with SC circuits [24].

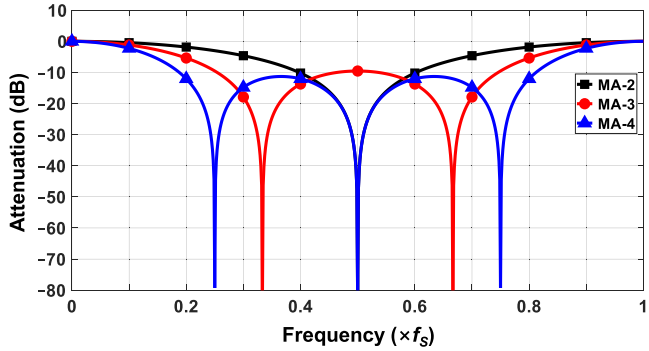


Fig. 16. Frequency responses of moving average (MA)-2, MA-3, and MA-4 filters.

for widely varying $f_{C,LPF}$. Alternatively, each LC pair of the LC ladder can be implemented with SC integrators by using the conversion method shown in Fig. 15(b). When R_S, which is the scaling resistance for calculating the LC values, is set to 1 Ω, the corresponding on-chip capacitances in the SC integrators are expressed as follows [24]:

$$C_{L(k-1)} = L_{k-1} C_0 f_S \tag{11}$$

$$C_{C(k)} = C_k C_0 f_S \tag{12}$$

where L_{k-1} and C_k are the targeted inductance and capacitance of the LC ladder, respectively. C_0 is the unit capacitance of the SC integrators. By using this conversion, large-sized inductors and capacitors can be replaced by SC integrators with small on-chip capacitors. When $C_0 = 300$ fF and $f_S/f_{C,LPF} = 100$, the maximum capacitance of 11.4 pF only is needed for designing the 5th-order DT LPF [24]. Thanks to this filter, the SSG achieves $< 0.1\%$ THD from the 50%-duty square waveform for f_{SG} from 40 mHz to 40 kHz.

The DT filters based on SC integrators have several advantages likewise. Compared to CT filters, they can accurately obtain $f_{C,LPF}$ because their equivalent inductance and capacitance (L_{k-1} in (11) and C_k in (12)) depend on f_S and a capacitor ratio, not on any active or passive components like g_m, R, or C. Moreover, $f_{C,LPF}$ can be adjusted by changing f_S over a wide frequency range. In addition, high-order roll-off and low-$f_{C,LPF}$ filters can be integrated on-chip because large-sized passive components can be implemented by using small-size capacitors.

On the other hand, the DT filters based on SC integrators have two main disadvantages: 1) a trade-off between area and power consumption and 2) difficulty in supporting high f_{SG} ranges. As shown in (11–12), f_S should be increased to reduce $C_{L(k-1)}$ and $C_{C(k)}$ for given L_{k-1} and C_k. As f_S increases, the bandwidth of the amplifiers in the SC integrators should also be increased to be much larger than f_S, which results in the increase in the power consumption of the amplifiers. Second, this type of DT filters is not suitable for supporting a high f_{SG} range with a given f_S because it needs a high OSR for reducing the area. Moreover, since the required power consumption of amplifiers is proportional to f_S, there is another trade-off between the power consumption and the maximum f_{SG}.

2) Techniques Using Nulls of FIR Functions: Because DT filters based on FIR functions can attenuate the low-order harmonics at a low OSR, they have been adopted to increase the highest f_{SG} range [44], [45]. In order to see how the FIR functions can attenuate the low-order harmonics with a low OSR, Fig. 16 shows frequency responses of the MA-2, MA-3, and MA-4 filters, which are the basic and representative FIR filters. From 0 to f_S, the MA-N filters have several nulls at integer multiples of f_S/N. These frequency responses are repeated for every f_S according to the sampling theory. These nulls can be used to attenuate the harmonics by locating them exactly at the harmonic frequencies. The null positions can be varied by changing the weights of the input samples [108], [109]. For example, in [108], the null positions are analyzed when three consecutive sample weights are [1, α, 1]. As shown in Fig. 16, the MA-3 filter of which sample weights are [1, 1, 1] has two nulls at $f_S/3$ and $2f_S/3$. When $1 < \alpha < 2$, the null at $f_S/3$ is moved to a position between $f_S/3$ and $f_S/2$. At the same time, the null at $2f_S/3$ is also moved to a position between $f_S/2$ and $2f_S/3$. In [109], the required sample weights for attenuating the odd-order harmonics are found for OSR of 6, 8, 10, 12, 14, and 16.

As a practical implementation example, a block diagram of an SSG based on DT FIR filter is shown in Fig. 17(a) [45]. Since the DT filter operating with OSR of 16 can attenuate the low-order harmonics by using the frequency response shown in Fig. 17(b), the SSG can adopt a simple waveform generated by an 8-tap DAC with N_{DAC} of 3 and OSR of 16. The DT frequency response in Fig. 17(b) is obtained from sample weights of [1, 1, 1.4, 1.4, 1, 1]. The block diagram of the DT FIR filter with these sample weights is shown in Fig. 17(c). The DT FIR filter has nulls at $3f_{SG}$, $5f_{SG}$, $8f_{SG}$, $11f_{SG}$, $13f_{SG}$, attenuating the 3rd- and 5th-order harmonics effectively. Although there is no null at $7f_{SG}$ and $9f_{SG}$, the null at $8f_{SG}$ along with the following CT LPF attenuates the 7th and 9th harmonics by about 35 dB. Therefore, all the low-order harmonics other than 15th harmonic can be suppressed effectively. Since both

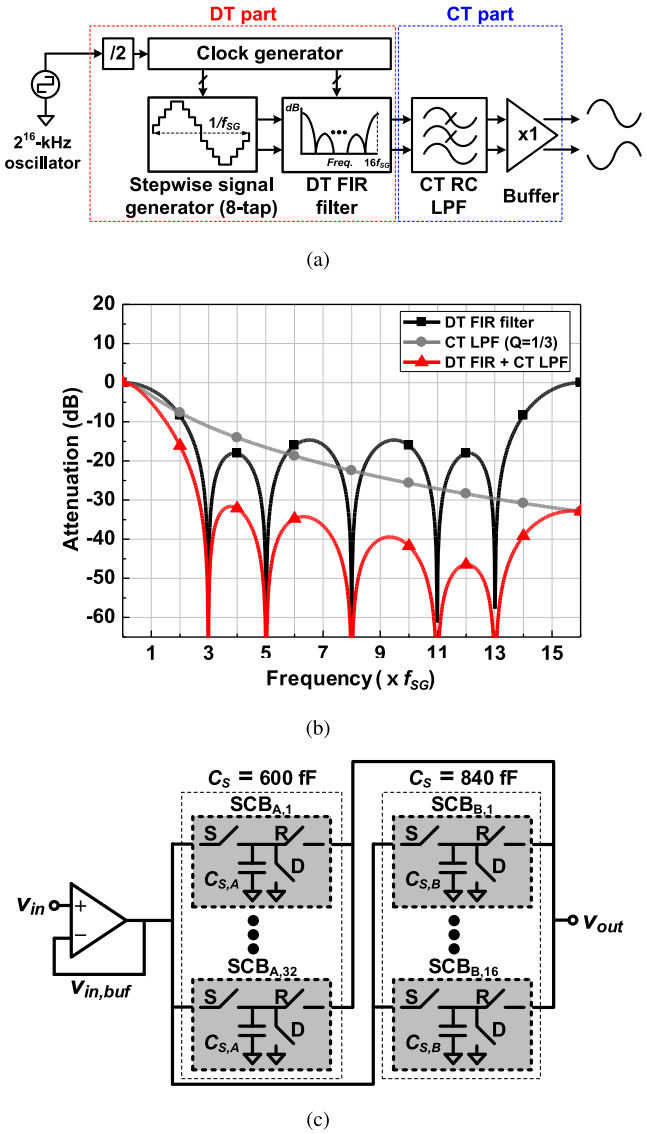


Fig. 17. A SSG based on DT FIR filter [45]: (a) a block diagram of the overall architecture, (b) frequency responses of the DT and CT filters, and (c) a block diagram of the DT FIR filter.

the starting waveform and the DT filter operate with OSR of 16, the 15th harmonic still needs to be attenuated further, so the following 2nd-order passive RC LPF attenuates it and other high-order sampling harmonics near the integer multiples of f_S. In summary, this SSG effectively attenuates the low-order and high-order harmonics using the combination of DT and CT filters so that it can use a simple starting waveform and low OSR. Thanks to the low OSR, this SSG is more suitable for obtaining higher f_{SG} compared to other SSGs based on SC integrators. On the other hand, since this structure requires a low-order CT filter, the lowest f_{SG} is limited by the minimum achievable $f_{C,LPF}$ of the CT filter. This achieves 0.2% THD_{10} and 0.7% THD_{40} for f_{SG} from 1 kHz to 2.048 MHz. Since the frequency response of the DT filter can be adjusted by controlling f_S, a lower f_{SG} can be supported by replacing the RC filter with a g_m-C filter.

Two other types of DT filters have been adopted for on-chip SSGs [44], [109]. The DT filter in [44] uses a g_m cell instead of the voltage buffer in Fig. 17(c). As a result, the gain of the DT FIR filter in [44] is proportional to T_S since the charge accumulated on the sampling capacitor is proportional to T_S. To compensate for such dependence, the SSG embeds a gain control function in the following active g_m-C filter. However, the gain control range limits the possible f_{SG} range.

Another type of DT FIR filters is employed in the SSG which generates sinusoidal signals from 150 MHz to 850 MHz [109]. To obtain the target input sample weights, a current is generated from the input voltage signal using a variable resistor. The current is accumulated on a sampling capacitor. Thus, the sample weights can be obtained by controlling the resistance of the variable resistor (R_V). In this design, $2\pi R_V C_S \ll 1/f_{SG}$ should be met when C_S is the capacitance of the sampling capacitor. Thus, a wide f_{SG} range is difficult to support. To support f_{SG} of 1 kHz, Mohm-order R_V and nF-order C_S, which are too large to be integrated on-chip, are required. Therefore, this type of DT FIR filters is not suitable for designing on-chip SSGs for EIS systems.

Here is a summary of the DT filters. One of the main advantages of DT filters is their precisely scalable frequency response according to f_S. Therefore, DT filters are typically suitable for SSGs supporting a wide f_{SG} range. In addition, DT filters can achieve low $f_{C,LPF}$ by simply reducing f_S. Therefore, when an SSG adopts a DT filter without a CT filter, the SSG can support a low f_{SG} range without increasing the size of passive components. As a result, in [24], the SSG, which adopts a DT filter based on SC integrators, can generate a sinusoidal signal up to a very low f_{SG} of 40 mHz. However, since the DT filters based on SC integrators typically require a high OSR, its highest f_{SG} is limited by the system clock. In contrast, the SSGs using DT FIR filters can support higher f_{SG} due to their lower required OSR. However, since the high-order harmonics caused by the sampling operation should be attenuated, a following CT filter is typically required, limiting the lowest f_{SG}. The highest f_{SG} of [24] is 40 kHz with OSR of 100 and that of [45] is 2.048 MHz with OSR of 16. If 2.048-MHz is generated by the SSG in [24], a too high f_S of 204.8 MHz is required. Finally, unlike CT filters adopted in on-chip SSGs, DT filters can attenuate the low-order harmonics more effectively by using their high-order roll-off characteristics [24] and/or locating their nulls at the harmonics [44], [45]. For example, the 50%-duty square waveform is adopted by utilizing the 5th-order Chebyshev type-I frequency response in [24]. A simple waveform generated by a DAC with N_{DAC} of 3 is adopted by utilizing the enhanced attenuation at the low-order harmonics thanks to the nulls of the FIR filters [44], [45]. As a result, compared to on-chip SSGs based on CT filters, simpler starting waveforms can be adopted along with these DT filters.

C. Trade-Offs and Summary

Wide-frequency-range SSGs need to control $f_{C,LPF}$ of the LPFs over their wide frequency range. In this regard, CT filters have a trade-off between the minimum supporting f_{SG} and the area due to the passive components. Compared to RC filters, using g_m-C filters relaxes the trade-off because a low $f_{C,LPF}$

can be achieved by just lowering the g_m, not by increasing the size of passive components. Therefore, g_m-C filters have been employed for EIS systems that need to support a low f_{SG} range.

DT LPFs do not have the same trade-off because a low $f_{C,LPF}$ can be easily obtained by reducing f_S. As the OSR of a DT LPF increases, the values of passive components can be reduced, thus decreasing the required area. However, increasing the OSR may decrease the maximum f_{SG} for a given clock frequency. On the other hand, because DT FIR filters can be operated with a low OSR, a higher f_{SG} range can be supported. However, a lower OSR induces higher sampling harmonics at lower frequencies. Thus, a following CT filter is typically required, limiting the lowest supporting f_{SG} due to the area. Since the power consumption of DT circuits is normally higher than that of CT circuits, DT filters are not adequate for low-power implantable and wearable applications, but for miniature EIS instruments. In particular, DT LPFs based on SC integrators are suitable for supporting very low f_{SG}. In contrast, DT FIR filters with a low OSR are suitable for EIS systems that support high f_{SG}.

V. Current Drivers

When a current is injected to the tissue for impedance measurement, the current amplitude is likely to change by the tissue impedance variations due to the finite output impedance of the current driver. Without knowing the injected current exactly, accuracy of the impedance measurement cannot be ensured. By adding a reference resistor in series with the target impedance and measure the voltage across the resistor, the actual current that flows through the target impedance can be known for more accurate impedance measurements [30], [110]. However, this technique requires more circuits and power for measuring the voltage across the reference resistor. If the reference resistor is not used, the current driver of SSGs should have a large output impedance to provide a constant-amplitude current regardless of the target impedance. Furthermore, this output impedance should be kept large over a wide frequency range to provide a constant-amplitude current over an entire target frequency range. Besides, the driver should ensure the linearity of the sinusoidal signal as well.

Current drivers in SSGs can be largely divided into open-loop and closed-loop structures. Since the open-loop architectures inject a sinusoidal current without feedback, they can achieve a wider bandwidth with a given same power consumption and simpler hardware complexity than the closed-loop ones. In contrast, the closed-loop architectures inject a current with feedback so that it can achieve a larger output impedance and higher linearity and obtain more invariant transconductance compared to the open-loop ones. While a detailed review on current drivers can be found in [40] and [41], this section reviews main characteristics and representative structures in each category.

A. Open-Loop Current Drivers

The open-loop architectures have been adopted in on-chip SSGs because of their wide bandwidth and simple hardware implementation. In addition, they do not cause any oscillation at the output or have peaking in their frequency response.

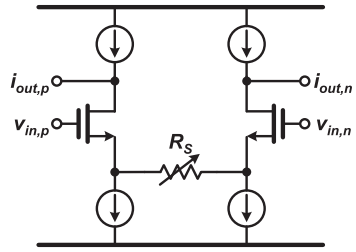


Fig. 18. An open-loop current driver using the source degeneration [5], [28], [84], [85].

The simplest open-loop method of injecting a current to an impedance is to generate a waveform using a current DAC and inject the DAC's output current directly to the target impedance [48], [53]–[57], [65], [70]–[72], [74]–[80]. Many of such current DACs use the cascode current-source structures to have an high output impedance [48], [53]–[57], [70], [77]. Among them, there are two advanced current mirrors with higher output impedance than the typical cascode structures: a regulated cascode structure [71] and a triple cascode structure [74]. The regulated cascode structure biases its cascode transistor through a negative feedback using an amplifier. When A is the amplifier's open-loop gain, an $(1 + A)$ times higher output impedance at DC can be obtained than the typical cascode structure, but at the expense of the additional current consumption of the amplifier. The triple cascode structure is adopted for further improvement in the output impedance without using an additional amplifier. However, the maximum injecting current is limited by their low voltage headroom, especially in low-supply designs. Especially, the DEM or chopping technique presented in Section III-B has been incorporated with the 1-bit current DAC for reducing the 1/f noise and/or the mismatch between the source and sink current sources.

The waveform generation and current injection can be merged by generating a waveform directly through the current DAC. But, most circuits for the waveform generation and linearity enhancement operate in the voltage domain, so it cannot be directly used for such merged structures. Instead, other types of DACs, oscillators, or circuits have been demonstrated with separate current drivers [5], [28], [38], [39], [47], [58], [59], [61], [62], [73], [84]–[86], [89], [101], [112].

Among them, many open-loop current drivers adopt a source degeneration resistor for better linearity [5], [28], [39], [47], [61], [84], [85]. Fig. 18 shows an example current driver using the source degeneration technique [5], [28], [84], [85]. When R_S is much larger than $1/g_m$ of the input transistors, the overall trasnconductance of the current driver (G_{DRV}) in Fig. 18 is as follows:

$$G_{DRV} = \frac{1}{R_S + 1/g_m} \approx \frac{1}{R_S}. \tag{13}$$

As shown, G_{DRV} depends on the resistor only, so it can achieve better linearity compared to the current driver generating a current output by using intrinsic g_m of the input transistors without the degeneration resistor. While g_m of the input transistors is likely to vary by the input signal amplitude and the bias voltage,

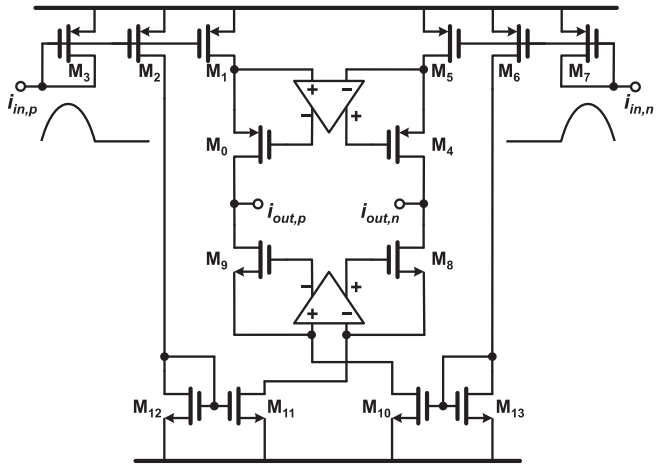


Fig. 19. An output stage of open-loop current driver with the regulated cascode output stage [111].

R_S is invariant regardless of them. As R_S increases, both the linearity and the output impedance increase, but G_{DRV} itself decreases. When G_{DRV} gets smaller, a large input signal is required for generating a same target current amplitude. The enlarged input signal varies g_m, degrading the linearity eventually. Alternatively, g_m can be increased, but at the expense of high power consumption. For alleviating the need of large g_m and high R_S, a current driver with an auxiliary low-dropout regulator (LDO) is proposed [39].

After these current drivers like the one in Fig. 18, an output stage shown in Fig. 19 can be cascaded for current multiplication and output impedance boosting. This output stage employs four current sources called H-bridge configuration for injecting the output current to the load in both directions. The two current sources driven by M_1 and M_{10} are active during the positive half cycle of the sinusoidal input. The other two current sources driven by M_5 and M_{11} are active in the following negative half cycle. The input current signal can be amplified by the current mirrors that consist of M_1–M_3 and M_5–M_7. In addition, the output impedance is increased by $(1 + A)$ times through the regulated cascode structure when A is open-loop gain of the amplifier. Since this output stage determines the maximum current range and the output impedance, the burden of designing the source degenerated transconductor in Fig. 18 can be relieved.

B. Closed-Loop Current Drivers

Closed-loop current drivers, which can offset the disadvantages of the open-loop structures, have been developed for on-chip SSGs [8], [58], [89], [101], [113]–[119]. In particular, most of the close-loop current drivers have been employed to be more robust to variations of circuit parameters such as g_m of the input transistors and parasitic capacitances [8], [58], [89], [113]–[119].

Fig. 20 shows one of the simplest implementations of closed-loop current drivers. It consists of a resistor (R_{CD}) and an amplifier while the target impedance (Z_m) is placed in the feedback of the amplifier [89]. Detailed analysis with actual circuit parameters of this structure can be found in [120]. The

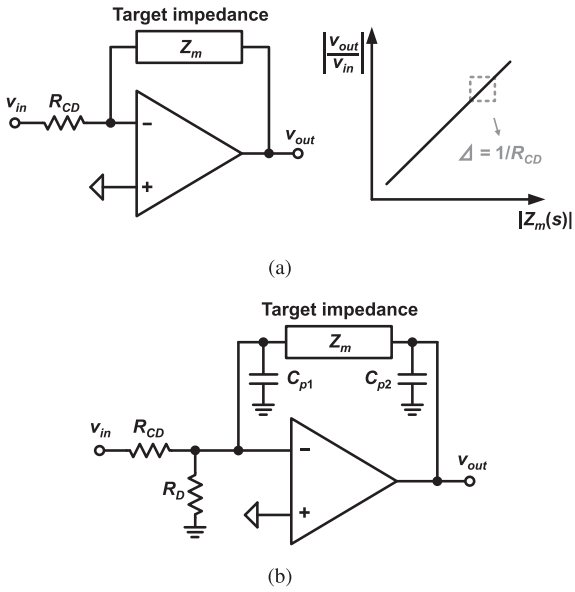


Fig. 20. (a) A closed-loop current driver based on the auto-balancing bridge and the gain ($\frac{V_{\rm out}}{V_{\rm in}}$) over the target impedance [89] and (b) a loop-stability compensation scheme for this structure [89].

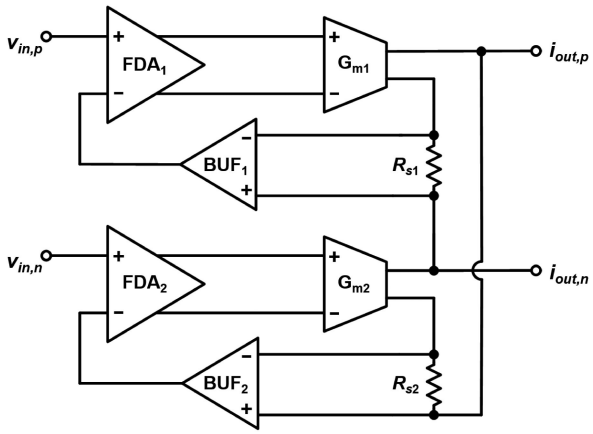


Fig. 21. A closed-loop current driver with a linear feedback [113].

input voltage ($v_{\rm in}$) is linearly converted to a current through R_{CD}. When the input impedance and open-loop gain of the amplifier is large enough, the current of $v_{\rm in}/R_{CD}$ flows into the target material, and the resulting voltage ($v_{\rm out}$), which will be demodulated, is linearly proportional to $Z_m(s)/R_{CD}$. The structure shown in Fig. 20(a) works well at low frequencies, but it is likely to become unstable at high frequencies due to parasitic capacitances. Fig. 20(b) shows a loop-stability compensation scheme adopted in [89] for the structure in Fig. 20(a). In order to reduce the effect from the parasitic capacitor at the input of amplifier (C_{p1}), a compensation resistor (R_D) is added. In [89], the phase margin increases from -20° to 36° by this scheme.

Besides, a linear feedback has been adopted to reduce the influence of the internal circuit parameter such as g_m of the input transistors of amplifiers, while achieving a high output impedance and a high enough G_{DRV} [8], [58], [113]–[117]. Fig. 21 shows an example of such closed-loop current driver with

linear feedback [58], [113]. Here two identical current-driving blocks operate in a balanced mode to minimize the common-mode voltage error across the load. Each current-driving block consists of a fully differential pre-amplifier stage (FDA_1, FDA_2), a following transconductance stage (G_{m1}, G_{m2}), a buffer (BUF_1, BUF_2), and a sensing resistor (R_{S1}, R_{S2}). Each of R_{S1} and R_{S2} senses the current, and each resulting voltage is fed back to the negative input terminal of the corresponding pre-amplifier through the buffer, which is implemented using a differential difference amplifier (DDA). When a resistive load (R_L) is assumed, G_{DRV} is expressed as follows [113]:

$$G_{DRV} = \frac{1}{R_s\left(1+\left(\frac{r_o+R_S+R_L}{r_o}\right)\frac{1}{AG_mR_S}\right)} \approx \frac{1}{R_S}, \quad (14)$$

where R_S is the resistance of two sense resistors, A is the gain of FDA_1 and FDA_2. G_m and r_o are g_m and the output impedance of the transconductance stages, respectively. When $r_o \gg R_S + R_L$ and $AG_mR_S \gg 1$, G_{DRV} depends on R_S only, which is not an internal parameter of any circuit blocks. Note that R_S in Fig. 18 should be much larger than $1/g_m$ of the input transistors for open-loop current drivers based on the source degeneration to obtain G_{DRV} as in (13). In contrast, this closed-loop current driver obtains G_{DRV} as in (14). Compared to the open-loop current driver, this current driver can further reduce the effect of G_m thanks the feedback. The output impedance of current driver ($R_{O,DRV}$) is also improved and is expressed as follows:

$$R_{O,DRV} = r_o + (AG_mr_o + 1)R_S. \quad (15)$$

A similar topology based on the same principle is applied to the current driver in [114]. In order to improve the bandwidth and linearity with lower power consumption compared to the current driver in [113], the current driver in [114] adopts differential difference transconductance amplifiers (DDTAs) instead of FDAs and adopts two single-ended buffers instead of differential-to-single-ended buffers. By doing so, $R_{O,DRV}$ is improved from 372 kΩ at 500 kHz [113] to 362 kΩ at 1 MHz [114]. In addition, the THD is improved from 0.53% [113] to 0.1% [114] for 1 mA_{pp} output signal.

Fig. 22 shows a closed-loop current driver using two current drivers for source and sink currents [8], [115]–[117]. In addition to the two current drivers, a buffer (BUF_1) is optionally used in [115] and [116] for feeding back the voltage signal more precisely. The source (master) current driver sources a current signal to the target impedance while the sink (salve) current driver sinks the current signal from the target impedance. The source current driver merges the FDA and the BUF of the structure shown in Fig. 21 to a differential difference transconductance amplifier (DDTA). A BUF_2 can be optionally added for driving low impedance loads [117]. Like the current driver in Fig. 21, this also obtains a reliable G_m and an increased $R_{O,DRV}$.

However, these current drivers in Fig. 21 and Fig. 22 are hard to keep constant and high $R_{O,DRV}$ in high frequencies. Their bandwidth is less than 1 MHz mostly [8], [113]–[117]. Note that AG_m in (15) has two poles in its transfer function because each of A and G_m has a dominant pole. As a result, $R_{O,DRV}$ also has low-pass characteristic. Moreover, since these current drivers

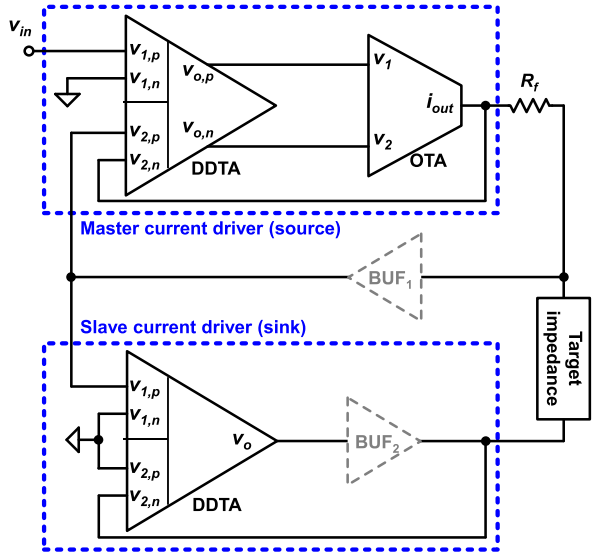


Fig. 22. A closed-loop current driver employing simple source and sink current drivers [8], [115]–[117]. The BUF_1 is used in [115], [116] and the BUF_2 is used in [117].

using linear feedback structure have stability issues, some of them include a compensation capacitor at the output of the FDA in Fig. 21 or the DDTA in Fig. 22 [58], [113], [115], [116] to prevent any oscillation and peaking in the frequency response. These compensation capacitors further lower the bandwidth of AG_m.

To address the bandwidth issue, nonlinear feedback has been used in current drivers [118], [119]. For example, a single-ended current driver with nonlinear feedback using a multiplier is implemented with discrete components and analyzed in [121]. Here the dominant poles required for the stability do not affect its high frequency performance, and thus this current driver achieves a wider bandwidth compared to the current drivers using linear feedback. In [119], which implements IC version of differential current driver based on the nonlinear feedback, a bandwidth of 3 MHz is achieved. However, this design occupies more area and requires more complex circuits. In addition, the transient response (and the settling time) gets longer due to the low frequency dominant pole of their low-pass filters.

VI. Discussion And Conclusions

This paper presents a methodological review of on-chip sinusoidal signal generators (SSGs) for EIS systems. Overall, on-chip SSGs consist of three stages: waveform generation, linearity enhancement, and current injection. Table II summarizes the design methods applied to each stage and performances of on-chip SSGs for EIS applications.

As shown in the table, SSGs for implantable EIS systems usually support one or a few f_{SG} only, and the frequencies are generally low as less than 20 kHz. Moreover, they consume as small power as possible. For example, for ensuring the life time of pacemaker over 10 years, the power consumption of the implantable EIS system is required to be less than 10 μW [39].

TABLE II
SUMMARY OF ON-CHIP SINUSOIDAL SIGNAL GENERATORS

	f_{SG} (Hz)	Waveform generation				Linearity enhancement			Current injection[a]	THD [%]	SFDR [dB]	Tech. [nm]	Area [mm²]	Supply [V]	Power [W]
		Waveform	N_{DAC} [bit]	OSR	f_S [Hz]	Topology	Order (CT)	OSR (DT)							
Sinusoidal signal generators for implantable EIS systems															
[39]	20k	DAC-based sinusoid	6	64	1.28M	CT active g_m-C	2	–	I (CD)	0.66	44.6	65	0.61[b]	0.5	4.62µ
[53]	2k, 20k	DAC-based sinusoid	4	1280, 128	2.56M	–	–	–	I (DAC)	N. R	N. R	180	0.74[b]	1.8	18.0µ – 72.0µ
[61]	2k – 2M	DAC-based sinusoid	N. R (5 tap)	8	16k – 16M	–	–	–	I (CD)	N. R	~20	150	N. R	1.8	52.2µ
[38]	20k	DAC-based sinusoid (DSM)	3	128	2.56M	CT active g_m-C	2	–	I (CD)	0.088	65.2	65	0.059	0.5	6.2µ
[73][c]	10k	50%-duty square	–	–	–	CT active g_m-C	6	–	I (CD)	1.4	36.7	N. R	N. R	N. R	N. R
Sinusoidal signal generators for wearable EIS systems															
[47]	15.625k – 125k	DAC-based sinusoid	8	N. R	N. R	CT active RC	2	–	I (CD)	N. R	> 58.0	130	0.41[b]	1.0	N. R
[58]	10k – 5M	DAC-based sinusoid	N. R	N. R	N. R	–	–	–	I (CD)	< 0.5	N. R	65	0.99	1.2	2.79m
[65]	5k – 200k	DAC-based sinusoid	4.3	N. R	N. R	–	–	–	I (DAC)	N. R	N. R	180	N. R	1.8 / 3.0	61.0µ
[28]	0.1k – 100k	Osc.-based sinusoid	–	–	–	–	–	–	I (CD)	< 0.2	> 59.0	180	0.74[b]	1.8	N. R
[5]	10k – 200k	Osc.-based sinusoid	–	–	–	–	–	–	I (CD)	N. R	> 60.0	180	2.98[b]	1.8	N. R
[84]	10k – 76k	Osc.-based sinusoid	–	–	–	–	–	–	I (CD)	< 2.44	> 33.7	180	2.02[b]	1.5	N. R
[85]	90k	Osc.-based sinusoid	–	–	–	–	–	–	I (CD)	< 1.0	42.0	180	0.73[b]	1.2	2.0m
Sinusoidal signal generators for miniatue EIS instruments															
[48]	4k – 8M	DAC-based sinusoid	8	32M/f_S	32M	–	–	–	I (DAC)	N. R	N. R	180	0.37[b,d]	1.8	N. R
[59]	~1k – 2M	DAC-based sinusoid	N. R	16, 32	32k – 32M	CT active g_m-C	2	–	I (CD)	N. R	> 40.0	180	1.62	1.8	0.75m – 2.06m
[52]	1m[e] – 10k	DAC-based sinusoid	~10[f] (32 tap)	64	6.4k – 640k	CT active g_m-C	2	–	Voltage	< 0.6	> 50.0	500	1.0	3.0	0.18m
[60]	0.1 – 10k	DAC-based sinusoid	8 (< 31 tap)	< 64	6.4 – 50k	–	–	–	Voltage	< 0.8	N. R	130	0.012[d]	1.2	1.1m[d]
[62]	4k – 100k	DAC-based sinusoid	N. R (5 tap)	8	32k – 800k	CT active RC	1	–	I (CD)	1.4	N. R	130	N. R	1.5 / 3.5	95.0µ
[45]	1k – 2.048M	DAC-based sinusoid	3 (8 tap)	16	16k – 32.768M	DT FIR + CT passive RC	2	16	Voltage	0.2[g], 0.7[h]	> 47.0	180	0.72	1.8	5.1m
[67]	1k – 100k	DAC-based sinusoid (DSM + FIR)	5	100	100k – 10M	–	–	–	I (DAC)	0.17	N. R	180	0.052	1.2	55.6µ – 249.3µ
[24]	40m – 40k	50%-duty square	–	–	–	DT LPF	5	100	Voltage	< 0.1	63.0	350	0.64	3.3	N. R
[89]	500k – 10M	Osc.-based sinusoid	–	–	–	–	–	–	I (CD)	N. R	N. R	180	0.084[b]	3.3	N. R
[92][c]	1k – 1M	Osc.-based triangle	–	–	–	–	–	–	Voltage	< 0.41	N. R	350	N. R	3.3	N. R
[101]	1k – 16k	Osc.-based triangle	–	–	–	CT active g_m-C	2	–	I (CD)	N. R	N. R	800	N. R	3.0	N. R
Current drivers for EIS system [40]															
	f_{SG} (Hz)	Feedback	Output current [A_{pp}]	Output impedance [Ω]		Current accuracy [%]			THD [%]			Tech. [nm]	Area [mm²]	Supply [V]	Power [W]
[112]	10k – 1M	Open-loop	< 0.5m	160k @ 500 kHz		0.8% for f_{SG} < 1 MHz			0.79			350	2.0	5.0	1.0m
[58][i]	10k – 5M	Closed-loop[j]	< 0.4m	1M @ 1 MHz		< 1			< 0.5			65	N. R.	1.2	2.42m[j]
[113]	< 1M	Closed-loop	< 5.0m	64k @ 1 MHz		0.47 for f_{SG} < 1Mz			< 0.69			600	0.64	18.0	N. R
[114]	< 1M	Closed-loop	< 1.0m	360k @ 1 MHz		0.86 for f_{SG} < 1Mz			0.1			350	0.40	5.0	N. R
[116]	< 500k	Closed-loop	< 6.0m	1.12M @ 500 kHz		N. R			0.18			350	N. R	18.0	N. R
[117]	< 500k	Closed-loop	< 1.0m	750k @ 500 kHz		N. R			0.8			180	0.05	3.3	N. R
[119]	100k – 3M	Closed-loop	< 1.8 m	> 1M @ 3MHz		0.45 for f_{SG} < 2 MHz			0.4			350	1.20	5.0	15m

[a]CD - current injection by additional current driver, DAC - current injection by current DAC, [b]Estimated area, [c]Simulation results, [d]DAC only,
[e]For $f_{SG} < 100$ Hz, a sub-sampling technique is adopted., [f]1000 unit resistors $= \sim$10 bit, [g]THD_{10}, [h]THD_{40}, [i]It includes on-chip sinusoidal signal generation, [j]Current driver only.

DAC-based sinusoids have been adopted as the starting waveform in most implantable SSGs [38], [39], [53], [61], while the square waveform is also a good candidate due to its simplicity [73]. Many of them adopts g_m-C filters for their linearity enhancement stage due to their better area efficiency than RC filters [38], [39], [73]. Sinusoidal oscillators would be a good candidate for implantable SSGs although they have not been used yet. Since the required f_{SG} and the number of f_{SG} are low, the burden of designing the amplifier and the frequency-tuning circuit can be relieved in the design of oscillator-based SSGs.

In general, the power budget of wearable EIS systems is higher than that of implantable EIS systems. Using the increased power budget, most SSGs for wearable EIS systems can support wider f_{SG} ranges. To support wide ranges up to several hundred kHz, DAC-based sinusoids [47], [58], [65] and RC-controlled sinusoidal oscillators [5], [28], [84], [85] have been adopted as their starting waveform. On the other hand, when a higher f_{SG} such as few MHz is required, DAC-based sinusoids are considered more suitable as the starting waveform [58]. If an RC-controlled sinusoidal oscillator is adopted for high f_{SG}, the required GBW of amplifier in the oscillator should be much higher, leading to a significant power consumption. For instance, the DAC-based SSG in [58] supports a much higher f_{SG} range than the oscillator-based SSG in [85] with the similar power

consumption. In the area point of view, RC-controlled sinusoidal oscillators have a trade-off between the area and the minimum f_{SG} unlike DAC-based sinusoids. As f_{SG} decreases, the required area consumed by the passive components increases. Thus, it is difficult for them to achieve a low f_{SG}. The lowest f_{SG} supported by the oscillators is 0.1 kHz [28]. When f_{SG} less than several hundreds of kHz is required to cover, the DSM techniques in [38] and [67] can be used with a smaller area. [67] embeds an FIR filter in its current DAC, avoiding the use of an explicit current driver. Thus, it also achieves a good power efficiency as well.

SSGs for miniature EIS instruments can support lower and also higher f_{SG} much more easily due to the available power, compared to implantable and wearable applications. In this category, most SSGs adopt DT waveforms such as DAC-based sinusoids and the 50%-duty square waveform, of which f_{SG} can be easily controlled by adjusting f_S for a wide frequency range. Filters used in their linearity enhancement stage are different by the target f_{SG} range. When supporting low f_{SG}, g_m-C filters have been more widely used for enhancing the linearity than RC filter due to their area efficiency [52], [59], [101]. Since CT filters require a large area and power for obtaining a high-order roll-off, 2nd-order g_m-C filters have been employed for DAC-based sinusoids and a triangular waveform, which have lower harmonics compared to the 50%-duty square waveform [52], [59], [101]. On the other hand, DT filters can achieve a high-order roll-off while reducing the area occupied by passive components. Therefore, the 50%-duty square waveform, which is the simplest starting waveform, can be employed with such high-order roll-off DT LPFs [24].

High-order roll-off DT LPFs typically require a high OSR to reduce the required area. But, high OSRs limit the maximum achievable f_{SG} and increases the required power consumption of the amplifiers in the filter. Thus, this type of filters is not suitable for SSGs that cover high f_{SG} as several MHz. On the contrary, DT FIR filters can operate with a lower OSR because they can attenuate the low-order harmonics using their nulls. Thus, they can be used to extend the maximum f_{SG} [45]. For example, the highest f_{SG} of the SSG with a DT LPF in [24] is 40 kHz with an OSR of 100 while the SSG with a DT FIR LPF in [45] is 2.048 MHz with an OSR of 16. However, the DT FIR filter requires a following CT filter due to its low OSR. Hence, their lowest f_{SG} is limited by the following CT filter, which requires passive components.

The current injection is preferred to the direct voltage excitation in most biomedical applications to prevent any injection of unwanted high currents. When the target impedance is small as $<$1 kΩ [48], the simplest way, in which a waveform is generated by a current DAC and the current is injected directly to the target material, can be adopted without any current driver [48], [67]. In many cases, a separate current driver is needed because most waveform-generation and linearity-enhancement circuits are operated in the voltage domain. Besides, when the target impedance is large, a separate current driver is required. The open-loop current drivers can achieve a wider frequency bandwidth while the closed-loop ones typically have better linearity and a higher output impedance. The SSGs for implantable EIS systems should be low power even with a separate current driver. However, the current drivers typically consume a significant portion of the total power consumption when they covers a high f_{SG} range. For example, the waveform generation and linearity enhancement stages of the SSG in [58], which supports f_{SG} from 10 kHz to 5 MHz, consumes 0.37 mW while the current driver of the SSG consumes 2.42 mW. Therefore, the development of low-power current drivers which can support the MHz range is in demand.

f_{SG} and the output amplitude are dominant factors for the output signal's linearity. As the required f_{SG} increases, circuits operated in the DT domain typically require a higher OSR and analog circuits in both CT and DT domains require the amplifiers to have a high GBW. Therefore, it gets more difficult to maintain high linearity as f_{SG} increases. The output amplitude also affects the linearity, especially when g_m cells are adopted in any stages of SSGs. Because g_m of transistors varies by the signal amplitude, the linearity degrades for larger amplitudes. Furthermore, the impedance measurement sensitivity, which is defined as the minimum detectable impedance, is affected by the output current amplitude of SSGs. The sensitivity, $\overline{R^2_{n,M}}$, when the electrode-tissue impedance is negligible, is expressed as [21]:

$$\overline{R^2_{n,M}} = \frac{\overline{v^2_{n,IA}} + (\overline{i^2_{n,IA}} + \overline{i^2_{n,SSG}})R^2_M}{I^2_{SSG}}, \tag{16}$$

where $v_{n,IA}$ and $i_{n,IA}$ are the voltage and current noises of the instrumentation amplifier of the demodulator. I_{SSG} and $i_{n,SSG}$ are the current magnitude and the current noise of the SSG, respectively. R_M is the target material's impedance. In order to improve the sensitivity, I_{SSG} has to be maximized while minimizing $i_{n,SSG}$. However, as the output amplitude of SSGs increases, it gets more difficult to maintain the linearity in the current driver. Therefore, the current drivers should be carefully designed to maximize the linear range by using various techniques demonstrated in Section V.

In order to implement an on-chip SSG supporting a wide frequency range with precise frequency control, it is favorable to use a DAC-based sinusoid since its f_{SG} is accurately controlled by f_S rather than by passive components or g_m. When high linearity and a wide f_{SG} range are achieved by a current DAC alone, low power consumption can be achieved by avoiding any linearity enhancement and current injection stages. For achieving high linearity with a DAC alone, DAC-based sinusoids typically require high N_{DAC} and OSR, increasing the hardware complexity and limiting the maximum f_{SG}, respectively. Adopting a DSM in on-chip SSGs can reduce N_{DAC} and ease the filter requirements [38], [66]–[69]. However, they still need a high OSR. Alternatively, a time-interpolation technique can be used. It reduces the required OSR and filter performances, but it still requires a high clock frequency for interpolation and a high N_{DAC} [63]. Therefore, a design method that can achieve high linearity using a current DAC alone with a low OSR and low N_{DAC} would be a future direction of research. As another aspect, algorithmic methods or improved frequency mixing techniques that prevent

the harmonic folding at the mixing stage would be in demand to reduce the hardware requirements for high-linearity SSGs.

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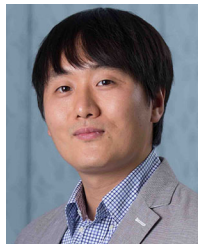

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