Design of a Low Noise Bio-Potential Recorder With High Tolerance to Power-Line Interference Under 0.8 V Power Supply

Deng Luo, *Member, IEEE*, Jiaxin Lei, *Student Member, IEEE*, Milin Zhang, *Senior Member, IEEE*, and Zhihua Wang, *Fellow, IEEE*

***Abstract*—A bio-potential recorder working under 0.8 V supply voltage with a tunable low-pass filter is proposed in this paper. The prototype is implemented in TSMC 180 nm CMOS technology, featuring a power consumption of 2.27 μW, while preserving a high tolerance of power-line interference (PLI) up to 600 mV_{pp}, a common-mode rejection ratio (CMRR) of higher than 100 dB, a THD of -65.5 dB, and a noise density of 50 nV/$\sqrt{Hz}$ by employing four new techniques, including 1) low noise chopper modulator, 2) feedback loop based common-mode cancellation loop (CMCL), 3) offset cancellation loop (OCL) with PMOS backgate control scheme, and 4) a very-lower transconductance (VLT) operational transconductance amplifier (OTA) using in the DC-servo-loop (DSL). The measured mid-band gain is 43.3 dB with a high-pass cut-off frequency of 1.2 Hz. The low-pass cut-off frequency can be configured from 650 Hz to 7.5 kHz. The measured input-referred integrated noise is 1.2 uVrms in the frequency band of 1-650 Hz and 4.1 uVrms in the 1 Hz–7.5 kHz frequency band, respectively, leading to a power efficiency factor (PEF) of 7.49 and 7.59.**

***Index Terms*—Bio-potential recorder, chopper amplifier, common-mode cancellation loop, low noise, power-line interference, very low transconductance OTA.**

I. Introduction

A POWER efficient bio-potential recorder plays a critical role in a Brain-Machine-Interface (BMI) system [1]–[3]. The amplitudes of the targeted signals, such as action potential (AP), local field potential (LFP), electrocardiograph (ECG), electromyography (EMG) and electroencephalo-graph (EEG) are typically in the order of tens of μV to a few mV, with a frequency band distribute from sub-Hz to about 10 kHz [4]–[7]. The power consumption performance is crucial, especially in the design of the bio-potential recorder. Various methodologies have been proposed in literature aiming to the reduction of power consumption. The majority of those existing low power designs improved power consumption performance by reducing the current, but sacrificing the noise performance. In order to optimize the power efficiency factor (PEF), [8]–[10] proposed to reduce the supply voltage to sub-V, but leading to higher total harmonic distortion (THD). In addition, these circuits are susceptible to the common-mode interference (CMI), especially the power-line interference (PLI). The amplitude of the PLI can be as high as hundreds of millivolts at 50 Hz [11].

A common-mode rejection ratio (CMRR) of higher than 80 dB is required for bio-potential recording [11]–[14]. The driven-right-leg (DRL) circuits [15]–[17] are widely used to enhance the CMRR by feeding PLI back to the subject. However, the DRL circuits are at a risk of instability [18]. The chopper-stabilized topologies [19], three op-amps instrument amplifiers [20], common-mode feedback circuits [12] and common-mode feedforward circuits [18] are demonstrated to enhance CMRR. However, to achieve a higher CMRR under large PLI, new techniques are required, especially with sub-V supply voltage. To cancel out CMI, [5] proposed a feedforward loop based common-mode cancellation loop (CMCL). However, the feedforward capacitors suffer from the noise multiplication effect, which increases the input referred noise significantly. [21] proposed a common-mode feedback loop based on charge-pump technique to suppress CMI, which can even exceed the supply rail. However, the noise and power consumption is relatively large.

In this paper, a feedback loop based CMCL is proposed. Under a supply voltage of 0.8 V, the proposed bio-potential recorder achieves a THD of -65.5 dB measured with a PLI up to 600 mV_{pp}. In addition, an offset cancellation loop (OCL) using PMOS backgate control scheme is proposed to reduce the ripples generated by the offset of the input stage OTA. Compared to state-of-the-art ripple reduction technique [5], the proposed technique is suitable for the chopper amplifier, where the input stage OTA is biased by a sub-GΩ resistor. A DC-servo-loop (DSL) integrated an integrator with a large time constant is

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Deng Luo is with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China (e-mail: luod14@mails.tsinghua.edu.cn).

Jiaxin Lei and Milin Zhang are with the Department of Electronic Engineering, Tsinghua University, Beijing 100084, China (e-mail: leijx19@mails.tsinghua.edu.cn; zhangmilin@tsinghua.edu.cn).

Zhihua Wang is with the Research Institute of Tsinghua University in Shenzhen, Shenzhen, China (e-mail: zhihua@tsinghua.edu.cn).

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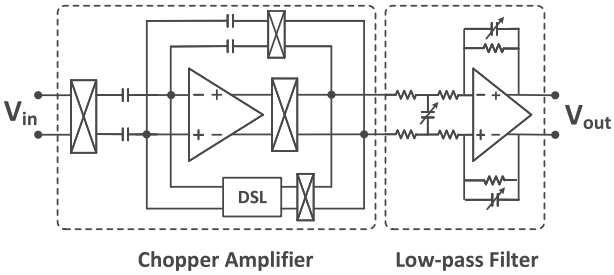

Fig. 1. Architecture of the proposed bio-potential recorder. A chopper amplifier and an adjustable low-pass filter are integrated in this recorder.

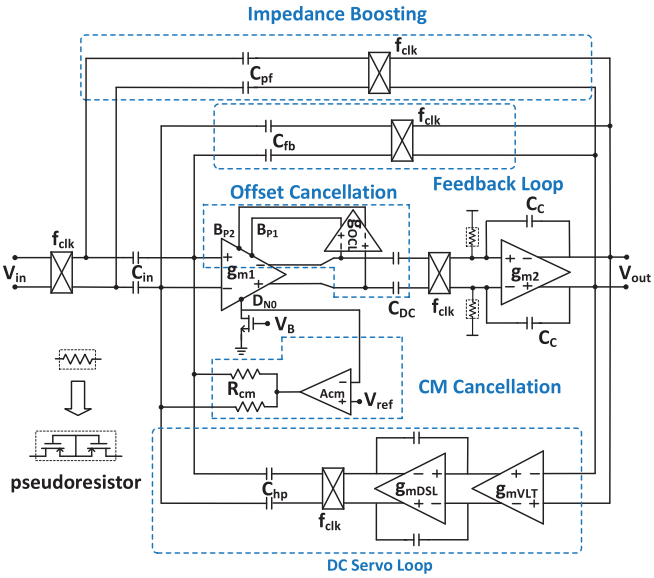

Fig. 2. Architecture of the proposed bio-potential recorder.

widely used to filter out the electrode DC-offset (EDO). In our previous work, an active Gm-C integrator integrated a very-low transconductance (VLT) OTA is used in DSL [22]. However, it is not useful for sub-V supply voltage application. In this paper, a modified VLT OTA is proposed to form a 1.2 Hz high-pass cut-off frequency.

The rest of the paper is organized as follows. The architecture of the bio-potential acquisition amplifier, more detailed analysis on the low noise chopper modulator, CMCL, OCL and DSL structure are introduced in Section II. The experimental results are shown in Section III, while Section IV concludes the entire work.

II. Architecture of the Proposed Bio-Potential Recorder

The overall architecture of the proposed bio-potential recorder is as shown in Fig. 1. It consists of a chopper amplifier and an adjustable low-pass filter. The cut-off frequency of the low-pass filter can be programmed from 650 Hz to 7.5 kHz. For the acquisition of EEGs, ECGs and LFPs, the cut-off frequency can be set to 650 Hz. The cut-off frequency is set to 7.5 kHz for the acquisition of EMGs and APs. This paper focuses on the design of the chopper amplifier. The two-stage chopper amplifier is illustrated in Fig. 2. It consists of i) a two-stage

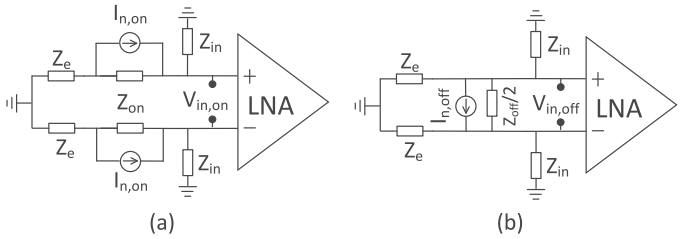

Fig. 3. Noise model of the input chopper modulator. (a) the noise model of the on-resistance, (b) the noise model of the off-resistance.

Miller-compensated OTA, labeled as g_{m1} and g_{m2}, ii) a positive feedback technique based input impedance boosting loop, iii) an active Gm-C integrator based DSL using the proposed VLT OTA, labeled as g_{mVLT}, iv) a capacitive feedback loop, v) an offset cancellation loop, and vi) a common-mode cancellation loop.

A. Design of the Low Noise Chopper Modulator

The proposed circuit is designed working under sub-V supply voltage to reduce the power consumption. Significant noise will be introduced from the input chopper modulator due to the relatively low off-resistance and large on-resistance, under low supply voltage mode. Fig. 3 shows the noise model of the input chopper modulator. The input referred noise generated by on-resistance and off-resistance of the input chopper modulator can be calculated as

$$\overline{v_{in,on}^2} = 2\overline{I_{n,on}^2}\left(\frac{Z_{in}Z_{on}}{Z_{in}+Z_{on}+Z_e}\right)^2 \tag{1}$$

$$\overline{v_{in,off}^2} = 4\overline{I_{n,off}^2}\left(\frac{Z_{in}Z_e}{Z_{in}+Z_e}\right)^2 \tag{2}$$

where Z_{in} is the input impedance of the amplifier. Z_e is the electrode tissue interface impedance. Z_{on} and Z_{off} are the on-resistance and off-resistance of the input chopper modulator separately. Generally, Z_{in} is much larger than Z_e and Z_{on}. Thus, the equations can be simplified as

$$\overline{v_{in,on}^2} \approx 8kTZ_{on} \tag{3}$$

$$\overline{v_{in,off}^2} \approx \frac{32kT}{Z_{off}}Z_e^2 \tag{4}$$

Generally, the input noise density of a bio-potential recorder is around 50 nV/$\sqrt{\text{Hz}}$. In order to reduce the contribution of the input modulator noise to the amplifier noise as much as possible, $\overline{v_{in,on}}$ and $\overline{v_{in,off}}$ must be smaller than 10 nV/$\sqrt{Hz}$. If Z_e is assumed to be equal to 1 MΩ, the off-resistance will be larger than 1.3 GΩ, and the Z_{on} will be smaller than 3 kΩ.

Fig. 4(a) shows four kinds of switches to implement a modulator. A same size is applied to all the switches shown in the figure, but different threshold voltages are used. For PMOS transistors, the lowest threshold voltage is 0.37 V in the process used in the proposed design. With 0.8 V supply voltage, the on and off resistance is sensitive to the threshold voltage. Fig. 4(b) and (c) illustrate the on and off resistance of these four switches

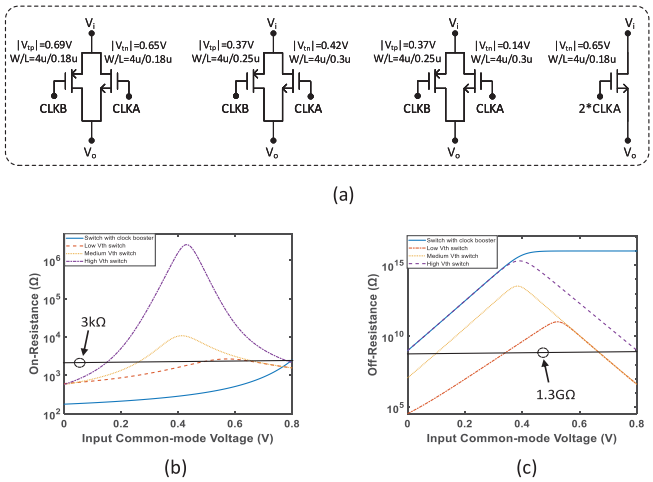

Fig. 4. (a) 4 topologies of the switches to form a modulator. From the left to the right are switches with high threshold voltage transistors, medium threshold voltage transistors, low threshold voltage transistors, and the clock booster technique. (b) On-resistance and (c) off-resistance of the 4 different modulators.

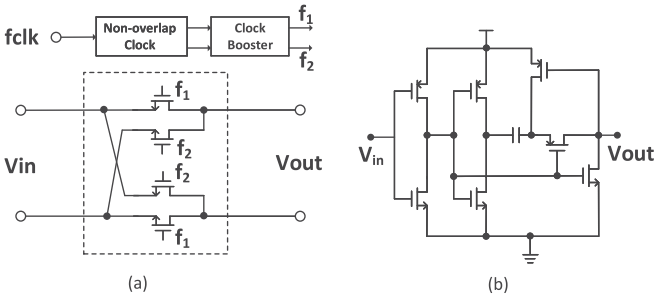

Fig. 5. (a) Architecture of the proposed chopper modulator. A non-overlap clock and a clock booster are used to meet the requirements. (b) The schematic of the clock booster used in the chopper modulator.

separately. It clearly shows that only the switch using the clock booster technique can meet the requirement.

The proposed chopper modulator integrated the clock booster technique is shown in Fig. 5(a), whereas Fig. 5(b) illustrates the design of the clock booster.

B. Design of the Common-Mode Cancellation Loop

The two-stage Miller-compensated OTA used in the chopper amplifier is illustrated in Fig. 6. The output stage, g_{m2}, of the two-stage OTA employs a common-source amplifier structure. While, the input stage g_{m1} is implemented by an inverter-based OTA. In order to reduce the noise further, the input transistors in g_{m1} are biased in the subthreshold region.

Under sub-V supply voltage, large PLI will degrade the THD of the bio-potential acquisition amplifier significantly, or even make it out of work. In order to increase the headroom for the tail current sources, the medium threshold voltage transistors are used in g_{m1}. Hence, $V_{GS,N1-2}$ and $V_{SG,P1-2}$ can be reduced to about 0.25 V. The gate bias $V_{in,CM}$ of the input transistors

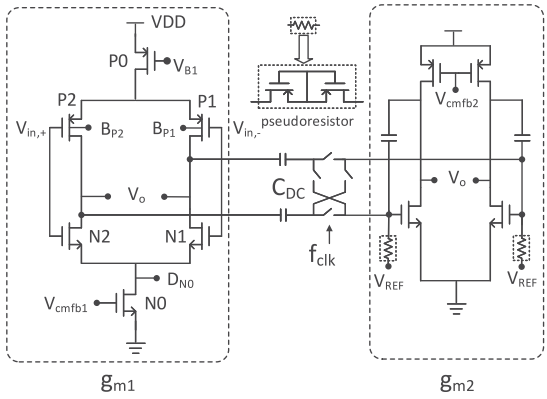

Fig. 6. Schematic of the two-stage Miller-compensated OTA. g_{m1} is the input stage, which is biased in subthreshold region to reduce noise.

N_{1-2} and P_{1-2} must meet the requirements as addressed in [5]

$$V_{ov,N0} + V_{GS,N1-2} < V_{in,CM} < V_{DD} - V_{ov,P0} - V_{SG,P1-2} \tag{5}$$

where V_{DD} is the supply voltage, which is set to 0.8 V. $V_{ov,N0}$ and $V_{ov,P0}$ are the overdrive voltages of the tail current transistors. The typical value of $V_{ov,N0}$ and $V_{ov,P0}$ is 0.1 V. Hence, the range for $V_{in,CM}$ is 0.35 V $< V_{in,CM} <$ 0.45 V. That means the CMI is limited to 100 mVpp.

In order to improve the robustness to large PLI while preserving the accompanying bio-potential signals with low amplitude, a feedback loop based CMCL is designed and used in the input stage to cancel the PLI under sub-V supply voltage as shown in Fig. 7(a). The input PLI coupled from the environment passes to the input of g_{m1} unaltered [5]. Since g_{m1} utilizes the fully differential structure, and the drain resistance of the tail transistor $N0$ is large enough, the PLI will appear at the node of D_{N0}. The PLI is later amplified by A_{CM}. The output of A_{CM} is fed back into the input of g_{m1} through R_{CM}. Thus, a closed-loop negative feedback CMCL is established. The transfer function from E_{CM} to $V_{in,CM}$ in Fig. 7(a) can be calculated as

$$\frac{V_{in,CM}}{E_{CM}} = \frac{sR_{cm}C_{in}}{1 + A_{cm} + sR_{cm}C_{in}} \tag{6}$$

Fig. 7(b) illustrates a quantitative result according to eq. (6). For PLI, an attenuation of -53.6 dB at 50 Hz can be achieved. Assuming the PLI is 600 mVpp, the residual common-mode interference at $V_{in,CM}$ is only 1.25 mVpp.

Fig. 8 shows the architecture of A_{cm} used in the proposed common-mode cancellation loop. It consumes only 62.4 nW to cancel out the large PLI. The bias voltage of the input stage in is established by A_{cm} through resistors R_{CM}. A level shifter is used to ensure the drain voltage of the tail source in the input stage is equal to $V_{ref} - V_{GS}$, where V_{GS} is the difference between the gate voltage and the source voltage of the NMOS transistor in the level shifter. Hence, the bias voltage of the input stage is set to $V_{ref} - V_{GS} + V_{GS,N1-2}$, which is approximately equal to V_{ref}.

The proposed CMCL features two advantages over the technique utilized in [5]. First, the noise of the proposed technique

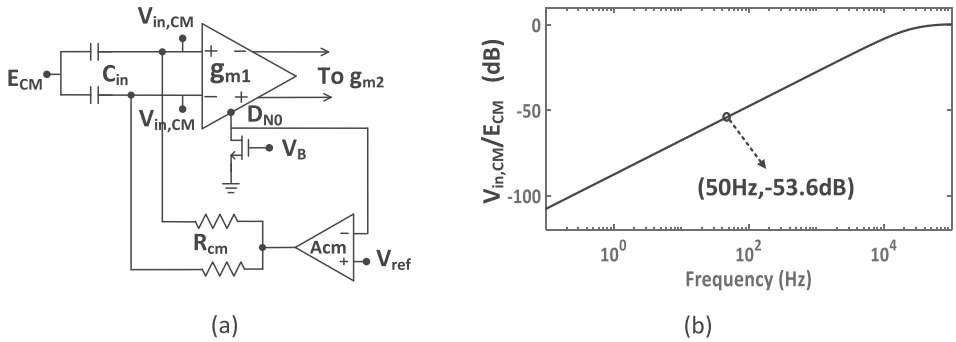

Fig. 7. (a) The proposed common-mode cancellation loop used in the input stage. It is designed to cancel the PLI under sub-V supply voltage. (b) The transfer function from E_{CM} to $V_{in,CM}$ as calculated in eq. (5).

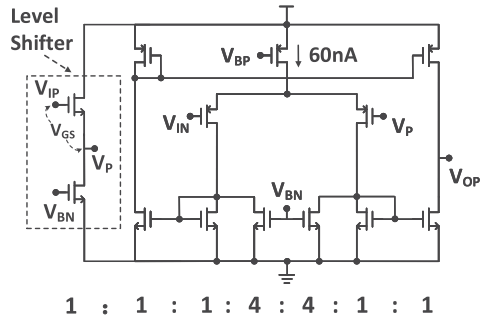

Fig. 8. The schematic of A_{cm} used in common-mode cancellation loop.

is lower. Since noise multiplication effect caused by R_{CM} is much smaller. The detailed noise analysis is given in the rest of the paper. Secondly, the input stage OTA is biased by R_{CM} directly. While, A_{cm} is biased by the input stage OTA. Hence, the pseudoresistors can be avoided in the signal path.

C. Design of the Offset Cancellation Loop

The offset of g_{m1} will generate large ripples at the output. [23] inserted a pair of block capacitors C_{DC} between g_{m1} and g_{m2} to solve this issue. However, it may cause a saturation at the output of g_{m1}. Since g_{m1} is working in open loop at the DC frequency. In order to attenuate the offset, an OCL with PMOS backgate control technique is proposed as shown in Fig. 9(a). The offset at the output of g_{m1} is amplified by g_{ocl}. Then it is fed back to the backgate of the PMOS pair. With the backgate effect, an offset larger than ± 13 mV can be handled according to simulation. Fig. 9(b) shows the schematic of the g_{ocl}. The total current of the g_{ocl} is only 18 nA, including the common-mode feedback loop.

Since the bio-potential signals are modulated by the input chopper modulator as shown in Fig. 2, the frequency of the modulated signals is around the chopping frequency f_{clk}. As long as the bandwidth of the OCL is much lower than f_{clk}, OCL causes no impact on the signals of the interest. The bandwidth of the feedback branch in the OCL is determined by C_{OCL} and R_{ocl}, which is set to about 25 Hz. In order to further evaluate the effect of the OCL on the offset and flicker noise of g_{m1}, the transfer function from V_{in} to V_o in Fig. 9(a) for $f \ll f_{clk}$ is given as

$$\frac{V_o}{V_{in}} \approx \frac{g_m}{g_{ocl}R_{ocl}g_{mb}} \frac{1+sC_{OCL}R_{ocl}}{1+sC_{OCL}/g_{ocl}g_{mb}R_L} \tag{7}$$

where

$$R_L = \frac{R_o}{1+sC_{DC}R_o} \tag{8}$$

g_m and g_{mb} are the transconductance and backgate transconductance of g_{m1} separately. Fig. 10 shows V_o/V_{in} with and without the OCL. Without OCL, the dc offset of g_{m1} will be amplified with a gain of 34 dB. While, with OCL, it is attenuated by a factor of 45 dB. It's important to note that the flicker noise of g_{m1} is blocked by the block capacitors C_{DC} as discussed in [24]. In this design, the flicker noise is suppressed by the OCL further.

The loop transfer function of the OCL is given as follow to evaluate the effect of OCL on the instability of g_{m1}.

$$L(s) = \frac{g_{ocl}R_{ocl}g_{mb}R_o}{(1+sC_{OCL}R_{ocl})(1+sC_{DC}R_o)} \tag{9}$$

In order to achieve a phase margin of 60°, the frequency of the second poly f_{p2} should are larger than twice of the unity-gain bandwidth f_{ugb}, where

$$f_{p2} = 1/2\pi C_{DC}R_o \tag{10}$$

and

$$f_{ugb} = g_{ocl}g_{mb}R_o/2\pi C_{OCL} \tag{11}$$

According to the simulation, f_{ugb} is round 2.3 kHz, and f_{p2} is about 9.2 kHz. Thus, a phase margin of nearly 76° can be expected.

The flicker noise $V_{fn,gocl}$ of g_{ocl} can be ignored, since $V_{fn,gocl}$ is blocked by C_{DC}. The residual flicker noise passed through C_{DC} is modulated and integrated by the output stage. The ripples are generated at the output, which can be filtered out. The thermal noise $V_{tn,gocl}$ of g_{ocl} distribute around the chopping frequency may increase the total input referred noise of the chopper amplifier. The input referred noise $V_{in,gocl}$ contributed by $V_{tn,gocl}$ is expressed as

$$V_{in,gocl} = \frac{g_{ocl}g_{mb}}{2\pi f_{clk}C_{OCL}g_m} V_{tn,gocl} \tag{12}$$

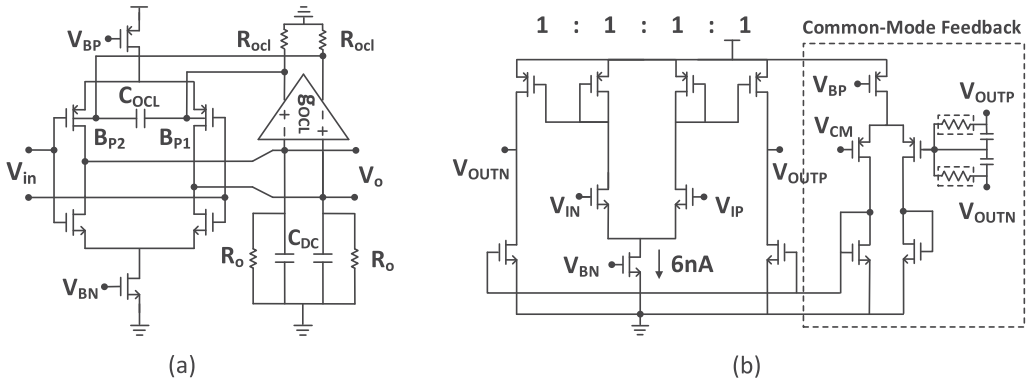

Fig. 9. (a) The proposed offset cancellation loop. It integrates PMOS backgate control to suppress the ripple generated by the offset of g_{m1}. (b) The schematic of g_{ocl} used in offset cancellation loop.

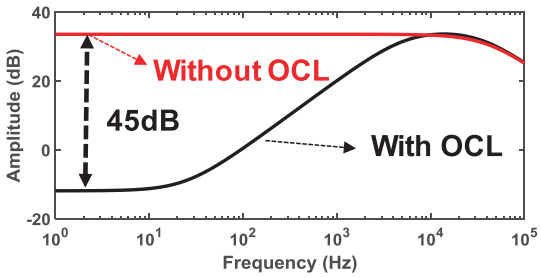

Fig. 10. The transfer function from V_{in} to V_o with and without OCL according to eq. (7).

The value of $V_{in,gocl}$ depends on the chopping frequency f_{clk}. If a typical frequency 20 kHz is used as the chopping frequency f_{clk}, a $V_{in,gocl}$ of about 3.5 nV/$\sqrt{Hz}$ can be expected according to the simulation.

D. Design of the DC Servo Loop

The DSL is utilized to form a high pass frequency corner to filter out the EDO. In our previously work, a DSL integrated an active Gm-C integrator with large time constant is proposed [22]. In order to realize a Gm-C integrator, the very-lower-transconductance (VLT) OTA with complementary input structure is used. However, in order to maintain a high linear performance, the supply voltage is limited to 1.75–1.85 V. In order to solve this issue, the threshold voltage of the source-degeneration transistors $P_{S1,2}$ ($|V_{tp}| = 0.69$ V) used in the PMOS pair is larger than that of the input PMOS transistors $P_{I1,2}$ ($|V_{tp}| = 0.37$ V), as shown in Fig. 11(a). For the NMOS pair, the traditional source degeneration technique is applied to increase the linearity. The output differential current of the proposed OTA is

$$I_d = \frac{2I_b}{N}\left(\beta\frac{e^{\frac{\kappa V_d}{V_T}} - e^{\frac{-\kappa V_d}{V_T}}}{\zeta_N + e^{\frac{\kappa V_d}{V_T}} + e^{\frac{-\kappa V_d}{V_T}}} + \frac{e^{\frac{-\kappa V_\Delta}{V_T}}\left(e^{\frac{\kappa V_d}{V_T}} - e^{\frac{-\kappa V_d}{V_T}}\right)}{\zeta_P + e^{\frac{-\kappa V_\Delta}{V_T}}\left(e^{\frac{\kappa V_d}{V_T}} + e^{\frac{-\kappa V_d}{V_T}}\right)}\right) \quad (13)$$

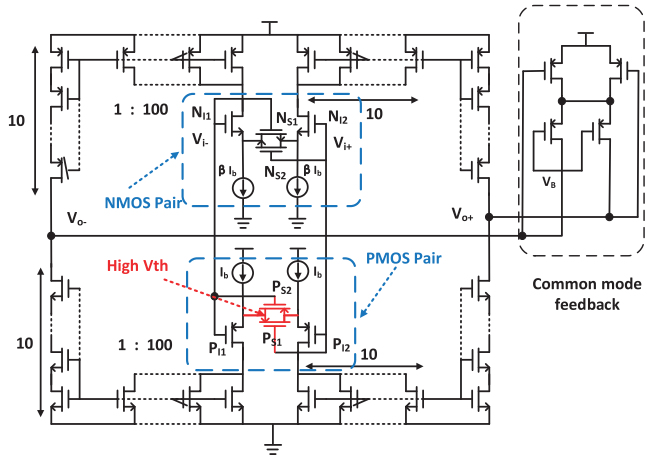

Fig. 11. (a) The schematic of the proposed g_{mVLT} used in DSL. (b) The output current of g_{mVLT} versus the input voltage. The proposed g_{mVLT} extend the input linear range from 100 mVpp to 400 mVpp. (c) Monte Carlo simulation results of g_{mVLT}. The mean value of g_{mVLT} is 24 pS with a standard deviation of 5.3 pS.

where I_b is the bias current of $P_{I1,2}$, which is set to 0.2 nA. N is the current division factor as discussed in [22], which is set to 100. β is the bias current ratio between $N_{I1,2}$ and $P_{I1,2}$, which is set to 0.8. ζ_N and ζ_P are determined by the size of the transistors. ζ_N is defined by $W_{NI1,2}L_{NS1,2}/W_{NS1,2}L_{NI1,2}$, which is set to 1. While, ζ_P is defined by $W_{PI1,2}L_{PS1,2}/W_{PS1,2}L_{PI1,2}$, which is set to 1/8. V_Δ is the difference of the threshold voltage between $P_{S1,2}$ and $P_{I1,2}$, which is 0.32 V. By implementing the

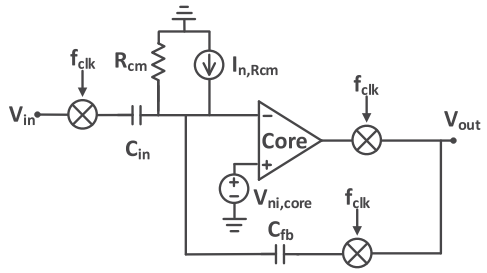

Fig. 12. Noise model for the discussion on the noise contributed by the proposed CMCL.

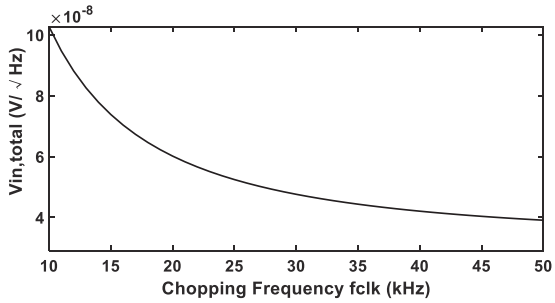

Fig. 13. Relationship between the $v_{in,total}$ and f_{clk} according to eq. (17).

proposed VLT OTA, the input linear range of DSL is extended to 400 mVpp as shown in Fig. 11(b). Fig. 11(c) shows the Monte Carlo simulation results. With 1000 runs, the simulated g_{mVLT} value is 24 pS with a standard deviation of 5.3 pS. The EDO cancellation range can be expressed as [22]

$$V_{EDO} = \frac{V_{DD} C_{hp}}{C_{in}} \tag{14}$$

Where V_{DD} is the supply voltage. C_{hp} is chosen to be 800 fF to ensure a EDO cancellation range of 50 mV.

E. Noise Analysis

Fig. 12 shows the noise model for a discussion on the noise contributed by CMCL. The input-referred noise of the chopper amplifier is dominated by the input stage OTA as

$$\overline{v_{in,core}^2} = \overline{v_{ni,core}^2} \left(\frac{C_{in} + C_{fb} + C_{hp} + \frac{1}{2 f_{clk} R_{CM}}}{C_{in}} \right)^2 \tag{15}$$

Where f_{clk} is the chopping frequency. R_{CM} is set to 10 M Ω. C_{in} is set to 10 pF. $v_{ni,core}$ is the input noise of the core OTA. In the proposed design, the bias current of the input stage is 1.35 μ A, leading to a $v_{in,core}$ of about 30 nV/$\sqrt{Hz}$. R_{CM} will generate thermal noise. The input-referred noise of the amplifier contributed from R_{CM} is

$$\overline{v_{in,RCM}^2} = \left(\frac{\sqrt{2} I_{n,Rcm}}{2\pi f_{clk} C_{in}} \right)^2 = \frac{2kT}{(\pi f_{clk} C_{in})^2 R_{CM}} \tag{16}$$

The total input-referred noise

$$\overline{v_{in,total}^2} = \overline{v_{in,core}^2} + \overline{v_{in,RCM}^2} \tag{17}$$

The relationship between $v_{in,total}$ and f_{clk} is plotted in Fig. 13. A higher f_{clk} leads to low thermal noise, but decreases the input impedance. By applying the impedance boosting technique, the input impedance can be expressed as

$$Z_{in} = \frac{1}{2(1 - C_{pf}/(C_{in} + C_{pf})G) C_{in} f_{clk}} \tag{18}$$

where G is the closed-loop gain. According to eq. (18), when C_{pf} is equal to $C_{in}/(G-1)$, Z_{in} will be infinitely. However, Z_{in} is limited by the parasitic capacitance as discussed in [19]. In this paper, a C_{pf} of 68f F is used. Eq. (18) also implies that Z_{in} is inversely proportional to f_{clk}. Thus, the input impedance can be improved by reducing the chopper frequency.

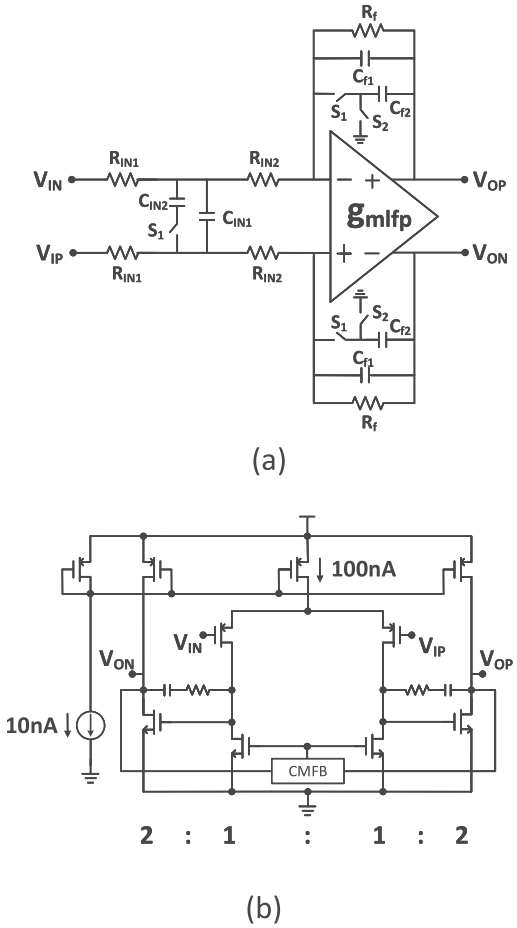

Fig. 14. (a) The schematic of the second-order low-pass filter. (b) The schematic of g_{mlpf} used in the low-pass filter.

Fig. 13 illustrates the input noise density versus the chopping frequency. When f_{clk} is larger than 30 kHz, $v_{in,total}$ decreases very slowly. Thus, in this paper, a f_{clk} of 30 kHz is used. Due to the use of the boosting path, the input impedance is increased from 1.67 MΩ to 70 MΩ at a chopping frequency of 30 kHz.

F. Design of the Low-Pass Filter

The second-order low-pass filter is illustrated in Fig. 14(a). The cut-off frequency of the low-pass filter is determined by the capacitors and the resistors in both the input path and the

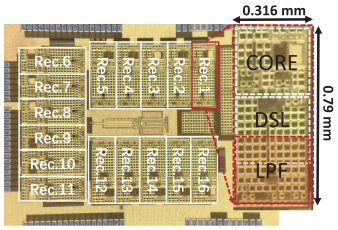

Fig. 15. Micrograph of the fabricated prototype showing 16 bio-potential recorders implemented in TSMC 180 nm CMOS technology.

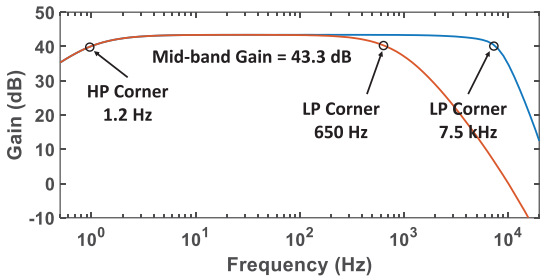

Fig. 16. Measured frequency response of the bio-potential acquisition amplifier. A mid-band gain is 43.3 dB with a high-pass cut-off frequency of 1.2 Hz. The low-pass cut-off frequency can be switched between 650 Hz and 7500 Hz.

feedback path. A tunable switch S_1 is used to configure the low-pass cut-off frequency varying from 650 Hz to 7.5 kHz. The working state of the switch S_2 is opposite to that of S_1. When S_1 is turned off, the bottom of C_{f2} is floating. S_2 should be turned on to pull up the bottom voltage of C_{f2} to a certain level. The schematic of g_{mlpf} in Fig. 14(a) is shown in Fig. 14(b). g_{mlpf} employs a two-stage Miller-compensated structure, which consumes 330 nA of total current including the common-mode feedback circuit.

III. Experimental Results

The proposed design was fabricated in TSMC 180 nm CMOS process with a silicon area of 0.25 mm ^{2}. A microphotography of the prototype die was as shown in Fig. 15. The total power drawn from a 0.8 V supply is measured to be 2.27 μW. The chopper amplifier and the low-pass filter consumes 2 μW and 0.27 μW, respectively.

The chopping frequency is set to 30 kHz. The measured mid-band gain is 43.3 dB with a high-pass cut-off frequency of 1.2 Hz as shown in Fig. 16. The low-pass cut-off frequency of the recorder is decided by the low-pass filter, which is tunable from 650 Hz to 7.5 kHz. Fig. 17 shows the measured noise. In the frequency band of 1 Hz to 650 Hz, the measured integrated noise is 1.2 uVrms. While in the band of 1 Hz to 7.5 kHz, the integrated noise is 4.1 uVrms. The input noise density is 50 nV/$\sqrt{\text{Hz}}$.

Fig. 18 shows the measured CMRR versus the frequency. An CMRR larger than 100 dB is achieved at 50 Hz. With CMCL, the CMRR is enhanced by more than 30 dB. Fig. 19 illustrates the input-referred noise versus the chopping frequency. The input-referred noise decreases while the chopping frequency is increasing. However, when f_{clk} is larger than 30 kHz, the

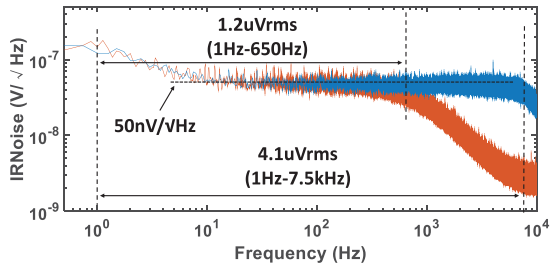

Fig. 17. Measured input-referred noise of the proposed bio-potential recorder with different low-pass cut-off frequency. The noise density is about 50 nV/$\sqrt{Hz}$.

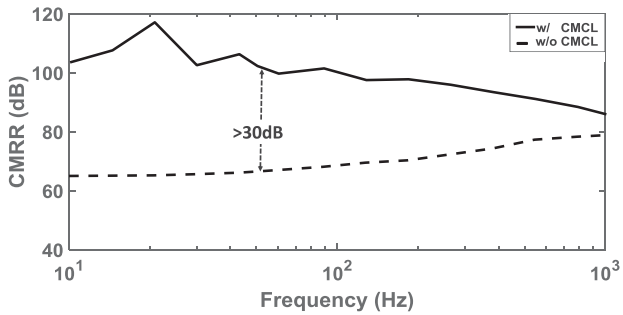

Fig. 18. The measured CMRR of the chopper amplifier under a PLI of 600 mVpp at 50 Hz with and without CMCL.

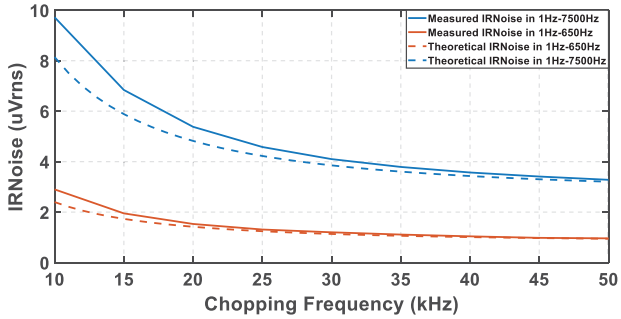

Fig. 19. Measured and theoretical input-referred noise versus the chopping frequency.

input-referred noise decreases very slowly. The theoretical results according to eq. (17) was also plotted in the dash lines in Fig. 18. The experimental results fit the theoretical analysis well.

For a 4mVpp input at 1 kHz in the presence of a 600 mVpp PLI at 50 Hz, the measured THD is -65.5 dB. As shown in Fig. 20(a), a signal-to-interference of 53.4 dB is achieved. When the input frequency is lowered to 5 Hz, the measured THD and signal-to-interference are -61 dB and 55 dB respectively as shown in Fig. 20(b). When the CMCL is turned off, a large distortion appears at the output as shown in Fig. 20(a) and Fig. 20(b). In order to evaluate the effect of PLI on the proposed chopper amplifier with and without CMCL, the measured signal-to-noise and distortion (SINAD) versus the PLI is plotted in Fig. 20(c) and Fig. 20(d). A SINAD larger than 45 dB is achieved under a PLI of 600 mVpp with CMCL. While, without CMCL, the

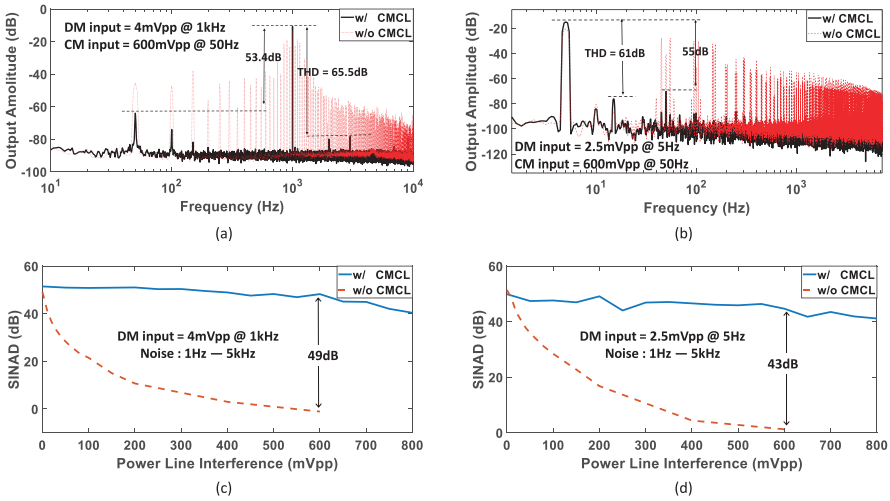

Fig. 20. Measured signal quality of the chopper amplifier under a PLI at 50 Hz. (a) Measured total harmonic distortion for an input signal at 1 kHz under a PLI of 600 mVpp with and without CMCL. (b) Measured total harmonic distortion for an input signal at 5 Hz under a PLI of 600 mVpp with and without CMCL. (c) Measured SINAD versus PLI for an input signal at 1 kHz with and without CMCL. (d) Measured SINAD versus PLI for an input signal at 5 Hz with and without CMCL.

TABLE I
PERFORMANCE & COMPARISON OF THE PROPOSED BIO-POTENTIAL ACQUISITION AMPLIFIER S

Reference	[8] ISSCC'13	[9] ISSCC'14	[5] ISSCC'17	[10] JSSC'17	[14] JSSC'16	[21] ISSCC'19	[25] JSSC'18	This work
Supply	0.45V	0.5V	1.2V	0.2/0.8V	1V	1.2V	1V	0.8V
Gain	52dB	—	25.7dB	57.8dB	52.1dB	35dB	25.6dB	43.3dB
Power/Ch	0.73uW	2.3uW	2.8uW	0.79uW	3.28uW	27.8uW	0.25uW	2.27uW
IRnoise (Vrms)	3.2u (1-10kHz)	1.29u (1-500Hz)	1.8u (1-200Hz) 5.3u (0.2k-5kHz)	0.99u (1-500Hz)	4.13u (1-8.2kHz)	5.05u (1-100Hz)	5.5u (10-10kHz)	1.2u (1-650Hz) 4.1u (1-7500Hz)
NEF/PEF	1.57/1.12 (1-10kHz)	4.76/11.3 (1-500Hz)	7.4/65.7 (1-200Hz) 4.4/23.2 (0.2k-5kHz)	1.6/2.1 (0.5-670Hz)	3.19/10.2 (1-8.2kHz)	93.5/10491 (1-100Hz)	1.07/1.14 (10-10kHz)	3.06/7.49 (1-650Hz) 3.08/7.59 (1-7500Hz)
CMRR	73dB	88dB	78dB	85dB	>90dB @100Hz	68dB	84dB	>100dB @50Hz
Tolerance to large CMI	No	No	Up to 650mVpp	30mVpp	220mVpp	30Vpp	—	Up to 600mVpp
PEF/CMI	—	—	101 (1-200Hz) 35 (0.2k-5kHz)	93.57 (1-500Hz)	46.36 (1-8.2kHz)	349.7 (1-100Hz)	—	12.48 (1-650Hz) 12.65 (1-7500Hz)
THD	-46dB	-48dB (@1mVpp)	-76dB (@80mVpp)	-50.4dB	-40dB	—	—	-65.5dB (@4mVpp)
Off-chip caps	NO	NO	NO	YES	NO	NO	NO	NO
Max.EDO	∞	50mV	—	—	∞	—	∞	50mV
Area/ch	—	0.025mm^2	0.071mm^2	—	0.042mm^2	—	0.097mm^2	0.25mm^2
Technology	180nm	65nm	40nm	180nm	65nm	180nm	180nm	180nm

SINAD decreases dramatically with the increase of PLI. By using CMCL, the SINAD is enhanced by 49 dB and 43 dB at an input frequency of 1 kHz and 5 Hz, respectively.

Two common bio-potential, EMG and ECG, are used to demonstrate the functionality of the proposed design in bio-sensing applications. To demonstrate the amplifier's tolerance to large PLI, a large PLI is applied to the subject while monitoring ECG and EMG. The electrodes are placed as shown in Fig. 21(a). The PLI is applied to the subject through the right arm. A common mode interference of about 600 mVpp at 50 Hz is detected in the recoding sites. Fig. 21(b) shows the raw data of the collected ECGs under large PLI with and without CMCL. Due to the mismatch of the electrode impedance, the common mode interference was converted into differential mode

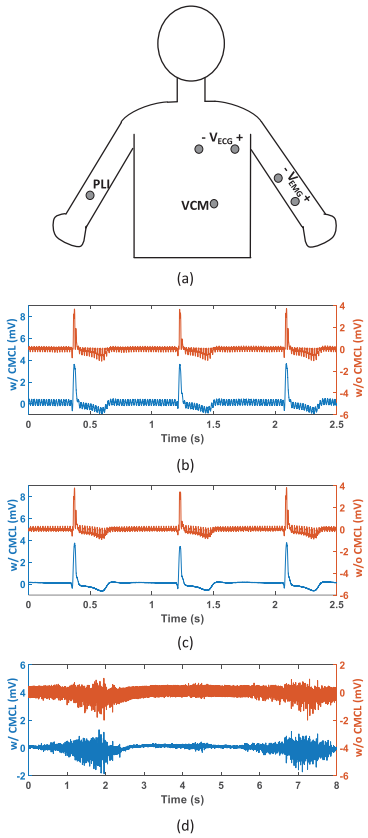

Fig. 21. In-vivo recording of ECGs and EMGs under a PLI of 600 mVpp at 50 Hz. (a) The electrodes configuration. (b) The raw data of the ECGs recorded with and without CMCL. (c) The ECGs filtered by a second-order notch filter. (d) The EMGs filtered by a second-order notch filter.

interferences [14]. Hence, the raw data of ECGs are contaminated by the PLI. However, when a second-order notch filter located at 50 Hz with a bandwidth of 35 Hz was applied to the raw acquired data outputted from the amplifier, the interference in the ECGs recoded with CMCL is removed by the notch filter. However, the ECGs recorded without CMCL still shows poor quality as shown in Fig. 21(c). This can be even worse when recording EMGs. Since the interference was distributed in the frequency band of EMG. Fig. 21(d) shows the EMGs recorded with and without CMCL, which are filtered by the notch filter. The EMGs recorded with CMCL shows a better quality, while comparing with that without the CMCL. To summarize, the proposed CMCL combined with notch filter can be used to record bio-potential signals under large PLI, especially when the supply voltage is very low.

Table I compares the performance of the proposed work and state-of-the-art designs. PEF is defined as

$$PEF = NEF^2 V_{DD} \tag{19}$$

where

$$NEF = V_{ni,rms}\sqrt{2I_{tot}/\pi \cdot V_T \cdot 4kT \cdot BW} \tag{20}$$

NEF is a merit that normalizes the input noise of the amplifier to that of a single BJT which consumes the same total current [26]. PEF is widely used to compare the power efficiency of amplifiers with the same noise. Bio-potential recrder often suffers from the CMI. The tolerance range of CMI depends on the supply voltage. A higher supply voltage often means a higher tolerance range. Under low supply voltage, the CMCL is needed to improve the tolerance to large CMI, but at a cost of higher noise. PEF/CMI is a merit that takes the power, system noise, and CMI all into account. If two circuits feature the same PEF, a low PEF/CMI represents a higher tolerance to CMI, which means the CMCL is more noise friendly. The proposed work achieves a PEF/CMI smaller than 12.65, which is one of the best in the state-of-the-art designs. It is important to note that the proposed work occupies a relatively larger silicon area compared to the state-of-the-art. It is suitable for applications requires limited channels but high THD and low noise.

IV. Conclusion

A bio-potential recorder designed in 180 nm CMOS technology, achieving a 2.27 μW under 0.8 V supply voltage is proposed in this paper. In order to reduce the noise, a low noise chopper modulator is proposed. A CMCL based on feedback structure is proposed to tolerate the large PLI. An OCL is designed to cancel out the input offset voltage of higher than $\pm$13 mV by using the backgate control scheme. A VLT OTA is integrated in DSL to form a high pass frequency at 1.2 Hz. By using these techniques, the proposed chip enables a tolerance of PLI up to 600 mVpp under 0.8 V supply voltage, a noise density of 50 nV/$\sqrt{Hz}$, a THD of -65.5 dB and a CMRR of larger than 100 dB.

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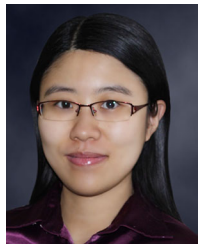
Deng Luo (Member, IEEE) received the B.S. degree in electronic engineering from the Huazhong University of Science and Technology, Wuhan, Hubei, China, in 2014. He is currently working toward the the Ph.D. degree with Tsinghua University, Beijing, China, focusing on low noise, low power, low voltage analog circuit design. His research interests include analog and mixed signal circuit designs, especially for biomedical applications.

Jiaxin Lei (Student Member, IEEE) received the B.S. degree in electronic engineering from Tsinghua University Beijingi, China, in 2019. He is currently working toward the Ph.D. degree with Tsinghua University, Beijing, China, focusing on low power circuit and system design. His research interests include various low power circuit and system design for biomedical applications.



Milin Zhang (Senior Member, IEEE) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree with the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology (HKUST), Hong Kong.

After finishing her doctoral studies, she worked as a Postdoctoral Researcher with the University of Pennsylvania. She joined Tsinghua University as an Assistant Professor with the Department of Electronic Engineering in 2016. Her research interests include designing of traditional and various non-traditional imaging sensors, such as polarization imaging sensors and focal-plane compressive acquisition image sensors. She is also interested in analog and mixed signal circuit designs oriented for various applications.

She has served as Technology Program Committee member of the IEEE ISSCC, A-SSCC, CICC, and BioCAS committee. She has received the Best Paper Award of the BioCAS Track of the 2014 International Symposium on Circuits and Systems (ISCAS), and the Best Paper Award (1st place) of the 2015 Biomedical Circuits and Systems Conference (BioCAS).

Zhihua Wang (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering in 1983, 1985, and 1990, respectively, from Tsinghua University, Beijing, China, where he has served as Full Professor and the Deputy Director of the Institute of Microelectronics since 1997 and 2000. He was a Visiting Scholar with CMU (1992–1993) and KU Leuven (1993–1994), and was a Visiting Professor with HKUST (September 2014 to March 2015). He has coauthored 12 books/chapters, more than 197 (514) papers in international journals (conferences), more than 246 (29) papers in Chinese journals (conferences) and holds 118 Chinese and 9 US patents. His current research mainly focuses on CMOS RFIC and biomedical applications, involving RFID, PLL, low-power wireless transceivers, and smart clinic equipment combined with leading edge RFIC and digital image processing techniques.

He has served as the Chairman of IEEE SSCS Beijing Chapter (1999–2009), an AdCom Member of the IEEE SSCS (2016–2019), the Technology Program Committee Member of the IEEE ISSCC (2005–2011), a Steering Committee member of the IEEE A-SSCC (2005), the Technical Program Chair for A-SSCC 2013, a Guest Editor for IEEE JSSC Special Issues (December 2006, December 2009 and November 2014), an Associate Editor of IEEE Trans on CAS-I, II and IEEE Trans on BioCAS, and other administrative/expert committee positions in China?s national science and technology projects.