1225-Channel Neuromorphic Retinal-Prosthesis SoC With Localized Temperature-Regulation

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***Abstract*—A 1225-Channel Neuromorphic Retinal Prosthesis (RP) SoC is presented. Existing RP SoCs directly convert light intensity to electrical stimulus, which limit the adoption of delicate stimulus patterns to increase visual acuity. Moreover, a conventional centralized image processor leads to the local hot spot that poses a risk to the nearby retinal cells. To solve these issues, the proposed SoC adopts a distributed Neuromorphic Image Processor (NMIP) located within each pixel that extracts the outline of the incoming image, which reduces current dispersion and stimulus power compared with light-intensity proportional stimulus pattern. A spike-based asynchronous digital operation results in the power consumption of 56.3 nW/Ch without local temperature hot spot. At every 5×5 pixels, the localized (49-point) temperature-regulation circuit limits the temperature increase of neighboring retinal cells to less than 1 °C, and the overall power consumption of the SoC to be less than that of the human eye. The 1225-channel SoC fabricated in 0.18 μm 1P6M CMOS occupies 15mm^2 while consuming 2.7 mW, and is successfully verified with image reconstruction demonstration.**

***Index Terms*—Distributed image processor, image processor, retinal prosthesis, neural prosthesis, neuromorphic, neuromorphic image processor, temperature regulation, temperature safety.**

I. Introduction

THERE are over 2 million patients worldwide who suffer from retinitis pigmentosa [1] and 8 million US patients with age-related muscular degeneration (AMD) [2], [3]. These patients cannot see due to the loss of their photoreceptors; however, they still have their inner retinal cells intact. Retinal Prosthesis System on a Chip (RP SoC) treats the retinal degenerative disease by providing electrical stimulation to the inner retinal cells [1], and 60-channel (Ch) RP SoC (Argus II) was commercialized in 2013 [4]. Many works have focused on increasing the number of channels to improve the spatial resolution for better visual information, and [5] developed Alpha IMS with 1500-Ch and received CE approval in 2016. However, the visual acuity is still deficient due to the stimulation current dispersion within the human retina [1]–[5], which requires new technologies with a scaled number of channels. RP SoC also involves the control of power consumption in the confined area. Even though delicate simulation of thermal increase has been studied, using the power consumption of the human eye itself is a more conservative criterion. Considering the physiological power consumption of the human retina [6], the overall power consumption of the RP SoC should not exceed 3.4 mW in the worst-case scenario, which we can potentially power up the SoC using body-coupled power transfer [7], [8].

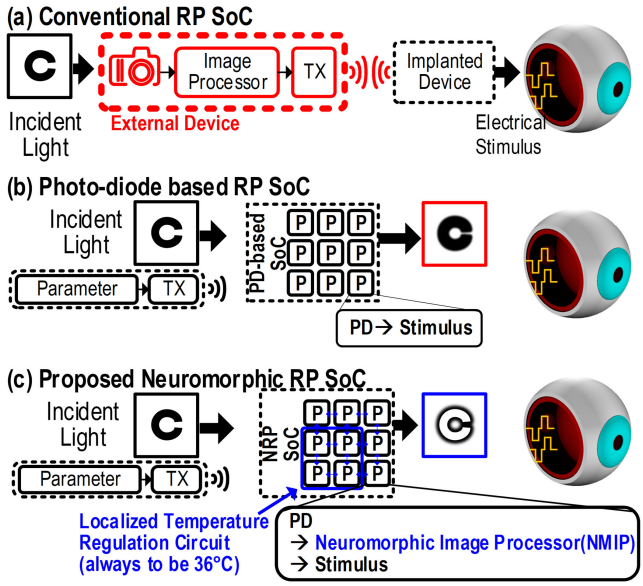

Fig. 1. System architectures of (a) conventional RP SoC, (b) photo-diode based RP SoC, and (c) proposed neuromorphic RP SoC.

Fig. 1(a) and (b) show the system architectures of the state-of-the-art RP SoCs for the detailed circuit analysis. Fig. 1(a) shows the conventional RP SoC with an external camera and an image processor [4], [9]. This methodology has high flexibility of controlling stimulus parameters according to patients' physiological responses. However, there are two bottlenecks. The first is the high power consumption; as the channel number

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increases, the transmitter (TX) power increases substantially [9]. Also, the data burden of the image processor becomes very high, resulting in additional power consumption. The second is the inconvenience of wearing external devices; it is cumbersome for patients to attach external cameras in goggles during daily life, which causes head movement as a replacement of the broad eye movement [10]. To mitigate the issues, [5] and [11] developed the photo-diode (PD) based RP SoCs. The PD of each pixel (P) integrated within the SoC senses the incident light and directly converts the light intensity into the electrical stimulus. Hence, the PD-based RP SoCs significantly reduce data bandwidth and do not require any external video cameras. However, the absence of an image processor within the SoC makes it challenging to deal with the current dispersion in the conductive human retinal environment, which degrades the electrical stimulus patterns. Temperature increase by excessive power consumption is another important issue. As most of the power consumption comes from stimulus generation, there is a limitation in the number of simultaneous stimuli, which reduces the stimulus rate. The absence of temperature regulation also decreases the stimulus rate due to the necessity of margin. For safety, we may add a global temperature monitoring feature to shut down the SoC in case of excessive temperature increase [12]; however, global shut down makes the patients temporarily blind until the chip cools down to the body temperature.

To resolve these issues, this paper presents the Neuromorphic Retinal Prosthesis (NRP) SoC for dedicated and safe stimulation (Fig. 1(c)) [13]. Each pixel contains the Neuromorphic Image Processor (NMIP), mimicking human retina function, which extracts the outline or edge from the light patterns for delicate stimulation. The localized temperature regulation circuit is placed at every 5×5 pixel group, which turns off only that partial pixel group if the local hot spot is detected. Therefore, even if a 5×5 pixel group is shut off, the patient can still retain the image pattern through the rest of the 35×35 pixels.

This paper is organized as follows. Section II describes the key design considerations of the proposed NRP SoC: 1) Outline extraction strategy, 2) the neuromorphic image processor, and 3) the localized temperature sensor. Section III denotes the system architecture of the proposed NRP SoC, and Section IV describes its circuit implementation details. Section V shows the measurement results. Finally, Section VI concludes the paper.

II. Design Considerations

A. Outline Extraction Strategy

To increase the spatial resolution while suppressing the power consumption and maintaining the visual acuity, the proposed NRP SoC employs the outline extraction strategy. Conventional light intensity mode stimulates the whole human retinal area with proportion to light intensity incoming retinal region. Outline extraction mode, on the other hand, uses the edge of the incident light pattern, which reduces a significant amount of stimulus power. Moreover, the outline extraction improves immunity to the current dispersion in the human retina in terms of delivering visual information. As we scale up the number of channels, the current dispersion degrades the visual acuity. To assess the dispersion effect, we employ a Finite Element Method (FEM) simulation: Considering the change of dot size depending on the stimulus level, we infer that the conductive human retina environment blurs stimulus patterns due to the current dispersion [14]–[16]. Based on the properties of retinal cells and electrode in [15], we first simulate the normalized current distribution.

Fig. 2(a) shows the FEM simulation setup. Since geometrical factors affect current dispersion more than conductivity [16], we choose a circular Au electrode with 80 μm diameter (to match our SoC electrode size) and isotropic retinal cells with electrical conductivities of 4.1×10^7 S/m and 1.56 S/m, respectively, for simplified simulation. The stimulation charge is applied with level from 1 nC to 100 nC.

Fig. 2(b) shows the E-field distribution divided by maximum E-field with a distance of 50 μm. It is found that the distribution trends are the same, regardless of which current stimulation level is applied.

Fig. 2(c) shows the electrical current dispersion effects based on the result of Fig. 2(b). Assuming that the charge distribution of each channel is independent and the E-field has a linear relationship with charge distribution, the current distribution is mapped into a 35 × 35 matrix and multiplied with stimulus patterns of each image processing mode. From the result, the dispersed stimulus pattern from outline extraction is still recognized as the Landolt-C pattern, compared with that of the conventional light intensity mode (which corrupts the pattern due to blurs). Therefore, the proposed NRP SoC employs the outline extraction mode.

B. Neuromorphic Image Processor (NMIP)

Human retina networks consist of photoreceptors, bipolar cells, and ganglion cells that convert light into electrical signals and deliver the electrical signals into the brain. Horizontal and amacrine cells are connected to neighboring cells and regulate the electrical signals. To extract the outline and edge from the incoming light information, the proposed Neuromorphic Image Processor (NMIP) mimics the human retina network that consists of photoreceptors, horizontal cells, and bipolar cells, as shown in Fig. 3(a). Firstly, the functional network among cells is analyzed, as shown in Fig. 3(b). The output of the bipolar cell ($O_{Bipolar}$) is expressed as Eq. (1):

$$\mathrm{O_{Bipolar}} = \mathrm{PR_C} - \sum \mathrm{PR_N} \tag{1}$$

where PR_C is the corresponding photoreceptor output, PR_N is the neighboring photoreceptor output, respectively. From Eq. (1), $O_{Bipolar}$ is the same as outline extraction or edge detection.

Using this network, we propose the NMIP (Fig. 4). The spike-based photo-diode sensor (Spike PD) generates the spike burst with a linear spike-rate modulation proportional to the incident light; simply by counting the number of spike bursts, an NMIP can calculate the light intensity and communicate with the neighboring NMIPs. By doing so, the outline or the edge of the incident light patterns are extracted based on Eq. (2):

$$\mathrm{O_{NMIP}} = \mathrm{Spike\ PD_C} - \sum \mathrm{Spike\ PD_N} \tag{2}$$

where O_{NMIP} is the output of the neuromorphic image processor, *Spike* PD_C is the output of corresponding spike PD, and

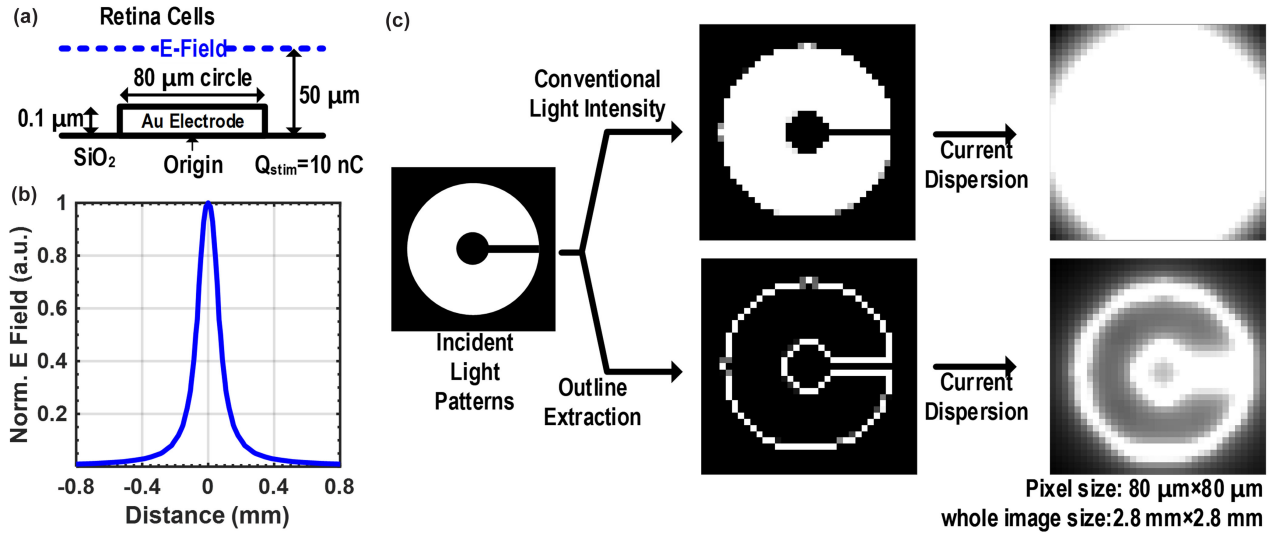

Fig. 2. FEM simulation of current dispersion: (a) FEM Simulation setup, Retina cells (1.56 S/m), Au Electrode (4.1×10^7 S/m), (b) normalized E-field (divided by maximum value), and (c) current dispersion effects of conventional light intensity and outline extraction mode based on (b).

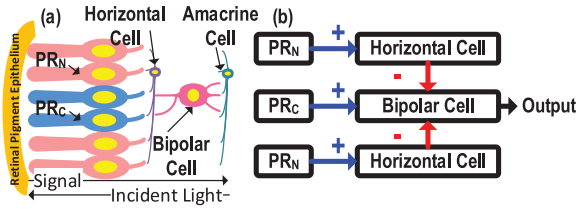

Fig. 3. (a) Human retinal network mimicked, (b) its block diagram.

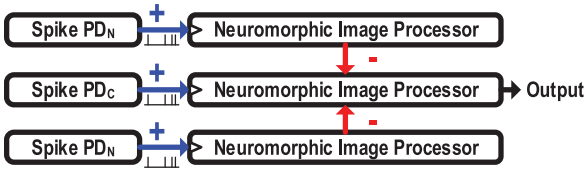

Fig. 4. Block diagram of the proposed Neuromorphic Image Processor (NMIP).

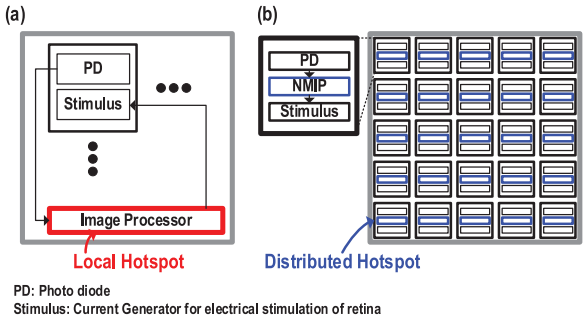

Fig. 5. Comparison between: (a) conventional single centralized-image processor configuration and (b) the proposed distributed Neuromorphic Image Processor (NMIP) configuration to reduce local hotspot.

Spike PD_N is the output of the neighboring spike PD. Thanks to the usage of the spike edges, the NMIP achieves an asynchronous digital operation. Considering the fastest stimulus rate below 60 Hz, the slow spike-rate range and scaling down of the supply voltage becomes possible, which saves power consumption.

Another advantage of mimicking the human retinal network is to avoid local hotspots occurred from the image processing, as shown in Fig. 5.

C. Localized Temperature Regulation Circuit

Even though the NMIP consumes low power, the most power-consuming portion of the RP SoC is the stimulus generation circuit, which is challenging to reduce the power level due to the threshold of the retinal cells' activation. If the continuous stimulus generation keeps with maximum current amplitude, it is unavoidable that the temperature increases in the localized region. For the detailed analysis, we simulate the temperature increase with a FEM simulation. Fig. 6(a) shows the test setup of the FEM simulation. Assuming that the static-state heat transfer and a constant heat source are used, the number of PIXELs is swept from 1×1 to 5×5. Also, we set up the worst case that each PIXEL generates the greatest stimulus patterns of 446 μW (3.3 V $\times$ 450 μA $\times$ 5 ms $\times$ 60 Hz), and this stimulus is changed into the heat.

Fig. 6(b) shows that temperature increase above 1 °C starts from 5×5 in the case of the body temperature of 36.5 °C, and this region can be formed in a specific region. From the FEM simulation, the conclusion is that every 5×5 PIXELs needs localized temperature regulation circuit. Although the stimulus in the worst case is less than 25×446 μW in the outline extraction mode, our system contains the conventional light-intensity mode that can consume 25×446 μW. Thus we integrate our temperature regulation circuit in every 5×5 NMPIXEL.

III. System Architecture

Fig. 7(a) shows the system architecture of the proposed 1225-Ch NRP SoC. There are 35×35 neuromorphic PIXELs (NMPIXEL) that sense the incident light and generate the

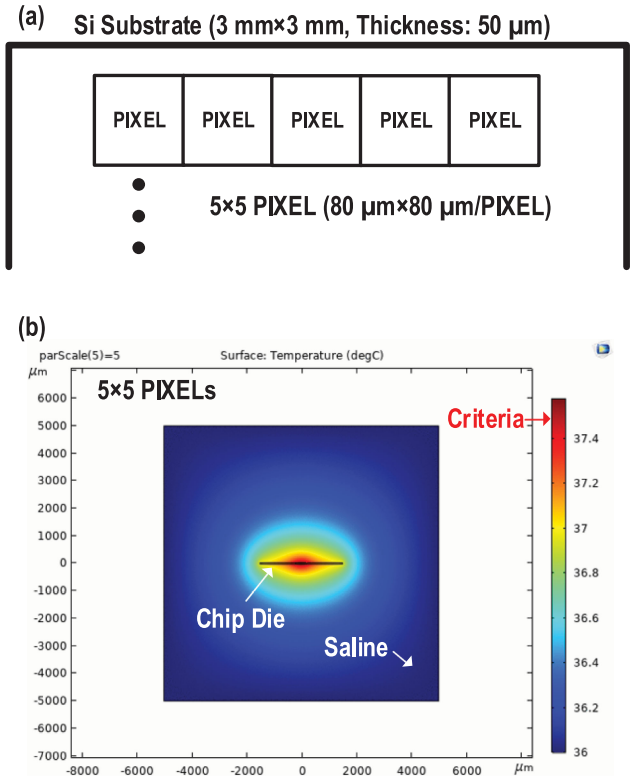

Fig. 6. FEM Simulation for localized temperature increase (a) test setup, (b) test result.

corresponding electrical stimulus patterns based on the outline of the incident light. The localized temperature regulation circuit is integrated with every 5 × 5 NMPIXEL group (the total is 49 points). Fig. 7(b) shows the block diagram of the 5 × 5 NMPIXEL group. If the temperature exceeds the criteria, the temperature regulation circuit regulates the power supply to turn off the hotspot region, which cools down naturally by the conduction of neighboring fluids such as blood and lymph in the human eye. This function is beneficial due to the little effect on the overall electrical stimulus pattern. Every NMPIXEL communicates with the neighboring NMPIXELs (Up, Down, Left, and Right) to mimic the human retinal network function for outline extraction. Fig. 7(c) illustrates the NMPIXEL block diagram. Each NMPIXEL senses the incident light by the Spike-Based Photo-Diode sensor (Spike PD). The neuromorphic image processor (NMIP) extracts the outline from the output of the Spike PD and the communication with the neighboring NMPIXELs. The output of the NMIP is converted into the current stimulus level in the current DAC (IDAC), and the biphasic current generator (I.stim.) produces the biphasic current pulse.

IV. Circuit Implementations

A. Neuromorphic Pixel(NMPIXEL)

1) Spike-Based Photo-Diode Sensor(Spike PD): Fig. 8(a) shows the layout of the DNWELL photo-diode used. The two reverse-biased diodes along the Pwell- Nwell- PSubstrate (PW-NW-PSUB) prevent the photocurrent from leaking into neighboring PIXELs and other circuits. The higher metal layer and circuit-under-pad (CUP) are used for the optical passivation.

Fig. 8(b) describes the schematic of the Spike PD. The leakage quenching Schmitt trigger [17] is used to remove the DC bias circuit and to reduce power consumption compared with using two comparators and the voltage references. The Schmitt trigger supports two output transition points depending on the input voltage, which determines the charging and discharging phase.

Fig. 8(c) shows the timing waveform of the Spike PD. PMOS (*MP1*) charges the parasitic capacitor (*C*), and photo-diode discharges *C* depending on light intensity. Voltage decrease gradient (ΔV) can be expressed as in Eq. (3):

$$\Delta \mathrm{V} = \mathrm{I_{PD}}/\mathrm{C} \;=\; \mathrm{k} \cdot \mathrm{Light}/\mathrm{C} \tag{3}$$

where I_{PD} is the photocurrent, k is coefficient; *Light* is the light intensity, respectively. As *C* and *MP1* size determines the charging phase duration, spike rate is determined by the discharging phase, and the spike rate (*SR*) is expressed as in Eq. (4), Eq. (5):

$$\mathrm{SR} \;=\; 1/\mathrm{P_{discharge}} = \; 1/\left\{\mathrm{C} \cdot (\mathrm{V_{MAX}} - \mathrm{V_{MIN}})/\mathrm{I_{PD}}\right\} \tag{4}$$

$$\mathrm{SR} = \mathrm{k}_{SR} \cdot \mathrm{I_{PD}} \propto \; \mathrm{Light} \tag{5}$$

where $P_{\mathrm{discharge}}$ is the discharge phase; V_{MAX} and V_{MIN} is the input voltage of the Schmitt trigger when the output is changed, and k_{SR} is the coefficient. From Eq. (5), the spike rate is linearly proportional to the light intensity.

2) Neuromorphic Image Processor (NMIP): Fig. 9(a) shows the conventional way to implement a distributed analog image processor by the current mirror topology [18], [19] that faces three main challenges. Firstly, mirrored current variation is 21% in the range of photocurrent from 10 pA to 10 nA, which affects the output distortion. Secondly, it is hard to scale down $\mathrm{V_{DD}}$ due to the necessity of drain-source voltage headroom. Lastly, the MOSFET size should be greater than the minimum size in order to suppress the process mismatch.

On the contrary, thanks to the Spike PD's output, the neuromorphic image processor (NMIP) achieves asynchronous and digital operation, which has the following advantages of 1) low output distortion, 2) $\mathrm{V_{DD}}$ down-scalable for low-power consumption, and 3) simple process migration. In the Monte Carlo simulation in Fig. 9(b), Spike PD has a variation of spike-rate within 2%, which results in low-output distortion. The slow spike range of less than 100 kHz enables scaling down the $\mathrm{V_{DD}}$ to 0.6 V. As a result, the power consumption excluding stimulus achieves 56.3 nW/Ch. As the NMIP is based on the digital operation, we design NMIP with hardware description language (HDL), which is easy to migrate to advanced process nodes for the area and power efficiency. The NMIP also contains the conventional light intensity mode processing as a stimulus power comparison with outline extraction.

Fig. 9(c) shows the timing diagram of the proposed NMIP operation for the detailed analysis. For the comparison with conventional light intensity mode, the NMIP can select the image processing mode by changing the signal of MODE (1 is the outline extraction, 0 is the light intensity mode). When the EN is 1, a 3-bit spike counter (3b Spk. COUNT) starts to count to 4 (100_2). When the output of 3b Spk. COUNT (OUT [2:0]) is 4,

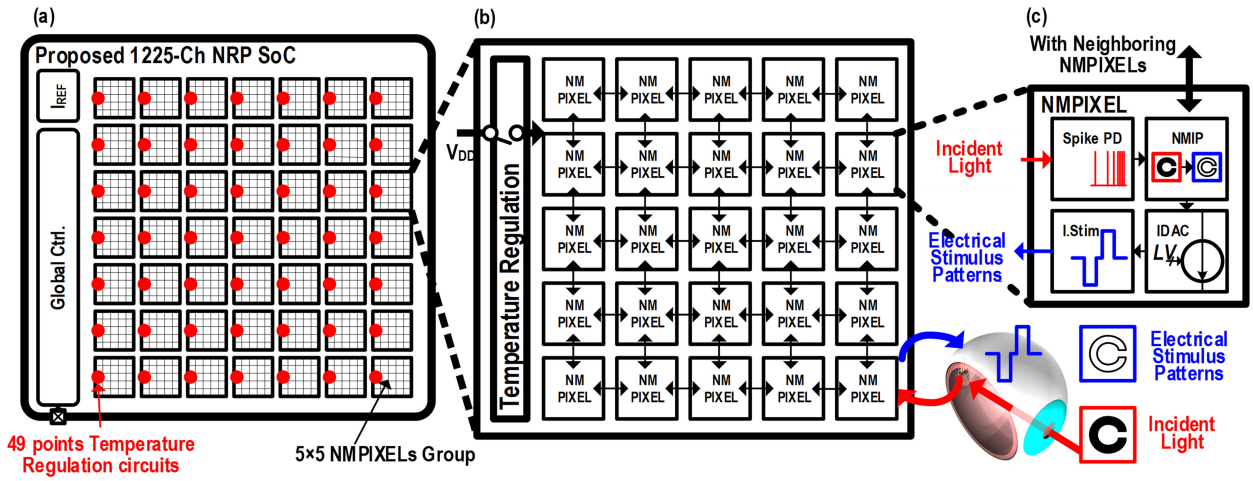

Fig. 7. System architecture of (a) 1225-Ch NRP SoC, (b) 5 × 5 NMPIXELs group, and (c) NMPIXEL.

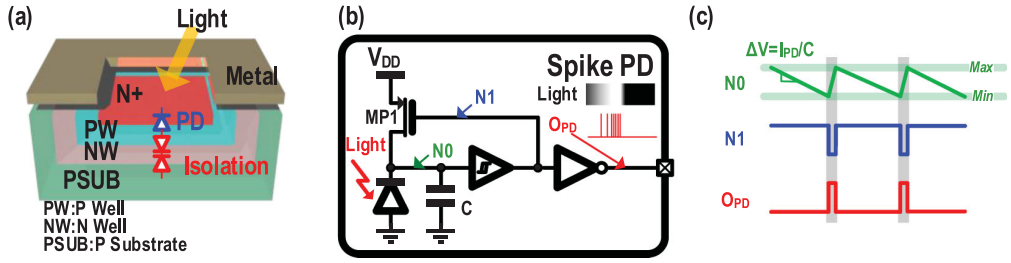

Fig. 8. (a) layout of the DNWELL photo-diode used (b) schematic of the Spike PD (c) timing waveform of the Spike PD operation.

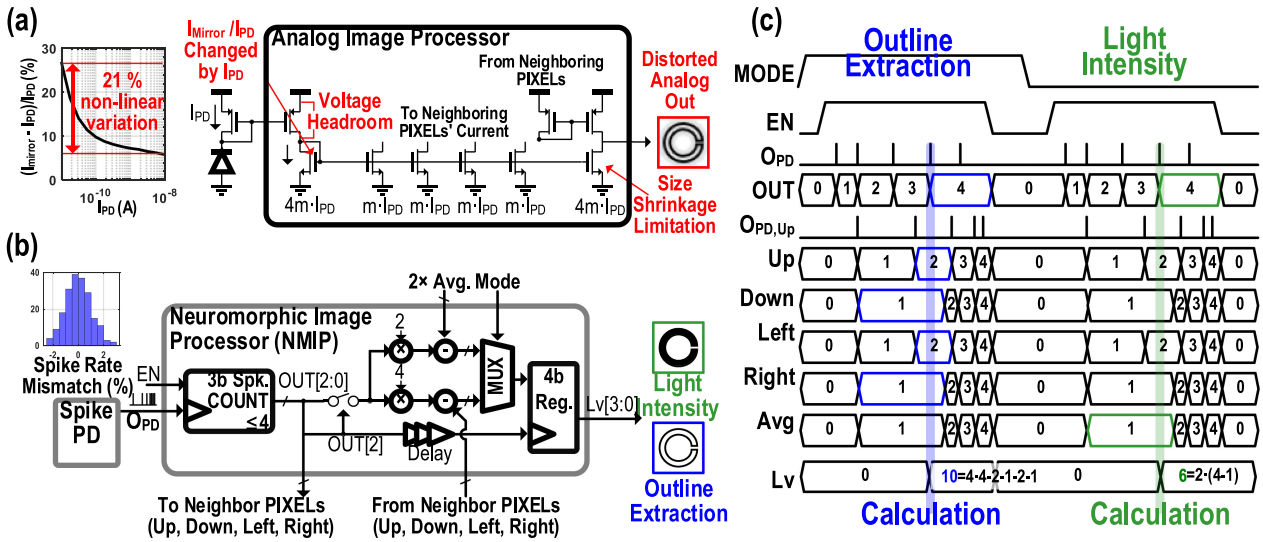

Fig. 9. Block diagrams of (a) conventional current mirror analog image processor, (b) the proposed fully digital Neuromorphic Image Processor (NMIP) for low image processing distortion by process variation (<2%) and its Monte Carlo Simulation of Spike PD, and (c) timing diagram of the proposed NMIP.

the NMIP calculates the outline (Lv[3:0]) with the neighboring OUT(Up, Down, Left, Right) as in Eq. (6):

$$Lv = 4 \cdot SR_{Center} - \sum SR_{Neighboring} \tag{6}$$

where SR_{Center} is the spike rate in the NMIP, and $SR_{Neighboring}$ is the spike rate in the neighboring NMIP. Changing SR into photocurrent, Eq. (6) can be expressed as in Eq. (7):

$$\begin{aligned} Lv &= 4 \cdot k_{SR} \cdot I_{PD-Center} - \sum (k_{SR} \cdot I_{PD-Neighboring}) \\ &= 4 \cdot \mathrm{k_{SR}} \cdot (\mathrm{I_{PD,Light-Center}} + \mathrm{I_{PD,Noise-Center}}) \\ &\quad - \sum \{\mathrm{k_{SR}} \cdot (\mathrm{I_{PD,Light-Neighboring}} \\ &\quad + \mathrm{I_{PD,Noise-Neighboring}})\} \end{aligned} \tag{7}$$

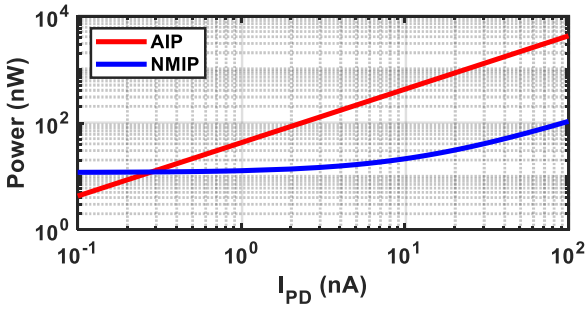

Fig. 10. Trends of power consumption between conventional analog image processor (AIP) and the proposed NMIP.

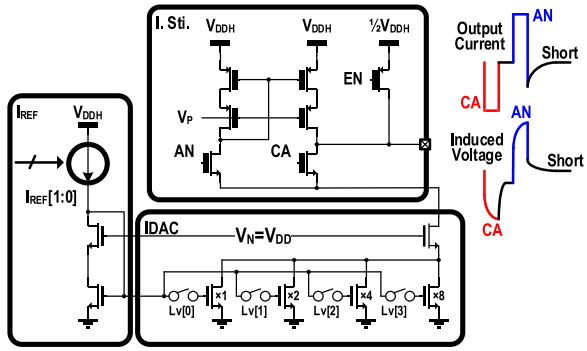

Fig. 11. Schematic of IDAC and biphasic current stimulator (I.Stim.).

where $I_{PD,Light}$ is photocurrent induced by the light and $I_{PD,noise}$ is the noise, including the dark current and the white noise. Since the photo-diode distance with those of neighboring NMPIXELs is less than 80 μm, $I_{PD,noise}$ between the corresponding NMPIXEL and the neighboring NMPIXEL can be similar. Hence, it can be canceled out as in Eq. (8):

$$\mathrm{Lv} = 4 \cdot k_{SR} \cdot (\mathrm{I}_{PD,Light-Center}) - \sum k_{SR} \cdot (\mathrm{I}_{PD,Light-Neighboring}) \quad (8)$$

By doing this way, we can control the noise of photo-diode efficiently. After finishing the calculation, Lv can be updated via the 4-bit register by the delayed signal of OUT[2], for giving sufficient calculation time of the arithmetic logic unit. The shift operator is used for minimizing power and area, in contrast to multipliers of $\times 2$ and $\times 4$.

Cell-based design with HDL relieves the design burden (*e.g.*, transistor sizing and manual routing) to scale down the process for area reduction, compared with the traditional full custom design methods. However, timing constraint is much challenging in the asynchronous design. The direct use of neighboring spikes' edges causes complex timing issues when spikes occur at the same time; hence NMIP gets the DC output of the neighboring spike counter to avoid such problems.

In terms of power consumption, conventional mirror-scheme consumes the power consumption ($P_{conv.mirror}$) of Eq. (9):

$$\mathrm{P}_{\mathrm{conv.mirror.}} = \mathrm{V}_{\mathrm{DD}} \cdot (13 \cdot \mathrm{m} \cdot \mathrm{I}_{\mathrm{PD}}) \quad (9)$$

where *m* is the ratio between photocurrent and mirrored current. By setting up the ratio of mirrored current as in Fig. 9(a), the total current is 13·m·I_{PD}. In contrast, the proposed NMIP power consumption (P_{NMIP}) is expressed as in Eq. (10):

$$\mathrm{P}_{\mathrm{NMIP}} = \mathrm{V}_{\mathrm{DD}} \cdot (\mathrm{K}_{NMIP} \cdot \mathrm{I}_{\mathrm{PD}}) + \mathrm{P}_{\mathrm{ALU}} \quad (10)$$

where K_{NMIP} is a coefficient contributed by Schmitt trigger and 3-bit spike counter, P_{ALU} is the computation power consumption fixed independent with I_{PD}. The Schmitt trigger and 3-bit spike counter provide $\mathrm{K_{NMIP}}$ to be 1.6, and $\mathrm{V_{DD}}$ can be scale down to 0.6 V by carefully choosing the standard cell. Assuming m is 1, and extracting K_{NMIP} from the simulation result, the power consumption of the analog image processor with mirror topology and the proposed NMIP can be shown in Fig. 10. Although the power consumption of the proposed NMIP is higher than the conventional analog image processor (AIP) in the dark state due to P_{ALU}, the power gradient is much smaller than that of AIP. Hence, power consumption in the whole range is much lower than that of AIP.

3) IDAC & Biphasic Current Generator (I.Stim.): Fig. 11 describes the schematic of IDAC and a biphasic current stimulator (I.Stim.). IDAC uses the 4-bit binary-weighted current mirror to change the current level linearly. Depending on the different patient environment (*e.g.*, electrode impedance, target cell distance), $\mathrm{I_{REF}}$ is configurable by the digital control signal (2-bit) in order to cover the maximum stimulus current range of 0.6-1mA depending on the patients' situation. Wide swing cascode is used for the large compliance voltage [20], and the bias voltage ($\mathrm{V_N}$) of 0.6 V (same as $\mathrm{V_{DD}}$) enhances to increase the compliance voltage and to remove voltage reference. Biphasic current stimulator operated in $\mathrm{V_{DDH}}$ (= 3.3 V) merges the current paths of the anodic and cathodic current sources to remove additional leakage paths. EN signal is for the residual charge removal in the rest state. As the stimulus rate is under 60 Hz [1]–[5], [9]–[12], the resting phase of retinal prosthesis SoC has the most abundant time, compared with that of other neural prosthesis SoCs. Thus, such passive charge cancelation is enough and achieves area efficiency.

B. Localized Temperature Regulation Circuit

Fig. 12(a) illustrates the schematic of the localized temperature regulation circuit. The temperature regulation circuit consists of 1) a spike-based temperature sensing circuit and 2) digital temperature feedback $\mathrm{V_{DD}}$ control circuit.

The spike-based temperature sensing circuit schematic is the modified circuit of the Spike PD, which replaces photo-diode into proportional to absolute temperature (PTAT) current source. Hence, the spike-based temperature sensing circuit generates the spike burst with a spike rate linearly proportional to temperature. Also, digitization by spike-counting is area and power-efficient, compared with the conventional temperature sensor with ADC.

The digital temperature feedback $\mathrm{V_{DD}}$ control circuit is designed with HDL, which has advantages of 1) low-power consumption by 0.6 V $\mathrm{V_{DD,TEMP}}$, 2) smooth process migration, which is similar to the NMIP design.

Fig. 12(b) is the timing waveform for the operation explanation. When *Temp ON* is 0, all the registers and the counter values are reset. When *Temp ON* is 1, and *EN* is 1, the 11-bit counter (11b counter) starts to count the spike bursts and resets

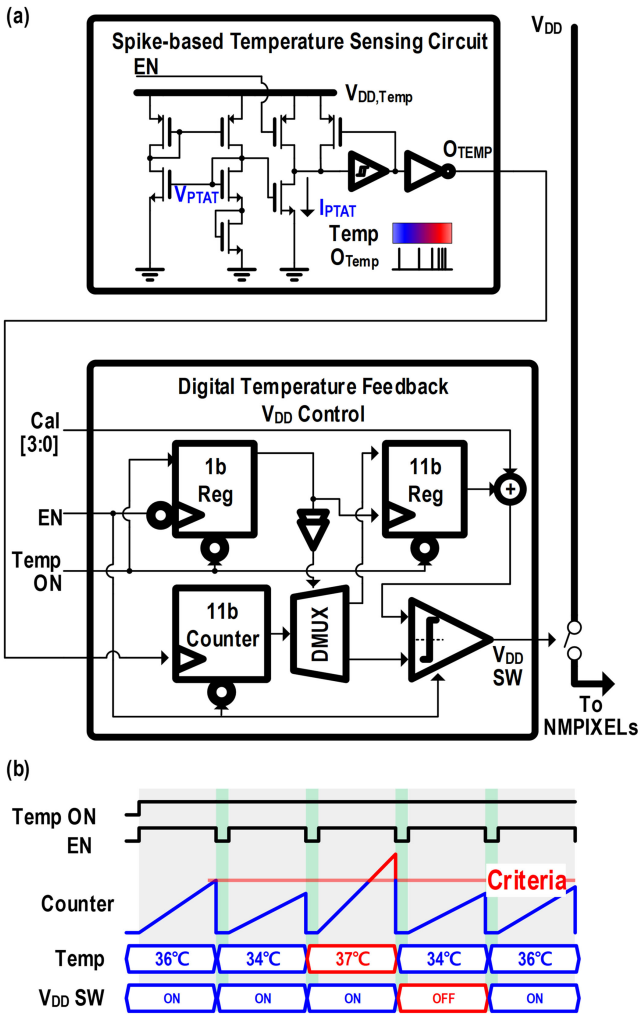

Fig. 12. (a) Schematic of temperature regulation circuit (b) timing waveform.

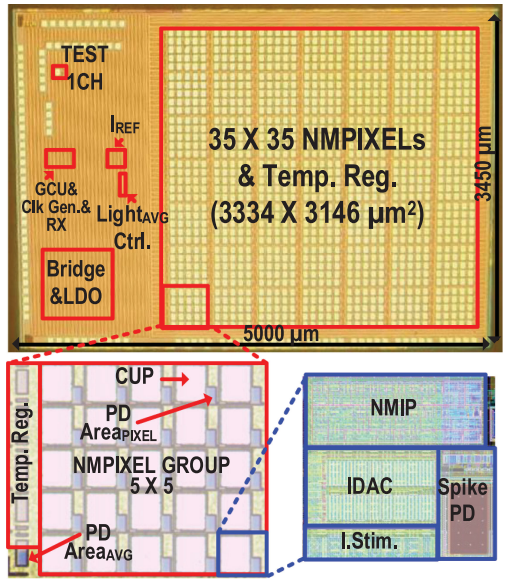

Fig. 13. Chip microphotograph.

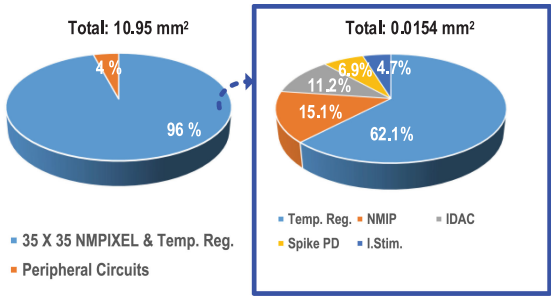

Fig. 14. Area breakdown.

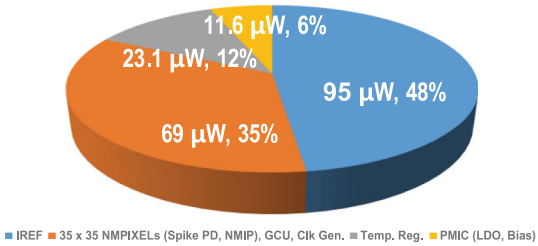

Fig. 15. Power consumption breakdown excluding stimulus.

the value when *EN* is 0. During the 1st *EN*, the 11b Reg saves the final count value by the help of 1b Register, delay circuit, and DMUX. The saved data can also be calibrated with Cal [3:0] with the adder to cope with the various human body environments. After saving the final value in the 1st *EN*, DMUX changes the path to the dynamic comparator, which compares at the negative edge of *EN*. After 2nd *EN*, the dynamic comparator compares the final counter value with the saved value in the 11b Reg with calibration, as the first value contains body temperature that can be used as the threshold value. If the final counter value exceeds the criteria, V_{DD} SW is off to disconnect the V_{DD} in the 5×5 NMPIXELs. The supply voltage of the temperature regulation circuit ($V_{DD,TEMP}$) is separated with a supply voltage of NMPIXELs (V_{DD}), which enables continuous temperature monitoring despite the inactive status of NMPIXELs.

V. Measurement Results

The proposed NRP SoC is fabricated in a 0.18 μm 1P6M standard CMOS process, as shown in Fig. 13. 35×35 NMPIXELs area is similar to an active macular area (10 mm^2), which can stimulate retinal cells efficiently. In order to implant into the human eye, additional eye-conformable fabrications would be necessary, such as transfer printing [21] or distributed chip concept [22]. The peripheral circuit occupies only 4% in the whole chip area, and the NMPIXEL area is 0.0072 mm^2/ch, as shown in Fig. 14.

Fig. 15 shows the power consumption breakdown in the rest state, excluding stimulus. The power consumption of total control logic, including Spike PD, NMIP, GCU, and Clock generator (Clk Gen.), is only 69 μW or 56.3 nW/Ch. I_{REF} power consumption is 95 μW due to the trade-off with the area efficiency of IDAC.

Fig. 16 shows the output of the Spike PD. Multiple spikes are measured, and spike-rate average and variance are calculated. In Fig. 16(a), the duration measured is 50 ns, which is much smaller than the spike-rate. The measured duration infers the linear spike rate modulation is not affected by the duration.

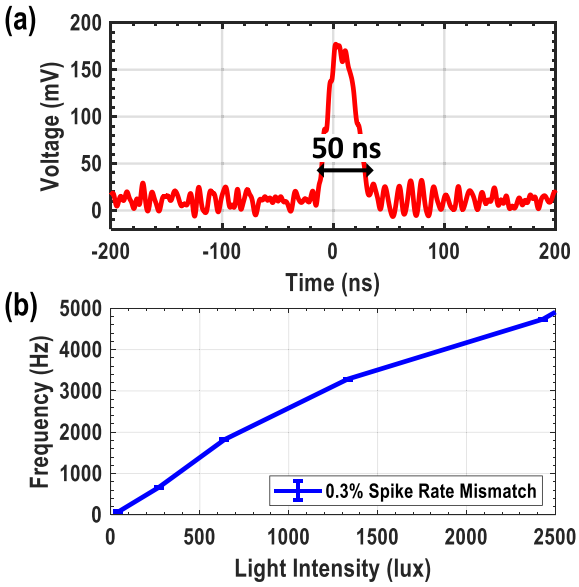

Fig. 16. Measurement of Spike PD: (a) single output (b) spike-rate.

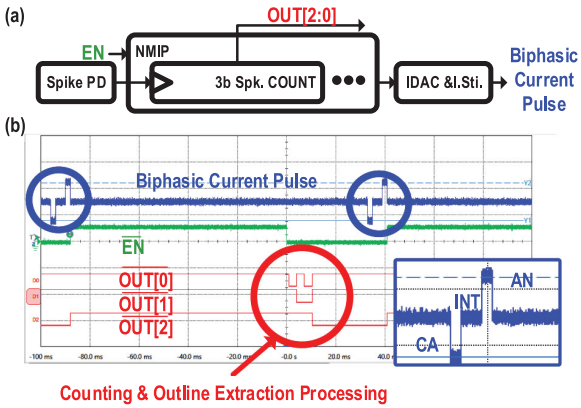

Fig. 17. Single NMPIXEL's measurement; (a) test points (b) its results.

Fig. 16(b) shows the spike rate that is linearly changed by the light intensity with a variation of 0.3%. Single NMPIXEL's measurement is shown in Fig. 17. Once the EN is 1, the 3b Spk. COUNT starts to count the number of the spike, and when the output reaches 100_2, NMIP calculates the value and generates the corresponding biphasic current pulse.

For the 35 × 35 NMPIXEL measurements, the customized test setup is configured, as shown in Fig. 18. A DLP projector generates the optical patterns of all the alphabet characters (A-Z, a-z), and projects to the proposed NRP chip. For the bench-top test, each NMPIXEL contains a transmission switch with the column selector for all the NMPIXEL current extraction. As a result, 35 × 35 current stimulus is extracted sequentially. Each current stimulus goes to the current-to-voltage converter by the configuration of the resistor of 2 kΩ and analog buffer (TLV6004, Texas Instrument) and is digitized in the ADC (ADC124S021, Texas Instrument). An FPGA (Atrix-7, Xilinx) communicates the control signal and the digitized current value of 35 × 35 NMPIXELs with a laptop using UART.

Fig. 19 shows the electrical stimulus patterns with outline extraction mode and conventional light intensity mode. The

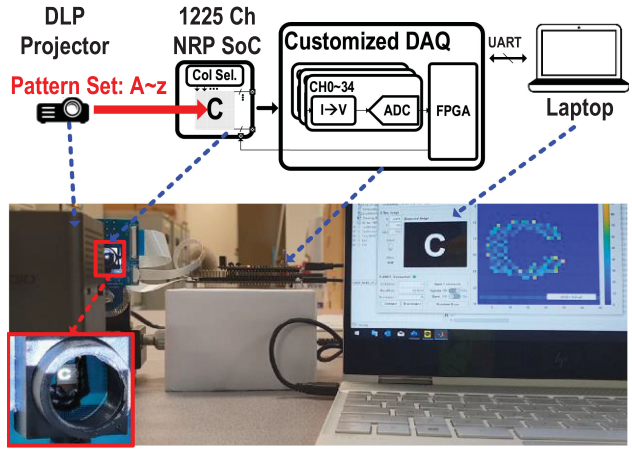

Fig. 18. Customized test setup for 35 × 35 NMPIXELs' measurement.

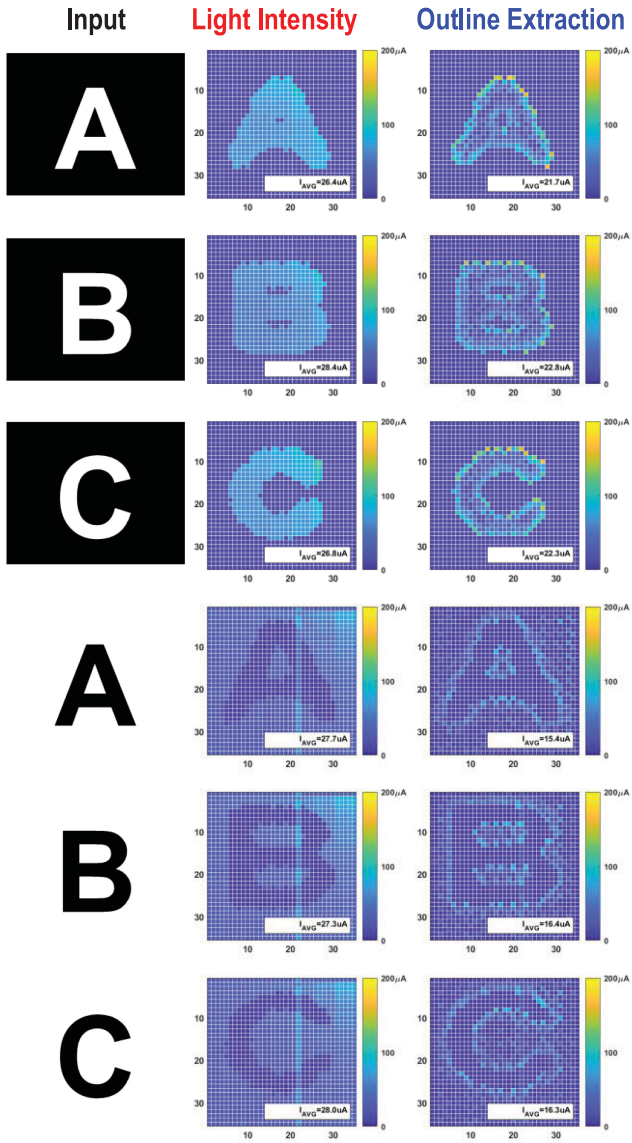

Fig. 19. Measurement results of 35 × 35 NMPIXELs current levels and their average (I_{AVG}) in the black and white background optical patterns.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART RP SOCS

		This work	TBioCAS'13[9]	JSSCC'09[11]	JSSC'14[12]	S&M'18[23]	VLSI'16[24]
Target		Sub-retina	Epi-retina	Sub-retina	-	Sub-retina	suprachoroidal
Temperature increase regulation		Yes (Localized 49 points)	No	No	Yes (1 point)	No	No
Spike PD NMIP Controller	Light sensor	On-chip PD \wth. Spike Out	Ext. Camera	On-Chip PD \wth. Voltage Out	Ext. Camera	On-Chip APS \wth. Voltage Out & Ext. IR Pattern Gen.	Ext. Camera
	On Chip Image processing	1) Outline Extraction 2) Light Intensity	No	Light Intensity	No	No	No
	Power/Ch.	56.3 nW	19.3 µW (Ctrl.)	1 µW	129 µW	1.04 µW	
Current stimulator	[a]Normalized Stimulus Power/Ch.	1.27 µW	35.2 µW	1.56 µW	89.45 µW	< 370 µW	
	Compliance voltage (V)	±1.6 (Open)	±10	±2	±1.35	0.5	
	Stimulus $Current_{MAX}$	0.6/0.8/1 mA	0.5 mA	0.1 mA	0.465 mA	19.97 µA	1.24 mA
	Stimulation Strategy	Simultaneous	Sequential	Sequential	Simultaneous	-	
Overall power consumption		2.7 mW	77.8 mW	[b]10.13 mW	33 mW	-	
Area	# of Ch	1225	1024	1600	256	256	
	Pixel size (µm×µm)	84.3×86.6	303×337/4Ch	70×70	150×150	85×85	
Power rectifier		On-chip LDOs	On-Chip HV LDOs	On-Chip	On-Chip LDOs	On-Chip PD	On-Chip HV LDOs
Process		0.18 µm CMOS	0.18 µm HV CMOS	0.35 µm CMOS	65 nm CMOS	0.18 µm CIS	0.35 µm HV CMOS

a. Absolute stimulus power /Ch / stimulus $current_{MAX}$ × 0.5 mA.
b. Converted stimulus power with same pulse rate with this work to generate whole patterns (17.06 Hz).

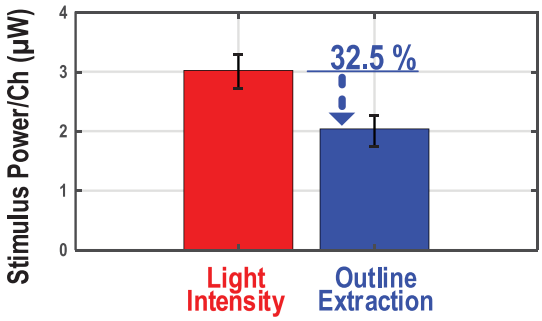

Fig. 20. Comparison of average stimulus power consumption per channel.

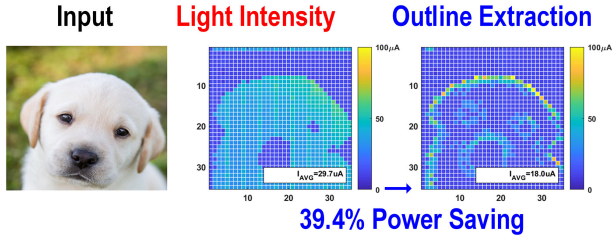

Fig. 21. Stimulus results of the dog image as an optical input.

input light patterns are alphabet set (A, B, C) in the white and black background, which is the highest contrast in the letter's outline region. Even though single-pixel stimulus power with the outline extraction mode is higher than that with light intensity mode, average stimulus power consumption (proportional to I_{AVG}) with outline extraction mode is 46% lower than that of conventional light intensity mode in the white background case, 18% lower in the black background, respectively. The variance in the two modes comes from the different optical input patterns due to the DLP limitation (manual lens focusing, variant white level). Despite the variance, outline extraction saves more stimulus power compared with light intensity mode.

We project all the alphabet characters and average all the stimulus of each mode, as shown in Fig. 20. In comparison, power consumption with outline extraction saves 32.5%, compared with that of conventional light intensity mode. When we use a dog as an input image, the result indicates that the stimulus of the outline extraction retains many details, compared with that of the conventional light intensity mode, as shown in Fig. 21. Some detail loss comes from the optical focusing, which has to be considered deeply in the clinical trials.

Table I compares the proposed NRP SoC with the state-of-the-art RP SoCs. The proposed NRP contains the localized 49 points temperature regulation circuit for the first time. Thanks to the on-chip spike-output & neuromorphic image processor, control power consumption is only 56.3 nW/Ch, which is the smallest among RP SoCs. Normalized stimulus power consumption per channel is 1.27 μW, which is the lowest among RP SoCs. Besides, such low power consumption makes it possible to increase the stimulus rate in the simultaneous stimulation mode. Overall power consumption is 2.7 mW, which is the only one lower than the physiological power consumption of the human eye. The number of channels is 1225, which is comparable with other RP SoCs.

VI. CONCLUSION

We proposed and verified a 1225 Ch. on-chip fully digital neuromorphic image processor (NMIP) with outline extraction to reduce image blurring and image processing and stimulus power with a reasonable number of channel integration. The

power consumption of the proposed NRP SoC is 56.3 nW/Ch as we control the power consumption by mimicking human retinal network, asynchronous, digital operation. Thanks to the on-chip outline extraction mode, the power consumption of stimulus, which is the most power-consuming among the blocks, is dramatically reduced to 1.27 μW/Ch., the lowest among the existing RP SoCs. The proposed NRP SoC proposes and verifies the localized temperature regulation circuit for the first time to prevent cell damage. Outline extraction stimulation is expected to provide better visual information to blind patients. Further studies for the clinical research, such as long-term implantable packaging, functional test in the electrolyte solution, and eye-conformable chip fabrication, are remained to realize the implantation of the proposed chip for the visual function restoration of blind patients.

REFERENCES

[1] E. Zrenner, "Fighting blindness with microelectronics," *Sci. Transl. Med.*, vol. 5, no. 210, 2013, paper. 210ps16.

[2] L. S. Lim *et al.*, "Age-related macular degeneration," *Lancet*, vol. 379, no. 9827, pp. 1728–1738, 2012.

[3] R. D. Jager, W. F. Mieler, and J. W. Miller, "Age-related macular degeneration," *N. Engl. J. Med.*, vol. 358, no. 24, pp. 2606–2617, 2008.

[4] M. S. Humayun *et al.*, "Interim results from the international trial of second sight's visual prosthesis," *Ophthalmology*, vol. 119, no. 24, pp. 779–788, 2012.

[5] K. Stingl *et al.*, "Artificial vision with wirelessly powered subretinal electronic implant alpha-IMS," *Proc. R. Soc. B.*, vol. 280, no. 1757, 2013, Art. no. 20130077.

[6] R. Sarpeshkar, "Neuromorphic electronics," in *Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems*, Cambridge: Cambridge Univ. Press, 2010, pp. 697–752.

[7] J. Li *et al.*, "Human-body-coupled power-delivery and ambient-energy-harvesting ICs for a full-body-area power sustainability," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 63, pp. 514–515, Feb. 2020.

[8] J. Li *et al.*, "Body-Area powering with human body-coupled power transmission and energy harvesting ICs," *IEEE Trans. Biomed Circuits Syst.*, early access, doi: 10.1109/TBCAS.2020.3039191.

[9] Y. K. Lo *et al.*, "A fully-integrated high-compliance voltage SoC for epiretinal and neural prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 761–772, Dec. 2013.

[10] J. O. Mills, A. Jalil, and P. E. Stanga, "Electronic retinal implants and artificial vision: Journey and present," *Eye*, vol. 31, no. 10, pp. 1383–1398, 2017.

[11] A. Rothermel *et al.*, "A CMOS chip with active pixel array and specific test features for subretinal implantation," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 290–300, Jan. 2009.

[12] N. Tran *et al.*, "A complete 256-electrode retinal prosthesis chip," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 751–765, Mar. 2014.

[13] J. H. Park, J. S. Y. Tan, H. Wu, and J. Yoo, "1225-Channel localized temperature-regulated neuromorphic retinal-prosthesis SoC with 56.3nW/channel image processor," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2020, pp. 508–509, vol. 63.

[14] R. Wilke *et al.*, "Spatial resolution and perception of patterns mediated by a subretinal 16-electrode array in patients blinded by hereditary retinal dystrophies," *Investig. Ophthalmol. Vis. Sci.*, vol. 52, no. 8, pp. 5995–6003, Jul. 2011.

[15] A. K. Ahuja, M. R. Behrend, M. Kuroda, M. S. Humayun, and J. D. Weiland, "An in vitro model of a retinal prosthesis," *IEEE Trans. Biomed. Eng.*, vol. 55, no. 6, pp. 1744–1753, Jun. 2008.

[16] R. G. H. Wilke *et al.*, "Electric crosstalk impairs spatial resolution of multi-electrode arrays in retinal implants," *J. Neural Eng.*, vol. 8, no. 4, 2011, Art. no. 046016.

[17] N. Lotze and Y. Manoli, "A 62 mV 0.13 μm CMOS standard-cell-based design technique using schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan. 2012.

[18] H. Naganuma, K. Kiyoyama, and T. Tanaka, "A 37 $\times$ 37 pixels artificial retina chip with edge enhancement function for 3-D stacked fully implantable retinal prosthesis," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, Nov. 2012, pp. 212–215.

[19] H. Schütz, S. Gambach, H. Kaim, and A. Rothermel, "Pixel array with 5x5 spatial highpass filter for a retinal implant," in *Proc. ESSCIRC 43rd IEEE Eur. Solid-State Circuits Conf.*, Sep. 2017, pp. 1–4.

[20] M. Ghovanloo and K. Najafi, "A compact large voltage-compliance high output-impedance programmable current source for implantable microstimulators," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97–105, 2005.

[21] M. A. Meitl *et al.*, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," *Nature Mater.*, vol. 5, no. 1, pp. 33–38, 2006.

[22] J. Ohta *et al.*, "Silicon LSI-based smart stimulators for retinal prosthesis," *IEEE Eng. Med. Biol. Mag.*, vol. 25, no. 5, pp. 47–59, Oct./Nov. 2006.

[23] C.-Y. Wu *et al.*, "A CMOS 256-pixel photovoltaics-powered implantable chip with active pixel sensors and iridium-oxide electrodes for subretinal prostheses," *Sens. Mater*, vol. 30, no. 2, pp. 193–211, 2018.

[24] Y. Terasawa, K. Shodo, K. Osawa, and J. Ohta, "Features of retinal prosthesis using suprachoroidal transretinal stimulation from an electrical circuit perspective," in *Proc., IEEE Symp. VLSI Circuits*, 2016, pp. 1–2.

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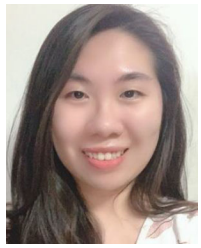

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