CMOS Image Sensor Design and Image Processing Algorithm Implementation for Total Hip Arthroplasty Surgery

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***Abstract*—As the average age of the population goes higher, the people undergo hip arthroplasty surgery to replace their stiff and painful damaged hip joints. To reduce the risk factor after the surgery we developed a visual aided system in previous works. In order to solve the integration problems of commercial camera with other sensors into the femoral head and to minimize the area and power consumption, in this paper we propose a CMOS image sensor of resolution 200 × 200 specially designed for the application in which each individual pixel measures around 15 μm × 15 μm in size and the image sensor chip size measures about 3.5 mm × 3.5 mm. The proposed sensor is simulated with the input current variations from 2 pA to 100 pA for the individual pixels and the corresponding measurements for each pixel range from 2 mV to 855 mV. Besides, we put forward a new method of pattern detection and recognition in the blood-covered situation, which provides an accurate segmentation of patterns from the blood. All the detected patterns are recognized by generating its right 9-bit binary ID required for the pose estimation calculation. Furthermore, to reduce system power consumption, we implement algorithms on FPGA to process the image data pixel by pixel and transmit it directly to the computer for post-processing. Experimental results show that the pattern detection rate goes as high as 99%, which is 5% better in accuracy compared to the top hat algorithm. The power consumption of the system is 213 mW, which is a 70% decrease compared to our previous work.**

***Index Terms*—FPGA, image processing, patterns detection, total hip arthroplasty.**

I. Introduction

With an increase in the average age of the population, a variety of diseases like arthritis and many other human activities make the hip joint stiff and extremely painful. The ultimate solution to alleviate pain and regain mobility is to replace the damaged hip joint [1]. Fig. 1 depicts a healthy and damaged joint, smooth rubbery cartilage covers the end of bones, letting the bones glide against each other easily. Whereas the damaged cartilage usually by arthritis and bone rub against each other makes the joint painful and stiff. According to the annual report published by the American Academy of Orthopedic Surgeons (AAOS) and American Joint Replacement Registry (AJRR) on hip and knee arthroplasty from the year 2012–2017. More than 443,219 various hip procedures including hip resurfacing, partial hip replacement or Hemiarthroplasty, hip revision and total hip replacement are performed in the United States, and the number is forecasted to increase in the next two decades. Total hip replacement (THR) procedure has been reported to be 79.2% of all the hip arthroplasty procedures that are quite significant [2].

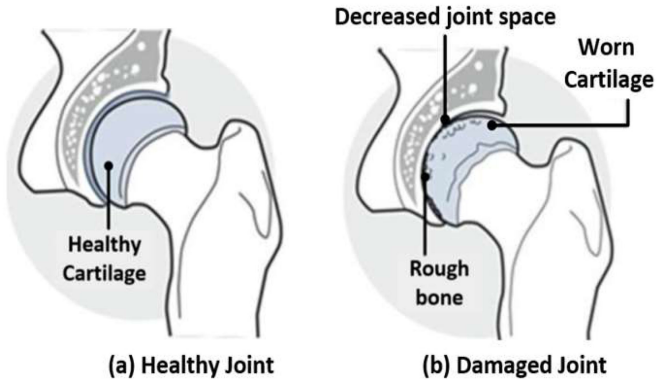

Fig. 1. Hip joint.

However, the total hip replacement arthroplasty surgeries have been reported a failure rate of about 10% which may cause intense complications such as dislocation, prosthetic impingement, infections, intraoperative fracture, leg length discrepancy among other complications of wear and loosening [3]. Common failures of THR are prosthetic impingement and dislocation whose occurrence is estimated between 0.5% to 11% [4], [5]. During THR surgery, placement of prosthetic components into the safe zone is a key step [6], if not placed properly it may lead to dislocation of the components and cause a limited hip range of motion (ROM) [7]. Therefore, surgeons strongly need a visualizing system in order to place prosthetic components into

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the safe zone during hip joint arthroplasty. Prosthetic component placement into the safe zone has been presented and discussed in [6], three-dimensional (3D) models designed by using computed tomography (CT) images helped surgeons to present motion restriction of the hip joint [8]. However, the preoperative system decision may need to be modified because of the possibility of uncertainty to occur during the surgery. Although the CT based navigation system has provided a significant development in the implantation of prosthetic components into the safe zone [9], but it cannot be used as a standard operating technique to position the prostheses, because it may cost an additional operation time, more money and furthermore the patients are exposed to the harmful radiations [9].

Orthopilot surgical robot has provided a CT free navigation system for more precise, accurate and reliable prostheses implants, where the patients do not need to undergo preoperative scanning requirements [10]. Nevertheless, it needs an extra marker affixing unit to the bony landmarks, hence making the calibration, data processing and collection more complex, which may cause extra damage and infections to the patients as well [11]. Moreover, it is quite expensive. In our work [12], we have designed a visually aided wireless monitoring system to estimate the relative pose between the femoral head prosthesis and acetabular cup prosthesis during the hip joint arthroplasty surgery. This CT free smart trial helps the surgeons to visualize the positioning of prosthetic components into the safe zone without creating bony anatomical landmarks during surgery; moreover, it is also cost-effective. Power consumption by the system is only 46.8 mW but it is hard to mount enough contact sensors on the femoral head prosthesis providing a limited range of motion inside the acetabular cup thereby increasing the system mean error to 4.40 degrees, hence making the system far from its practical use.

Later, to deal with the problems in mounting enough contact sensors onto the femoral head prosthesis. We proposed a design of monocular vision and IMU-based visual aided system [13], the system consists of a miniature camera inside the femoral head prosthesis from Omni Vision (OV7660) to capture images inside the acetabular cup, and an inertial measurement unit IMU for more precise pose estimation. The commercial camera module used in our previous works has a package dimension of 4.2 mm $\times$ 3.9 mm with an optical size 1/5 inch and active power consumption by the module is 40 mW without loading. Using the camera inside the femoral head to take images from the acetabular cup and then transmitting the data through a Wi-Fi module to the host computer to perform processing off-chip takes a lot of execution time and power. The power consumption by a monocular vision-based system is about 980 mW and with IMU the system consumes 768 mW, which is relatively high. This system can work for as long as 15 minutes. Furthermore, uncertain light conditions inside the acetabular cup and the blood interference during surgery may lead to the failure of a vision-based system where pose estimation is based on accurate detection of the features and coordinates of the customized patterns. Therefore, we need to design a system on chip to capture and process the image data on-chip inside the acetabular cup rather than sending the data off-chip for processing to minimize the modules integration problem with the least power consumption to prolong system operation time.

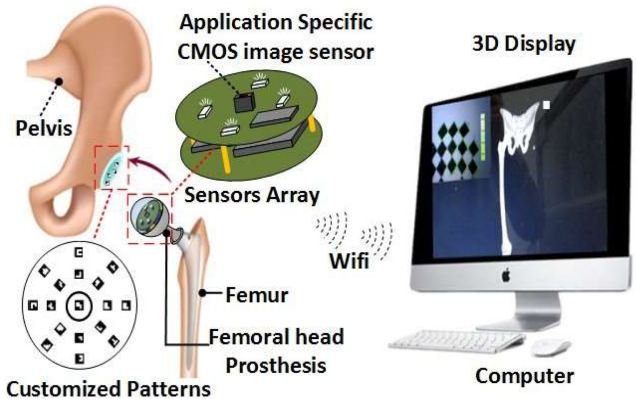


Fig. 2. Vision based smart trial.

The system architecture of our proposed smart trail is illustrated in Fig. 2, where our application-specific CMOS image sensor replaces the commercial camera from Omni Vision. The system comprises an application-specific CMOS image sensor of resolution 200 $\times$ 200 inside a femoral head prosthesis with other sensor circuits to capture the images from the acetabular cup. Whereas the acetabular cup has customized reference patterns on its inner liner. The captured images are further processed from uneven illumination and blood interference conditions on the hardware interface for on-chip image processing. The pose estimation calculation between the femoral head prosthesis and the acetabular cup is performed off-chip using software developed with a visual studio on the computer.

In this paper, we first present the design and simulation of CMOS image sensor for our smart trial. The proposed image sensor replaces a bulky camera from the femoral head, which consumes most of the system power. Secondly, during hip arthroplasty surgery there is a possibility of blood interference on the sight of the camera, which may lead to the failure in estimating the exact pose of femoral head prosthesis inside the acetabulum. An efficient image-processing algorithm is developed to detect the features and coordinates of each pattern from the blood-covered images. The method is compared with the top-hat algorithm [13]. Finally, the algorithms are implemented on FPGA for the ASIC development to provide an on-chip image processing. Performance and power consumption by the methods are compared.

The rest of the paper is organized as follows: The CMOS imaging system architecture is presented in Section II and image processing algorithm for pattern detection and recognition are discussed in Section III, the implementation of image processing and its hardware demonstration results are explained in Section IV. FPGA experimental results and discussions are given in Section V. Finally, Section VI concludes the paper.

II. Imaging System Architecture

The proposed imaging system architecture is presented in Fig. 3, in which the image sensor is composed of 4T pixels

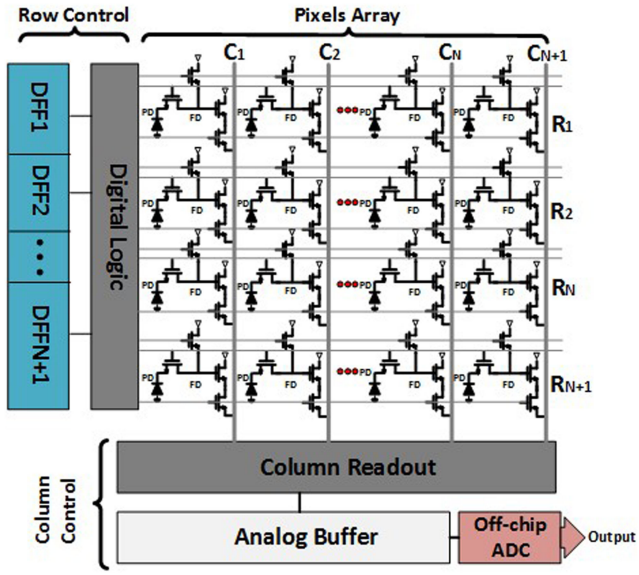


Fig. 3. Imaging system architecture.

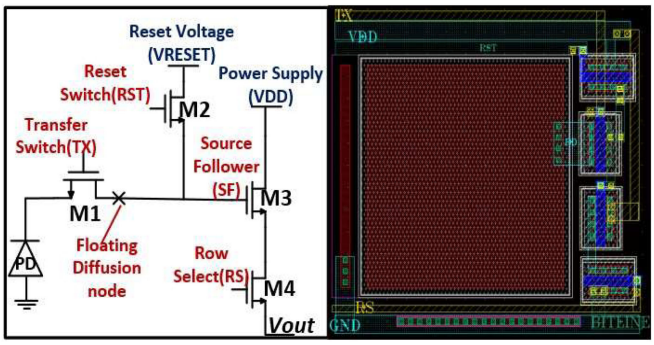


Fig. 4. 4T schematic view and layout of the pixel.

structure of an array size 200 × 200. Since the application requirement is dynamic illumination conditions with minimum power consumption and better integration capability CMOS technology is considered the right choice for the sensor design [14]. CMOS image sensors can be categorized as either operating in current mode or voltage mode depending on the type of readout circuit. In a voltage mode, when the electrons are transformed from charge to voltage domain they are accumulated on the floating diffusion (FD) node and are read out by the source follower (SF) [14]. Whereas in the current mode, either the readout transistor is biased in the velocity saturation region consuming large power because of high V_{ds} [15] or linear region where fixed pattern noise (FPN) is critical for linearity [16].

Voltage mode pixels are implemented in 0.18 μm 1P6M process technology. Vertical chain of DFFs and the digital logic circuits are used to generate global control signals to control the pixels connected in each row. To read the output values of the signal generated by each pixel is selected by the chain of DFFs and digital logic connected column-wise in the sensor array, the output will be finally buffered and digitalized using an off-chip ADC. Fig. 4 depicts the 4T structure of our pixel, which

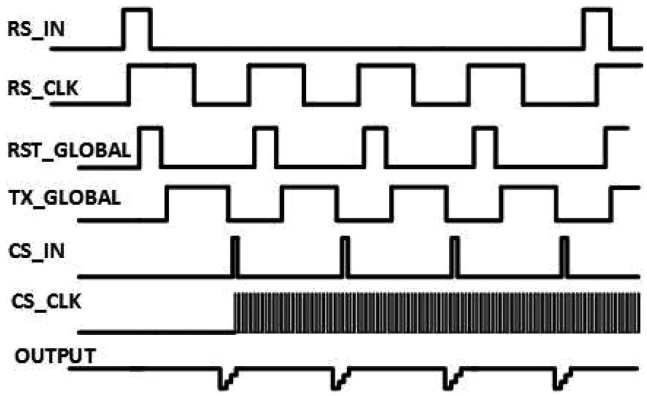


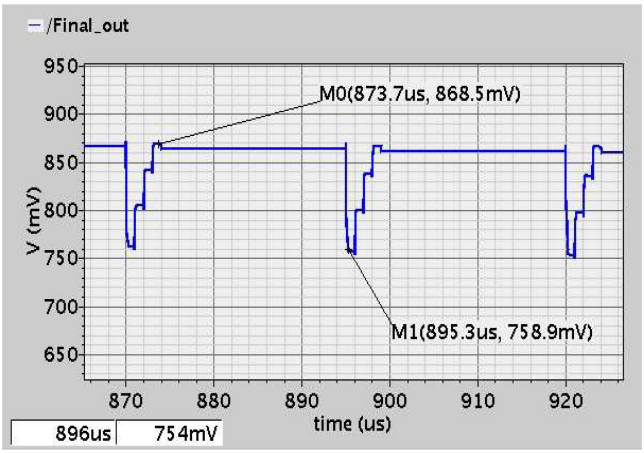
Fig. 5. Timing control signals.

comprises a photodiode, transfer switch (TX), reset switch (RS), source follower (SF) switch and a row select (RS) switch. The switches are controlled by the global control signals generated by the row control and column control circuits can be referred to our previous work [17]. Each unit pixel designed with a conventional 4T (four transistors) structure and a photodiode is designed to be around 10 μm × 10 μm making the total pixel size of about 15 μm × 15 μm to detect the low light variations each pixel has a fill factor of 60%.

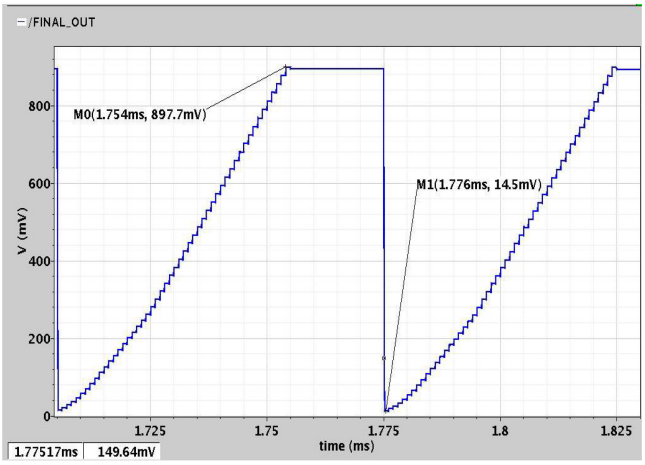
The timing sequence to control the array of pixels and generate an output signal is illustrated in Fig. 5. RS_IN is an input pulse signal to the vertical DFF chain, RS_CLK signal controls the respective rows in an array, and the clock frequency is set according to the number of rows in the sensor array. In a respective row cycle, all the pixels within a row are reset with a RST_GLOBAL signal, and TX_GLOBAL signal is used to turn on the gate of transfer switch for all the pixels. DFF chain and digital AND logic are used to control the pixels connected in rows. At the bottom of the imaging system horizontal chain of DFFs is used to generate CS_IN, a column control pulse. CS_CLK signals are produced to scan all the pixels within a respective row time to read the output signals column-wise. By changing the input signals the corresponding change at the output is observed.

A. Simulation Results for the Sensor

In this application, the image sensor can be used under dynamic light conditions, specially to the low light situations. To verify and analyze the sensor performance under different illumination conditions, we designed a capacitor and current source combination in a photogeneration block to model a circuit for each photodiode (PD) within a pixel to produce different input pixel signals. The output pixel values are verified with the corresponding change at the input stage. Different pixels array sizes have been implemented to test the design methodology. The output waveforms for 4 × 4 and 50 × 50 sensor array sizes are shown in Fig. 6(a) and (b) respectively, from which we can see that the 4 × 4 and 50 × 50 pixels array generate steps signal at the output, the design shows similar performances with 100 × 100 array size and 200 × 200 array size. The output voltage from the pixels ranges from 2 mV to 855 mV for the corresponding



(a) 4x4 Array simulation results.



(b) 50x50 Array simulation results.

Fig. 6. Simulation results from 4 × 4 and 50 × 50 Array.

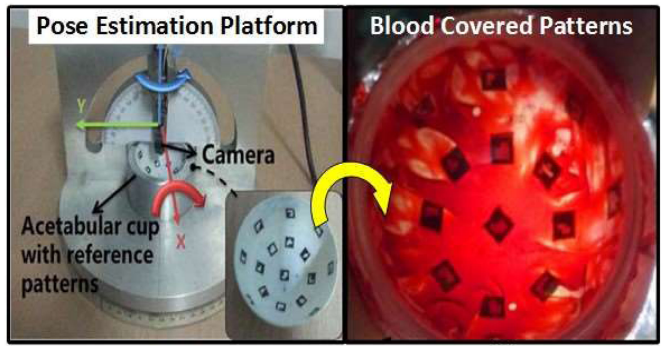
input values from the photodiode, the input signal variations ranges from 2 pA to 100 pA. The final output shows good linear performance for an input FD voltage of large swing varying from 0.09 V to 1.44 V with a power consumption of 20.8 mW. The linearity of the pixel can be further improved by choosing suitable design parameters, such as a smaller size of the SF and FD.

The image sensor module chip micrograph is shown in Fig. 7, the image sensor measures around 3.5 mm × 3.5 mm with pad frame, each unit pixel size measures around 15 μm × 15 μm big enough to detect low light signal variations [17]. Camera used in [13] is too bulky and it is hard to mount onto the femoral head and integrate with the other modules consuming most of the system power. The sensor size proposed in this paper is more compact and is designed to be integrated with an on-chip image processing ASIC for the SoC development. Table I presents the design summary of our image sensor, in which we can find the pixels resolution for the finished design is 200 × 200 with TSMC 0.18 μm process, which can be extended to any array size hence making the whole design flexible for different image processing algorithms.

Fig. 7. Sensor chip micrograph.

TABLE I
CMOS IMAGE SENSOR DESIGN SUMMARY

Process	TSMC 0.18µm 1-poly 6-metal standard CMOS process technology
Pixels Resolution	200 x 200
Pixel Size	15µm x 15µm (4T per pixel)
Fill Factor	60%
Chip Size	3.5mm x 3.5 mm
Supply Voltage	1.8/3.3



(a) (b)

Fig. 8. (a) Pose estimation platform. (b) Blood covered sample image.

III. IMAGE PROCESSING FOR PATTERNS DETECTION

A. Method for Patterns Detection

The pose estimation platform is depicted in Fig. 8, in which a camera is used to take the images inside the acetabular cup prosthesis [18], and liner inside the acetabular cup has some reference patterns in square shape and inside each square there is a combination of 3 × 3 small blocks colored white or black representing "1" or "0" respectively. Each pattern has

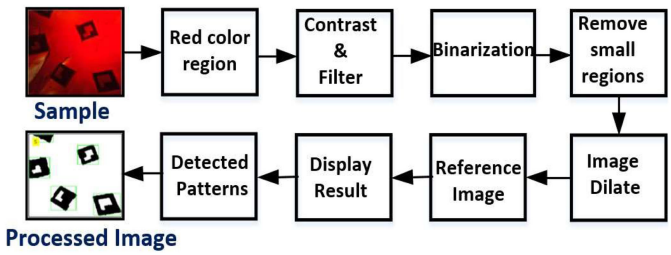


Fig. 9. Pattern dettion method.

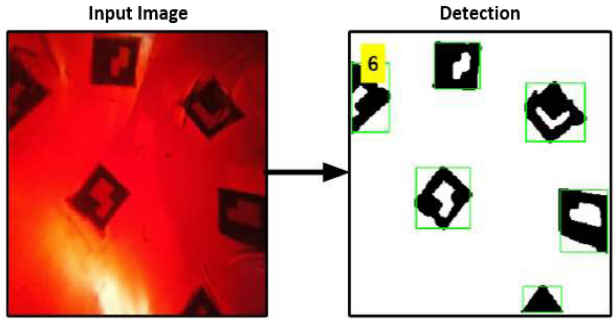


Fig. 10. Pattern detection.

its specific 9-bit binary ID and 4 vertexes, which are adopted to estimate the pose of the femoral head inside the acetabular cup. During outside body experiments, the light in the environment is enough and the images of reference patterns have uniform illumination the system works well. However, under dynamic light conditions and blood interference, the visual aided system may fail due to unrecognizable patterns. Therefore, an accurate segmentation method is required to detect and recognize each pattern with all four vertexes and features points to match with system initialized feature points for post-processing during THR surgery. Conventional monochrome image segmentation involve edge detection, histogram thresholding and region-based image segmentation use of these classical methods is limited because of low accuracy, while some other specific theories involve segmentation based on mathematical morphology, statistics and artificial neural network [19] are considered complex.

There are some techniques related to the segmentation of plants from the soil discussed in [20] and the segmentation of optic disc and optic cup in the detection of glaucoma using RGB color space [21]. In our application, we need to detect the patterns and recognize the binary IDs of the customized patterns, so we are proposing a new method to perform both the operations.

A sample image obtained from the pose estimation platform depicted in Fig. 9 is taken as an input image. We have used red ink in place of blood for our experiment to simulate a blood-covered situation. After selecting a red color in the image, an image enhancement technique is applied. In the image, edges for the patterns need to be preserved in order to detect it properly, for noise suppression and preserving the edges we applied a median filter, the generalized equation for the median filter [22] can be expressed as:

$$\widehat{f}(x,y) = \underset{(s,t)\in S_{xy}}{\text{median}} \{g(s,t)\}, \tag{1}$$

where $\widehat{f}(x,y)$ represents a restored image and S_{xy} represents the set of coordinates. In a square sub-image window, 3×3 (s,t) represents the pixel coordinates.

By considering the image sub-window of 3×3 square neighborhood the median filter calculates the median value by sorting all the pixel values from the surrounding neighborhood into numerical order and then replaces the pixel value under consideration with the median. Contrast variation, degraded image and uneven light illumination conditions where the pixels cannot be classified as a foreground or background locally adaptive thresholding is the right option, thresholding is always a vital part in an image binarization [23], $T(x,y)$ represents threshold and it can be expressed as follows:

$$b(x,y) = \begin{cases} 0, & \text{if } I(x,y) \le T(x,y), \\ 1, & \text{otherwise}, \end{cases} \tag{2}$$

$$T(x,y) = I_o(x,y) + T_o, \tag{3}$$

$b(x,y)$ represents a binary image and $I(x,y) \in [0,1]$ specifies the intensity of the pixel at any point location (x,y) of the image I. Morphological opening of the image, is denoted by $I_o(x,y)$ whereas T_o specifies the threshold of I_o. Images obtained from our platform have darker foreground patterns than the background for image binarization the features of thresholding including foreground polarity and sensitivity are properly controlled. Patterns are finally obtained by image dilation using square structuring elements. Opening in the morphological image processing is given as $I \circ b$, where dilation of the image I by a structuring element b can be expressed as:

$$I \circ b = (I \ominus b) \oplus b \tag{4}$$

Final output processed images are displayed using blob analysis, and Fig. 10 shows the performance of our proposed method to detect the patterns from the blood-covered situation, All the patterns in the input image can be extracted from the blood, without been affected by uneven light illumination condition. Each pattern with all its feature points and four vertexes can be easily recognized. The performance of a proposed algorithm is compared with the top hat algorithm from our previous work in Fig. 11.

Sample images with different orientations are taken as an input, the proposed method can recognize all the patterns their corresponding vertexes and respective features quite accurately.

The proposed algorithm compared to the top hat algorithm achieves a detection rate as high as 99% with less complexity and more accuracy.

B. Method for Patterns Recognition

After detecting patterns from the blood, the next step is to recognize the patterns, each pattern represents its specific 9-bit binary ID, and these customized patterns are made up of nine

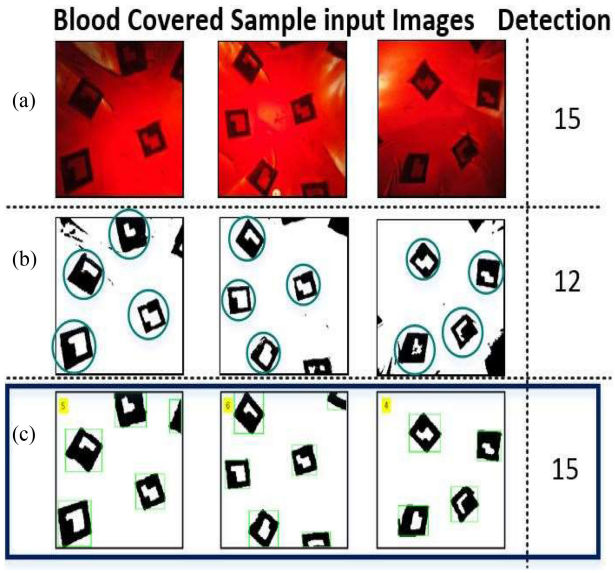


Fig. 11. Comparison of Patterns detection. The total number of detected patterns are listed at the end of each row. (a) Input sample images covered in the blood covered situation. (b) Patterns detected using top-hat algorithm [13]. (c) Patterns detection results using the proposed algorithm in this paper.

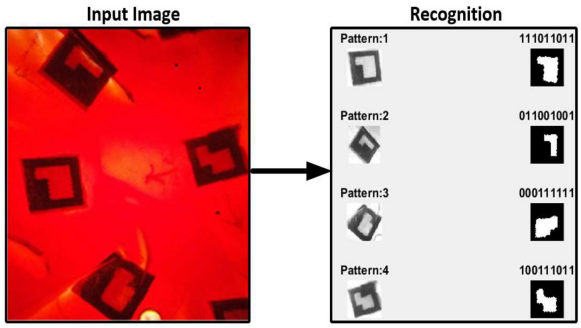


Fig. 12. Pattern recognition.

small blocks, black represents "0" while the white block represents "1". We have developed a method to recognize the detected patterns, and the algorithm will first find the contours of the patterns quadrangle in shape. These quadrangles are converted into squares of length 100 pixels, creating each cell of size 20 × 20 pixels inside each square. Next step in the algorithm is to find the center of each individual cell within a square if the center of the cell is black it will be detected as "0" and if the center of the cell is white, it will be read as "1".

Fig. 12 shows the output results of the pattern recognition method, it can be seen that all the patterns appeared in the frame can be recognized efficiently. These patterns detection and recognition has provided a major step forward towards pose estimation for the application.

IV. Image Processing on a Reconfigurable Hardware

Complete embedded vision system on chip is nowadays realizable [24]. We are integrating an image sensor with FPGA to develop a compact vision system on chip for THR surgery. Xilinx

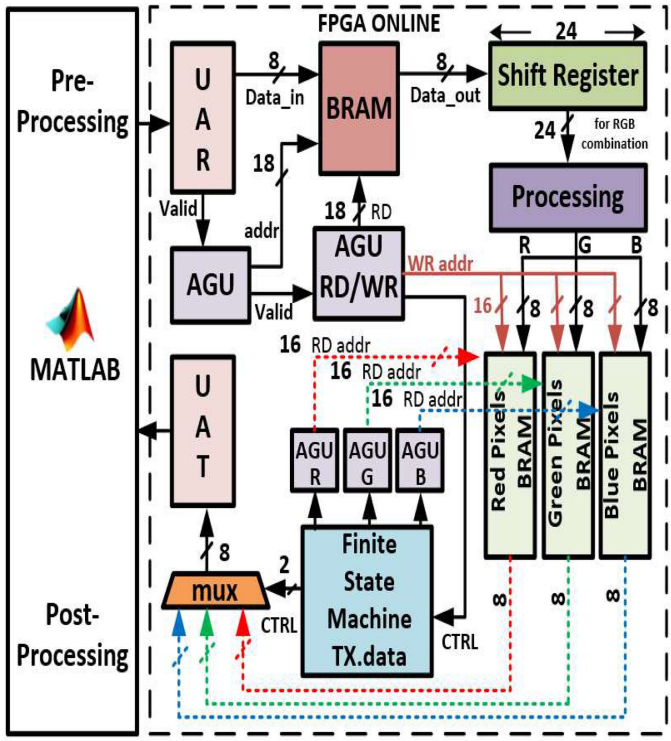


Fig. 13. Architecture for implementation on FPGA.

Virtex 7 board is used to implement image processing algorithms for the ASIC development and to perform parallel processing on the image data pixel by pixel received from the sensor. FPGA processes the image data and transmits the detected feature points of each pattern to the computer. Software developed with Visual Studio calculates the pose estimation based on the processed images. Image data transmission for post-processing using FPGA consumes less power compared to a Wi-Fi module used in our previous works.

For the realization of image processing on reconfigurable hardware, we are using the image data from the acetabular cup acquired by the CMOS image sensor of OV7660. The complete design flow of implementing image processing on FPGA is depicted in Fig. 13, the image size of resolution 286 × 186 from our smart trial prototype is chosen as an input for processing. Since the images cannot be read by FPGA in bitmap format the image is required to be converted into hexadecimal format. Pre-processing of converting the bitmap into hexadecimal is done in Matlab.

The hexadecimal format includes RGB data of the image, which is loaded onto the FPGA using RS 232 cable. The universal asynchronous receiver-transmitter (UART) port is used to establish a serial communication link between the computer and the FPGA. The RGB input data is saved onto on-chip BRAM at the address locations generated by the address generation unit (AGU). The RGB data is read out from block RAM and sent to the 24 bits shift register for RGB combination for further processing. To speed up the processing time, two pixels are processed and transmitted in parallel. The processing block

performs three operations (1) brightness control for uneven illumination conditions in the input images, (2) segmentation of patterns from red color is realized to avoid interference of blood in detecting the patterns, and (3) threshold operation is used for isolating the patterns of interest.

In the next step, the processed RGB image data is written onto three separate BRAMs. AGU sends a valid signal to the finite state machine block when the image writing process stops. The finite state machine generates a valid signal for the multiplexer and AGU to read the processed data from the BRAM. The processed image data is sent back to the computer for post-processing using UAT.

V. Experimental Results and Discussions

Xilinx 1SE 14.4 design suit and ModelSim 10.0 SE is adopted to implement the image processing algorithms for functional design verification and simulations. The processing algorithms are synthesized on Xilinx Virtex 7 of part number xc7vx485t-2ffg1761 FPGA board for its real-time implementation. For simulation purposes, red ink is used in place of blood and poured inside the acetabular cup, which is covered with the plastic wrap, and the images are obtained from the platform exemplified in Fig. 8. The input image of size 286 $\times$ 186 is converted into hexadecimal format because the FPGA cannot handle standard image formats, the hexadecimal image data is then sent through the serial communication protocol using Universal Asynchronous Receiver (UAR) into the block RAM, the image data is readout of the block RAM into 24-bit shift register for RGB combination. In the application, uneven light conditions, blood interference and features extractions are the key problems to address. We implemented three operations including brightness control, image inversion and thresholding to extract the features of the patterns effectively.

By adding a constant value to each pixel value can increase the brightness of low light intensity, whereas by subtracting the constant value from the pixel value will decrease the brightness of the image. Segmentation of patterns from the red color to see the details of each pattern in more detail, an inversion operation is applied to the input images. The output results can be seen in Fig. 14, where each pattern is segmented from the red color. This operation is useful in the application because of uneven light illumination can produce a shadowed or saturated regions [25] in the images causing it difficult to identify the patterns in the blood-covered situation.

The output from this operation can be used for pattern detection for further processing, required in the pose estimation. The inversion operation reverses the order of pixel values when multiplied by -1 and by adding the constant value maps the output result in the permissible range. Consider a pixel value $n = I(x, y)$ within the range $[0,\ n_{\max}]$; the inversion operation can be expressed as equation (5)

$$f_{inv}(n) = -n + n_{\max} = n_{\max} - n \tag{5}$$

as an input is a color image, the RGB component of each pixel is equalized by taking the average of these color components [26]. Threshold operation is also significant for our application. In the segmentation process, thresholding helps to isolate the patterns from the background. The operation transforms all the pixels in two values, in this type of quantization the pixel values are compared with the constant threshold value a_{th}, which allows separating the pixels into two different classes. The function can be expressed as equation (6) [27], the function $f_{th}(a)$ will map the pixels values to either a_0 or a_1 that is the

$$f_{th}(a) = \begin{cases} a_0, & \text{for } a < a_{th} \\ a_1, & \text{for } a \geq a_{th} \end{cases} \tag{6}$$

where $0 < a_{th} < a_{\max}$.

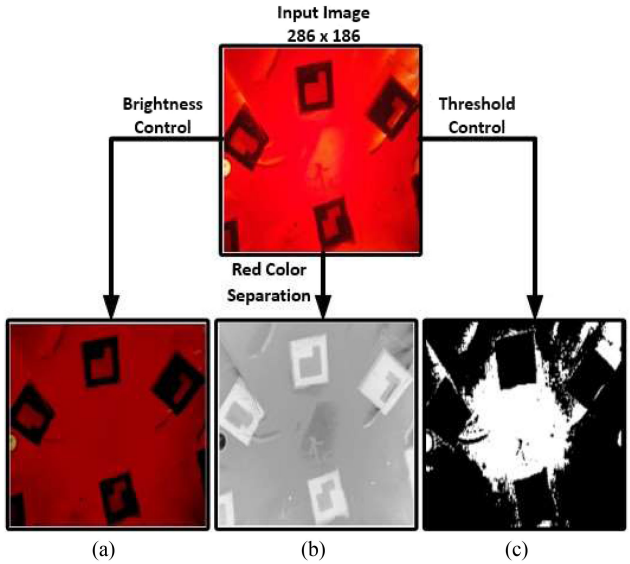


Fig. 14. Experiment results by implementing the image processing algorithms. (a) Output image after implementing brightness control operation. (b) Output image after segmentation of patterns from the red color by implementing image inversion operation. (c) Output image after the implementation of threshold control operation.

The processed image data is separated into its RGB components and sent into the three separate memory locations respectively. Once the process is complete the bitmap image data of the processed image is written onto the memory locations, the next step is to write the header for the image without the header image cannot be displayed at the output properly. The experiment setup is illustrated in Fig. 15, in which Xilinx FPGA is adopted in order to verify our processing on real-time hardware. The input image of size 286 $\times$ 186 with the patterns covered in the blood after three operations including the brightness, image inversion and the threshold the patterns can be analyzed quite efficiently in FPGA. Behavioral model of the algorithm is analyzed in ModelSim 10.0 SE and Xilinx ISE 14.4 is used for the synthesis and implementation. The implementation results are summarized in Table II. We can see that the synthesis frequency is 304 MHz using the LUTs and slice registers 760 and 819 respectively with a baud rate of 9600. Overall, power consumption in processing is around 213 mW, which considerably reduces power consumption by the whole system. The image data from the FPGA using serial communication link Universal Asynchronous Transmitter (UAT) is sent back to the computer for post processing.

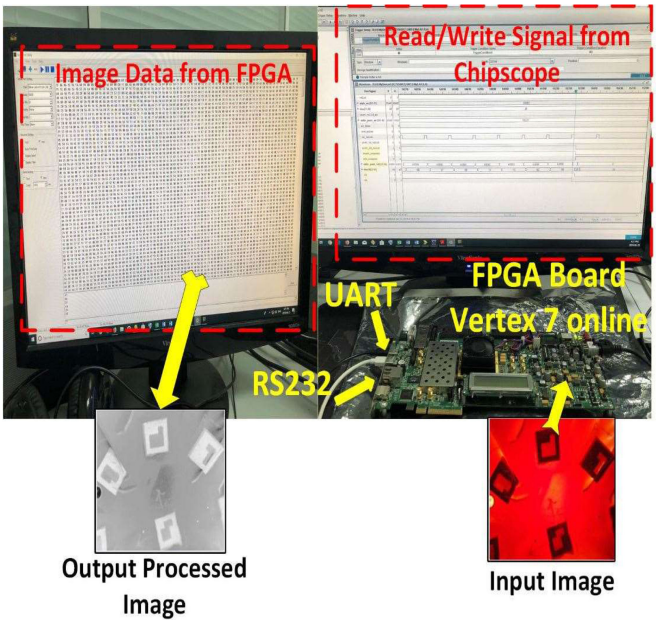


Fig. 15. Experiment setup.

TABLE II
IMPLEMENTATION SUMMARY FROM VIRTEX 7 FPGA BOARD

Design	LUTs	Slice Registers	Frequency	BRAMs	Power (mW)
Serial Test	760	819	~304 MHz	167	213

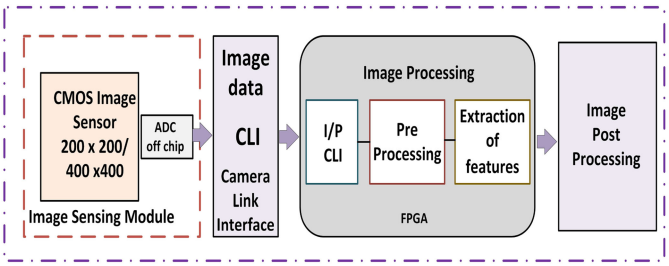


Fig. 16. Embedded vision system design flow.

An embedded vision system architecture to be used for the application is depicted in Fig. 16. The image data from our application-specific image sensor will be sent to the FPGA using a camera link interface. Where the FPGA will provide an on-chip image processing for the image data provided by the sensor.

Power consumption based on monocular vision (customized patterns) and IMU-based system are measured to be around 980 mW and 768 mW respectively, which is relativity high and consumes most of the system power. Implementation of algorithms proposed in this paper for on-chip processing and transmitting the images consumes only 213 mW that is considerably lower than the power consumptions presented in our previous work. Table III shows performance comparisons of the method proposed in our previous works. Parallel processing of the image data on-chip reduces the power consumed by the

TABLE III
PERFORMANCE OF IMPLEMENTATION METHODS

Method	Processing Platform	Accuracy (Patterns Detection)	Power
Monocular vision (customized patterns)	CPU	94.1%	980mW
IMU and monocular vision (chessboard patterns)	CPU	-	768mW
This Work (customized patterns)	Xilinx Vertex-7	99%	213mW

*The performance of monocular vision and IMU based methods are reported from our from previous work [13].

Wi-Fi transceiver. The feature points and coordinates of each detected pattern are transmitted directly to the computer using a serial communication link where software developed in Visual Studio estimates the relative pose between the femoral head and acetabular cup prosthesis from the extracted feature points after processing and the system initialized feature points.

So far, our image sensor with its custom resolution, size, and low power is considered enough for the application. However, in our future work, we will consider speed and accuracy by dividing the array of 200 × 200 pixels into 4 × 4 pixels block, to introduce signal processing within a single block as well as neighboring blocks of pixels for fast computation. This method will distribute the processing workload of our entire image sensor. ASIC design for image processing will be realized in the near future for the optimization of power consumption. As a result, the SoC design together with the CMOS image sensor for the application will be implemented.

VI. CONCLUSION

In this paper, we first present the design and simulation of CMOS image sensor for our smart trial. The proposed image sensor replaces a bulky camera from the femoral head, which consumes most of the system power. In future, we will consider speed and accuracy of the sensor by dividing the array of 200 × 200 pixels into 4 × 4 pixels block, for fast calculation within the block. Secondly, we propose a new method to detect each pattern from the blood-covered situation and then recognize each pattern from its features by generating its corresponding binary ID. The pattern detection rate is as high as 99%, which is 5% better in accuracy than the top hat algorithm. Furthermore, in order to reduce power consumption by the Wi-Fi module to transmit data wirelessly to the computer outside for pose estimation calculation. Image processing algorithms are implemented on FPGA to perform parallel processing on the image data pixel by pixel received from the sensor. The extracted feature points and coordinates are directly sent to the computer using a serial communication link without using a Wi-Fi transceiver, which reduced the overall system power. The design is synthesized using Xilinx Virtex 7 FPGA board for the ASIC development. Power consumption by the system is 213 mW, which is a 70% decrease compared to 980 mW and 768 mW consumed by monocular and IMU-based systems respectively. The reduction

of power consumption in this work significantly improves the operation time of our system. This digital design implementation will help for our final SoC design by integrating the CMOS image sensor with on-chip image processing in the future.

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