An ASIC for Recording and Stimulation in Stacked Microchannel Neural Interfaces

Henry T. Lancashire, Dai Jiang, *Member, IEEE*, Andreas Demosthenous, *Fellow, IEEE*, and Nick Donaldson

***Abstract*—This paper presents an active microchannel neural interface (MNI) using seven stacked application specific integrated circuits (ASICs). The approach provides a solution to the present problem of interconnect density in three-dimensional (3-D) MNIs. The 4 mm^2 ASIC is implemented in 0.35 μm high-voltage CMOS technology. Each ASIC is the base for seven microchannels each with three electrodes in a pseudo-tripolar arrangement. Multiplexing allows stimulating or recording from any one of 49 channels, across seven ASICs. Connections to the ASICs are made with a five-line parallel bus. Current controlled biphasic stimulation from 5 to 500 μA has been demonstrated with switching between channels and ASICs. The high-voltage technology gives a compliance of 40 V for stimulation, appropriate for the high impedances within microchannels. High frequency biphasic stimulation, up to 40 kHz is achieved, suitable for reversible high frequency nerve blockades. Recording has been demonstrated with mV level signals; common-mode inputs are differentially distorted and limit the CMRR to 40 dB. The ASIC has been used in vitro in conjunction with an oversize (2 mm diameter) microchannel in phosphate buffered saline, demonstrating attenuation of interference from outside the microchannel and tripolar recording of signals from within the microchannel. By using five-lines for 49 active microchannels the device overcomes limitations when connecting many electrodes in a 3-D miniaturized nerve interface.**

***Index Terms*—Biomedical electrodes, biomedical electronics, integrated circuit testing, microchannels, multiplexer, neural interfaces.**

I. Introduction

INTERFACES with the nervous system have many clinical and investigative applications. Peripheral nerve interfaces can help overcome two common complaints of upper limb prothesis users: limited degrees of freedom and unintuitive control [1]. Intended movements can be recorded from residual peripheral nerves [2]–[4], and neural stimulation can be used to provide sensory feedback [2], [4], [5], making bidirectional closed-loop control a possibility [6], [7]. One approach to intuitive sensory and motor interfaces is through increased selectivity by stimulating or recording from a small population of axons within a nerve [8], [9]. In addition, electroceuticals, and therapeutic neuromodulation, benefiting from selective recording can allow for temporally accurate closed-loop control of stimulation [8], [10], [11].

Neural interface design is a trade-off between surgical invasiveness and selectivity [12]. Epineural designs and cuff electrodes minimize damage to the nerve trunk, but record signals from the entire nerve or a large volume within the nerve [5], [9], [13], [14]. Intrafascicular interfaces, shanks or wires inserted into the nerve, risk damaging fibers, but allow increased selectivity [15]. Stiff intrafascicular electrode arrays originally designed for cortical implantation have been investigated in peripheral nerves [15], [16]. Over weeks to months of implantation nerve fibre damage and regeneration occurs, and fibrotic scarring occurs potentially making electrode-axon distances too large for effective recording, or ejecting the array from the nerve [17]. Flexible intrafascicular arrays exhibit very promising biological performance and selectivity [18], [19], however interference from adjacent muscles limits the recording signal-to-noise ratio.

Microchannel neural interfaces (MNIs, Fig. 1) are designed to provide a high selectivity interface to the nervous system [20]. MNIs achieve this with microchannels (small diameter tubes) through which axons are placed [21] or regenerate [22]. Microchannels, hundreds of μm diameter and mm in length, insulate a "mini-nerve" with a subset of axons from the surrounding nerve. Minimum "mini-nerve" diameter is limited to approximately 100 μm because smaller diameter microchannels become occluded with fibrotic tissue [23]. This design increases signal amplitude by restricting space for extracellular current flow [24]. It allows recording or stimulating from subsets of axons, increasing selectivity, makes recordings independent of node of Ranvier position, and reduces currents required for neural stimulation. High selectivity MNIs typically require nerves to be separated into a large number of closely packed microchannels.

The MNI imposes considerations for recording and stimulation which differ from standard neural interfaces. Recorded single fiber action potentials in MNIs range from 30 μV to 200 μV peak-to-peak [20], [25], [26]. Furthermore, the tripolar electrode arrangement in MNIs acts to reject interference from surrounding EMG, improving signal-to-noise ratio [27]. High extracellular resistance within microchannels means that action potentials can be achieved with low injected currents (5 μA to 25 μA mean reported [20]). However, the high impedance within

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H. T. Lancashire and N. Donaldson are with the Department of Medical Physics and Biomedical Engineering, University College London, London WC1E 6BT, U.K. (e-mail: h.lancashire@ucl.ac.uk; n.donaldson@ucl.ac.uk).

D. Jiang and A. Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, U.K. (e-mail: d.jiang@ucl.ac.uk; a.demosthenous@ucl.ac.uk).

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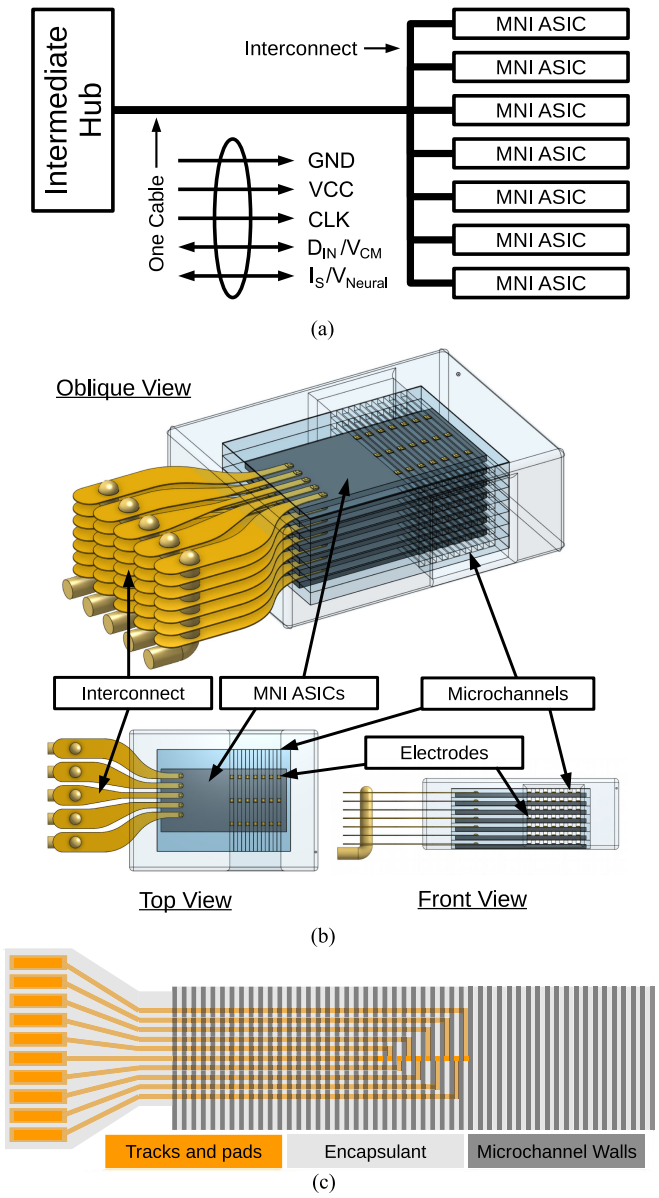

Fig. 1. Microchannel Neural Interface (MNI) designs. (a) The distributed system concept. (b) A 3D view of the microchannel neural interface, showing a stack of 7 MNI ASICs and microchannels (right), and the 5-line bus interconnect (left). (c) The spiral peripheral nerve interface design, rolled to form 50 microchannels as described in [30]. Part (b) modified from [35].

the channel (100 kΩ to 1.2 MΩ for similar devices [20], [21], [28]) necessitates a voltage compliance for stimulation greater than 10 V.

MNIs have been manufactured with a range of techniques: silicone casting [23], photopatterning polyimides [20], [29], [30], silicones [28], SU-8 photoresist [25], [31], and laser micromachining [32]. Existing MNI designs use passive conductors (metal thin-films, wires, or foils) to form electrodes and interconnects. Passive conductors limit the density and number of channels because each electrode requires one connecting wire. Fig. 1(c) shows the interconnect size requirements for a spiral peripheral nerve interface with 10 channels containing electrodes (devices with up to 20 electrode channels have been reported [30]). Tripole end electrodes add further connections, one for common end electrodes, and up to two additional connections per channel. To allow an increased number or density of electrodes the number of interconnect lines must be reduced. A single system-on-chip could be used to multiplex all MNI connection lines; however this would require one miniaturized connection per electrode, increasing the risk of failure. For example, CMOS neural probes intended for cortical applications with hundreds of electrodes have been presented [33], [34]. To achieve a 3-dimensional MNI structure separate electrodes would be required, each with its own connection to the single inflexible system-on-chip. Instead, using distributed application specific integrated circuits (ASICs) with electrodes at the ASIC surface, connections can be minimized and the 3-dimensional microchannel array achieved.

This paper presents the design and test of an ASIC for use in place of passive conductors in a MNI to solve problems with interconnect size in a 3-dimensional structure. The MNI ASIC multiplexes electrodes formed at the standard bonding pads on the ASIC surface reducing the number of connections required in the proposed interface design. Each ASIC comprises seven tripoles arranged to interface with seven microchannels and bidirectional multiplexing circuits for neural stimulation and recording. A single proposed MNI device contains 49 microchannels, from seven stacked ASICs, which allows selection from one of 49 "mini-nerves". This paper is an expansion of [35]. It provides a comprehensive description of the ASIC architecture including the biasing unit and the role of switch unit pairs in each mode, micrographs of manufacturing steps, ASIC ID setting for multi-ASIC multiplexing by laser ablation, measurements of biphasic current controlled stimulation, measurements of stimulation switching between ASICs, measurements of stimulation switching between channels on single ASICs, measurements of high frequency stimulation, results of biasing and recording across signal amplitudes and biasing setups, and tests using an in vitro microchannel demonstrating interference attenuation and tripolar recording.

The rest of the paper is organized as follows. Section II presents the system and ASIC architecture and details of the fabrication methods. Measurements are presented in Section III. Discussion and concluding remarks are provided in Section IV.

II. System and ASIC Architecture

A. Overall System

The system concept is shown in Fig. 1(a): MNI ASICs, stacked to form a single MNI as shown in Fig. 1(b), or distributed in different peripheral nerve locations, share a single communication link with a hub. A 3-dimensional view of the MNI device is shown in Fig. 1(b), where seven MNI ASICs are stacked with silicone layers in between. The system architecture is shown in Fig. 2. Each ASIC consists of seven tripoles, upon which seven microchannels are formed. The ASICs provide bidirectional multiplexing to each microchannel, and are powered and controlled by an intermediate hub via a 5-line parallel bus (GND, VCC, CLK, D_{IN}/V_{CM}, I_S/V_{Neural}).

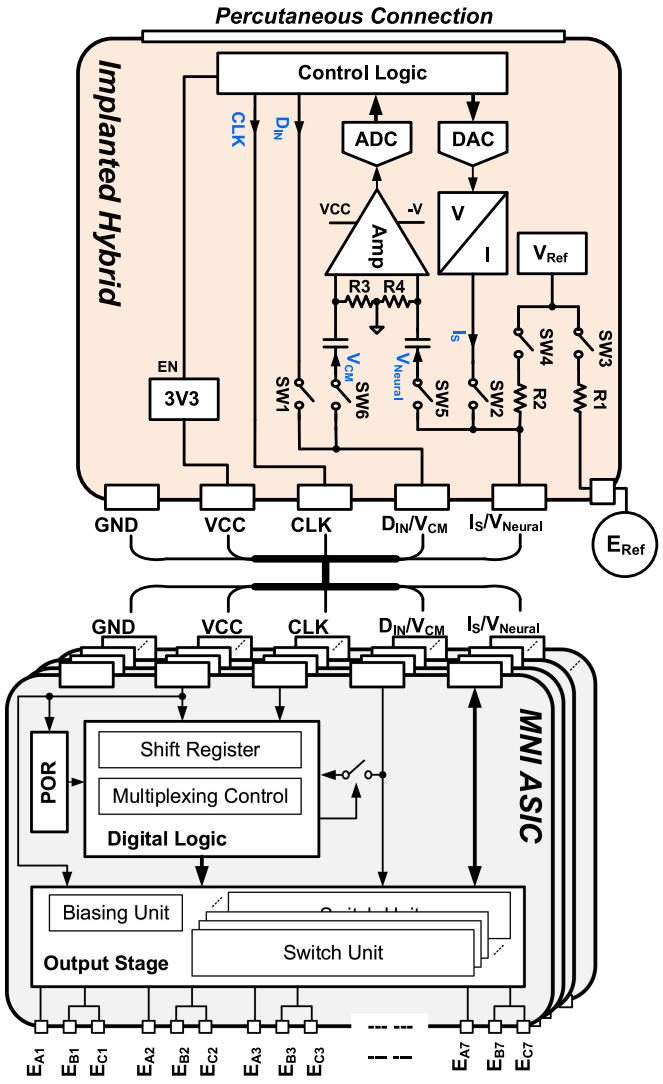

Fig. 2. Illustration of the system architecture of the intermediate hub and up to seven MNI ASICs. Modified from [35].

The separate intermediate hub consists of control logic, switching circuitry for stimulation and recording modes, reference voltage (V_{Ref}) generation, and a first stage differential amplifier. The differential amplifier is powered by dual supply (VCC, GND, and –V), while the MNI ASIC is powered by a single supply (VCC and GND). During stimulation, a unidirectional current (I_S) is supplied to the hub on line I_S/V_{Neural}, and is switched through to the MNI (SW2 is closed). By switching the MNI outputs a biphasic pulse is generated, as described in detail below.

During recording, lines I_S/V_{Neural} and D_{IN}/V_{CM} are rerouted to the inputs of a differential amplifier in the hub. Switching takes place after a command is sent to the MNI on D_{IN}/V_{CM}. I_S/V_{Neural}, and a remote reference electrode (E_{Ref}), are biased to the reference voltage, V_{Ref} (VCC/2), with R2 and R1 respectively (Fig. 2). In recording mode SW3, SW4, SW5, SW6, and SW7 are closed, while SW1 and SW2 are open. The reference electrode acts to bias D_{IN}/V_{CM} through the outer electrodes on the MNI.

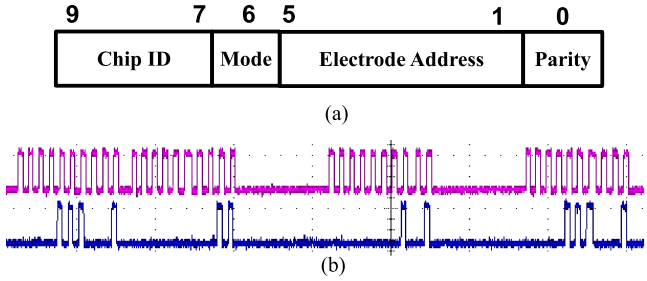

Fig. 3. Illustration of: (a) the command frame; (b) CLK (above) and D_{IN}/V_{CM} (below) lines, showing 4 command frames.

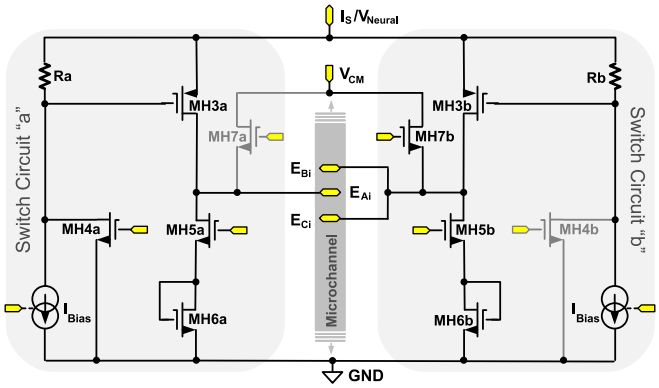

Fig. 4. Electrode multiplexing, from GND, I_S/V_{Neural}, or D_{IN}/V_{CM} to electrodes E_i showing: two MNI ASIC switch circuits, a and b, connected to E_{Ai} and E_{Bi}/E_{Ci} respectively in a single microchannel tripole. Each switching unit has an associated current sink I_{Bias}.

A remote controller instructs the hub to switch between stimulation and recording modes.

B. ASIC Design

Each MNI ASIC provides 21 bonding pads arranged in tripoles for forming electrodes for seven microchannels. In addition, there are five pads on each ASIC as the contact points to a 5-line parallel bus. The circuitry on the ASIC implements electrode multiplexing among the seven microchannels for stimulation or recording. Fig. 2 illustrates the overall architecture of the MNI ASIC. An output stage selectively connects the 21 electrode pads, E_{Ai}, E_{Bi} and E_{Ci}, for the desired stimulation and recording operation, where i = 1,2,3,...,7, indicating the seven microchannels. The electrode multiplexing is controlled by a logic unit according to the commands received from the hub via CLK and D_{IN}/V_{CM} on the parallel bus. A built-in power-on reset (POR) resets the logic each time the hub turns on the power supply to the MNI ASIC via VCC. After the reset, the hub sends 10-bit commands via the parallel bus to all the seven stacked MNI ASICs. The structure of the command frame is shown in Fig. 3(a). Bit 9 to Bit 7 in each command select one of the seven stacked ASICs, Bit 6 sets the mode of the desired operation, stimulation or recording, from this ASIC. Bit 5 to Bit 1 address a look-up table (LUT) in the logic containing pre-stored electrode combination for both the stimulation and recording modes. Bit 0 is an even parity bit for error detection. Fig. 3(b) is

TABLE I
OUTPUT STAGE TRANSISTORS CONDUCTING IN EACH SWITCHING MODE

Electrode(s)	Mode						
	Recording	Stimulating (Cathodic) [a]	Stimulating (Anodic) [a]	All STIM	All GND	Channel Leak Test [b]	
						Channel i	Channel i + 1
E_{Ai}	MH3a (MH4a on)	MH5a on	MH3a (HV mode with I_{Bias})	MH3a (HV mode with I_{Bias})	MH5a on	MH3a (HV mode with I_{Bias})	MH5a on
E_{Bi} / E_{Ci} [c]	MH7b on	MH3b (HV mode with I_{Bias})	MH5b on	MH3b (HV mode with I_{Bias})	MH5b on	MH3b (HV mode with I_{Bias})	MH5b on

Refer to Fig. 4 for transistor naming convention.
[a] Cathodic and Anodic are defined with respect to E_{Ai}.
[b] Two adjacent channels: E_{Ai}, E_{Bi}, E_{Ci}; and E_{Ai+1}, E_{Bi+1}, E_{Ci+1}.
[c] E_{Bi} and E_{Ci} are permanently connected.

an oscilloscope screenshot of the captured waveforms on CLK and D_{IN}/V_{CM}, showing four command frames on the D_{IN} line clocked by *CLK*.

1) Stimulation Mode: If a MNI ASIC is addressed by a command frame and the Mode bit is "0", this ASIC is set for stimulation. During stimulation, each command activates one microchannel to generate one current pulse. Each microchannel consists of three electrode pads, E_{Ai}, E_{Bi} and E_{Ci}, where E_{Ai} is located at the center of the channel, and E_{Bi} and E_{Ci} are on either side at an equal pitch. E_{Bi} and E_{Ci} are connected together to reduce inter-channel interference. Fig. 4 shows the switch circuits in the output stage unit for one microchannel. After power-on reset, all the high-voltage transistor switches, MH3, MH4, MH5 and MH7 associated with both E_{Ai} and E_{Bi}/E_{Ci} shown in Fig. 4 are off. Table I shows the sequence of conducting transistors in each switching mode. Once stimulation starts, each biphasic pulse is generated by two consecutive commands. Stimulation can either be cathodic first, or anodic first, defined with respect to E_{Ai}, the sequence for a cathodic first pulse is as follows. The first command turns on the high voltage transistor MH3b to connect electrode pads E_{Bi} and E_{Ci} to the line I_S/V_{Neural} where a direct stimulation current I_S is supplied, while MH5a, that connects to E_{Ai}, is also turned on to connect this electrode pad to GND via the diode-connected MH6a. This configuration allows the stimulation current to flow through the microchannel from E_{Bi} and E_{Ci} to E_{Ai}. The second command reverses the electrode configuration so that the current flows in the opposite direction from E_{Ai} to E_{Bi} and E_{Ci}. The interval between the two command frames decides the width of either phase in the biphasic pulse, and a power-on reset after the second phase completes the pulse.

The switches are implemented with high voltage MOSFETs in the ams (austriamicrosystems) H35B4D3 0.35-μm CMOS technology. In stimulation mode, high compliance voltage ($\leq$ 40 V) at I_S/V_{Neural} may be required due to the high impedance of a microchannel. Conventional complementary CMOS switches are not suitable because the maximum allowed gate-source voltage is only 18 V for these HV MOSFETs. To ensure the safety of the transistors, a current-biased level shifter is implemented [36]. As shown in Fig. 4, instead of grounding the gate of MH3 to turn this switch on, which is dangerous when the voltage at I_S/V_{Neural} is above 18 V, MH3 is turned on by enabling a current sink I_{Bias} to generate a 2 μA biasing current flowing through a 1 MΩ resistor between the gate and source of MH3, hence

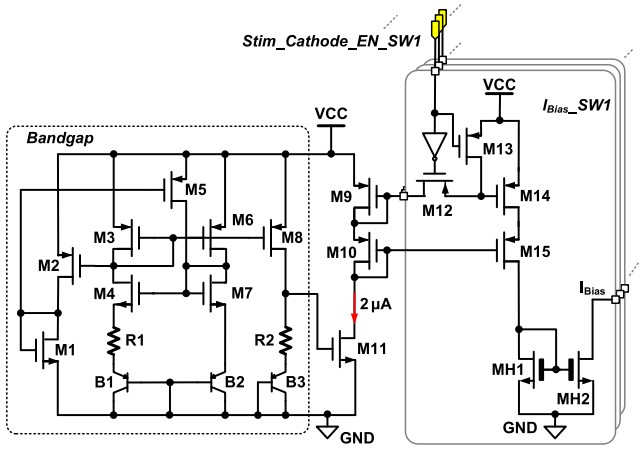

Fig. 5. Schematic of the biasing unit. Modified from [35].

generating a 2 V gate-source voltage for the p-MOS transistor MH3 (Ra and Rb in Fig. 4). Fig. 5 shows the circuit details of the biasing unit that generates I_{Bias}. A bandgap voltage reference biases the gate of an n-type MOSFET M11 sized for generating a stable 2 μA drain current. This current is copied into 14 parallel I_{Bias}_SWi units, providing two I_{Bias} current sinks for each microchannel, as shown in Fig. 4. Each I_{Bias} is switched by a control signal *Stim_Cathode_EN_SWi* from the logic to control the status of MH3 to which this I_{Bias}_SWi unit connects. In order to ensure MH3 is fully turned on the voltage at I_S/V_{Neural} must be higher than the 2 V plus the drain-source voltage of MH2 (refer to Fig. 5) when *Stim_Cathode_EN_SWi* is at "1", the drain-source voltage of MH2 is 0.4 V. The voltage at I_S/V_{Neural} depends on the voltage drop across the electrode. According to previous studies, the mean stimulus current in a similar microchannel is 26.2 μA [20] and the smallest expected impedance is around 50 kΩ [20], [28], [31], [32]. Therefore, the expected electrode voltage in this design 1.31 V. To ensure MH3 is fully turned on, a diode-connected transistor MH6 is added to the current path as a level shifter. MH6 shifts the electrode voltage by 1.2 V, so that the voltage at I_S/V_{Neural} is higher than 2.4 V. For example, as shown in Fig. 4, when the MH3a and MH5b are on, the current flows from E_{Ai} to E_{Bi} and E_{Ci} then to MH5b and MH6b to GND.

2) Recording Mode: When the logic receives a command setting the MNI ASIC to the recording mode after power-on

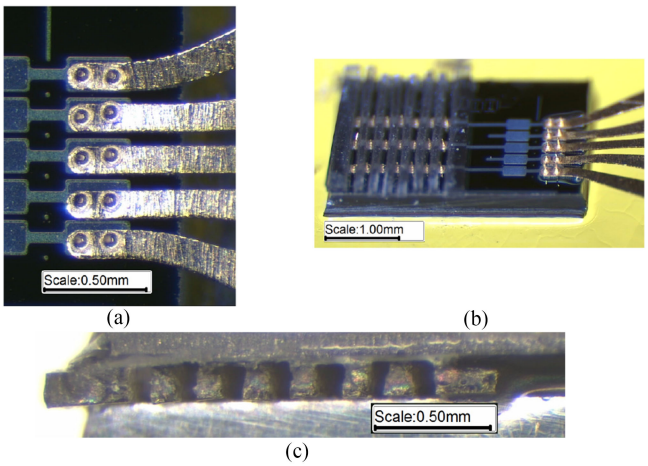

Fig. 6. Microphotographs of stacked MNI ASIC assembly: (a) micro-rivet bonding of gold ribbon interconnects to ASIC surfaces; (b) oblique view of ASIC-microchannel pair; (c) 7 microchannels stacked between two ASICs. The ASICs used here are passive dummy samples with the same pad layout as the active MNI ASICs. Fig. 6(a) and (b) modified from [41].

reset, it disconnects its data input from the D_{IN}/V_{CM} pad, as this pad now connects to the indifferent input of the recording amplifier in the hub. The logic also turns on MH4a in Fig. 4 to connect the gate of MH3a to GND in order to turn on MH3a, while the current source I_S remains off, so that E_{Ai} connects to the pad I_S/V_{Neural}, which now connects to the recording input of the recording amplifier. MH7b is also turned on to connect the outer electrodes E_{Bi} and E_{Ci} to D_{IN}/V_{CM} (Table I). At the end of a recording window, a power-on reset turns off all the switches and reconnects D_{IN}/V_{CM} to the data input of the logic.

3) Leak Test Mode: The electrode configurations for the channel leak test mode are included as a subgroup of the stimulation mode in the LUT. In this mode, two adjacent channels are activated at a time, with (E_{Ai}, E_{Bi}, E_{Ci}) connected to I_S and (E_{Ai+1}, E_{Bi+1}, E_{Ci+1}) to GND, see Table I.

C. Stacked ASIC Microchannel Neural Interface Assembly

The complete active MNI is assembled by alternately stacking thinned ASICs [37] and laser cut silicone microchannels [32]. Fig. 6 shows selected manufacturing stages. Fig. 1(b) shows the stacked MNI ASIC structure.

First, 25 μm gold foil is laser patterned to form ribbon interconnects. The gold interconnects are micro-rivet bonded to the thinned ASIC 5-line bus [Fig. 6(a) and 6(b)] [38], [39]. MNI ASIC electrodes (E_i) can then be electroless nickel - immersion gold plated [40], or electro-gold plated using stimulation mode for plating current supply, forming electrode sites at the MNI ASIC surface. ASICs are cleaned thoroughly in an ultrasound bath using organic solvents (acetone, isopropyl alcohol) followed by deionised water. ASIC surfaces are activated for bonding using low pressure oxygen plasma from dry air (0.6 mbar, Zepto B plasma system, Diener Electronic). ASICs are coated with a thin (<20 μm) layer of low-viscosity, two part, silicone (MED-6015, NuSil) at 4000 rpm for 1 minute using a WS-400E-NPP-Lite spin coater (Laurell Technologies).

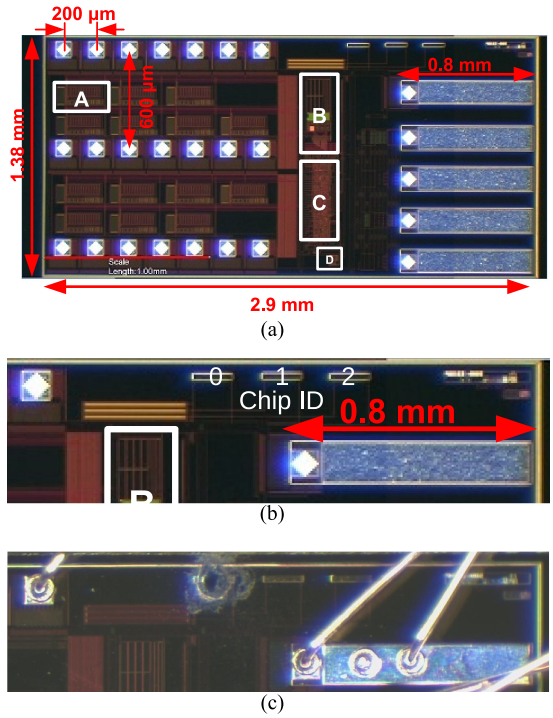

Fig. 7. Die microphotographs of the MNI ASIC: (a) including 14 identical switch units two for each pseudotripole (A), the biasing unit (B), the logic (C), the power-on-reset (D), five connecting pads and 21 electrode pads for seven microchannels. (b) "Chip ID" setting pull-down wires. (c) Laser ablation of "Chip ID" on a packaged MNI ASIC to specify ASIC as b001. Fig. 7(a) from [35].

TABLE II
SUMMARY OF THE MNI ASIC SYSTEM PERFORMANCE

Recording	
CMRR	40 dB
Bandwidth	300 Hz to 5 kHz
Input-referred noise	$2.48 \pm 0.54\ \mu V_{rms}$
Total harmonic distortion	–36.9 dB
Electrode offset voltage	0.29 ± 0.04 mV
Stimulation	
Stimulation frequency	≤ 40 kHz
Charge imbalance	$1.86 \pm 0.73\%$ at 40 kHz
Crosstalk	$0.56 \pm 0.15\%$

Laser cut silicone microchannels are formed using a previously described technique. Briefly, silicone with 2.5 wt% black pigment (Med-4800-2, Polymer Systems Technology) is spin coated onto polystyrene sulfonic acid (PSS, Sigma Aldrich) coated slides at 500 rpm to form a 100 μm layer. The silicone layer is cured at $\geq$100 °C for 1 hour and patterned to form 100 μm $\times$ 100 μm microchannels using an Nd:YAG laser (Laserval Violino-2, laser system by Laser Lines Ltd, UK).

Microchannels are oxygen plasma activated and placed on the silicone coated ASICs. The ASIC-microchannel pair is cured at $\geq$100 °C for 1 hour. Up to seven ASIC-microchannel pairs are stacked by spin coating a thin layer of silicone onto the underside of an ASIC (as detailed above), aligning the microchannel layer of another pair on top, and curing the stack [Fig. 6(b) and 6(c)].

ASICs are connected in parallel using a vertical 5-wire interconnect formed from gold foil [41]. To date the gold

TABLE III
COMPARISON WITH OTHER ACTIVE NEURAL INTERFACE DESIGNS

Reference	Nervous System Target	Technology (μm)	No. of Electrodes	Die area (mm^2)	Channel Density (mm^{-2})	Compliance Voltage (V)	Functionality	Power Consumption
[36]	Spinal cord	0.18	5	1.753	3.42	up to 25	Stimulation	144 μW
[61]	Retina	1.5	8	4.84	1.65	13	Stimulation	500 μW
[54]	Cerebral cortex	1.5	64	21.16	3.02	5	Stimulation	8.25 mW
[62]	Spinal nerve	0.6	12	27.3	0.15	18	Stimulation	30.11 mW
[63]	Retina	0.35	1	0.16	6.25	N/A	Stimulation	N/A
[33]	Brain	0.13	966	45.7	8	1.8	Recording	13.54 mW
[34]	Brain	0.18	455	10.57	5.26	1.8	Recording	1.45 mW
[64]	Brain	0.35	4 (+ 6 LEDs)	4.21	2.38	5	Stimulation and recording	13.4 mW
This work	Peripheral nerve	0.35	21 [a,b]	4	1.75	up to 40	Stimulation and recording	149 μW [a]

This table is modified from [35].
[a] Values for a single MNI ASIC.
[b] Electrodes are arranged in seven tripoles.

interconnects in multiple layers have been bonded using conductive epoxy resin (EpoTek H20E); however robust, biocompatible alternatives are being investigated, including gold-platinum microbrazing [42]. The ASIC sides and interconnects are encapsulated with a conformal silicone coating to prevent liquid water forming on device surfaces [43].

D. Intermediate Hub

A prototype intermediate hub was implemented as a non-implantable platform following the architecture shown in Fig. 2(b). An ATmega328P microcontroller (on Arduino Uno) generates the appropriate command frame, controls the current source, and controls discrete CMOS switches on the hub (SW1 to SW6). Commands to the MNI ASICs on lines CLK and D_{IN}/V_{CM} are sent at a rate between 35 kbit/s and 1.1 Mbit/s. A level-shifter is implemented to bridge between the 5 V control logic and 3V3 MNI ASIC.

The current source is implemented as an operational amplifier source (OPA2140, Texas Instruments) and an n-channel MOSFET defining the current for a cascode current mirror; this limits the voltage compliance to 36 V, however the MNI ASIC has been tested to +40 V compliance. The current source is only switched on in stimulation mode. To avoid saturation and achieve fast recovery of the current source an alternative load, with impedance matched or lower than the expected electrode impedances, is built into the current source and connected to the source output except when the MNI ASIC is stimulating [44].

A high accuracy instrumentation amplifier (AD620, Analog Devices) is used for neural signal amplification. Each input of the first stage amplifier on the hub is capacitively coupled to the recording lines and biased to GND through R3 and R4 to remove the dc bias due to V_{Ref}, and forming a 300 Hz first order high-pass filter. The amplifier output stage is low-pass filtered with a first order 5.9 kHz cut-off. This stage amplifies the received action potentials from the MNI before forwarding the signals to the controller ADC on I_S/V_{Neural}. V_{Ref} is supplied from a regulated voltage source.

III. MEASUREMENTS

The prototype ASIC is implemented in the ams 0.35-μm high-voltage CMOS technology (ams H35B4D3, via Circuits Multi-Projets, France). Fig. 7(a) shows the microphotograph of the ASIC. The total size of the die is 2.9 mm × 1.38 mm, including a length of 0.8 mm for the extended connection pads. Seven microchannels are fabricated on the ASIC with three electrode pads per channel in a pitch of 600 μm. The size of each electrode pad is 94 μm × 94 μm. The pitch between adjacent microchannels is 200 μm to allow for a 100 μm diameter microchannel with 100 μm wall thickness between microchannels. The "Chip ID" setting pull-down wires are designed to be readily visible under low magnification [Fig. 7(b)] and can be laser ablated without damaging other ASIC units [Fig. 7(c)]. A summary of the system performance is shown in Table II. A comparison with other chip designs for active electrodes is shown in Table III.

A. Power Consumption

The power consumption of a single MNI ASIC after power-on reset is 143 μW (43.3 μA with a 3.3 V supply), when all electrodes are connected to GND. When switched to stimulate on one channel (cathodically or anodically), power consumption is 149 μW. When all channels are connected for stimulation power consumption is 237 μW, however this mode is reserved for test and electroplating and is not intended for use in vivo. Following Chip ID setting, power consumption in all modes reduces by 15 μW per ablated resistor. Power consumption for seven stacked ASICs in a 49 channel MNI will be between 1 mW and 1.1 mW, dependent upon the mode.

B. Stimulation

The setup for nerve stimulation was tested. Current response under direct currents is shown in Fig. 8 and [35]. 1.44 ± 0.55 μA of the current supplied at I_S/V_{Neural} is used to switch on the stimulating circuit and is lost to the electrodes; therefore, to stimulate with a 10 μA current pulse, ~11.5 μA current must be supplied at I_S/V_{Neural}.

Response with biphasic pulses was also tested as shown in Fig. 9. A constant current is supplied to I_S/V_{Neural}. A 1 kHz, cathodic-first, biphasic pulse is generated at the electrodes by switching the electrodes between phases. Varying the control word timing varies pulse length and frequency; interphase delays are achieved by switching off the current source, I_S. For

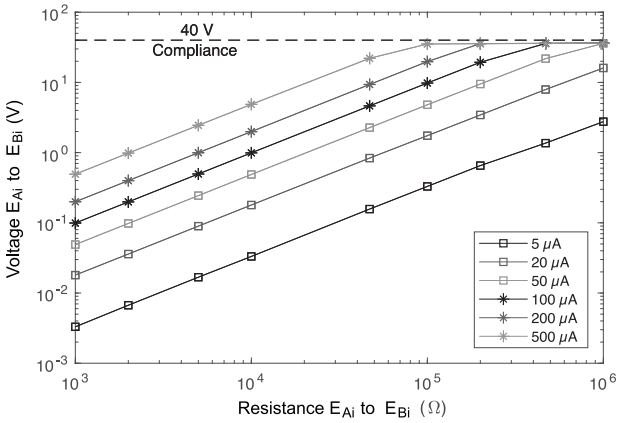

Fig. 8. Constant current stimulation on one MNI ASIC demonstrating 40 V compliance. Current applied to I_S/V_{Neural} is varied and resistance is varied between E_{Ai} and E_{Bi}/E_{Ci}. Current is lost to the electrodes due to switching on the stimulating circuit and due to the 40 V limit. Log-log plot.

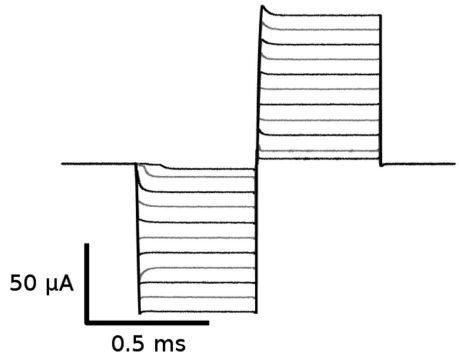

Fig. 9. Current controlled, cathodic first, biphasic 1 kHz stimulation. Applied currents of 5 μA and 10 μA to 100 μA in 10 μA steps. Cathode and anode are switched between phases by sending the appropriate command bitword to reverse the direction of current flow. 50 kΩ impedance between E_{Ai} and E_{Bi}/E_{Ci}.

currents < 20 μA it was observed that the first phase was delayed by a time that varies linearly from 3.5 μs at 20 μA to 40 μs at 5 μA. Delays were found to be due to the chosen current source and were corrected by introducing appropriate delays between switching commands. Delays are also avoided by using continuous stimulation pulse trains without interphase delays. For larger currents, and for voltage-controlled pulses, the setup delay totals about < 3.5 μs from the falling edge of the final clock pulse, which triggers switch setup. Chip ID setting allows stimulation on multiple ASICs in sequence, this is shown in Fig. 10(b). Crosstalk between ASICs is observed as capacitive spikes which are minimal with respect to the charge injection at the intended channel ($0.56 \pm 0.15\%$). Crosstalk is also small between stimulation channels of a single ASIC when each of the seven microchannels (E_{Ai}, E_{Bi}, E_{Ci}) is selected in sequence [see Fig. 10(a)]. When equal amplitude current pulses are applied to adjacent microchannels capacitive crosstalk between channels is $1.06 \pm 0.68\%$ of the charge injection at the intended channel.

Continuous pulses are shown in Fig. 11. Switching between phases requires a new command, therefore with a data rate of 1.1 Mbit/s, and a 10-bit command frame [Fig. 3(a)], 55 kHz

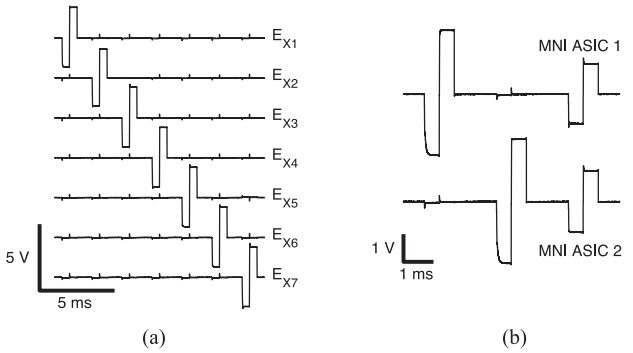

Fig. 10. Current controlled biphasic, 500 Hz stimulation with MNI ASICs. a) stimulation on one MNI ASIC demonstrating crosstalk between channels. i = 1 to i = 7 is selected in sequence while no other channels are selected. b) Stimulation on two ASICs connected in parallel. In the first stimulus pulse MNI ASIC 1 is specified by Chip ID, in the second stimulus pulse MNI ASIC 2 is specified, and in the final pulse both ASICs are addressed at the same time using Chip ID b000 the current therefore flows through two parallel loads and the stimulus amplitude is halved. 50 μA stimulation with 50 kΩ impedance between E_{Ai} and E_{Bi}/E_{Ci}.

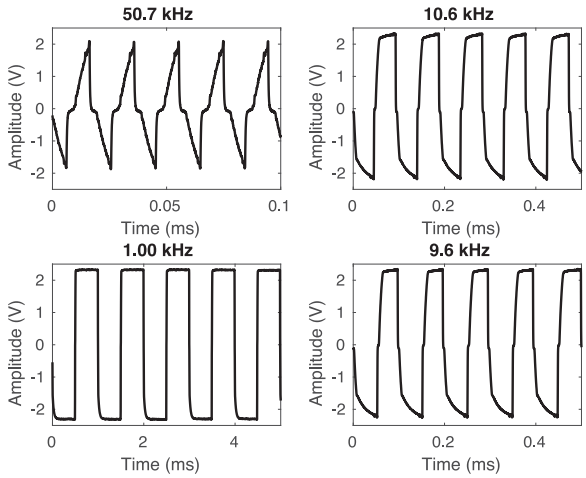

Fig. 11. Current controlled biphasic stimulation at a range of frequencies determined by switching command rate, a 1.00 kHz pulse train requires a 495 μs delay between bitwords. The 9.6 kHz biphasic stimulation is charge balanced to $0.48 \pm 0.27\%$ by adjusting the phase timing. 50 μA stimulation with 50 kΩ impedance between E_{Ai} and E_{Bi}/E_{Ci}. Voltage measured between E_{Ai} and E_{Bi}/E_{Ci}.

is the fastest predicted frequency. In practice the fastest rate achieved is circa 50 kHz. Lower frequencies are achieved by increasing the delay between bitwords (Fig. 11). Charge imbalance between phases is large for high frequencies: $16.9 \pm 6.4\%$ at 50 kHz stimulation. The slew rate of the current source, and mismatch between HV transistors MH3, are key factors in this mismatch. By adjusting command timing to account for mismatch this charge imbalance for each channel can be reduced to: $1.86 \pm 0.73\%$ at circa 40 kHz, $0.48 \pm 0.27\%$ at circa 10 kHz, and $1.20 \pm 0.92\%$ at 1 kHz stimulation frequency (Fig. 11) [45]. 50 kHz stimulation cannot be achieved with balanced pulses as suitable delays cannot be introduced between switching commands.

The averaged dc current error was measured with a method similar to [46], where a 2 kΩ sensing resistor was connected

in series to the electrodes and a dummy 50 kΩ load. The voltage across the sensing resistor was measured after being filtered with a second-order 0.3 Hz RC low-pass filter, where the dc current through the electrodes can then be calculated. In the experiments, the MNI ASIC generates through 50 μA biphasic current pulses at 1 kHz and 50% duty cycle, i.e., no interval between two biphasic pulses. Over a period of 5 minutes, dc voltage was measured across the sensing resistor using a Keithley 195A digital multimeter. Measured dc voltage was stable at 690 μV, suggesting a dc current error of 345 nA through the electrodes, with adjusted phase timing dc current error was stable at 45 nA. The test achieved the following dc current errors at the following adjusted pulse rates, also with 50% duty cycle: 5 kHz, 25 nA; 10 kHz, 35 nA; 20 kHz, 22 nA.

At the onset of a stimulation pulse train a voltage transient is observed (Fig. 9, Fig. 10). This is due to the response of the controlled current source to load changes, and mismatch between the switching times Switching to the alternative load equal to the impedance between electrodes considerably reduced this transient, in addition a faster settling current source should be used, in particular where electrode impedance is unknown.

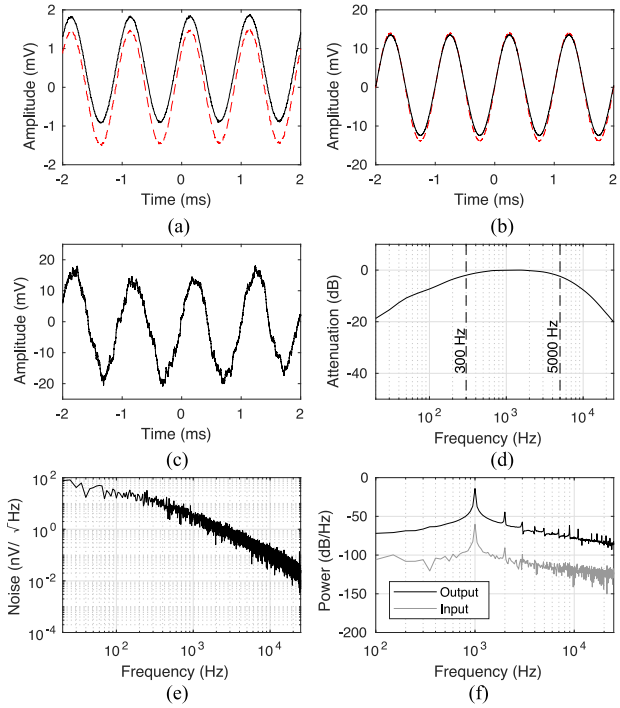

Fig. 12. Signal recording through an MNI ASIC. (a), (b): 1 mV rms and 10 mV rms 1 kHz sine wave signals applied at E_{Ai} (red dashed line) and recorded at I_S/V_{Neural} (black line). (c) 1000× amplified 30 μV_{p-p} 1 kHz sine wave signal applied at E_{Ai} and recorded using the intermediate hub. (d) Frequency response curve of the MNI ASIC and hub recording system. (e) Noise spectrum. (f) Frequency spectra of a 1 kHz signal recorded input E_{Ai} (grey) and amplified output (black) showing harmonic distortion. Parts (a) and (b) modified from [35].

C. Recording

In recording mode electrodes are biased to V_{Ref} (VCC/2) with an external bias source (Fig. 2). To bias the outer electrodes (E_{Bi}/E_{Ci}). V_{Ref} is applied to a remote reference electrode with resistor R1 in series; the inner electrode (E_{Ai}) is biased through I_S/V_{Neural} via a biasing resistor R2 to V_{Ref}. This arrangement ensures MH3 is directly turned on by V_{Ref}. The acceptable input voltage range for the MNI ASIC is therefore ±VCC/2 (±1.65 V). The expected maximum neural signal amplitude is ±100 μV, and expected maximum interference from muscles is ±10 mV. Electrode offset voltages (E_{Ai} and E_{Bi}/E_{Ci}) are dependent upon the relative electrode and tissue impedances and under normal conditions vary from 0.7 mV to 6.8 mV. Under normal conditions in recording mode an offset voltage is also present at the output lines (I_S/V_{Neural} and D_{IN}/V_{CM}) of 0.29 ± 0.04 mV. Recording mode was tested using signals applied differentially with a transformer and a 50 kΩ series resistor between E_{Ai} and E_{Bi}/E_{Ci}. Impedance from the reference electrode to E_{Bi}/E_{Ci} was set to 10 kΩ by a resistor. Outputs at I_S/V_{Neural} are shown in Fig. 12(a)-(b). Amplified output of a neural signal relevant amplitude is shown in Fig. 12(c).

The differential input impedance of the recording system including the MNI ASIC is 2 MΩ at 1 kHz. Excluding the MNI ASIC the input impedance of the recording system is 2.2 MΩ at 1 kHz. Noise in recording mode is 2.48 ± 0.54 μV rms referred to input with the MNI ASIC electrodes (E_{Bi}/E_{Ci}) shorted and 2.47 ± 0.61 μV rms referred to input with the MNI ASIC outputs (I_S/V_{Neural} and D_{IN}/V_{CM}) shorted, and noise density is 21.9 nV/$\sqrt{\text{Hz}}$ referred to input with the MNI ASIC electrodes (E_{Bi}/E_{Ci}) shorted. The frequency response of the MNI ASIC and recording system is shown in Fig. 12(d). The noise spectrum of the MNI ASIC and recording system is shown in Fig. 12(e).

Signal distortion is present at output lines, I_S/V_{Neural} and D_{IN}/V_{CM}, relative to the electrode inputs E_{Ai} and E_{Bi}/E_{Ci} (Fig. 2). To minimize common mode output from the first-stage differential amplifier, relative signal distortion must be minimized. A common-mode signal was applied by a second transformer. Minimum common mode output amplitude was achieved by adjusting the biasing resistors (R1 and R2 in Fig. 2). A minimum was with biasing resistors in the following ranges: remote reference electrode + R1 = 138 kΩ to 145 kΩ; R2 = 31.6 kΩ to 34.2 kΩ. The common mode rejection ratio (CMRR), 40 dB, compares poorly with the reported CMRR of a typical instrumentation amplifier for biomedical applications (e.g., >90 dB for AD620, Analog Devices).

Generally, distortion and electrode offset vary with signal magnitude and with bias resistance. In summary: large signal amplitudes (hundreds of mV) are clipped, with negative clipping of the signal from E_{Ai} to I_S/V_{Neural}, and positive clipping of the signal from E_{Bi}/E_{Ci} to D_{IN}/V_{CM}. It is not expected to observe these amplitudes in vivo at E_{Ai} and E_{Bi}/E_{Ci} as the largest expected signals are < ∼10 mV, interference from adjacent muscles. For 10 mV rms, 1 kHz signal, the total harmonic distortion (THD) due to the MNI ASIC and recording system is −36.9 dBc (1.43%). Harmonic distortion of the MNI ASIC and recording system is shown in Fig. 12(f).

For R2 ≤ 1 kΩ, signals from E_{Ai} to I_S/V_{Neural} are attenuated. For R2 ≥ 1 MΩ, signals from E_{Ai} to I_S/V_{Neural} are distorted

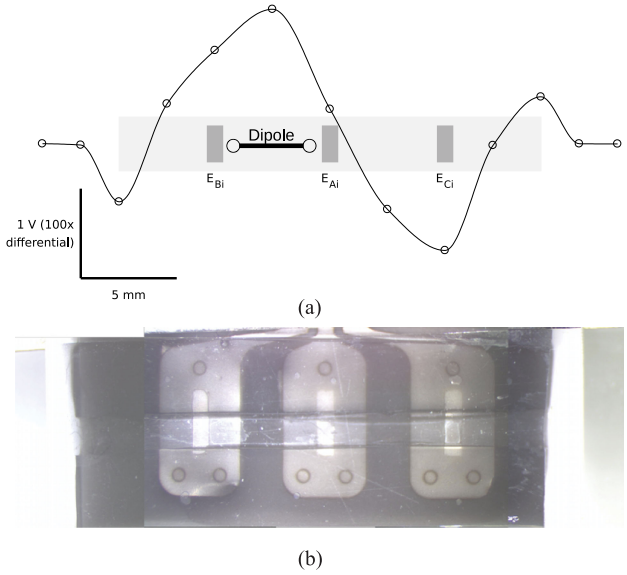

Fig. 13. The in vitro microchannel experiment. (a) Differential amplified signal amplitude recorded with the centre of the dipole at the given distances along the microchannel length. Electrodes are connected to MNI ASIC pads E_{Ai}, E_{Bi} and E_{Ci}, as shown. The dipole with 4 mm interelectrode distance is shown within the microchannel. Signal injected: 1 kHz sine wave, 10 mV amplitude. Three differential signal inversions are present: when the dipole passes the mid-point of the microchannel; and when the dipole passes the points ½ dipole interelectrode distance from the microchannel ends. Piecewise cubic interpolation. (b) Micrograph of the oversize microchannel to the same scale. The microchannel is 2 mm width, 22 mm length, and 1 mm height. The microchannel electrodes have 6 mm interelectrode distance, and are spaced at 5 mm, 11 mm, and 17 mm along the microchannel.

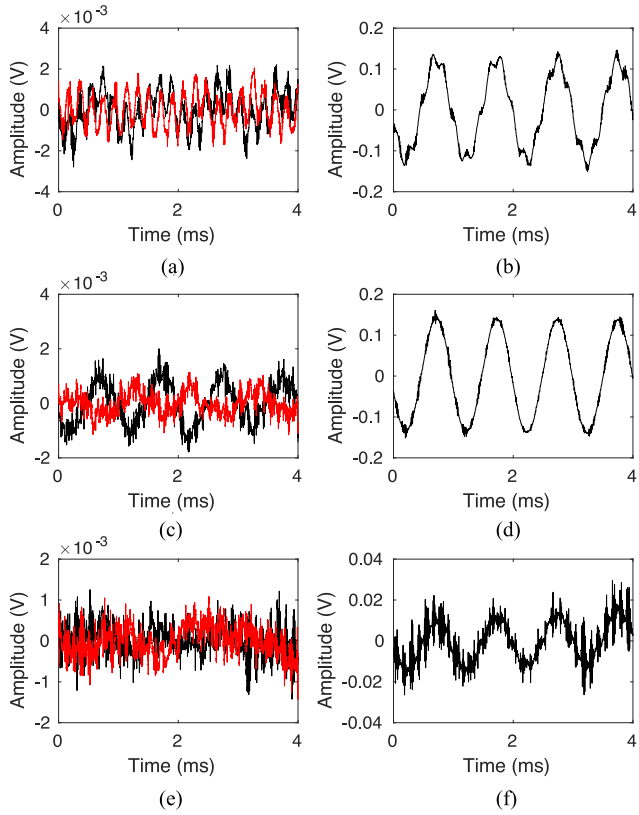

Fig. 14. Recordings from in vitro microchannel. Sine waves are injected as follows: 1 kHz "signal" with a dipole in the microchannel between the inner and outer electrodes (see Fig. 13); 5 kHz "interference" with a dipole outside the microchannel immediately above the central electrode. Injected amplitudes are: (a), (b), "signal" of 1 mV rms, "interference" of 100 mV rms; (c), (d), "signal" of 1 mV rms, "interference" of 10 mV rms; (e), (f), "signal" of 100 μV rms, "interference" of 10 mV rms. Recordings from: (a), (c), (e), E_{Ai} (black) and E_{Bi}/E_{Ci} (red); and (b), (d), (f), 100× differentially amplified output.

and amplified. Varying R2 does to alter the signal from E_{Bi}/E_{Ci} to D_{IN}/V_{CM}.

For R1 $\leq$ 1 kΩ, signals from E_{Ai} to I_S/V_{Neural} are distorted and amplified. For R1 $\geq$ 1 MΩ, signals from E_{Ai} to I_S/V_{Neural} are attenuated and the dc levels at E_{Ai} and E_{Bi}/E_{Ci} fall and the electrode potential offset increases.

D. In Vitro Microchannel Tests

To examine the effect of interference from local muscle activity on neural signal recordings the MNI ASIC was used in an in vitro microchannel setup. An oversized microchannel was manufactured using a previously described method [32]. Two fluoropolymer coated platinum wires (Johnson Matthey, 75 μm wire diameter, 115 μm outer diameter) were formed into a dipole as follows: approximately 50 μm of insulation was stripped from the ends of each wire to form two electrodes and the wires were adhered together with cyanoacrylate glue (Maplin, UK) to form a dipole with 4 mm interelectrode distance. The microchannel was immersed in a bath of phosphate buffered saline (PBS) and connected to the MNI ASIC in a tripolar arrangement (outer electrodes to E_{Bi} and E_{Ci}, inner electrode to E_{Ai}). The wire dipole was passed along the length of the microchannel. A stainless-steel rod, 8 mm diameter, was introduced into the bath at least 50 mm from the microchannel, the rod is used as the remote reference and biases the bath to V_{Ref}. All other biasing was carried out as described previously. The wire dipole was connected to a signal source via a step-down transformer. Signals were recorded from the microchannel electrodes (E_{Ai} and E_{Bi}/E_{Ci}) and the outputs of the MNI ASIC were differentially amplified and recorded. Response with the dipole at different locations within, and outside, the microchannel are shown in Fig. 13. Differential signal amplitude is largest when the dipole is within the microchannel. When the dipole is outside the microchannel the recorded signal amplitude drops rapidly with distance to $<$ 1% of the maximum signal amplitude.

The effect of interference was tested in the PBS bath (see Fig. 14). As above a dipole was passed along the length of the microchannel with the center of the dipole at 8 mm and was used to inject "signal", a second dipole was placed in the PBS outside the microchannel and was used inject "interference". Attenuation of interference due to the microchannel and common mode rejection suggests that efferent and afferent signals from some axons within microchannels ($<$ 100 μV at source) will be identifiable over the interference due to local muscle activity outside the microchannels ($<$ ~10 mV at source) [20].

IV. Discussion and Conclusion

The design and test of an ASIC for nerve stimulation and recording in a microchannel neural interface has been presented. Current controlled, biphasic stimulus pulses in the range

required for MNIs, has been demonstrated. The switch unit (Fig. 3 and Fig. 4) draws a small current (1.5 μA) during stimulation to safely turn on a high voltage transistor (MH3) with 40 V compliance; therefore this current must be supplied in addition to the stimulus level. This compliance voltage is required due to predicted stimulation currents and predicted high microchannel impedances [20], [32]. Stimulation frequencies over 50 kHz were achieved, although the large charge imbalances make this unsafe for in vivo use. Charge imbalances were reduced to $< 2\%$ error for up to 40 kHz stimulation [45]. High frequency stimulation can be used in reversible, kHz frequency nerve conduction blocking when treating pain and incontinence (frequencies of 1 kHz to 100 kHz are required) [47]. Higher stimulation frequencies are possible with the MNI ASIC, but would require a faster external controller. To achieve a 100 kHz stimulus frequency a data rate in excess of 2 Mbit/s is required such that two bitwords, each 10 bits, are sent every 10 μs. The proposed system can be adapted to generate stimulation pulses with imbalanced currents [48], this would require switching the current source output to I_S/V_{Neural} between stimulation phases. However, the system can achieve stimulation pulses with imbalanced phase durations and interphase delays. In this work charge error has been reduced to $< 2\%$ with no active discharge mechanism by adjusting command timing. Charge balancing can be achieved using a capacitor in series with I_S, switched to charge on the first phase and discharge on the second phase, the current in the second phase being cut-off when the charge reaches zero or an active charge balancing arrangement to achieve $< 1\%$ error [49], [50].

The ASIC is suitable for neural recording; however, the switching and biasing arrangement causes signal distortion and degrades common mode rejection. The signal distortion, and resulting poor CMRR, is due to the use of HV switches (MH3) to allow for the high microchannel impedance. Signals have been recorded from a differential input to the electrodes using an in vitro oversize microchannel. Tests with the in vitro microchannel demonstrate the role of a tripole in attenuating external interference, allowing the limited CMRR of this system to be acceptable in this application. The in vitro test gives an underestimate of the signal amplitudes, due to the larger channel dimensions, 0.25 mm² cross-section: signal amplitude will increase relative to interference as microchannel cross-section reduces (the proposed channels are 100 μm $\times$ 100 μm, 0.01 mm²) [24]. The in vitro microchannel is longer than the channel proposed for use on the MNI ASIC, at a minimum the channels can be 14$\times$ shorter (circa 1.4 mm), but will be 25$\times$ smaller diameter in practice microchannels 4 mm and 5 mm long have been used [23], [28], [32].

Multiplexing across electrodes within and between MNI ASICs has been demonstrated. This device only allows stimulation from one electrode, or all electrodes at the same time, not from a subset of electrodes [51]; however fast switching between electrodes can stimulate axons in different microchannels sequentially. Fast switching between recording channels is not proposed for this system. For example [21] identified three nerve activities correlated with bladder pressure with maximum firing rate of 15 Hz. Switching frequencies of 1 Hz to 2 Hz would allow for amplifier settling and firing rate recordings, and is appropriate for the case described in [21] where changes occur over minutes.

By using an active ASIC layer in an MNI design every microchannel can be addressed, in this case to a total of seven layers and 49 microchannels, while requiring only a 5-line bus. Due to the use of passive conductors previous MNI designs have been limited in the number of channels for stimulating and recording e.g., [28], [30], [31]. Here, reducing the number of interconnect wires has the additional advantage of reducing surgical complexity and failure risk due to cable damage [51].

The system uses a hard-wired connection for power, data, stimulation, and recording. Wireless power [52], [53], and wireless telemetry for stimulation [52], [54] and recording [55], [56] would avoid percutaneous connections.

A challenge for the use of these devices in vivo is the requirement for chronic, intimate contact between active silicon-based ASICs and extracellular fluid [43]. Due to the device size, presence of microchannels, and inclusion of electrodes at the ASIC surface a hermetic package is not suitable. The proposed device uses silicone encapsulation which has shown promise in accelerated aging test of silicon integrated circuits [57], [58]. Alternative encapsulation methods, for example alumina-parylene C coatings, may also be suitable [59], [60].

The MNI ASIC device is intended for use as a regenerative neural interface, where nerves are severed and axons re-grow along the microchannels. Regenerative interfaces are only suitable for locations where a residual nerve stump remains, or the nerve will otherwise be divided. The device, however, is not limited to these applications. A single layer device with one MNI ASIC and associated microchannels can be used with teased dorsal rootlets using a surgical approach which does not require the nerve roots to be cut. Further, all seven MNI ASICs do not need to be stacked in one device, seven separate devices with a parallel bus can be manufactured for implantation at different sites. The next stage of MNI development is to test the device with a suitable metal deposited on the tripole electrode pads. In addition, a second generation MNI ASIC is planned with on-ASIC amplifiers to address the low CMRR observed with the current design, and further system-level innovation is planned where the intermediate hub is integrated in an ASIC and stacked together with the MNI ASICs to form a single device.

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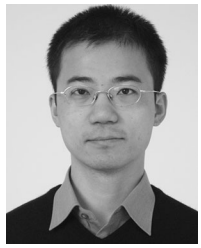
Henry T. Lancashire received the B.Sc.(Hons.) degree in biomedical materials science from the University of Nottingham, Nottingham, U.K., in 2010, the M.Res. degree in molecular modeling and materials science from University College London (UCL), London, U.K., in 2011, and the Eng.D. degree in molecular modeling and materials science from UCL, London, U.K., in 2015.

He was a Research Fellow with the Research Department of Materials and Tissue, UCL, from 2015 to 2017. In 2017, he joined the ASPIRE Centre for Rehabilitation Engineering and Assistive Technology, UCL as a Research Associate. Since 2018, he has been a Lecturer in active implantable medical devices with the Department of Medical Physics and Biomedical Engineering, UCL. His research interests include the micromanufacture, electrode properties, and biocompatibility, of active interfaces with nerve and muscle.

Dr. Lancashire is a member of the Institute of Physics and Engineering in Medicine (IPEM) and a member of the Institute of Materials, Minerals and Mining (IOM3).



Dai Jiang (S'07–M'09) received the B.Sc. and M.Sc. degrees from the Beijing University of Aeronautics and Astronautics, Beijing, China, in 1998 and 2001, respectively, and the Ph.D. degree from the University College London (UCL), London, U.K., in 2009, working on frequency synthesis. From 2001 to 2002, he was with Datang Telecom Group, China, developing FPGA functions for WCDMA signal processing. In 2006, he joined the Analog and Biomedical Electronics Group, UCL, where he is a currently a Senior Research Fellow. His research interests include CMOS analog and mixed-signal integrated circuit design for biomedical applications.

Dr. Jiang is a member of the Biomedical and Life Science Circuits and Systems Technical Committee of the IEEE Circuits and Systems Society.

Andreas Demosthenous (S'94–M'99–SM'05–F'18) received the B.Eng. degree in electrical and electronic engineering from the University of Leicester, Leicester, U.K., in 1992, the M.Sc. degree in telecommunications technology from Aston University, Birmingham, U.K., in 1994, and the Ph.D. degree in electronic and electrical engineering from the University College London (UCL), London, U.K., in 1998. He is a Professor with the UCL Department of Electronic and Electrical Engineering and leads the Analog and Biomedical Electronics Group. He has authored more than 300 articles in journals and international conference proceedings, several book chapters, and holds several patents. He has made outstanding contributions to improving safety and the performance in integrated circuit design for active medical devices, such as spinal cord and brain stimulators. His research interests include analog and mixed-signal integrated circuits for biomedical, sensor, and signal processing applications.

Dr. Demosthenous is a Fellow of the Institution of Engineering and Technology and a Chartered Engineer. He is currently the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and a Member of the International Advisory Board of Physiological Measurement. He is a member of the Technical Programme Committee of several IEEE conferences, including the European Solid-State Circuits Conference and the International Symposium on Circuits and Systems.

Nick Donaldson worked for the Neurological Prostheses Unit at the Medical Research Council under Giles Brindley who pioneered many neuroprostheses and other implanted devices. Since 1992, he has been the Head of the Implanted Devices Group, University College London, London, U.K. The Group has been involved in projects in implanted device design and technology, neural interfaces, functional electrical stimulation, particularly FES-cycling, and the application of electrical stimulation to promote neuroplastic recovery. He has been the Principal Investigator of 39 funded projects and has supervised 23 Ph.D. students.