A Multichannel High-Frequency Power-Isolated Neural Stimulator With Crosstalk Reduction

Dai Jiang, *Member, IEEE*, and Andreas Demosthenous, *Fellow, IEEE*

***Abstract*—In neuroprostheses applications requiring simultaneous stimulations on a multielectrode array, electric crosstalk, the spatial interaction between electric fields from various electrodes is a major limitation to the performance of multichannel stimulation. This paper presents a multichannel stimulator design that combines high-frequency current stimulation (using biphasic charge-balanced chopped pulse profile) with a switched-capacitor power isolation method. The approach minimizes crosstalk and is particularly suitable for fully integrated realization. A stimulator fabricated in a 0.6 μm CMOS high-voltage technology is presented. It is used to implement a multichannel, high-frequency, power-isolated stimulator. Crosstalk reduction is demonstrated with electrodes in physiological media while the efficacy of the high-frequency stimulator chip is proven *in vivo*. The stimulator provides fully independent operation on multiple channels and full flexibility in the design of neural modulation protocols.**

***Index Terms*—Chopped pulse, electric crosstalk, mixed-signal integrated circuit, multichannel neural stimulator, power isolation.**

I. Introduction

THE advance of CMOS technology and high-density electrode fabrication allows integrating stimulation on multiple channels into miniaturized fully implantable neuroprostheses. Besides conventional multichannel stimulators such as cochlear [1], [2] retinal [3], [4] and vestibular implants [5], [6] where stimulating multiple channels is necessary for creating real perceptual sensation, state-of-the-art neural stimulators for the spinal cord [7], and the peripheral nervous system [8], [9] are also enhanced with novel electrode design features such as three-dimensional [10] or microchannel arrays [8], [11] where a finer neural interface allows higher selectivity for stimulating targeted nerves. Additionally, advanced system architectures including active electrodes [7], [12] and networked topologies [13] allow localized stimulation with maximum efficiency.

Channel interference (electric crosstalk) is a major limitation to the performance of multichannel stimulation. Charge imbalance may be caused by the current flowing between different stimulation channels through the tissue, due to current loops formed when the power supply is shared. When multiple stimulators operate simultaneously, crosstalk will distort the charge available for the desired neural response on the targeted channel. To avoid current flow between channels the most common solution is to interleave the stimulation channels so that only one channel is active at a time, such as the continuous interleaved sampling (CIS) strategy [14] used in cochlear implants and a prototype vestibular stimulator design [15]. Despite its simplicity in implementation, stimulating the channels in sequence inevitably limits the available options for neural modulation, where independent, parallel and localized stimulation on individual channels might not be achievable for applications favoring such stimulation strategies, for example, vestibular [16] and optic nerve stimulation [17]. Spatial isolation is another popular choice for preventing current flowing to other channels, where current steering and electrical field focusing are often implemented in combination with tripolar [18] or multipolar [19], [20] electrode configurations. To focus the current field towards the targeted stimulation site, one or multiple return electrodes are located close to (or enclosing) the stimulating electrode, thereby allowing good isolation between the stimulation channels. The main drawback, however, is the increased physical size required by the multiple return electrodes.

The authors have recently reported a power isolation method [21] for reducing channel interference. In this method, stimulators are connected to the power supply via switches. When generating a stimulating pulse, the switches turn off so that the current path to other stimulation channels through the shared power supply is interrupted. During this isolation, each stimulator is temporarily supplied by an energy storage capacitor attached to this stimulator. Between stimulating pulses the capacitor is recharged from the system power supply. *In-vitro* results showed effective crosstalk reduction in multichannel bipolar stimulation. However, the size demand for the energy storage capacitor limits the total number of channels that can be supported; for example, with a stimulating pulse with a total charge of 400 nC (1 mA, 200 μs, biphasic pulse) or higher, the storage capacitor needs to be hundreds of nanofarad to avoid the supply voltage dropping below the minimum voltage compliance of the current driver. Capacitors of this size are not realistic to implement on chip; while discrete capacitors, on the other hand, require significant layout and routing area. Although this power isolation method satisfies its original target application (three-channel vestibular stimulation for the three semi-circular canals in the inner ear) it requires significant improvement to support a higher number of stimulation channels.

Manuscript received October 30, 2017; revised March 18, 2018; accepted April 12, 2018. Date of publication May 31, 2018; date of current version August 15, 2018. This work was supported in part by the EPSRC under Grant EP/F009593/1, and in part by the European Commission under project NEUWalk. This paper was recommended by Associate Editor R. Sarpeshkar. *(Corresponding author: Andreas Demosthenous.)*

The authors are with the Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, U.K. (e-mail: d.jiang@ucl.ac.uk; a.demosthenous@ucl.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2018.2832541

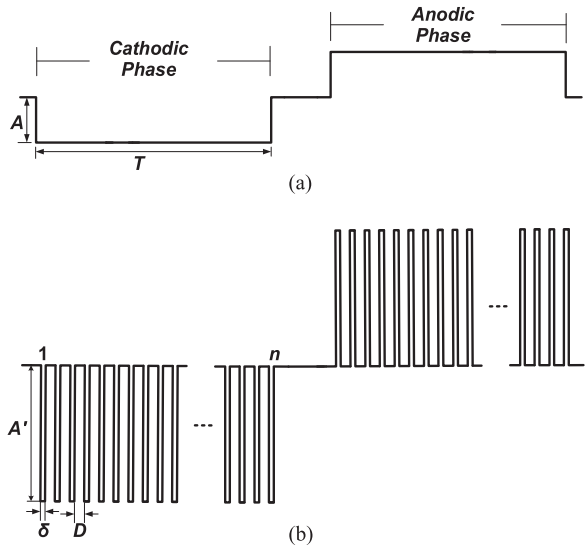


Fig. 1. Illustration of the profile of stimulating pulses: (a) conventional charge-balanced biphasic constant-current pulse; (b) biphasic, charge-balanced "chopped" pulse generated by the stimulator reported in this paper.

This paper presents a stimulator design that adopts a stimulation scheme different from the conventional pulsatile stimulation. A series of small packets of current pulses with a short interval between them are used for stimulation (i.e., performing high-frequency stimulation) instead of the conventional lumped constant-current pulses lasting hundreds of microseconds. The approach allows the storage capacitor to only supply its stimulation channel for one packet with a duration of one or two microseconds, hence its capacitance can be reduced by at least two orders of magnitude. It is feasible with this reduction to have the multichannel stimulator, including the storage capacitors, fully integrated onto silicon while maintaining the crosstalk reduction performance offered by power isolation.

The rest of the paper is organized as follows. Section II outlines the principle of high-frequency stimulation and the operation of power-isolated stimulation based on it. Section III describes the system architecture and circuit details of the multichannel, high-frequency, power-isolated neural stimulator. Section IV shows its measured performance including *in-vitro* results on crosstalk reduction with electrodes on two closely placed channels in physiological saline. Section V shows *in-vivo* stimulation results on a vestibular nerve using either the chopped pulses or the conventional biphasic pulses with equal amounts of total charge. Section VI concludes the paper.

II. Principle of High-Frequency Power-Isolated Stimulation

In conventional constant-current monophasic or charge-balanced biphasic or multiphasic pulsatile stimulation, the cathodic phase (generally lasting for hundreds of microseconds) delivers an amount of charge above the threshold which evokes an action potential. A charge-balanced biphasic pulse is shown in Fig. 1(a). The stimulator in this paper generates pulses in a different profile as shown in Fig. 1(b), where a series of small packets of current pulses of the same polarity with a short interval between them, function similarly as the cathodic phase of a conventional biphasic pulse. The packets are followed by another series of small packets in the opposite polarity for charge balance. This stimulation strategy is based on the assumption that the neural membrane acts as a leaky integrator to accumulate the charge from the subthreshold packets over time to ultimately exceed the threshold to evoke neural activity [22]. If the overall charge in the entire series of packets is equal to the charge in the cathodic phase of a conventional biphasic pulse, i.e., according to Fig. 1, $A \cdot T = n \cdot A' \cdot \delta$, where A and T are the amplitude and width of the cathodic phase in Fig. 1(a), respectively, A' and δ are the current amplitude and duration of one packet in Fig. 1(b), respectively, and n is the total number of packets in the series, the series of packets should evoke similar action potential to that by the conventional pulse. The efficacy of neural stimulation using a series of subthreshold packets has been demonstrated *in-vivo* on the auditory nerve [22] and *in-vitro* on Purkinje cells [23].

This paper provides further evidence on the efficacy of high-frequency stimulation applied to the vestibular nerve as detailed in Section V, where the vestibulo-ocular reflex (VOR) by both the conventional and high-frequency stimulation was recorded and compared. As the shape of the packet series looks like a conventional biphasic pulse being chopped, this pulse profile is called a "chopped pulse".

Stimulating with a series of high-frequency packets for reducing channel interference has been previously implemented in multichannel stimulator design [24]–[27]. The principle of interference reduction in these designs is to interleave the packets on multiple channels to achieve "quasi-simultaneous" stimulation. Due to the short duration of the packets, the delay caused by interleaving is acceptably short. However, when the number of channels increases, interleaving will demand longer intervals between the packets on each channel, resulting in loss of charge at the neural membrane during the packet series, and hence less neural response to the stimulation. This loss was shown in [23].

Instead of interleaving, the multichannel stimulator design in this paper incorporates the high-frequency chopped pulse scheme into the power isolation method, so that the packets on different channels can appear simultaneously while the channels are isolated. The operation of the stimulator is depicted in Fig. 2. Using two channels as an example (*Channel A* and *Channel B*), the stimulator on either channel is connected to the supply rails via a pair of power switches between the high voltage supply and the ground, S_{A1} and S_{A2}, and S_{B1} and S_{B2}, respectively. Each channel also has a storage capacitor, C_A or C_B, connected between the power switches. Electrodes on either channel are activated or deactivated via a pair of electrode switches (S_{A3}, S_{A4}, and S_{B3}, S_{B4}). When *Channel A* is in operation, for example, S_{A1} and S_{A2} turn off when the stimulator on this channel is generating a current packet, during which time S_{A3} and S_{A4} are on to pass current packets through the electrodes, and the circuits in this channel are supplied by C_A. At the interval between the packets, S_{A1} and S_{A2} turn back on to charge the storage C_A while S_{A3} and S_{A4} are off. In this way, the electrodes on *Channel A* are always isolated from *Chan-*

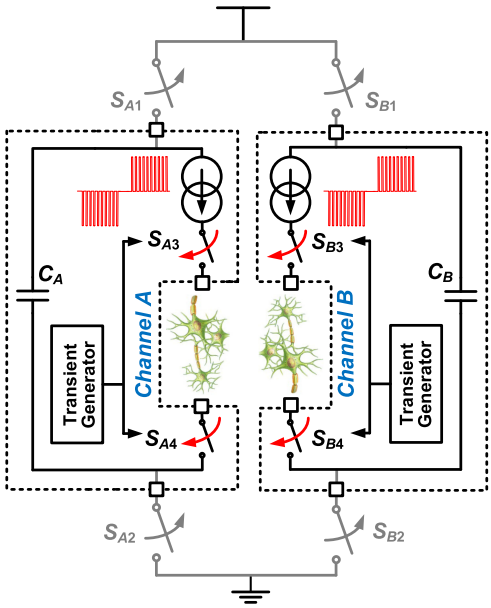


Fig. 2. Operation of the proposed multichannel high-frequency power-isolated stimulator using the chopped pulse.

nel B and the system supply rails. The same operation is also performed in *Channel B*. A transient generator on either channel controls the power and electrode switches to synchronize the isolated stimulation and capacitor recharge. Also, by reversing the direction of the current flow, a second series of current packets in the anodic orientation can be delivered to the electrodes for charge balancing. With this arrangement, the electrodes on each channel are always isolated from the supply rails, hence electric inter-channel crosstalk can be minimized. For the same reason, the current packets on different channels can appear simultaneously without cross channel interference.

The chopped pulse profile significantly relaxes the capacitance requirement of the storage capacitor in the power isolation method. For a conventional biphasic pulse, as shown in Fig. 1(a), the minimum necessary stored charge in the capacitor, without considering the energy required for the operation of the circuits, is equal to the total charge in the two phases of the pulse, $2A{\cdot}T$. Using the chopped pulse, however, because the capacitor can be charged during the interval between the small packets, the minimum charge is reduced to the charge in a packet, $A'{\cdot}\delta$. As δ can be smaller than T by two orders of magnitude, the capacitance of the storage capacitor is greatly reduced and is feasible for on-chip implementation.

III. System Implementation

Fig. 3 shows the system architecture of the high-frequency, power-isolated stimulator for one channel. This arrangement is scalable for multichannel design, where the circuits for each channel are identical, with all the channels sharing the same serial peripheral interface (SPI) and the power supply rails, *VDDH* and *GND*. The hardware for each channel, as shown in the figure, comprises a power and control module and a stimulator module. The power and control module handles the switching on the power rails to the stimulator module via built-in power switches, which connect or isolate the stimulator module. The stimulator module generates chopped pulses from a programmable current driver and an 'H-bridge' output stage, controlled by a pulse control logic and a monostable multivibrator. This module has a built-in storage capacitor, C_S, which supplies the module during stimulation when it is isolated from *VDDH* and *GND* by the power and control module. There is also a voltage regulator in the stimulator module providing *VDD* at 5 V.

In a multichannel stimulator design, the power and control modules for all the channels can be supplied from the same *VDDH* and *GND*, while the stimulator modules must have their own isolated supplies. To achieve optimum isolation, the stimulator module for each channel must be physically separated from the substrate of other stimulator modules and the power and control module. There is then no common substrate where crosstalk current occur in the event that the ground voltage of a stimulator falls below the bias voltage of the common substrate, as detailed in Section III-F. To provide this isolation, one option is to implement the power and control modules on one application specific integrated circuit (ASIC), and each stimulator module on a separate ASIC. This option was adopted for the prototype stimulator in this paper. A better option would be to implement all the modules on a single ASIC by using silicon-on-isolator (SOI) technology, where the modules can be implemented in trench-isolated tubs, and hence there is no shared common substrate. The layout of the modules on SOI must minimize the coupling capacitance between the tubs that might compromise the isolation.

A. Power-Isolated Stimulation

As shown in Fig. 3, the power and control module connects to the stimulator module via power switches S_{VDDH} and S_{GND}, and communication switches S_{CK}, S_D and S_T. When the stimulator is idle, the switches are all turned on. Before starting a chopped pulse, the stimulation management unit sends to the stimulator module (via switches S_{CK} and S_D) pulse parameters including the current amplitude, electrode multiplexing and a 2-bit current setting for adjusting the width of each current packet. After the data transmission, the stimulation control turns off S_{CK} and S_D, and starts synchronously turning on and off S_{VDDH}, S_{GND} and S_T. At the time instant when S_T is turned off, the pull-up resistor R_3 causes a rising edge (*Trigger*) which triggers the monostable multivibrator to generate a single output pulse, *Mask*. The length of *Mask* is defined by the internal current digital-to-analog converter (DAC) in the monostable multiviborator. The single *Mask* pulse enables the current source and the 'H-bridge' in the output stage through the switches SW_1–SW_5 and SW_C that are controlled by S_{1L}–S_{5L} and S_{CL}, so that a current packet appears at the stimulator output. The duration of this current packet is the same as the single *Mask* pulse. After *Mask* returns to logic 0, S_{VDDH}, S_{GND} and S_T are turned on again to charge the storage capacitor C_S in the stimulator module, and to pull *Trigger* back to logic 0. After a short interval, the power and control module repeat this pro-

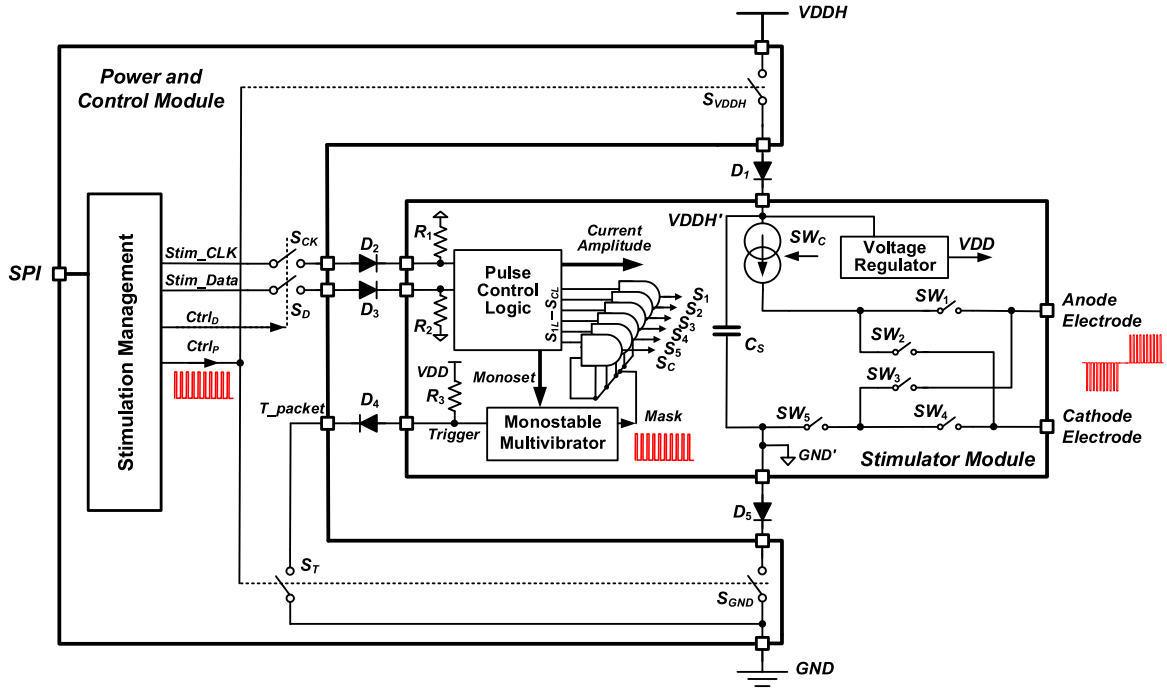


Fig. 3. System architecture showing the arrangement for one stimulation channel. Multichannel design can be implemented by replicating this scalable arrangement for multiple channels, with all the channels sharing the same SPI and power supply rails, *VDDH* and *GND*.

cedure to generate another current packet. This process repeats until all current packets in the cathodic phase are delivered. After the cathodic phase, and before the anodic phase, the power and control module turns on S_{CK} and S_D to send clock pulses to the stimulator module to trigger the pulse control logic in the module to alter the 'H-bridge' to change the current direction through the electrodes. Current packets in the anodic phase are then generated. After the anodic phase, switches SW_3 and SW_4 in the stimulator module are turned on and remain on until the next chopped biphasic pulse to remove any residual charge on the electrodes, while all other switches in this module remain off.

B. Stimulation Control

The details of the stimulation control, including both the stimulation management unit and the pulse control logic, are shown in Fig. 4. The power and control module receives the stimulation setting parameters via SPI from an external controller through a telemetry link [28]. The stimulation management unit stores the parameters into the built-in memory block when addressed, and repeatedly loads the parameters into the management state-machine at the beginning of every chopped biphasic pulse until the parameters are updated again from the SPI. The management state-machine comprises four cascaded counters corresponding to periods of the cathodic phase, IPD (inter-phase delay), anodic phase and pulse interval (interval between two chopped biphasic pulses). Operating at a 1 MHz clock (*CLK*), the counters can achieve a resolution of 1 μs in pulse width and pulse interval. The counters load the initial values from the memory simultaneously at the beginning of a chopped biphasic pulse, and then count down to zero in a round-robin fashion. Before reaching zero, each counter keeps the output signal *Active* at logic 1 which disables the operation of the following counters. Once all the four counters reach zero, they are reloaded with the initial values again by triggering the *Read* input on the memory block to start a new biphasic pulse. The output control is triggered at the same time as *Read*, to send the pulse parameters to the stimulator module via *Stim_CLK* and *Stim_Data*. When *Catho Cnt* or *Ano Cnt* is counting down, *Trigger Cnt* is enabled to count down to zero and reload. The length of the countdown period of *Trigger Cnt* defines the duration of the $Ctrl_P$ signal that turns S_{VDDH}, S_{GND} and S_T on and off.

The pulse control logic in the stimulator module operates at *Stim_CLK,* as shown in Fig. 4(b). The logic controls the output stage switches and the current source to create cathodic and anodic current, while the monostable multivibrator "chops" the current into small packets. The logic also sets the 8-bit current DAC in the current source, as well as the 8-bit electrode multiplexer. At the beginning of a chopped biphasic pulse, the output control sends 25 *Stim_CLK* pulses and a stream of alternating '1's and '0's on *Stim_Data* for resetting the pulse control logic, a similar resetting process to the logic in [21]. After this PreReset, the output control sends a 24-bit frame including settings for the current DAC, the electrode multiplexer and the monostable multivibrator. After loading the frame, the pulse control logic enters a "one-shot" mode, where every *Stim_CLK* pulse moves the state-machine into the next state. The logic sets S_{1L}–S_{CL} accordingly in each state. After the anodic phase, the logic receives another 25 *Stim_CLK* pulses and an alternating '1' '0'

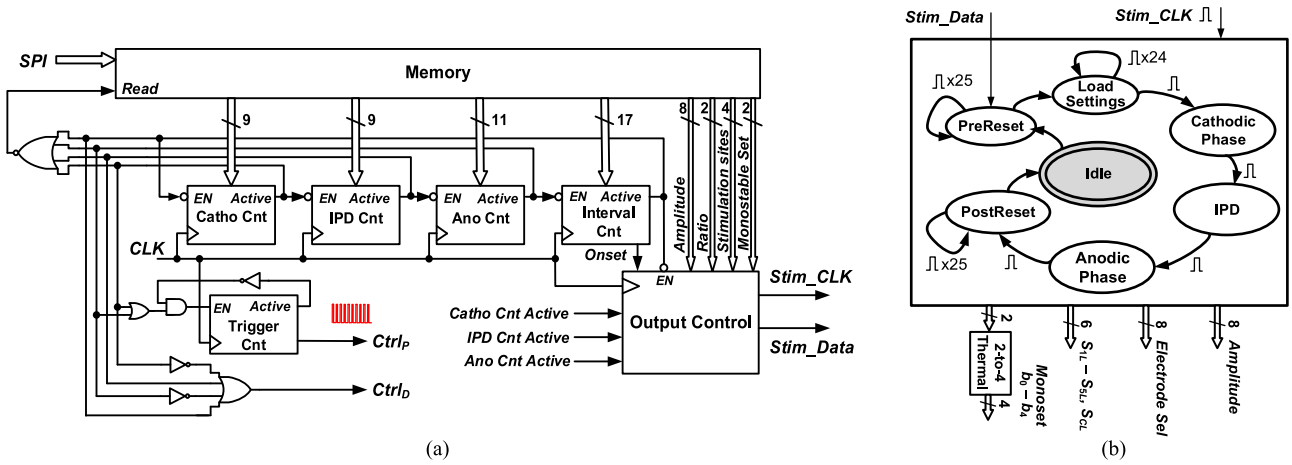


Fig. 4. Stimulation control: (a) system architecture of the stimulation management unit; (b) the state-machine in the pulse control logic.

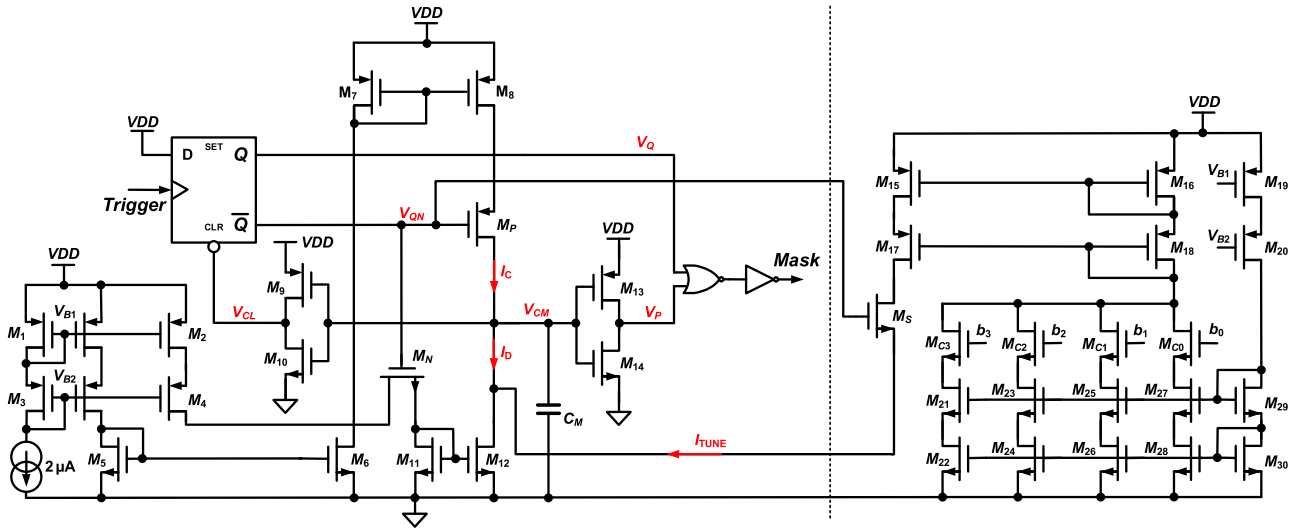


Fig. 5. Schematic of the monostable multivibrator.

bit stream for resetting the output stage into the isolated passive discharge mode.

C. Monostable Multivibrator

The monostable multivibrator generates a positive pulse when triggered by a rising edge at the *Trigger* input. The circuit architecture is similar to [28]. The schematic is shown in Fig. 5. When the *D* flip-flop is at the reset state, V_Q is logic 0 and V_{QN} is 1, hence V_{CM} on the capacitor C_M is discharged to zero, which sets V_P and V_{CL} to logic 1, so that the output signal, *Mask*, is forced to zero. The arrival of a rising edge on *Trigger* flips V_Q to logic 1 and V_{QN} to 0, which turns transistor M_P on and M_N off, starting charging the capacitor C_M with a constant current I_C, causing the rise of V_{CM}. Once V_{CM} rises to the threshold voltage of the inverter consisting of transistors M_{13} and M_{14}, V_{TH1}, V_P jumps to logic 0. Concurrently V_{CM} continues rising to the threshold voltage of the inverter consisting of M_9 and M_{10}, V_{TH2}, turning V_{CL} to logic 0 hence resetting the *D* flip-flop. As a result, V_Q goes back to logic 0 and V_{QN} to 1, turning M_P off and M_N on, starting discharging C_M with a constant current I_D. V_{CM} starts falling at this point. Once reaching V_{TH1} again, it turns V_P to logic 1. The output signal, *Mask*, which was turned to logic 1 at the arrival of the rising edge on *Trigger*, is pulled back to logic 0. Therefore, a positive pulse on *Mask* is triggered by the input rising edge, but its width, T_M, is entirely decided by the internal circuits of the monostable multivibrator as

$$T_M = \frac{C_M}{I_D}\left(V_{TH1}\frac{I_D + I_C}{I_C} - V_{TH2}\right). \tag{1}$$

In this design, the two inverters were sized to have $V_{TH1} = 1.88\,\text{V}$ and $V_{TH2} = 2.93\,\text{V}$, while C_M is an integrated capacitor of 35 pF. The charging current I_C is fixed at 120 μA, while the discharging current I_D can be fine-tuned by adding the tuning current I_{TUNE} to a base current of 32 μA. Ideally, $T_M = 2\,\mu\text{s}$ when $I_{\text{TUNE}} = 0$. To overcome

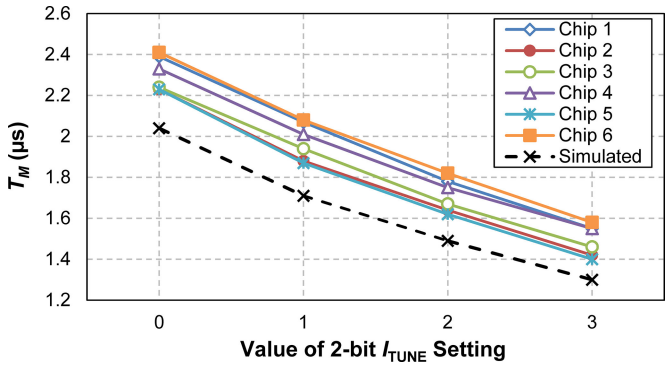


Fig. 6. Measured and simulated T_M at different I_{TUNE} settings.

possible process variations and parasitic capacitance that might increase the length of T_M, I_{TUNE} is programmable by sending a 2-bit setting from the stimulation management unit, which is then converted into a 4-bit thermal code, *Monoset*, by the pulse control logic. *Monoset* controls b_0–b_3 of the 4-bit current DAC shown in Fig. 5 that generates I_{TUNE}. Increasing I_{TUNE} makes C_M discharge faster and thus T_M shorter. The available values for I_{TUNE} are 0, 1.5 μA, 3.5 μA and 7.5 μA. Fig. 6 shows the simulated values of T_M and the measured ones at different I_{TUNE} settings. It is shown that the actual value of T_M in all the fabricated ASICs are higher than expected, but can be fine-tuned close to 2 μs.

D. Output Stage

Current packets are generated from the cascode current source with active feedback and the 'H-bridge' output stage in the stimulator module, as shown in Fig. 7(a). An 8-bit current DAC provides the reference for the current source [29]. The output current ranges from 0 to 1 mA at a step size of 4 μA. The current flows through SW_2 and SW_3 during the cathodic packets, and SW_1 and SW_4 during the anodic packets. The electrode multiplexer, set by the pulse control logic, enables multi-site stimulation on this channel. At the current packet interval, the 'H-bridge' switches and SW_5 are all off to isolate the electrodes. Also, the transistor M_C at the active feedback output is switched on to force the gate-source voltage of M_4 to zero, turning off the current source.

The switch control signals S_C and S_1–S_5 are synchronized. To avoid significant glitching at the onset of each current packet [15], the turn-on speed of the current source is slightly slower than the switches in the output stage. Fig. 7(c) shows the simulated turn-on time of the current source switch M_C and one of the 'H-bridge' SW_2, as well as the current packet generated from the switching. As shown, after SW_2 turns on, the gate-source voltage of M_4 takes 1.18 μs to recover to the operating level. As a result, the onset of the current packet starts with a small glitch from zero current, followed by a ramp to the set current level. M_4 is driven by a folded-cascode operational transconductance amplifier (OTA) shown in Fig. 7(b). The bias voltages, while $VDDH' = 12$ V, are $V_{B1} = 10.36$ V, $V_{B2} = 10.02$ V,

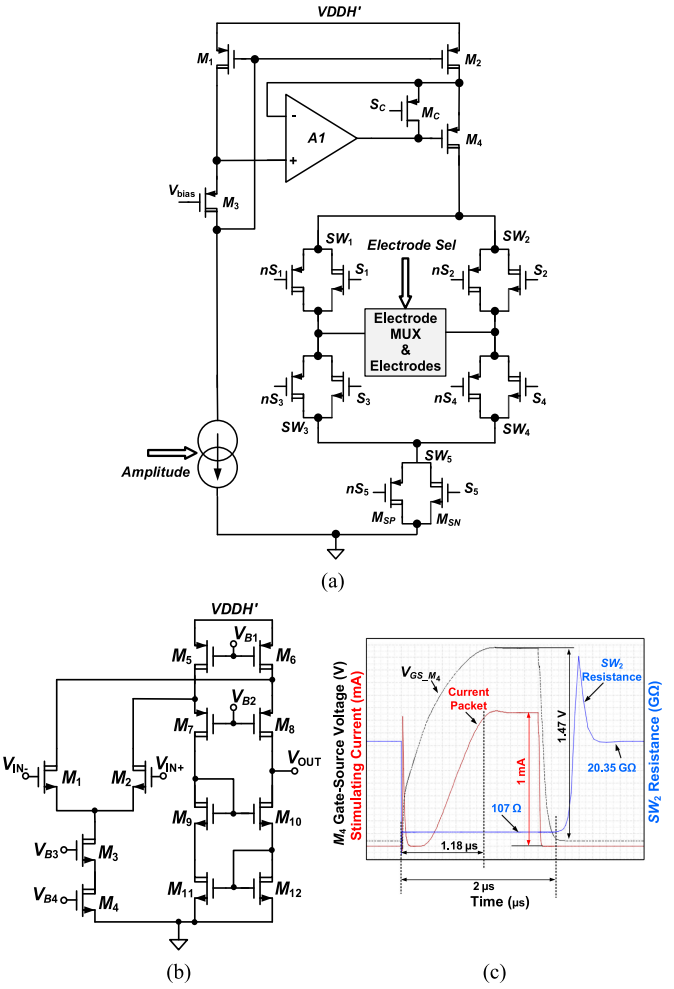


Fig. 7. The stimulator output stage: (a) schematic of the output stage; (b) schematic of the OTA in the output stage; and (c) post-layout simulated switch operation for generating one current packet.

$V_{B3} = 1.51$ V, and $V_{B4} = 1.508$ V. The bias current through M_3 is 16 μA.

E. Storage Capacitor C_S

The minimum capacitance of C_S can be calculated as

$$C_{S\_\min} = \frac{\delta\,(I_{\max} + I_{OP})}{VDDH' - V_{\mathrm{Compliance\_min}}} \tag{2}$$

where $I_{\max}$ is the maximum stimulation current amplitude, I_{OP} is the current consumed by the operation of the stimulator module, and $V_{\mathrm{Compliance\_min}}$ is the minimum value of the compliance voltage for the output stage to maintain correct operation. In this design, $I_{\max}$ is 1 mA, I_{OP} is around 500 μA at the maximum stimulation current, and the difference between $VDDH'$ and $V_{\mathrm{Compliance\_min}}$ is limited to within 2 V. Since δ is set to 2 μs, the minimum capacitance for C_S is 1.5 nF. An on-chip 2.38 nF POLY1-POLY0 capacitor was implemented in the chosen CMOS technology (XFAB 0.6 μm HV CMOS [30]) with a physical area of 1.27 mm^2.

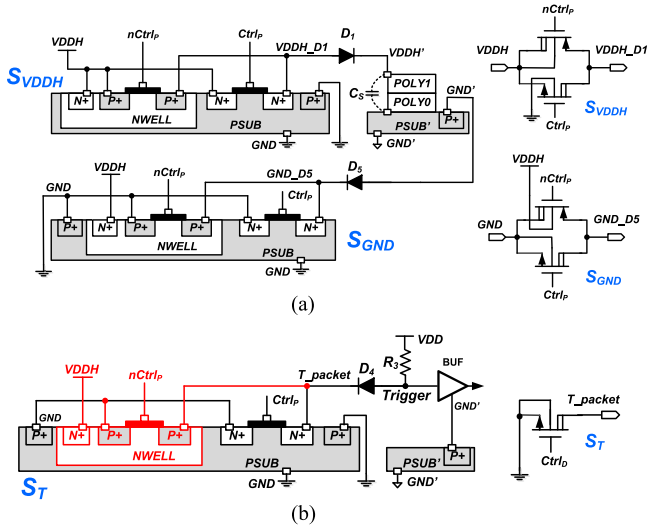


Fig. 8. Layout of the isolation switches and simulated isolation performance: (a) S_{VDDH} (upper) and S_{GND} (lower) on the positive supply rail; (b) S_T at the monostable multivibrator input. The blocks in red are not implemented.

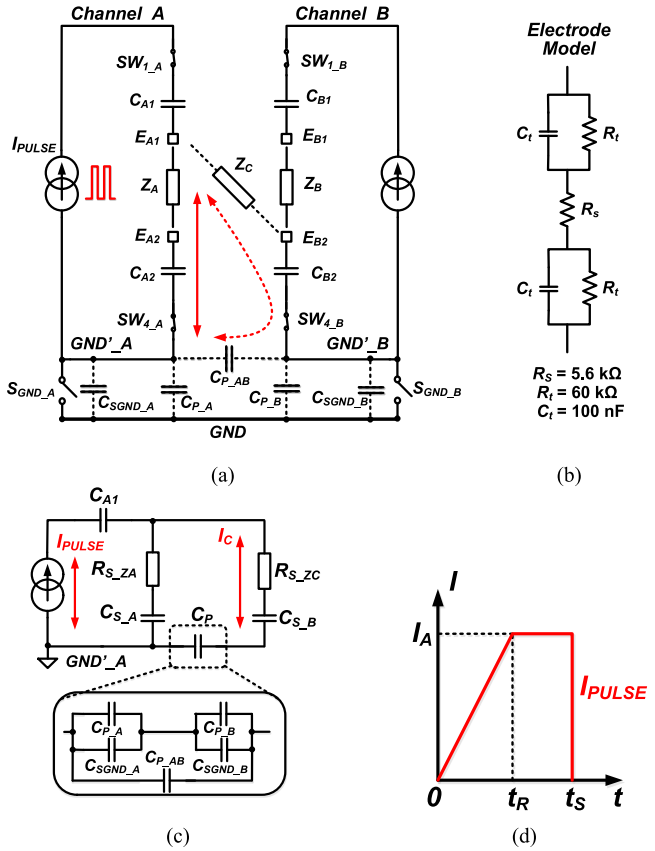


Fig. 9. Analysis of possible channel interaction due to the capacitive coupling path: (a) illustration of possible current paths; (b) electrode model; (c) equivalent circuits of the current path for analyzing crosstalk effect to I_{PULSE}; (d) simplified shape of a current packet in I_{PULSE}.

F. Isolation Switches

When isolated during stimulation, the supply potentials on a stimulator module, *VDDH*$'$ and *GND*$'$, are floating with reference to *VDDH* and *GND*. However, since the electrodes connected to the stimulators are located in close vicinity inside the body, the electrodes on the resting stimulators, which are connected to *VDDH* and *GND*, will force the voltage potential on the nearby tissue, and hence the voltage potential on the electrodes of active stimulators, to be between *VDDH* and *GND*. Therefore, *VDDH*$'$ will stay higher than *GND*, and *GND*$'$ will stay lower than *VDDH*. The arrangement of the isolation switches between the power and control module and the stimulator module is shown in Fig. 8(a), (b). The substrates of the two modules are separated. The substrate potential of the power and control module, including the switches, is at *GND*, while the substrate of the stimulator module is at *GND*$'$. The power switches S_{VDDH} and S_{GND} are complimentary switches. Their on resistance is around 28 Ω, hence the RC time constant of two power switches in series with the storage capacitor is 0.13 μs, sufficiently fast for voltage recovery during the current packet interval. Two floating Schottky diodes, D_1 and D_5, are connected in series between the two modules to prevent current leak. Without D_1, for instance, if *VDDH*$'$ is higher than *VDDH* during isolation, the voltage on the *P*-node of the PMOS in S_{VDDH} will be higher than the voltage of the n-well for this PMOS, hence the p-n junction is forward-biased and current will leak through the S_{VDDH}. Similarly, D_5 prevents current leak from the substrate to the *N*-node of the NMOS in S_{GND} if *GND*$'$ is lower than *GND*. The three control switches, S_T, S_{CK} and S_D, cannot be implemented using complimentary switches. For example, as shown in the layout of S_T in Fig. 8(b), during isolation the voltage at the input of the monostable multivibrator, *Trigger*, is pulled up to *VDD*, which is 5 V with reference to *GND*$'$; hence it is both possible that *Trigger* $>$ *VDDH* or *Trigger* $<$ *GND*, which leads to leakage current in either the PMOS or the NMOS respectively in a complementary switch. A floating diode in series, however, can only stop the leakage current in one direction. S_T uses a NMOS and a floating diode, D_4, with its anode connected to the stimulator module to stop leakage current when *Trigger* $<$ *GND* (the PMOS in the switch is eliminated, as shown in the figure). S_{CK} and S_D are implemented with PMOS, and the cathodes of D_2 and D_3 are connected to the stimulator module. Post-layout simulation shows that the off isolation of switches S_{VDDH} and S_{GND} is around -50 dB and their power supply rejection ratio is -30 dB, both at 1 MHz. The off capacitance of S_{VDDH} between *VDDH* and $VDDH\_D_1$ is 0.36 pF and the off capacitance of S_{GND} between *GND* and GND_D_5 is 2 pF.

G. Crosstalk Analysis

When two stimulation channels operate simultaneously, any parasitic capacitance between the two stimulator modules may result in crosstalk current. Fig. 9(a) shows a simplified circuit showing the two stimulator modules operating at the same time. Switches SW_1 and SW_4 on *Channel A* are on for a cathodic phase, while SW_1 and SW_4 on *Channel B* are on for an anodic phase. Between SW_1 and SW_4 on *Channel A* is the desired current path on this channel, shown as a solid red line, where

the current packets in I_{PULSE} passes through the electrodes E_{A1} and E_{A2}, and the blocking capacitors C_{A1} and C_{A2}. The electrode-load impedance Z_A is modeled as shown in Fig. 9(b). Both S_{GND_A} and S_{GND_B} are off to isolate the two channels from the master ground rail *GND*, but capacitive coupling path may exist between the stimulation modules and *GND* due to the off capacitance of S_{GND_A} and S_{GND_B}, C_{SGND_A} and C_{SGND_B}, respectively, as well as parasitic capacitance between the layout of the stimulator modules and *GND*, C_{P_A} and C_{P_B}, and parasitic capacitance between the stimulator modules, C_{P_AB}. This capacitive coupling introduces a possible crosstalk path between the stimulation channels shown as a dotted red line in Fig. 9(a). Assuming that in the worst case the distance between E_{A1} and E_{B2} is similar to the distance between E_{A1} and E_{A2}, the impedance in the crosstalk path, Z_C, has the same equivalent circuit as Z_A and Z_B.

Fig. 9(c) shows a simplified circuit model of *Channel A* with the crosstalk path, where C_{S_A} is the combined capacitance of C_{A2} connected in series with the two C_t in Z_A, C_{S_B} is the combined capacitance from C_{B2} and the two C_t in Z_B, and C_P is the combined coupling capacitance between *GND*$'$*_A* and *GND*$'$*_B*, as shown in the figure. Referring to Fig. 9(c), assuming $C_{S\_A} \gg C_P$ and $C_{S\_B} \gg C_P$, the crosstalk current $I_C(s)$ is

$$I_C(s) = I_{\mathrm{PULSE}}(s) \cdot \frac{s\tau_1 + 1}{s\tau_2 + 1} \cdot \frac{C_P}{C_{s\_A}} \tag{3}$$

where

$$\tau_1 = R_{s\_Z_A} \cdot C_{S\_A} \tag{4}$$

$$\tau_2 = (R_{s\_Z_A} + R_{s\_Z_C}) \cdot C_P. \tag{5}$$

A current packet in I_{PULSE}, such as the simulated packet shown in Fig. 7(c), can be simplified as the pulse shown in Fig. 9(d), written as

$$I_{\mathrm{PULSE}}(t) = \frac{I_A}{t_R} \cdot t - \frac{I_A}{t_R} \cdot (t - t_R) - I_A \cdot u(t - t_S) \tag{6}$$

whose Laplace transform is

$$I_{\mathrm{PULSE}}(s) = \frac{I_A}{t_R} \cdot \frac{1}{s^2}\left(1 - e^{-s \cdot t_R}\right) - \frac{I_A}{s} e^{-s \cdot t_S} \tag{7}$$

where I_A is the specified pulse amplitude, t_R is the time instant when the amplitude of the current packet reaches I_A, and t_S is the time instant when the current amplitude returns to zero. Substituting (7) into (3) and applying the inverse Laplace transform, the crosstalk current before t_S is

$$\begin{aligned} I_C(t)|_{t<t_S} = {} & \frac{I_A}{t_R} \cdot \frac{C_P}{C_{S_A}} \left[(\tau_1 - \tau_2)\left(1 - e^{-t/\tau_2}\right) + t\right] \\ & - u(t - t_R) \cdot \frac{I_A}{t_R} \cdot \frac{C_P}{C_{S_A}} \\ & \times \left[(\tau_1 - \tau_2)\left(1 - e^{-(t - t_R)/\tau_2}\right) + (t - t_R)\right]. \end{aligned} \tag{8}$$

The last expression in (7) has been ignored in deriving (8) since SW_{1_A}, SW_{4_A}, SW_{1_B}, and SW_{4_B} turn off at t_S, hence the circuit model in Fig. 9(c) is no longer valid after t_S.

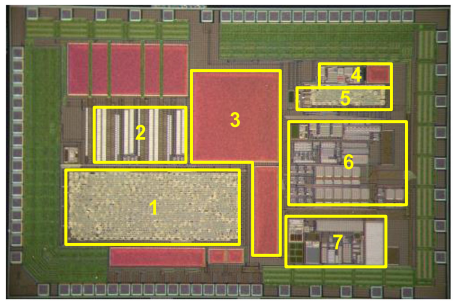


Fig. 10. Microphotograph of the high-frequency power-isolated stimulator ASIC: (1) stimulation management in two supply and control modules; (2) power and control switches in two supply and control modules; (3) storage capacitor for the stimulator module; (4) monostable multivibrator; (5) pulse control logic; (6) current source and output stage; (7) voltage regulator.

TABLE I
ASIC FEATURES AND PERFORMANCE

Technology	X-FAB 0.6-μm HV CMOS
Die size	10 mm^2
Supply voltage	*VDDH*: 12 V
	VDD: 5 V
Stimulation parameters:	
Stimulation type	Biphasic, chopped
Stimulation current	≤ 1 mA
Pulse rate	1–1000 pps
Pulse interval resolution	2 μs
Pulse duration (the total	Cathodic phase: 0–500 μs,
length of a packet series)	Anodic phase: 1–8 times cathodic duration
Current packet width	2 μs
Current packet interval	2–8 μs
Current consumption	4.18 mA*

* dc current measured from *VDDH* on the power and control module, with one stimulator module generating 1 mA biphasic pulses at the pulse rate of 1000 pps, a current packet width of 2 μs and 200 μs per phase.

Equation (8) shows that minimizing the capacitive coupling between the grounds of the stimulator modules and to master ground is critical for the channel isolation. For example, using the electrode model in Fig. 9(b), and having the blocking capacitor $C_{A2} = C_{B2} = 200$ nF, for a current packet of $I_A = 1$ mA, $t_R = 1.18\,\mu$s and $t_S = 2\,\mu$s, a C_P smaller than 2.1 pF is required to achieve a peak amplitude of I_C below 1% of I_A.

IV. IN-VITRO MEASUREMENTS

The stimulator ASIC was implemented in the X-FAB 0.6-μm HV CMOS technology. Fig. 10 shows the microphotograph of the ASIC with the building blocks labeled. The ASIC comprises two parallel power and control modules and one stimulator module. The area of the ASIC is 10 mm^2. Table I lists some of the features and measured performance of the ASIC.

A. Test Setup

The setup for *in-vitro* benchtop tests is shown in Fig. 11. Since the power and control modules and the stimulator modules should have separate substrates, three ASICs were used

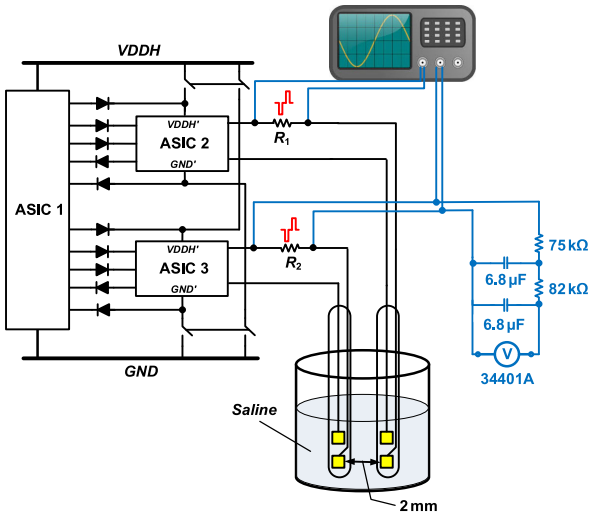


Fig. 11. Setup for *in-vitro* benchtop tests. A two-pole low-pass filter is also shown, which can be temporarily connected across one of the sensing resistors for measuring the average dc current error.

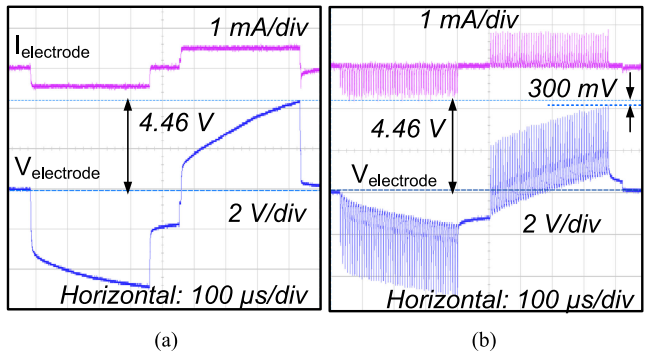


Fig. 12. Oscillograms showing current and voltage potential on electrodes in saline solution with an electrode impedance of 3 kΩ at 1 kHz with (a) conventional biphasic pulse, 500 μA, 180 μs per phase, (b) chopped biphasic pulse, 1 mA, 180 μs per phase, 2 μs packet width and 2 μs packet interval.

in the setup, where the power and control module in ASIC 1, as well as the isolation switches, are connected to the stimulator modules in ASIC 2 and ASIC 3 via discrete Schottky diodes. ASIC 2 and ASIC 3 drive two electrode arrays. The two arrays were placed at a 2 mm separation in saline solution with a conductivity of 16.4 mS/cm. On each ASIC, a 1 kΩ current sensing resistor was connected in series between the electrode array and the anode electrode port (see Fig. 3) on the stimulator module. The voltage across the sensing resistor was measured with differential probes (TA044, Pico Technology) and an oscilloscope (DSO-X 2024A, Keysight Technologies). *VDDH*′ and *GND*′ of ASIC 2 and ASIC 3 could also be switched to the master power supply *VDDH* and *GND* to override the isolation, in order to compare the isolation performance with non-isolated stimulation. To measure the average dc current error, a two-pole low-pass filter was connected to one of the sensing resistors and the dc voltage after filtering was measured with a digital multimeter (34401A, Keysight Technologies).

B. Charge Integration

ASIC 2 was programmed to generate both conventional biphasic pulses and chopped pulses, separately, while ASIC 3 stayed idle. The current pulses and the voltage potential on the electrodes in saline were recorded, as shown in Fig. 12. The conventional pulse has a current amplitude of 500 μA and a pulse width of 200 μs per phase, with a 50 μs inter-phase delay. The chopped pulse was set to have the same amount of total charge per phase as the conventional pulse, with either phase consisting of 50 current packets at a width of 2 μs, an interval 2 μs and current amplitude doubled to 1 mA. As shown in Fig. 12(b), the electrode potential from the chopped pulse rises and falls at every current packet as a result of the resistive components in the electrode-electrolyte interface, but its envelope is at a level close to the electrode potential in Fig. 12(a) from the conventional pulse. It indicates the charges from the packets are integrated by the capacitive components in the electrode-electrolyte interface. The peak electrode voltage from the chopped pulses in Fig. 12(b) is 300 mV lower than the voltage from the conventional pulses. This loss is due to the finite rise time of each current packet, as shown in Fig. 7(c).

C. Crosstalk Reduction

To measure the effectiveness of crosstalk reduction due to power isolation, two sets of tests were conducted: ASIC 2 and ASIC 3 delivering conventional pulses without power isolation, and chopped pulses with isolation. The results are shown in Fig. 13. Fig. 13(a) shows the two ASICs generating conventional charge-balanced asymmetrical biphasic pulses. The collapse in the cathodic phase in both pulses is evident where the two pulses overlap. The cathodic phase from ASIC 2 has three segments. The current level in the first segment exceeds the expected value due to incoming crosstalk current from ASIC 3, while the current level on ASIC 3 drops as part of the current from the cathode on ASIC 3 flows to the anode on ASIC 2. The magnitude of the drop in amplitude, as shown in Fig. 13(a), is 467 μA, which is 58.36% of the expected current amplitude of 800 μA. The second segment of the cathodic phase on ASIC 2 is normal during the inter-phase delay on ASIC 3, but the third segment has a much lower current level suggesting crosstalk current from the cathode on ASIC 2 to the cathode on ASIC 3. Since the sensing resistors are connected to the anode ports, the distortion on the anodic phase is not shown.

Fig. 13(b) shows the measured voltage on the electrodes under the condition in Fig. 13(a). The distortion due to crosstalk is evident. Fig. 13(c) shows the measured current pulses in the high-frequency power-isolated stimulation mode. The detailed view in Fig. 13(d) shows that the current packets from the two ASICs are concurrent, but it is evident that the crosstalk has been reduced. When the current packets occur simultaneously, the drop in the current amplitude has been significantly reduced to 32.5 μA, 4.06% of the desired amplitude of 800 μA. This drop in amplitude may be due to crosstalk current resulted from capacitive coupling. Simulation shows $C_{SGND\_A} = C_{SGND\_B} = 2$ pF, while the measured parasitic

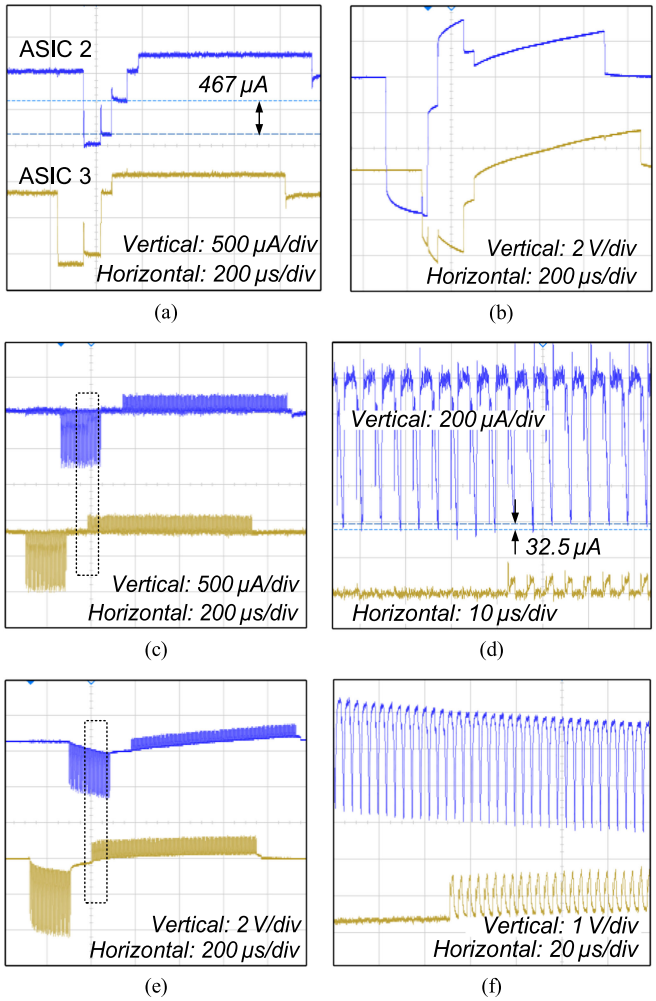


Fig. 13. Oscillograms showing current pulses on the two electrode arrays in saline solution: (a) two conventional biphasic pulses without power isolation; (b) electrode voltage at the condition in (a); (c) two chopped biphasic pulses with power isolation; (d) details of the current packets inside the dotted box in (c); (e) electrode voltage at the condition in (c); (f) details of the electrode voltage inside the dotted box in (e).

capacitance between the ground planes *GND′_A* and *GND′_B* on the printed circuit board used in the test setup is 6.4 pF. With measured $t_R = 1.1\ \mu$s, $t_S = 1.4\ \mu$s, and the electrode modeled with the values in Fig. 9(b), the peak crosstalk current calculated using (8) is 30.1 μA, 3.78% of the desired 800 μA, close to the measured result. The crosstalk current was also measured with I_A set to 200 μA, 400 μA, 600 μA and 1 mA. The crosstalk current was between 3.72% and 4.75% of I_A. Fig. 13(e), (f) show the measured electrode voltage under the condition in Fig. 13(c).

D. Stimulation Control

The measured control signals, *Stim_CLK* and *Stim_Data*, for generating a chopped biphasic pulse on ASIC 2 are shown in Fig. 14 together with the current measured on the sensing resistor, $I_{\text{electrode}}$. Before the cathodic phase, there are 49 pulses on *Stim_CLK* to reset the pulse control logic in the stimulator module. Once the pulse starts, there are *Stim_CLK* pulses at the

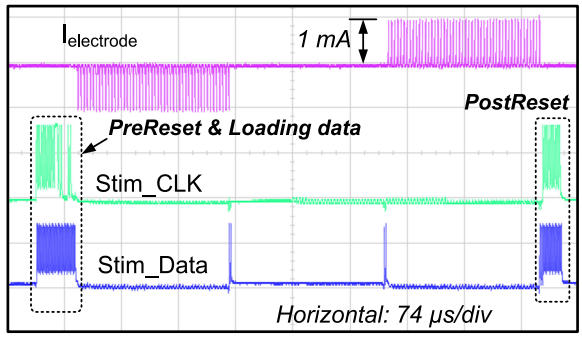


Fig. 14. Oscillograms showing the control signals on *Stim_CLK* and *Stim_Data* for generating a chopped biphasic pulse, also shown.

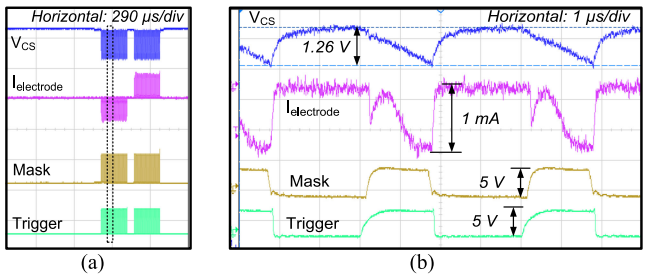


Fig. 15. Oscillograms showing the measured supply and control signals during a chopped biphasic pulse: (a) the supply voltage across the storage capacitor, V_{CS}, during the chopped biphasic pulse, $I_{\text{electrode}}$, as well as the *Trigger* and *Mask* signals for generating the current packets; (b) details inside the dotted box in (a).

beginning and end of both the cathodic and anodic phases to operate the switches in the output stage. After the anodic phase of the current packet series, there are 25 *Stim_CLK* pulses to reset the output stage to the mode for electrode isolation and passive discharging.

The measured voltage V_{CS} across the storage capacitor on ASIC 2, and the input and output signals from the monostable multivibrator, *Trigger* and *Mask*, are shown in Fig. 15 alongside the current from the ASIC. In the detailed view in Fig. 15(b), *Trigger* is repeatedly pulled up for 2 μs by turning off switch S_T that is synchronized to the power isolation switches. A positive pulse on *Mask* is generated by the monostable multivibrator each time *Trigger* goes high. This pulse turns on the current source and the output stage to allow 1 mA current packet to go through the sensing resistor. Since the stimulator module is supplied by the storage capacitor during this period, V_{CS} starts falling until *Trigger* goes low again when the power switches are turned on to reconnect the stimulator module to the system power supply. At the point of reconnection, V_{CS} dropped by 1.26 V.

E. Pulse Modulation

Fig. 16 shows chopped biphasic pulses from ASIC 2 and ASIC 3 modulated with different pulse modulation schemes. On ASIC 2, 4.2 Hz sinusoidal amplitude modulation was applied to 250 Hz pulses with a base amplitude of 75 μA, while on ASIC 3, 4.2 Hz sinusoidal frequency modulation was applied to 100 μA pulses with a based pulse rate of 200 Hz.

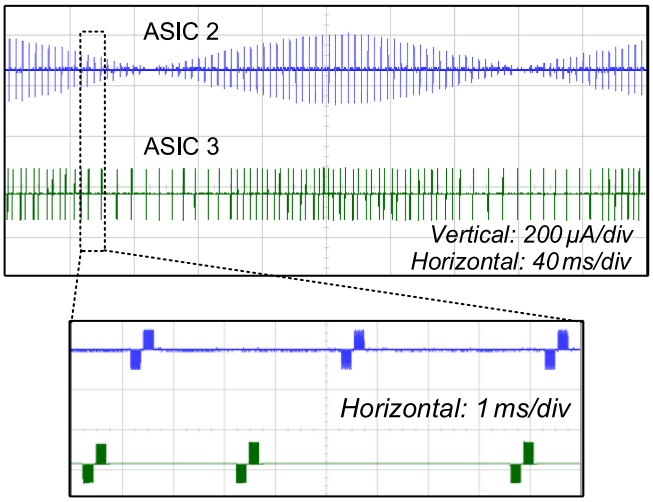


Fig. 16. Oscillograms showing pulses on ASIC 2 and ASIC 3 modulated in different formats, where 4.2 Hz pulse amplitude modulation was applied to ASIC 2 and 4.2 Hz pulse phase modulation to ASIC 3. Details in the dotted box show the pulses from the two ASICs are chopped biphasic pulse.

F. Charge Balance

To evaluate the charge balance the average dc current error and residual charge error were measured. Average dc current error was calculated from the measured dc voltage on the current sensing resistor after 2-pole filtering, as illustrated in Fig. 11 [29]. In the test, ASIC 2 was set to generate 1 mA chopped pulses at 1000 pps (pulse per second), with 100 current packets in each phase, and a 50 μs inter-phase delay. Both the packet width and packet interval were 2 μs. After continuous generation of pulses over 1 million cycles, the measured dc voltage on a 2 kΩ current sensing resistor was 11 μV, suggesting a residual dc current of 5.5 nA, below the safety limit in neural implants of 25 nA [31].

Residual charge error was measured by connecting a 2 kΩ resistor and a 100 nF capacitor in series as a RC load to the stimulator, and measuring the dc voltage across the load over 600,000 pulse cycles at a pulse rate of 500 pps. The normalized charge error per phase was calculated following the procedure in [32], where the measured dc voltage was averaged into each cycle and then multiplied by the capacitor value in the RC load. The normalized charge errors at different total charge per phase are plotted in Fig. 17.

G. Discussion

Comparison between the prototype stimulator and state-of-the-art integrated stimulators with crosstalk reduction is shown in Table II. Compared to other designs, the proposed high-frequency power-isolated stimulator has the following advantages:

1) Supports fully independent operation on multiple channels, where the timing of stimulating pulses on each channel is independent of other channels, unlike the interleaving methods in [15], [24].

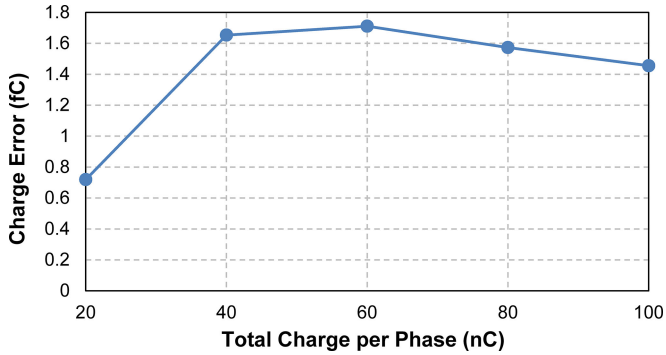


Fig. 17. Normalized charge error per pulse against the total charge per phase in a chopped pulse, measured from a dummy RC load.

2) Enables fully integrated design without requiring external components for isolation (assuming implementation on SOI technology).
3) Requires only two electrodes per channel, unlike the current steering methods in [19], [20] where multiple return electrodes are needed for current focusing, hence is less demanding on the physical volume.
4) Allows precise control of both pulse amplitude and frequency, hence providing full flexibility in the design of neural modulation protocols.

The costs of achieving fully-integrated power isolation are the extra power consumed by the fast switching activity, and the area increase for the additional storage capacitor and the isolation switches. The dc current on *VDDH* was measured when generating chopped pulses at 500 pps with each current packet lasting 2 μs and a full cathodic/anodic phase lasting 200 μs, at five different current amplitudes of 200 μA, 400 μA, 600 μA, 800 μA and 1 mA. The values of the dc current were compared to the dc current when generating conventional biphasic pulses at the same pulse rate and the same total charge per phase. As shown in Fig. 18, in all the five scenarios, the dc current for generating the chopped pulse increased by about 300 μA. In future developments the power efficiency can be improved by, for example, implementing the design in an advanced technology with a lower digital supply voltage, hence reducing the current consumption due to switching, and applying dynamic supply voltage control to the stimulator output stage to reduce the redundant voltage headroom on the electrodes [33]–[35]. The area increase is mainly from the storage capacitor and the power switches, which occupy 1.27 mm^2 and 0.81 mm^2 respectively. This area can be further reduced by using an advanced technology with smaller gate sizes, and improving the switching speed of the stimulator to achieve shorter duration of the current packet, and hence smaller storage capacitors.

V. In-Vivo Testing

The physiological effectiveness of stimulating with biphasic pulses consisting of a series of high-frequency current packets was investigated *in-vivo* by stimulating the vestibular nerve of a male adult guinea pig and recording the evoked VOR. A double-sided electrode array [36] was implanted into the lateral canal

TABLE II
COMPARISON OF INTEGRATED STIMULATORS FEATURING CROSSTALK REDUCTION

Parameter	[15]	[19]	[20]	[21]	[24]	[26]	[27]	This Work
Technology	0.35 µm	0.5 µm	0.35 µm	0.6 µm	3 µm	0.18 µm	0.18 µm	**0.6 µm**
Supply voltage	10 V	12 V	up to 20 V	12 V	12 V	20 V	5 V	**12 V**
Maximum stimulation current	735 µA	1.45 mA	4.03 mA	1 mA	2 mA	10 mA	190 nC [1)]	**1 mA**
Stimulus type	Conventional biphasic	Conventional biphasic	Conventional biphasic	Conventional biphasic	Chopped pulse	Chopped pulse	Chopped pulse	**Chopped pulse**
Crosstalk reduction method	Pulse interleaving	Current steering	Current steering	Power isolation	Pulse interleaving	Pulse interleaving	Pulse interleaving	**Power isolation**
Stimulation mode	Monopolar	Multipolar	Multipolar	Bipolar/ Multipolar	Monopolar	Arbitrary	Bipolar	**Bipolar/ multipolar**
No. of electrodes per channel	2 [2)]	4	7	2	2 [2)]	2	2	**2**
Simultaneous multichannel stimulation supported?	No	No	Yes	Yes	No	No	No [3)]	**Yes**
Supported pulse modulation methods [4)]	PAM	PAM and PFM	PAM	PAM and PFM	PAM	PFM	PFM	**PAM and PFM**
No external component required? [5)]	Yes	Yes	Yes	No [6)]	Yes	No	Yes	**Yes [6)]**

[1)] Maximum charge; [2)] Shared remote return electrode; [3)] Could also be used as power isolation for simultaneous stimulation;
[4)] PAM: Pulse amplitude modulation; PFM: Pulse frequency modulation; [5)] Not including blocking capacitors; [6)] When implemented on SOI technology.

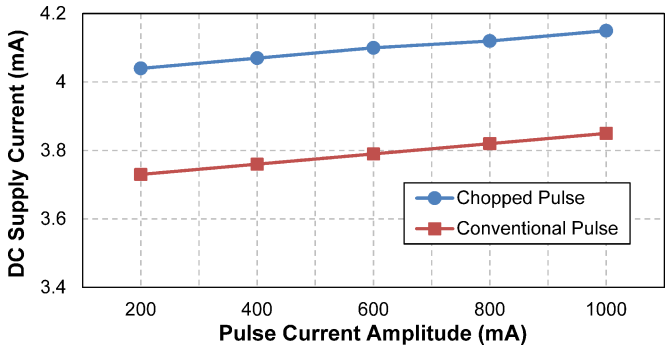


Fig. 18. Measured dc supply current for both the chopped pulse stimulation and conventional non-isolated stimulation at the same stimulation settings.

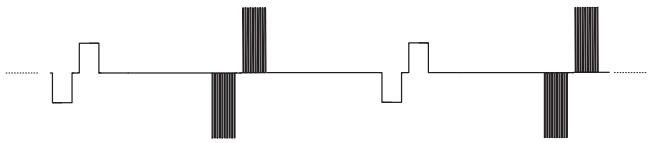


Fig. 19. Profile of pulse trains used for testing the VOR to individual biphasic pulses.

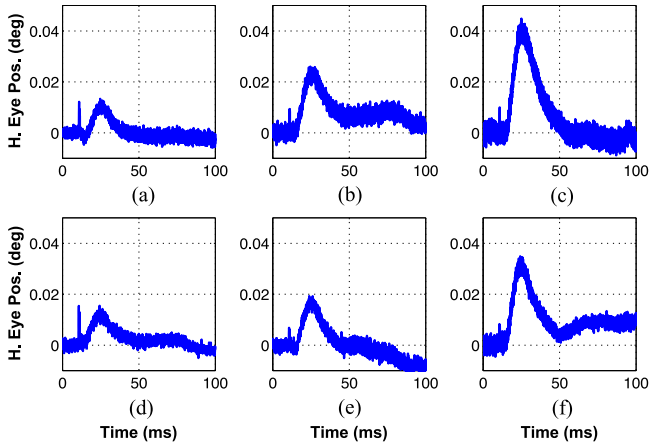


Fig. 20. Recorded horizontal eye position by individual biphasic pulses: (a) conventional pulse in Session 1; (b) conventional pulse in Session 2; (c) conventional pulse in Session 3; (d) chopped pulse in Session 1; (e) chopped pulse in Session 2; and (f) chopped pulse in Session 3.

in the rodent's left ear and a remote electrode was inserted into the neck muscle. The *in-vivo* preparation was similar to [37].

Horizontal eye positions evoked by both the high-frequency chopped pulses and the conventional stimulating pulses were recorded to compare the stimulation effect. The profile of the pulse trains used is shown in Fig. 19. Symmetrical conventional biphasic pulses and chopped pulses were interleaved in a back-to-back fashion with an interval of one second to minimize the difference in eye positions caused by variation of the rodent's physical condition and other environmental factors. The chopped pulses were arranged so that the width of the cathodic and anodic phases, as well as the inter-phase delay, were equal to the conventional biphasic pulse, and the amplitude of the current packets was increased accordingly to make the total charge in a biphasic chopped pulse equal to the charge in the conventional pulse. Each test session lasted for 62 seconds. The recorded eye positions were averaged from responses evoked by 31 conventional pulses and 31 chopped pulses. Fig. 20 shows the horizontal eye positions recorded from three test sessions. The pulse profiles used in the three sessions are summarized in Table III.

The recorded eye positions in Fig. 20 suggested that: 1) despite containing the same amount of charge, the conventional pulses with pulses having higher amplitude but shorter width evoked more significant eye movement; 2) a similar pattern was also shown with the chopped pulses, where pulses with

TABLE III
PULSE PROFILES FOR VOR TO INDIVIDUAL PULSES

	Session 1	Session 2	Session 3
Conventional Pulse			
Amplitude	20 μA	40 μA	80 μA
Width per phase	192 μs	96 μs	48 μs
Total charge per phase	3.84 nC	3.84 nC	3.84 nC
Chopped Pulse			
Amplitude	60 μA	120 μA	240 μA
Packet width	2 μs	2 μs	2 μs
Packet interval	4 μs	4 μs	4 μs
Total no. of packets per phase	32	16	8
Total charge per phase	3.84 nC	3.84 nC	3.84 nC

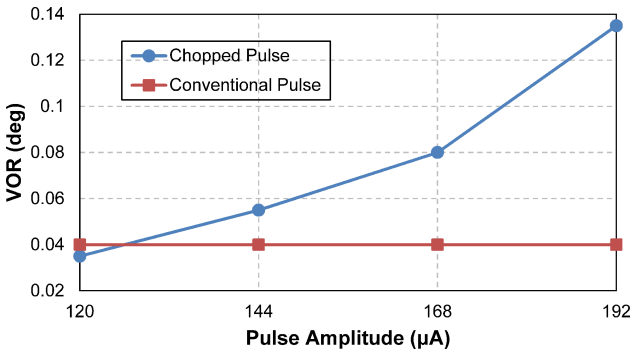


Fig. 21. Measured VOR against the pulse amplitude resulted from both the chopped pulse stimulation and conventional pulse stimulation schemes. The amplitude of the conventional pulse was fixed at 40 μA.

higher amplitude but fewer packets evoked more significant eye movement; 3) the averaged peak eye movement evoked by the chopped pulses, in each session, was less than that by the conventional pulses. This could be due to small charge loss during the packet interval, and/or the factor that the slow turn-on time of the current source reduced the actual amount of charge per packet from the expected level, as also shown in Fig. 12(b).

The VOR response to both conventional pulses and chopped pulses suggests that the chopped pulses have similar physiological efficacy for stimulation to the conventional biphasic pulses with the same amount of charge, while slightly less magnitude of evoked response was also observed. These results agree with the study of auditory nerve stimulation reported in [22].

Fig. 21 shows the recorded VOR response to both conventional and chopped pulses where the pulse parameters for the conventional pulses remained constant at 40 μA and 192 μs per phase, while the chopped pulses provided 19 μs per phase containing 32 current packets of 2 μs and 4 μs between packets. The amplitude of the packets was varied from 120 μA to 192 μA at a step size of 24 μA. At a packet amplitude of 120 μA, the total charge per phase in the chopped pulses equals that of the conventional pulse. However, the VOR response to the chopped pulse, according to Fig. 21, was slightly lower than the response to the conventional pulse, suggesting a charge loss. By increasing the current amplitude by 24 μA, the loss was over compensated, as shown in the figure. The recorded VOR continued rising with the increase of current amplitude of the chopped pulses.

VI. CONCLUSION

This paper has presented the design of high-frequency power-isolated stimulation for multichannel stimulation with minimal channel interference. The stimulator generates biphasic chopped pulses, where each phase consists of a series of high-frequency current packets with a short interval between them. Power isolation is applied to the stimulator during each current packet so that the stimulator on each channel is isolated from other channels and is supplied by an on-chip storage capacitor. This isolation effectively prevents the current crosstalk between stimulation channels caused when using a common power supply shared by all the stimulation channels. A prototype ASIC has been fabricated and tested. The performance of crosstalk reduction has been demonstrated *in-vitro*. Crosstalk was reduced from 58.36% to 4.06% with the prototype ASIC. Analysis of the crosstalk suggests that it could be further reduced by strategic layout design of the test setup. In addition, the physiological efficacy of stimulating with biphasic chopped pulses has been proven *in-vivo* for vestibular stimulation.

As a proof-of-concept, this stimulator is a step forward from the design presented in [21] towards a fully-integrated multichannel, power-isolated stimulator system. Compared with the state-of-the-art techniques for reducing channel interference, this design is more compact in physical volume, and also provides full independence to each stimulation channel. Future improvements may involve reducing capacitance coupling due to the parasitic capacitance between the isolated modules, a faster current source to allow shorter current packets, hence smaller size storage capacitors, and implementation in SOI technology so that all the stimulator modules, control and supply modules and the diodes in series with the isolation switches can be integrated onto a single chip.

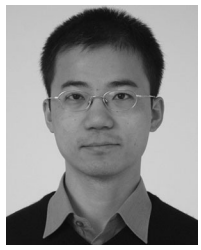
ACKNOWLEDGMENT

The authors would like to thank Prof. D. M. Merfeld and Dr. W. Gong at the Massachusetts Eye and Ear for their help with the *in vivo* study.

REFERENCES

[1] F. Zeng, S. Rebscher, W. Harrison, X. Sun, and H. Feng, "Cochlear implants: System design, integration, and evaluation," *IEEE Rev. Biomed. Eng.*, vol. 1, pp. 115–142, Nov. 2008.
[2] B. Wilson and M. Dorman, "Interfacing sensors with the nervous system: Lessons from the development and success of the cochlear implant," *IEEE Sens. J.*, vol. 8, no. 1, pp. 131–147, Jan. 2008.
[3] M. Ortmanns, A. Rocke, M. Gehrke, and H. Tiedtke, "A 232-channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007.
[4] J. Weiland, W. Liu, and M. Humayun, "Retinal prosthesis," *Annu. Rev. Biomed. Eng.*, vol. 7, pp. 361–401, Aug. 2005.
[5] W. Gong and D. Merfeld, "A prototype neural semicircular canal prosthesis using patterned electrical stimulation," *Ann. Biomed. Eng.*, vol. 28, no. 5, pp. 572–581, May 2000.
[6] C. Della Santina, A. Migliaccio, and A. Patel, "A multichannel semicircular canal neural prosthesis using electrical stimulation to restore 3-D vestibular sensation," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 6, pp. 1016–1030, Jun. 2007.
[7] V. Giagka, C. Eder, N. Donaldson, and A. Demosthenous, "An implantable versatile electrode-driving ASIC for chronic epidural stimulation in rats," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 3, pp. 387–400, Jun. 2015.

[8] D. Chew *et al.*, "A microchannel neuroprosthesis for bladder control after spinal cord Injury in rat," *Sci. Transl. Med.*, vol. 5, no. 210, Nov. 2013, Art. no. 210ra155.
[9] S. Raspopovic *et al.*, "Restoring natural sensory feedback in real-time bidirectional hand prostheses," *Sci. Transl. Med.*, vol. 6, no. 222, Feb. 2014, Art. no. 222ra19.
[10] A. Cutrone *et al.*, "A three-dimensional self-opening intraneural peripheral interface (SELINE)," *J. Neural Eng.*, vol. 12, no. 1, Feb. 2015, Art. no. 016016.
[11] H. Lancashire *et al.*, "Microchannel neural interface manufacture by stacking silicone and metal foil laminae," *J. Neural Eng.*, vol. 13, no. 3, Jun. 2016, Art. no. 034001.
[12] X. Liu, A. Demosthenous, A. Vanhoestenberghe, D. Jiang, and N. Donaldson, "Active Books: The design of an implantable stimulator that minimizes cable count using integrated circuits very close to electrodes," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 216–227, Jun. 2012.
[13] X. Liu, Z. Zong, D. Jiang, B. Bougaila, N. Donaldson, and A. Demosthenous, "Advances in scalable implantable systems for neurostimulation using networked ASICs," *IEEE Des. Test*, vol. 33, no. 4, pp. 8–23, Aug. 2016.
[14] B. Wilson, C. Finley, D. Lawson, R. Wolford, and M. Zerbi, "Design and evaluation of a continuous interleaved sampling (CIS) processing strategy for multichannel cochlear implants," *J. Rehabil. Res. Develop.*, vol. 30, no. 1, pp. 110–116, 1993.
[15] T. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 106–113, Jun. 2008.
[16] N. Davidovics, G. Fridman, and C. Della Santina, "Co-modulation of stimulus rate and current from elevated baselines expands head motion encoding range of the vestibular prosthesis," *Exp. Brain Res.*, vol. 218, no. 3, pp. 389–400, May 2012.
[17] Y. Lu, Y. Yan, X. Chai, Q. Ren, Y. Chen, and L. Li, "Electrical stimulation with a penetrating optic nerve electrode array elicits visuotopic cortical responses in cats," *J. Neural Eng.*, vol. 10, no. 3, Jun. 2013, Art. no. 036022.
[18] B. Chiang, G. Fridman, C. Dai, M. Rahman, and C. Della Santina, "Design and performance of a multichannel vestibular prosthesis," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 19, no. 5, pp. 588–598, Oct. 2011.
[19] K. N. Hageman, Z. K. Kalayjian, F. Tejada, B. Chiang, M. A. Rahman, and G. Y. Fridman, "A CMOS neural interface for a multichannel vestibular prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 269–279, Apr. 2016.
[20] Y. Wong *et al.*, "Retinal neurostimulator for a multifocal vision prosthesis," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 15, no. 3, pp. 425–434, Sep. 2017.
[21] D. Jiang, D. Cirmirakis, and A. Demosthenous, "A vestibular prosthesis with highly-isolated parallel multichannel stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 124–137, Feb. 2015.
[22] R. Shepherd and E. Javel, "Electrical stimulation of the auditory nerve: II. Effect of stimulus waveshape on single fibre response properties," *Hearing Res.*, vol. 130, nos. 1/2, pp. 171–188, Apr. 1999.
[23] M. van Dongen, F. Hoebeek, S. Koekkoek, C. De Zeeuw, and W. Serdijn, "High frequency switched-mode stimulation can evoke post synaptic responses in cerebellar principal neurons," *Frontiers Neuroeng.*, vol. 8, Mar. 2015, doi: 10.3389/fneng.2015.00002.
[24] H. McDermott, "A custom-designed receiver-stimulator chip for an advanced multiple-channel hearing prosthesis," *IEEE J. Solid-State Circuits*, vol. 26, no. 8, pp. 1161–1164, Aug. 1991.
[25] H. McDermott, "An advanced multiple channel cochlear implant," *IEEE Trans. Biomed. Eng.*, vol. 36, no. 7, pp. 789–797, Jul. 1989.
[26] M. van Dongen and W. Serdijn, "A power-efficient multichannel neural stimulator using high-frequency pulsed excitation from an unfiltered dynamic supply," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 61–71, Feb. 2016.
[27] W. Y. Hsu and A. Schmid, "Compact, energy-efficient high-frequency switched capacitor neural stimulator with active charge balancing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 878–888, Aug. 2017.
[28] D. Jiang, D. Cirmirakis, M. Schormans, T. Perkins, N. Donaldson, and A. Demosthenous, "An integrated passive phase-shift keying modulator for biomedical implants with power telemetry over a single inductive link," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 64–77, Feb. 2017.
[29] D. Jiang, A. Demosthenous, T. Perkins, X. Liu, and N. Donaldson, "A stimulator ASIC featuring versatile management for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 2, pp. 147–159, Apr. 2011.
[30] XFAB, Process Specification XC06 - 0.6 μm Modular CMOS Process, Release 4.0, Jul. 2009.
[31] J. Sit and R. Sarpeshkar, "A low-power, blocking-capacitor-free, charge-balanced electrode-stimulator chip with less than 6nA DC error for 1 mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, Sep. 2007.
[32] S. Nag, X. Jia, N. V. Thakor, and D. Sharma, "Flexible charge balanced stimulator with 5.6 fC accuracy for 140 nC injections," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 266–275, Jun. 2013.
[33] S. Kelly and J. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 20–29, Jan. 2011.
[34] S. Arfin and R. Sarpeshkar, "An energy-efficient adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 1–14, Feb. 2012.
[35] I. Williams and T. Constandinou, "An energy-efficient dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 129–139, Apr. 2013.
[36] W. Poppendieck *et al.*, "Development, manufacturing and application of double-sided flexible implantable microelectrodes," *Biomed. Microdevices*, vol. 16, no. 6, pp. 837–850, Dec. 2014.
[37] D. Merfeld, W. Gong, J. Morrissey, M. Saginaw, C. Haburcakova, and R. Lewis, "Acclimation to chronic constant-rate peripheral stimulation provided by a vestibular prosthesis," *IEEE Trans. Biomed. Eng.*, vol. 53, no. 11, pp. 2362–2372, Nov. 2006.



Dai Jiang (S'07–M'09) received the B.Sc. and M.Sc. degrees from Beijing University of Aeronautics and Astronautics, Beijing, China, in 1998 and 2001, respectively, and the Ph.D. degree from University College London (UCL), London, U.K., in 2009. His Ph.D. work was on frequency synthesis. He was with Datang Telecom Group, China, from 2001 to 2002, working on developing FPGA functions for WCDMA signal processing. From 2006 to 2008, he was a Research Assistant, and since 2009 a Postdoctoral Research Associate, both with the Analog and Biomedical Electronics Group, UCL. His research interests include CMOS analog and mixed-signal integrated circuit design for biomedical applications.

Dr. Jiang is a member of the Biomedical and Life Science Circuits and Systems of the IEEE Circuits and Systems Society.

Andreas Demosthenous (S'94–M'99–SM'05–F'18) received the B.Eng. degree in electrical and electronic engineering from the University of Leicester, Leicester, U.K., in 1992, the M.Sc. degree in telecommunications technology from Aston University, Birmingham, U.K., in 1994, and the Ph.D. degree in electronic and electrical engineering from the University College London (UCL), London, U.K., in 1998. He is a Professor with the Department of Electronic and Electrical Engineering, UCL, and leads the Analog and Biomedical Electronics Group. His research interests include analog and mixed-signal integrated circuits for biomedical, sensor, and signal processing applications. He has made outstanding contributions to improving safety and performance in integrated circuit design for active medical devices, such as spinal cord and brain stimulators. He has authored more than 300 articles in journals and international conference proceedings, several book chapters, and holds several patents.

Dr. Demosthenous is currently the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and serves on the International Advisory Board of Physiological Measurement. He is a member of the Technical Programme Committee of several IEEE conferences, including the European Solid-State Circuits Conference and the International Symposium on Circuits and Systems. He is a Fellow of the Institution of Engineering and Technology and a Chartered Engineer.