An Analogue Front-End Model for Developing Neural Spike Sorting Systems

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***Abstract*—In spike sorting systems, front-end electronics is a crucial pre-processing step that not only has a direct impact on detection and sorting accuracy, but also on power and silicon area. In this work, a behavioural front-end model is proposed to assess the impact of the design parameters (including signal-to-noise ratio, filter type/order, bandwidth, converter resolution/rate) on subsequent spike processing. Initial validation of the model is provided by applying a test stimulus to a hardware platform and comparing the measured circuit response to the expected from the behavioural model. Our model is then used to demonstrate the effect of the Analogue Front-End (AFE) on subsequent spike processing by testing established spike detection and sorting methods on a selection of systems reported in the literature. It is revealed that although these designs have a wide variation in design parameters (and thus also circuit complexity), the ultimate impact on spike processing performance is relatively low (10–15%). This can be used to inform the design of future systems to have an efficient AFE whilst also maintaining good processing performance.**

***Index Terms*—Analogue Front-End (AFE), Brain-Machine Interfaces (BMI), neural interface, spike detection, spike sorting.**

I. Introduction

UNDERSTANDING how the action potentials propagating through billions of neurons in the brain produce our thoughts, perceptions, and actions is one of the greatest challenges of 21st century science. The ability to interface to these neurons using electronics is presenting new opportunities for neural rehabilitation with prosthetic devices. For example, sensory cochlear implants, are already impacting the quality of life of around 300,000 individuals with profound deafness [1]. More recently, owing to the developments in robotics, neuroscience and microelectronics, emerging motor prosthetics have already demonstrated that mobility, lost due to spinal cord injury or neural diseases, could be restored [2].

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Experimental recording of large numbers of neurons is thus an extremely important task, but one that requires overcoming several technical challenges. Recent years have seen the development of micro-fabricated neural probes such as the Utah and Michigan arrays, now commonplace in experimental labs, and likely soon in clinical applications such as brain-machine interfaces for paralysis [3], [4]. For any portable or implantable device, such probes require miniature electronics locally to amplify the weak neural signals, filter out noise and out-of-band interference, and digitise for transmission. With recent advances in modern semiconductor technology, this is now possible and has sparked significant research activity in the community, particularly in this last decade [5]–[19].

The specifics of the electrode material, the electrode/tissue interface as well as the nature of the bio-potential signal itself pose challenges on the front-end microelectronics [20]. The signals observed contain an electrode offset potential (due to the electrode-electrolyte interface) as well as both the extracellular action potentials (EAPs) and local field potentials (LFPs). The EAPs typically have amplitudes of 25 μV-1 mV and are recorded with a signal band of 300 Hz-5 kHz, whereas the LFPs have amplitudes up to 10 mV recorded with a signal band of 1–300 Hz [21]. Additionally, the electrode-electrolyte interface introduces an offset that can be several hundreds of millivolts, with the micro-electrodes themselves contributing thermal noise due to their relatively high impedance. All these factors dictate the minimum requirements for the front-end electronics, that are additionally limited by resource constraints (power, size and bandwidth). In particular, the desire to make such systems implantable poses limits on size and thermal dissipation (i.e., to prevent tissue damage) [22], as well as requiring wireless transmission (i.e., thus limiting communication channel capacity) [23], [24].

Following the front-end processing, spike sorting is a technique commonly used on EAP recordings to separate the signal into spike patterns of individual units (i.e., neurons) [25]. This is based on the fact that the dynamics of each neuron varies, in addition to the topological placement of the micro-electrodes (i.e., in orientation and proximity) [26]. This results in each neuron having a slightly different spike profile when observed at the electrode that can be identified by means of feature extraction followed by clustering. There exists numerous methods for achieving feature extraction (e.g. templates, peaks, derivatives, wavelets, principle component analysis) [25], [27], and clustering (e.g. valley detection, k-means, expectation maximisation, super-paramagnetic clustering) [25].

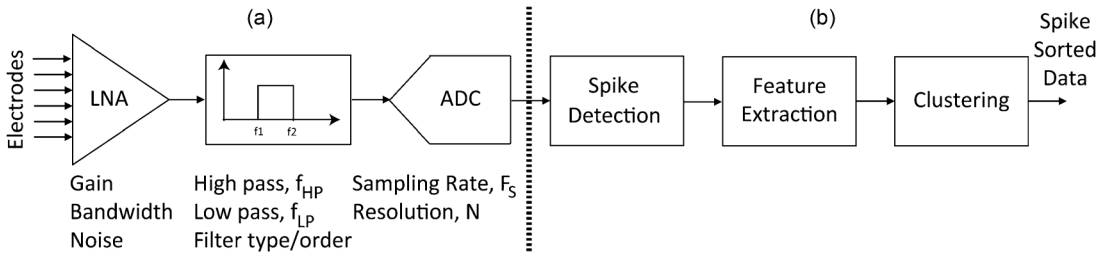

Fig. 1. General architecture of a neural interface. (a) Analogue Front-End (AFE), consisting of a low noise amplifier (LNA), filter and analog-to-digital converter (ADC). (b) Back-end spike processing.

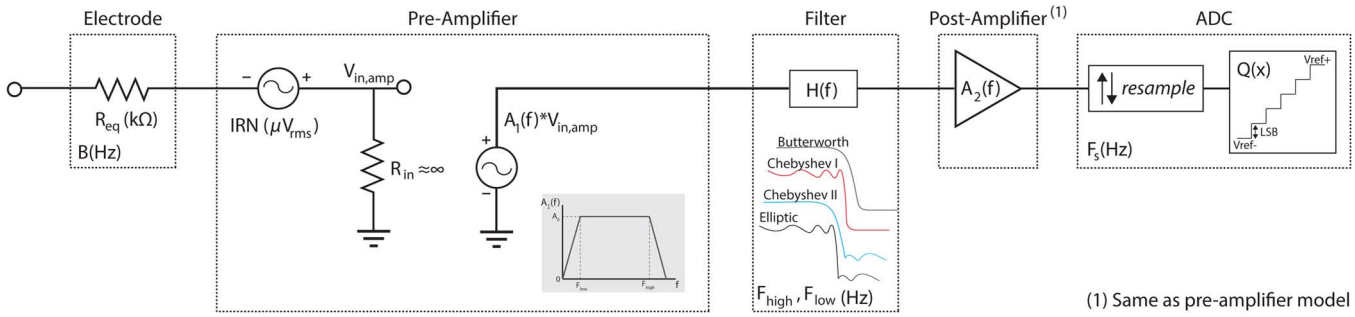

Fig. 2. Basic system behavioural macromodel, including input parameters for each functional block. This include the electrode (equivalent resistance and bandwidth), pre-amplifier (gain, IRN and frequency cut-offs), filter (type and cut-off frequencies) and ADC (sampling frequency, resolution and references).

Regardless of the choice of sorting method, sorting accuracy directly correlates with the performance of front-end electronics [28]. While the demand for sorting performance enforces minimum requirements on the front-end, the resource constraints (power and area) limit the scalability but also strike a trade-off with the front-end specifications. In order to ensure a good balance between accuracy and hardware requirements, one must identify all parameters associated with each stage of front-end, and analyse their effect on accuracy and hardware resources.

Our early work, [28], investigated the effect of varying the front-end design parameters in order to maximise spike sorting performance. Although this does give single dimensional trends, since there are several parameters, this is essentially a high dimensional problem. It is therefore challenging to converge on any single "ideal solution". The work in this paper therefore tackles this issue by taking a holistic approach, considering the system as a whole. By developing a behavioural model, the impact of front-end circuitry on back-end processing can be easily established. With the proposed tool, the designer can investigate the effect of different parameters in a fast way, and before committing to a specific circuit implementation. A good balance between design complexity and outright system performance can therefore be struck at design time.

This paper is organised as follows: Section II describes the methodology (front-end modelling, test data, spike detection/sorting and evaluation), Section III briefly outlines the Matlab-based tool developed, Section IV validates the proposed model by comparing its response to an integrated circuit implementation, and finally, Section V applies the behavioural model to relevant systems reported in the literature and discusses hardware impact on system performance.

II. Methodology

A. Front-End Neural Interface Architectures

The typical architecture of any front-end neural interface (for applications of EAPs) contains three fundamental blocks: (1) a low noise bio-potential amplifier, (2) bandpass filter, and (3) data converter (Fig. 1). The signal analysis chain that follows typically includes spike detection, feature extraction and clustering methods to achieve some level of inference about the spike data (e.g. extracting spike intervals, features, identity, etc.). When an element of the signal analysis chain is implemented online (i.e., in a chip implementation), one can achieve significant levels of data compression, and subsequently reduce bandwidth requirements [24].

In this section we will describe, model and identify the key parameters associated with the fundamental building blocks of a neural interface front-end. Spike detection and sorting methods and metrics, as well as test data, will also be described.

B. Front-End Behavioural Model

To accurately characterise front-end architectures and circuits, we must consider not only ideal behaviour, but also the non-idealities that a realistic circuit implementation introduces [29]. This can significantly affect the signal fidelity and as such may impact downstream spike processing.

1) Electrode Model: The electrode is the conduit between acquisition electronics and neural tissue. Over the last several years, with the drive of microtechnology and fabrication techniques the number of simultaneously recorded single neurons has greatly increased and projected to double every seven years

[30]. Commercially available multi-electrode arrays today can interface with 10 s to 100 s of electrodes [31].

Each electrode is typically characterised by its charge density (for stimulation) and impedance characteristics [32], the latter a vital parameter for recording. In-depth characterisation of some of the state-of-the-art in electrodes can be found in [31]. The impedance characteristics of the electrode play a vital role in deriving the noise added to the signal prior to amplification [32], [33]. This non-ideality is attributed to electrochemical effects at the tissue-electrode interface, scar tissue formation, and inherent electrical properties of the electrode (i.e., material, area) [32]. When in contact with tissue, the electrode forms an electrical double layer capacitance.

This capacitance depends on the electrode surface texture and area [21], [32], and it is calculated as a series combination of double layer and diffusion layer capacitance. It is typically modelled as as constant phase element (CPE) [34], which is highly dependant on electrode area.

We can also consider impedance changes due to injury related mechanisms, possibly as a result of electrode insertion into the tissue. For simplicity, the electrode can simply be modelled as a frequency independent model [32], [35], where the dominating restive contribution includes spreading or seal resistance (resistance between electrode and medium, i.e., neural tissue). The noise is then defined as

$$V_{rms} = \sqrt{4kTR_{eq}B} \tag{1}$$

where k is Boltzmann's contestant, T is temperature in Kelvin, R_{eq} is the electrode resistance and B the signal bandwidth. In a number of studies R_{eq} is measured at a specific frequency [30], [31].

2) Pre and Post Amplifier Model: After the electrode a low noise pre-amplifier is required to increase the signal level from sub-mVs to 10 s of mVs with minimal additional noise. These are typically designed to be AC-coupled to remove DC electrode offset which can be in the order of 100 s of mV depending on electrode material. Gains of 50–200, bandwidths of 3–10 kHz, and input-referred noise (IRN) of 2–10 $\mu\mathrm{V}_{\mathrm{rms}}$ are typical specifications for these amplifiers [6], [15].

Since both the pre- and post-amplifiers are the same in terms of functionality, the model described below applies to both. Due to the pole introduced by the device parasitic capacitances, the gain of the amplifier starts to roll-off (20 dB/dec) at high frequencies, which can be characterised by a low-pass response. In addition, since the DC offset introduced by the electrodes need to be removed [8], often front-end amplifiers are built with a high-pass response introduced via a feedback loop [36]. Therefore, we used a 2nd order Butterworth filter with a mid-band gain to model the amplifier. Although amplifiers may contain a second pole, this is typically placed at frequencies higher than the ones of interest for phase stability.

The IRN of the amplifier is a combination of thermal and flicker noise and is normally measured in $nV/\sqrt{(Hz)}$. In a model, this is a key target specification, and it can be combined with the amplifier bandwidth to give an indication of the added V_{rms} noise. In our implementation we use Matlab's *randn* function to generate this noise.

The non-idealities of the system are therefore: input/output offsets, non-linearities, among other noise sources. However, it is typically the gain, bandwidth and noise that are the target specifications in the design of these amplifiers.

3) Bandpass Filter Model: Following pre-amplification, a bandpass filter is required to: (1) reject out-of-band LFPs (high pass), and (2) prevent aliasing (low pass). The high-pass cut-off frequency is typically set between 100–300 Hz, and low-pass between 3–10 kHz. Due to the close proximity between the high- and low-pass cut-off frequencies, a sharp response is required to avoid in-band attenuation and it is thus desirable to use high order filters. A key challenge is however, to minimise the effect of phase distortion as this will impact subsequent signal processing.

The most important parameters associated with filtering are filter type, order, cut-off frequencies, passband and stopband ripple. The filter stage is thus modelled based on these parameters, where a bandpass filter transfer function is utilised in conjunction with the built-in Matlab function *filter*.

Our filter model preserves the phase information of the filter, as opposed to other filtering methods such as *filtfilt* (a Matlab built-in function). Preserving this attribute of analogue filters is of utmost importance, since it has been shown that non-linear phase dependence with frequency, may cause significant distortions in the shape of the observed spikes, thus affecting the spike detection and sorting performance [28].

In the developed model, the user can input any filter order and cut-off frequencies, and is given the choice of four different filter implementations: Butterworth, elliptic and Chebyshev Type I & II.

4) Analogue-to-Digital Converter Model: The main design specifications for the analog-to-digital converter (ADC) are the resolution and sampling rate (typically 8–12 bit, and 16–32 kS/s). Although these set the numerical accuracy in subsequent spike computation (detection and sorting), this is fundamentally limited by the signal-to-noise ratio (SNR), dynamic range and bandwidth of the signal.

In our model, the primary parameters for ADC are sampling rate, resolution (ENOB) and reference voltages for the ADC. Based on these parameters, first the signal is resampled (using the built-in Matlab function *resample*) and then the resampled signal is quantised using (2) and (3).

$$LSB = \frac{V_{\mathrm{ref}+} - V_{\mathrm{ref}-}}{2^N - 1} \tag{2}$$

$$Q = \mathrm{sgn}(x)\left\lfloor \frac{x}{LSB} + \frac{1}{2} \right\rfloor \tag{3}$$

where Least Significant Bit (LSB) is the ADC step size, $V_{\mathrm{ref}+}$ and $V_{\mathrm{ref}-}$, are the positive and negative voltage references, N is the number of bits (resolution), x is the sample to be quantised, and Q the quantised signal.

It should be noted that the behaviour modelled is of an ideal ADC, and there are numerous non-idealities that impacts ADC output. These include offset and gain errors, integral and differential non-linearities, aliasing and quantisation effects. These non-linear effects and non-idealities will be minimised according to the performance of the prior analogue stages, and

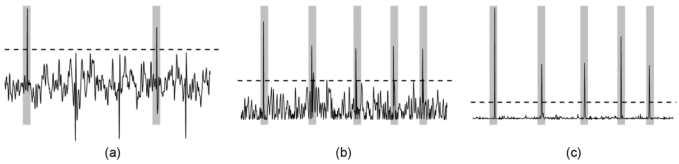

Fig. 3. Illustration of 5 neurons being detected with (a) a single positive threshold, (b) an absolute value threshold, and (c) a single threshold after NEO processing. Note the shaded regions indicate successfully detected spikes.

resolution requirements for the spike detection and sorting, so that the equivalent non-ideal effects of the ADC referred to the input will be smaller than the input referred noise of the analogue circut and electrodes.

On the other hand, quantisation effects are quantified in the definition of resolution and reference levels. In fact, instead of using the ADC resolution, our model uses the effective number of bits (ENOB) that is typically effective in encompassing ADC non-idealities, especially for the following detection and sorting stages.

C. Testing and Evaluation

As mentioned, we aim to: (1) establish a behavioural front-end model translated into a software tool (2) validate the model using an application specific integrated circuit implementation, and finally (3) demonstrate the tool's usefulness in establishing a good balance between spike processing performance and hardware efficiency during design time. In the following sections we define the test methodologies and accuracy quantifiers associated with detection and sorting.

1) Spike Detection: Spike detection is the process of identifying that an EAP has occurred and has been recorded by the system. We utilise three common spike detection methods: single positive thresholding, absolute value thresholding, and single positive thresholding with the Non-linear Energy Operator (NEO) (Fig. 3).

a) Single Threshold: Single positive thresholding applies an amplitude threshold to the signal, whereby a spike is detected upon crossing it. The threshold level is set as described in [25]

$$thr = 4\sigma_n = 4 \times median\left\{\frac{|x|}{0.6745}\right\} \tag{4}$$

where σ_n is the estimation of the background noise standard deviation [37].

b) Absolute Value: This method applies the amplitude threshold of (4) to the absolute value of the signal, i.e., $|x|$.

c) NEO: In this detection method, the amplitude threshold is applied after processing the neural signal with a Non-linear Energy Operator (NEO) ψ given by (5). The NEO, also known as the Teager Energy Operator [38], estimates energy by taking the square of the product of amplitude [39], and is defined as [40]

$$\psi\left[x(n)\right] = x^2(n) - x(n+1) \times x(n-1). \tag{5}$$

As described similarly in [41] and [42], threshold Th_{NEO} is the mean of the NEO scaled by a constant, C, which is defined empirically to be 7.5.

$$Th_{NEO} = C\frac{1}{N}\sum_{n=1}^{N}\psi\left[x(n)\right] \tag{6}$$

2) Spike Sorting: Once a spike is detected, the process of identifying to which of the detectable neurons in the vicinity of the electrode it belongs to, is referred to as spike sorting. For the results reported herein, spike sorting is carried out with three different methods.

a) Template Matching (TM): This method involves aligning the maximum peak of the signal with a spike template and using the Squared Euclidean Distance (7) as a similarity/distance measure.

$$ED = \sqrt{\sum_{i=1}^{n}(x_i - T_i)^2} \tag{7}$$

where n is the number of data points in the spike template, x is the detected spike and T the template. The templates are created by taking the mean of the spikes (within each cluster), aligned to their individual maximum peaks. To create templates, we used a training dataset, and TM performance was assessed using a separate training set.

b) Principle Component Analysis (PCA): PCA is a well established method for extracting orthogonal components of a signal and is typically used as a benchmark for spike sorting systems. Here, we take the first two principle components (for each spike) and use k-means for clustering (50 iterations). We use the Matlab's in-built function *princomp*.

c) First and Second Derivative Features (FSDE): This method is based on taking the minimum and maximum values of the 2nd derivative and the maximum value of the 1st derivative (within each spike) which has been shown to provide good performance in resource constrained hardware [27]. Matlab function *gradient* is used to calculate the derivatives.

For both methods we use Matlab's in-built clustering function, *K-means*.

3) Evaluation: Here we define the quantifiers for accuracy in both spike detection and sorting. These will be used as the metric for evaluating the effect of different neural interface architectures on detection and sorting.

a) Spike detection accuracy: (SD_a) is given by

$$SD_a = P_d \times \theta(P_d) \tag{8a}$$

and

$$P_d = (1 - \frac{N_e}{N_{su}}) \tag{8b}$$

where N_e is the total number of missed spikes and false positives, and N_{su} is the number of spikes. $\theta(x)$ is the unit step

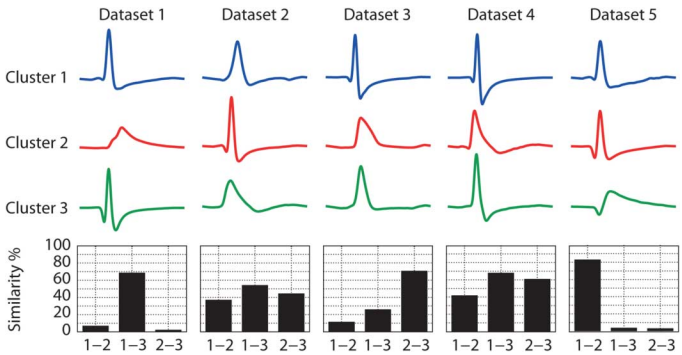

Fig. 4. Mean spike profiles for the 5 datasets with corresponding Bray-Curtis similarity measures applied between each neuron cluster within each dataset.

function which ensures that detection performance is zero when the number of errors are higher or equal to number of spikes.

$$\theta(x) = \begin{cases} 1, & \text{for } x \geq 0 \\ 0, & \text{for } x < 0 \end{cases} \tag{9}$$

b) Spike sorting accuracy: is defined as

$$SS_a = \frac{N_{cs}}{N_{det} - N_e} \tag{10}$$

where N_{cs} is the number of correctly identified spikes, N_{det} is the number of detected spikes, and N_e is the number of detection errors as described above. Eq. (10) only reflects the accuracy of spike sorting algorithm and does not include errors associated with detection. Furthermore, a combined accuracy figure-of-merit (FOM) for spike detection and sorting accuracy SDS_a is defined as

$$FOM_a = SD_a \times SS_a \times 100\%. \tag{11}$$

D. Test Data

Test data has been generated using the process described in [43]. The methods were tested using a total of 30 synthetic datasets that were created using a database of 594 different average spike shapes (obtained from real recordings of monkey neocortex and basal ganglia) [25]. These contain five different groups of 6 datasets (each using 3 single units), Fig. 4. Each group further comprised both training and test datasets at varying SNR levels. In addition to single-unit activity (SUA), the simulated datasets also contain LFPs, background and multi-unit activity [43].

In order to simulate LFPs and background activity, surrogates of a real extracellular recording from the human medial temporal lobe were used. The subject, a patient with pharmacologically intractable epilepsy, was implanted with intracranial electrodes for clinical reasons. The intracranial probe had 9 micro-wires at its end (8 active recording channels and 1 reference) to record single-neuron activity, and the differential signal from the microwires was amplified and sampled at 28 kHz and

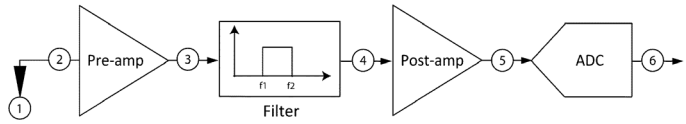

Fig. 5. Behavioural model system architecture showing different I/O nodes.

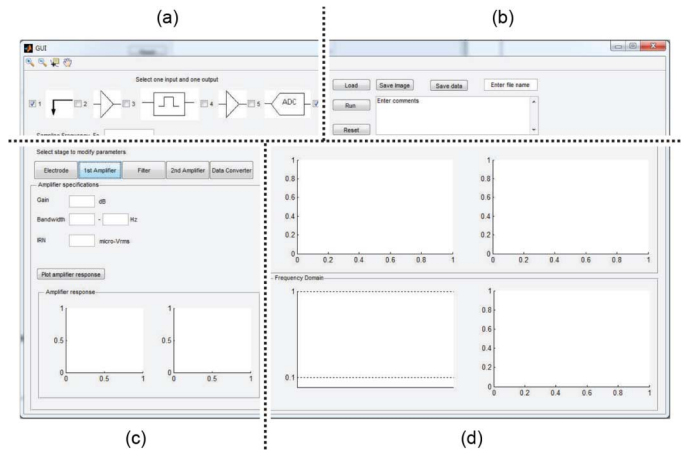

Fig. 6. Graphical user interface for the front-end behavioural model. Annotated are the four main panels. (a) Node Select. (b) Function Select. (c) Stage Select. (d) Node Display.

16-bit resolution (signal input range ±1 mV) [44]. The channel used contained neither single-unit nor multi-unit activity, but had the same power spectrum and amplitude characteristics of neighbouring channels that had both types of activity.

Spike shapes of varying amplitudes were superimposed on the background noise and LFP to generate the SUA. Single-unit spike amplitudes were set to 50 μV (low SNR), 75 μV (medium SNR), and 100 μV (high SNR), in order to create datasets with different SNRs. Each spike train followed a Poisson process, with a mean firing rate of 5 Hz. Spikes that fell within a 2 ms window of each other were removed so as to introduce a refractory period and delete overlapping spikes.

By mixing the activity of the whole database of 594 spike shapes, multi-unit activity with uniformly distributed amplitudes (between 20 μ and 40 μ) and a firing rate of 20 Hz was created. Both the synthetic MUA and SUA were added to the LFP and background noise.

III. Behavioural Model Realisation

Based on the behavioural model established in Section II-B, a graphical user interface (GUI) was developed in MATLAB, and is available on our website.[1] The tool provides a front-end modelled as a single recording channel (Fig. 5),in which the signals can be analysed at each node (1–6) to study the behaviour of each front-end block. Through the GUI, the user can input all the critical front-end design parameters, and observe the input and output signals in a simple and user-friendly graphical user interface.

The GUI has been designed to operate within a single window in four main panels, as presented in Fig. 6.

[1]www.imperial.ac.uk/bioinspiredtechnology/research/neuralinterfaces/tools

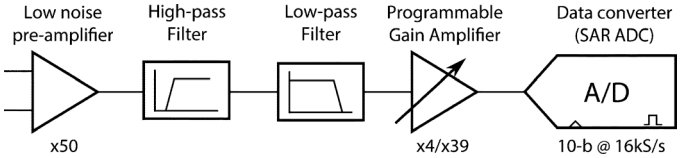

Fig. 7. Channel architecture of the front-end neural interface IC.

- The *Node Select* panel shows a graphical representation of the model with check boxes for the user to define the desired input and output nodes. Based on the node selection, the corresponding blocks are activated to facilitate parameter input. No more than two nodes can be selected at the same time.
- The *Function Select* panel provides the user with the option to run the simulations, reset the system, input the data to be processed and save the signals at every (activated) node in the defined signal processing chain.
- The *Stage Select* panel allows the user to configure each activated front-end stage. Furthermore, amplifier and filter tabs have additional response plots, so that user can visually see the magnitude and frequency response of the corresponding blocks. In addition to the front-end parameters, the user is also prompted to enter the original sampling frequency of the input signal.
- The *Node Display* panel displays time and frequency responses of both the input and output nodes, after each simulation.

IV. Behavioural Model Validation

To demonstrate the validity the behavioural model proposed herein, a neural recording integrated circuit (IC) is used. The neural recording IC and the behavioural model are configured with the same parameters, and their frequency responses (as well as responses to different test stimulus) are compared. These comparisons are done for several different configurations and are further discussed in Section IV-B.

The implemented channel architecture is shown in Fig. 7 including the front-end amplifier (FEA), the analogue signal processing, (i.e., filters), and the data converter. The total gain of the system is set to 65.8 dB for EAPs and 46 dB for LFPs, such that the input signal was amplified/mapped onto the input range of the data converter. To compare the real system with the proposed model, the low and high pass filters have been implemented separately with individually tunable corner frequencies.

A. Circuit Implementation

The FEA is based on the established Harrison topology with a symmetric operational transconductance amplifier (OTA) [21], shown in Fig. 8(a). A gain of 50 (33 dB) is set by the capacitance ratio to avoid saturation and reduce the distortion by further filtering. The capacitors are implemented by an array of Metal-Insulator-Metal (MIM) capacitors with unit capacitance of 150 fF selected for good noise and matching performance [21]. The current consumption of the OTA is 3 μA with a 600/1.5 μm input differential pair to minimise flicker noise.

This is then followed by a second order high pass filter (HPF) based on a Bessel function for removing the LFP before further amplification (if only action potentials are required). This filter is realised using a gm-c topology arranged as 2nd order ladder configuration, shown in Fig. 8(b). To increase the dynamic range, bump linearisation was applied to the gm cell [45]. A second order low pass filter (LPF) is implemented in a similar manner with a cross coupled input differential pair to further increase the linearity, also shown in Fig. 8(b). The cut-off frequency of both the HPF and LPF is tunable by switching in capacitance, providing corner frequency settings at 120 Hz, 240 Hz, 300 Hz for HPF, and 3 kHz, 4 kHz, 6 kHz for LPF. Bypass switches are applied to both filters, to allow the inputs and outputs to be shorted thus bypassing the filtering. This is followed by a programmable gain amplifier based on capacitive feedback to further boost the gain, shown in Fig. 8(d). This uses a flyback capacitor configuration [11] to provide either a gain of 4 for LFPs, or 39 for EAPs. A 2-stage miller amplifier with open loop gain of 72 dB, and gain-bandwidth (GBW) of 1 MHz is used to drive the ADC capacitive input. A standard charge redistribution Successive Approximation (SAR) analogue digital converter (ADC) with a 16 kHz sampling rate and 10-bit resolution is used (not detailed herein). The capacitor array is implemented by MIM capacitors with 33 fF unit capacitance and 9:1 split configuration [16] to reduce the total active area while maintaining good linearity. The specifications of the circuit used for comparison with the proposed model is summarised in Table II.

The chip microphotograph together with overlaid floorplan is shown in Fig. 9. This includes 16 recording channels with each channel occupying a footprint of $400\ \mu\mathrm{m} \times 400\ \mu\mathrm{m}$ including all components. For test purposes, a single channel has been implemented separately and connected to a buffer to allow for direct analogue signal recording.

B. Comparison Between Integrated Circuit Measurements and Behavioural Results

As previously mentioned, in order to confirm the validity of the proposed model, the neural recording IC described in Section IV-A and the behavioural model are configured with the same parameters, and their frequency responses are compared for various configurations.

Frequency responses of the behavioural model, as well as the simulated and measured frequency responses of the corresponding implemented system are presented in Fig. 10. It should be noted that the implemented design uses capacitor and transconductance values derived directly from the model without accurate modification regarding to the parasitics and non-linearity. In other words, a model oriented design approach rather than a circuit oriented approach has been followed. This helps the realistic validation and comparison of the behavioural model results.

As shown in Fig. 10, the frequency responses of the behavioural model and the hardware system closely match, with small distortion around 3 dB due to device mismatch and parasitic capacitances in cascading stages. These non-ideal influences depend on device sizes and circuit topologies, and are beyond the main scope of this paper.

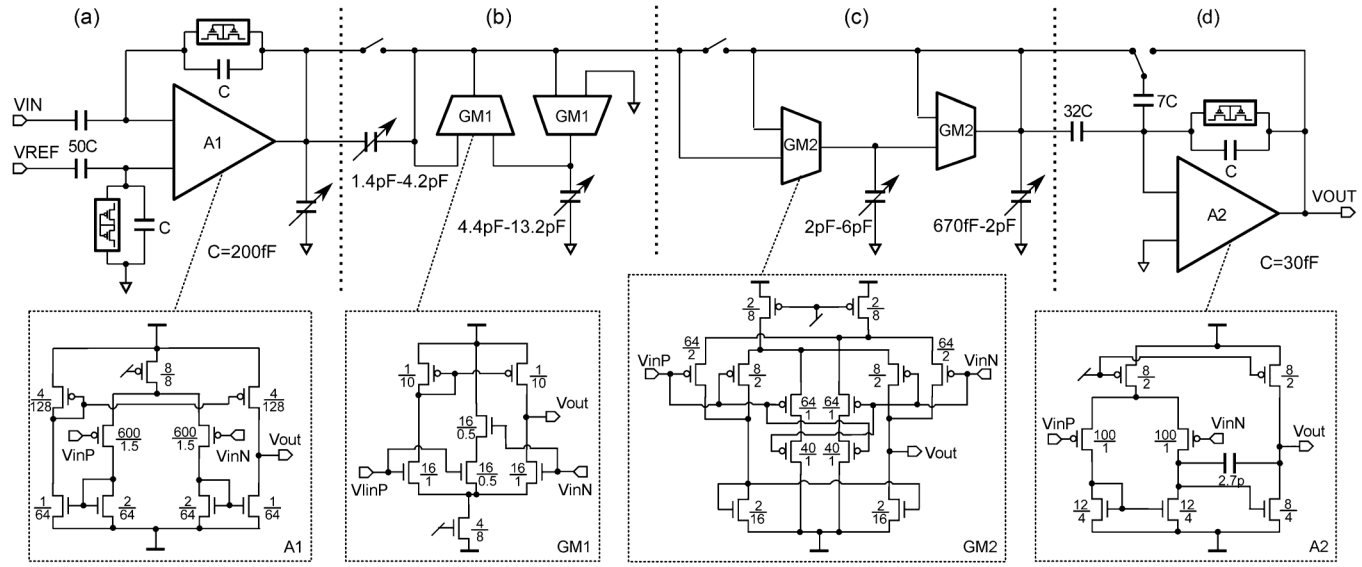

Fig. 8. Circuit implementation of the front-end neural interface. Schematics shown for (a) low noise pre-amplifier, (b) high-pass filter, (c) low-pass filter, and (d) programmable gain amplifier that directly drives the SAR ADC (schematic not shown).

TABLE I
BEHAVIOURAL MODEL INPUT DESIGN PARAMETERS

Electrode	Amplifiers	Filter	ADC
Impedance	Gain	High-pass cut-off	Sampling Rate
Bandwidth	Bandwidth	Low-pass cut-off	Resolution
	IRN	Filter Type	V_{ref+}
		Filter Order	V_{ref-}
		Passband Ripple	
		Stopband Ripple	

TABLE II
TECHNICAL SPECIFICATIONS OF THE FRONT-END NEURAL INTERFACE IC

Parameter	Simulated	Measured
	Signal Conditioning	
Gain	66dB	62dB
Noise (300Hz-3kHz)	4.2 μV_{rms}	5 μV_{rms}
HP corner	{0.1, 180, 240, 320}Hz	{0.5, 190, 240, 360}Hz
LP corner	{3, 5, 6, 7}kHz	{3.2, 4.2, 5.1, 5.6}kHz
Power consumption	9.1 μW	10 μW
	Data Conversion	
Sampling frequency	16 kHz	15.5 kHz
ENOB	9.2b	9.1b
Power consumption	3.4 μW	5 μW

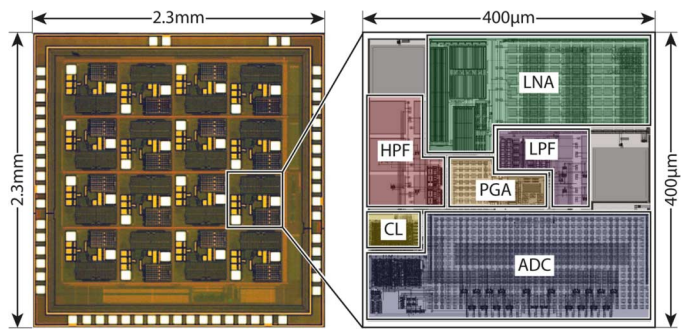

Fig. 9. Microphotograph of the circuit implemented in a 0.18 μm CMOS technology showing (a) the entire 16-channel system, and (b) floorplan of a single recording channel (AFE).

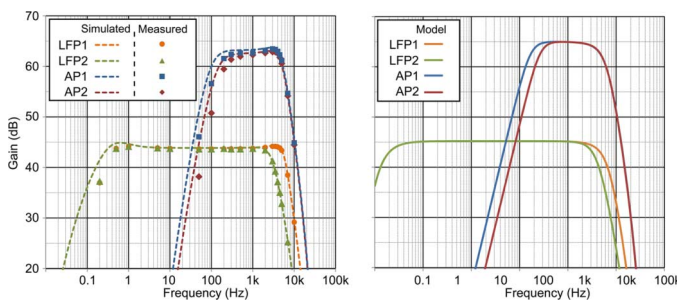

Fig. 10. Comparison of neural front-end IC and the behavioural model frequency responses at various configurations. (a) Measured (dashed lines) and simulated in a EDA tool (marks) frequency response of neural IC. (b) Simulated frequency response of the behavioural model.

Fig. 11 shows the time domain input and output from the neural IC and the front-end model for comparison, which reveal a close match between the two outputs. It should be noted that the measured data exhibits higher noise levels than modelled. Although the measured IRN level is 5 μV_{rms} (hence within expectations), an estimated 18 μV_{rms} is additionally introduced by test setup. More specifically, this noise is due to external signal generator circuits, which output attenuated datasets of different noise levels, and also include line frequency harmonics and environmental noise. Moreover, the neural recording IC implements a Bessel filter, while behavioural model uses a Butterworth filter configuration (since Bessel option is not available), thus additional mismatch between the results are introduced.

For further validation of the behavioural model, all neural test data (with different noise levels) are used as the input to both the integrated circuit and the proposed model. The system (as described previously) is configured as follows: gain $=$ 66 dB, high-pass $f_c = 210$ Hz, low-pass $f_c = 4.2$ kHz. Spike detection and sorting performances of modelled and measured outputs are compared in Table III and Table IV, respectively. It should be noted that data presented in these tables represent the difference

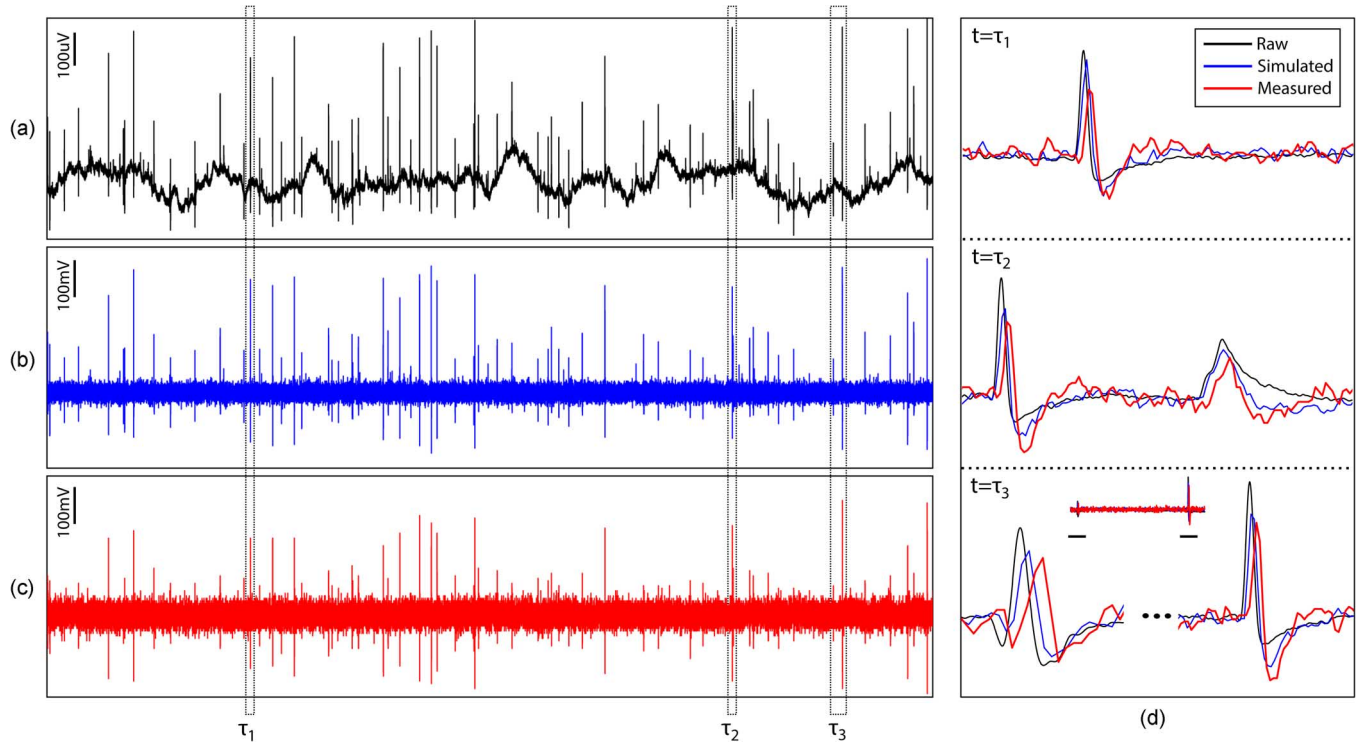

Fig. 11. Comparison of simulated (behavioural) and measured (chip) response to a test stimulus (spike waveform). Shown are (a) raw neural input, (b) behavioural model output, (c) measured output, and (d) magnified sample spikes (with normalised amplitude and added time increment). Please note that for $t = \tau_3$, smaller spike on the left have been scaled-up for illustrative purposes (relative scale is shown above the spikes).

TABLE III
SPIKE DETECTION PERFORMANCE DIFFERENCE BETWEEN THE MODELLED AND MEASURED OUTPUT

Dataset	SNR	Detection Difference %		
		ST	AT	NEO
D1	High	11.11	7.94	28.57
	Med.	0	0	1.27
	Low	-1.39	-1.39	2.78
D2	High	0	-1.47	0
	Med.	-1.43	0	1.43
	Low	1.28	1.28	-1.28
D3	High	0	1.45	-5.80
	Med.	3.03	3.03	0
	Low	-2.90	-2.90	-1.45
D4	High	1.69	1.69	0
	Med.	1.47	1.47	-1.47
	Low	0	0	-1.33
D5	High	1.30	1.30	0
	Med.	-1.52	0	1.52
	Low	4.11	5.48	1.37

TABLE IV
SPIKE SORTING PERFORMANCE DIFFERENCE BETWEEN THE MODELLED AND MEASURED OUTPUT

Dataset	SNR	Sorting Difference %		
		TM	PCA	FSDE
D1	High	0	0	11.11
	Med.	0	0	-1.27
	Low	0	1.39	13.89
D2	High	0	0	-8.82
	Med.	0	0	22.86
	Low	0	0	-24.36
D3	High	0	0	-4.35
	Med.	0	0	-1.52
	Low	1.45	0	0
D4	High	0	0	-1.69
	Med.	0	26.47	4.41
	Low	0	0	-2.67
D5	High	0	0	-5.19
	Med.	0	0	-16.67
	Low	0	1.37	-4.11

between the modelled and measured spike processing performance.

It can be seen from Table III and Table IV that spike detection and sorting performances of the model and measured output closely match. Across all detection methods, datasets and different noise levels, the mean difference in spike detection is 1.34% with standard deviation of 4.97%. On the other hand, average sorting performance difference (Table IV) between the model and the measurement is 0.27% with standard deviation of 7.67%. However, it should be noted that there are a few exceptions in which larger differences compared to the majority of results are observed. These are due to additional noise introduced in the experimental setup as discussed above. These relatively larger differences are especially observed across several datasets for FSDE which has a higher sensitivity to white noise.

V. BEHAVIOURAL MODEL DEMONSTRATION

Here, the AFE parameters are investigated (through the proposed behavioural model) in terms of their impact on subsequent spike processing (detection and sorting), as well as their

TABLE V
REVIEW OF STATE-OF-THE-ART NEURAL INTERFACES SHOWING KEY DESIGN PARAMETERS

Ref.	Vdd (V)	Tech (μm)	Electrode Z (kΩ)	Electrode fc1 (Hz)	Electrode fc2 (Hz)	Pre-Amplifier Gain (dB)	Pre-Amplifier fc1 (Hz)	Pre-Amplifier fc2 (kHz)	Pre-Amplifier IRN (μV_{rms})	Filter Type*, Order	Filter fc1 (Hz)	Filter fc2 (kHz)	Post-Amplifier Gain (dB)	Post-Amplifier fc1 (Hz)	Post-Amplifier fc2 (kHz)	Post-Amplifier IRN (μV_{rms})	Data Converter Fs (kS/s)	Data Converter Res. (bit)	Data Converter Vref (V)	Data Converter Vref (V)	Resource Power (mW)	Resource Area (mm^2)	Resource Power/ch.‡ (μW)	Resource Area/ch.‡ (mm^2)
[8]	3.3	0.5	400	0	fso/2	40	0	5	5.1	BW,2	300	fso/2	20	0	5	5.1	15	10	2.475	0	13.5	27.73	67.5	0.056
[10]	3.3	0.5	1000	0	fso/2	40	94	8.2	1.94	BW,2	0	fso/2	0	0	fso/2	0	16	7	0.125	-0.125	1.8	9	112.5	0.563
[12]	1.65	0.35	190	0	fso/2	40	100	10	4.9	BW,2	0	fso/2	20	0	fso/2	0	40	9	0.5	-0.5	6	63.36	33.5	0.449
[13]	0.8	0.13	100	0	fso/2	49	100	6.2	14	BW,2	0	fso/2	0	0	fso/2	0	80	8	1	0	0.02	1.54	20	0.080
[15]	1.4	0.18	1000	0	fso/2	40	1	100	11.2	BW,2	350	12	26	0	fso/2	0	31.25	7.5	1	0	0.325	9.92	10.1	0.310
[16]	1.2	0.13	100	0	fso/2	56	0.1	100	3	BW,2	280	10	0	0	fso/2	0	31.25	10	0.6	-0.6	6.5	25	68	0.26
[17]	3.3	0.35	100	0	fso/2	56	200	6	2.9	BW,4	200	6	20	0	fso/2	0	12.5	12**	1	-1	5.94	25.2	231	1.575
[18]	1.2	0.13	100	0	fso/2	47.5	167	6.9	2.84	BW,2	0	fso/2	18	0	fso/2	0	22.5	7.62	0.6	-0.6	0.0028	0.16	2.8	0.16
[6]†	3.3	N/A	100	0	fso/2	74	0	fso/2	1	BW,10	250	7.5k	0	0	fso/2	0	30	12	1	-1	N/A	N/A	N/A	N/A

*BW = Butterworth, **uses an off-the-shelf ADC, † only considered for accuracy comparisons (discrete implementation), ‡ area/power per channel only taken for systems quoting these for AFE.

impact on hardware. This is achieved by configuring the proposed behavioural model with the design parameters of relevant state-of-the art front-end architectures reported in literature.

A. State-of-the-Art Front-Ends

We consider state-of-the-art front ends [6]–[8], [10], [12], [13], [15]–[18] by applying their design parameters to our model. Whenever possible, the measured system specifications such as gain, bandwidth, and effective number of bits were chosen as input parameters (instead of design targets). For any missing information regarding each stage, reasonable approximations were made. For example, for any system with missing electrode information, a typical impedance value of 100 kΩ was assigned, with the electrode bandwidth assumed to cover the entire signal band.

For the behavioural model to accurately represent the front-ends being investigated, adjustments were required in order to ensure that the overall transfer function of the model matches that of the front-end architectures. Considering the fact that the presented model is a fixed five stage system and that the front-ends investigated have varying stages of amplification and filtering, not all of the parameters for each stage required by our model were available. Therefore, whenever the architecture differed from the expected (in our model), the parameters of interest had to be adjusted to have minimal impact on the overall transfer function. This typically only affected a number of the amplification and filtering stages, and involved adjusting gain, bandwidth, filter order and type, and input referred noise parameters. For any architecture with a "missing" stage, gain and IRN were always set to 0 dB and 0 μV_{rms}, and filter was configured as a second order Butterworth filter. Most crucially, the bandwidth was set at the entire frequency band (i.e., half the sampling rate of the original input signal to the system) in order to ensure that the configuration of these missing stages had minimal impact, if any, on the input signal.

On the other hand, whenever the number of stages exceeded those specified in our model, parameters were re-distributed to ensure that the overall transfer function of the original circuit was accurately represented. For example, [17] consists of four bandpass amplifier/filter stages, which cannot be represented with the proposed model. However, this can be easily resolved by combining the two middle stages together as a 4th order filter stage with (unity gain), and with the gain of the middle stages being transferred to the pre and post amplifiers such that the overall gain of the model is equivalent to that of the real circuit. The complete list of specifications (modified/redistributed where necessary to fit our model) is presented in Table V.

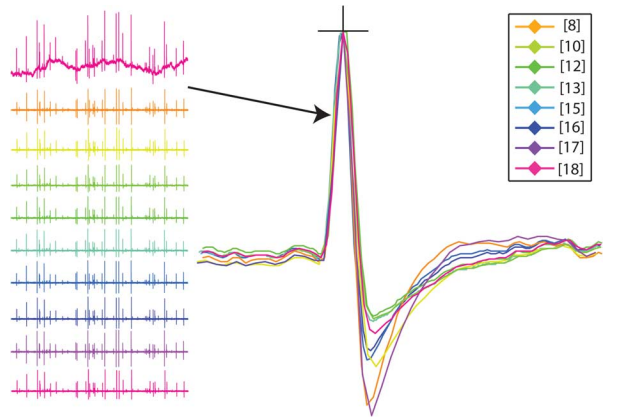

Fig. 12. Effect of analogue front-end on spike waveform. Shown is a test signal passed through all front-end configurations reviewed using the behavioural model developed. Spike outputs have been peak aligned and normalised for different gain and quantisation levels.

B. Spike Processing Accuracy and Hardware Requirements

Having extracted all relevant parameters and applied them to our proposed model, all datasets were processed with each front-end configuration. Fig. 12 illustrates the output of each front-end and its effect on spike shapes. All outputs have been re-scaled for illustration purposes, i.e., to account for different gains and ADC resolutions.

As stated earlier, front-end performances were quantified in terms of the spike detection and sorting methods, and the overall accuracy was compared to the power and silicon area utilisation of each design. Tables VI and VII present the detection and sorting accuracies across all state-of-the-art front-end designs.

1) Spike Detection: We observed that the relative accuracy of the front-ends were constant (across all methods), although the detection performance varied depending on the threshold method. Although the variation in spike detection performance is around 18% to 20% on average (depending on the detection method), it should also be noted that 88% of the AFEs had variations of 10% to 13% on average. Both simple and absolute threshold methods performed with 80% and above accuracy in general.

2) Spike Sorting: Spike sorting performance of front-ends showed significantly less variation when compared with spike

TABLE VI
SPIKE DETECTION PERFORMANCE OF STATE-OF-THE-ART FRONT-END CIRCUITS

Dataset	SNR	Detection Accuracy %					
		ST		AT		NEO	
		mean	std.	mean	std.	mean	std.
D1	High	92.43	11.74	91.81	11.45	92.48	9.18
	Med.	90.67	16.72	90.11	16.50	86.60	15.75
	Low	82.13	22.91	82.28	23.01	69.60	22.23
D2	High	92.99	10.24	92.74	10.19	86.18	20.10
	Med.	88.01	18.21	87.88	18.20	78.28	25.16
	Low	72.58	28.99	72.44	29.04	58.24	28.37
D3	High	92.63	10.73	92.33	10.61	85.26	13.06
	Med.	89.80	17.72	89.50	17.72	77.79	14.53
	Low	77.16	28.17	76.87	28.20	58.33	17.29
D4	High	95.92	7.38	95.67	7.29	95.28	7.67
	Med.	91.46	17.66	91.18	17.58	91.05	13.91
	Low	83.33	30.06	83.17	30	74.12	23.57
D5	High	88.58	21.49	88.04	21.34	78.89	22.97
	Med.	82.31	29.26	82.04	29.14	66.16	25.83
	Low	67.44	32.55	67.35	32.61	44.55	22.67

TABLE VII
SPIKE SORTING PERFORMANCE OF STATE-OF-THE-ART FRONT-END CIRCUITS

Dataset	SNR	Sorting Accuracy %					
		TM		PCA		FSDE	
		mean	std.	mean	std.	mean	std.
D1	High	99.59	0.10	99.47	0.32	85.87	8.65
	Med.	99.54	0.11	99.43	0.38	79.86	8.34
	Low	98.49	1.14	97.77	2.96	71.86	10.40
D2	High	99.59	0.15	99.56	0.26	65.47	20.00
	Med.	99.05	1.13	99.15	1.08	51.60	12.19
	Low	97.07	3.51	97.48	3.07	47.41	12.65
D3	High	99.36	0.22	99.35	0.20	78.24	9.52
	Med.	99.19	0.68	99.44	0.53	74.00	8.24
	Low	96.05	2.74	97.40	2.90	66.30	10.54
D4	High	99.53	0.15	96.16	9.43	86.43	10.40
	Med.	99.36	0.23	98.87	0.79	81.44	13.38
	Low	98.11	1.72	97.45	2.80	66.89	15.20
D5	High	99.40	0.40	99.30	0.42	63.21	15.99
	Med.	98.16	1.50	98.32	1.57	54.15	7.45
	Low	94.63	5.45	94.83	5.84	53.59	9.31

detection performance. It can be observed that variations in performance for TM, PCA and FSDE were within 1.28%, 2.17% and 11.5% on average. More specifically, for TM and PCA the worst case variation amongst the front-end performances were 5.45% and 9.43%. We note again that these spike sorting results do not include the spike detection and since the "ground truth" to our datasets are known the spike detection accuracy is essentially 100%.

3) Power and Silicon Area Requirements: When considering the spike processing performance, i.e., both detection and sorting, the variation in accuracy between different front-end interfaces was relatively low. However, these minor differences were accompanied by much larger differences in power and silicon area specifications. Although some designs achieve higher specifications (in terms of individual component performance), their overall spike processing performances barely exceed others. It is therefore common that individual component specifications are over-engineered due to the fact that impact on system performance is unknown. The choice of the FE parameters is thus a critical element of the design that can be informed using a behavioural model.

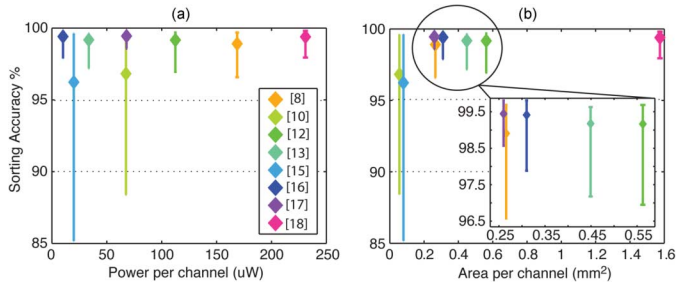

Fig. 13. Spike sorting performance plotted against hardware resource requirements for all front-ends. Shown are (a) power consumption per channel, and (b) silicon area per channel, for a single spike sorting method (across all test datasets at all noise levels).

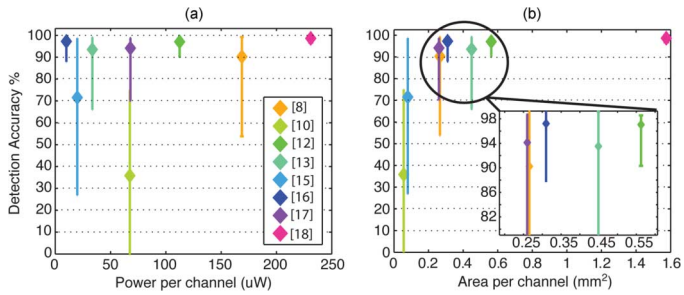

Fig. 14. Spike detection performance plotted against hardware resource requirements for all front-end configurations. Shown are (a) power consumption per channel, and (b) silicon area per channel, for a single spike sorting method (across all test datasets at all noise levels).

More specifically, when sorting performances are compared (Fig. 13) the spread of the majority of works fall within 5% of each other while there exists orders of magnitude difference in power and silicon area per channel. On the other hand, when detection results (Fig. 14) are compared, one can observe again that among the works with similar performances, there exists large differences in silicon area and power. Note these illustrate the absolute power and silicon requirements and does not take the effect of technology scaling into account. For example, transistor area generally scales with feature size and dynamic power consumption scales proportionally to Vdd^2. However, as the ratios of static to dynamic power and passive to active device area are generally not reported, a more general technology-independent FOM cannot be established.

The results, however, clearly demonstrates that it is possible to achieve good detection/accuracy while making further savings by not over-designing some aspects of the front-end. The proposed tool presented herein therefore has more impact in minimising resource requirements rather than maximising performance. This essentially helps designers to make hardware efficient design choices that do not significantly degrade spike processing.

VI. CONCLUSION

With next generation neural interfaces targeting hundreds to thousands of channels, the power and silicon area budgets on

the front-end electronics are becoming increasingly stringent. While the demand for spike detection and sorting performance enforces minimum front-end requirements, the limited power and silicon area resources, in addition to fundamental limitations posed (such as maximum power dissipation not to damage neural tissue), necessitate careful design of front-end specifications. To address this problem a front-end behavioural tool, with which the designer can investigate front-end parameters at design time, is proposed.

The validity of the model is verified through a real front-end implementation by comparing their frequency responses at various configurations, and comparing the spike processing performance of the modelled and measured results. Following verification of the model, its use have been demonstrated through various state-of-the art front-end parameter configurations reported in literature. The impact of FE parameters have been discussed in terms of spike processing performance and hardware requirements.

The reported results show that while the variation in the observed spike processing accuracy between different front-end interfaces is relatively low and comparable, the designs show significant spread in specifications for individual components which translate into the large deviations in power and silicon area requirements (up to orders of magnitude).

In other words, despite some designs achieving higher specifications, their overall spike processing performance barely exceed each other. Hence, by not over-engineering some aspects of the front-end, power and silicon area can be minimised while maintaining the spike processing performance. The proposed behavioural model provides the designer a platform to investigate the effects of different parameters in a fast way. Thus, a good balance between resource efficiency and performance can be achieved during design time.

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