A CMOS Power-Efficient Low-Noise Current-Mode Front-End Amplifier for Neural Signal Recording

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***Abstract*—In this paper, a new current-mode front-end amplifier (CMFEA) for neural signal recording systems is proposed. In the proposed CMFEA, a current-mode preamplifier with an active feedback loop operated at very low frequency is designed as the first gain stage to bypass any dc offset current generated by the electrode-tissue interface and to achieve a low high-pass cutoff frequency below 0.5 Hz. No reset signal or ultra-large pseudo resistor is required. The current-mode preamplifier has low dc operation current to enhance low-noise performance and decrease power consumption. A programmable current gain stage is adopted to provide adjustable gain for adaptive signal scaling. A following current-mode filter is designed to adjust the low-pass cutoff frequency for different neural signals. The proposed CMFEA is designed and fabricated in 0.18-μm CMOS technology and the area of the core circuit is 0.076 mm^2. The measured high-pass cutoff frequency is as low as 0.3 Hz and the low-pass cutoff frequency is adjustable from 1 kHz to 10 kHz. The measured maximum current gain is 55.9 dB. The measured input-referred current noise density is 153 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$, and the power consumption is 13 μW at 1-V power supply. The fabricated CMFEA has been successfully applied to the animal test for recording the seizure ECoG of Long-Evan rats.**

***Index Terms*—Current-mode, front-end, low-noise low power design, neural recording, offset cancellation.**

I. Introduction

IT is known that the acquisition device for neural signal recording is one of the most important components in a biomedical electronic system. In the acquisition device, the Front-End Amplifier (FEA) is one of the key elements, which senses and amplifies the neural signals such as Electrocorticography (ECoG), Electrocardiogram (ECG), action potential, local field potential (LFP) etc., through electrode-tissue interfaces. Since the amplitude of neural signals is very small and the electrodes are easily interfered by external noise sources like 60-Hz noise from power lines or other disturbance sources, a low-noise FEA is required. With the increasing number of input electrodes required for clinical and implant applications, a FEA must meet the requirements of low power consumption and small chip area. The required low-pass cutoff frequency for neural signals varies from several hundred Hz to kilo Hz whereas the required high-pass cutoff frequency is below 0.1 Hz. Thus the low-pass cutoff frequency of FEAs should be adjustable. Moreover, the amplitude of the dc input offset voltage caused by the electrode-tissue interface varies with both material and size of electrodes. It must be eliminated to prevent the saturation of FEAs while amplifying neural signals below 0.1 Hz.

To reject the dc offset, the AC coupled techniques are proposed in some voltage-mode FEAs. In [1]–[3], MOS-bipolar or MOS pseudo resistors are adopted to realize ultra-large resistances which are highly dependent on the voltage across them. This causes large signal distortions and large variations of high-pass filter characteristics. Moreover, a reset signal is required [3] to reset the pseudo resistor and keep the bias condition stable. This makes the circuit design more complicated and the periodic reset signal causes the switched-capacitor effect which degrades the high-pass cutoff frequency. On the other hand, large external capacitors are used to achieve a high-pass cutoff frequency below 1 Hz [4], [5]. However, the use of discrete component increases the size of acquisition devices and limits the use of devices in implantable applications.

Generally, the internal nodes in current-mode circuits have low impedance characteristics and low voltage swings. Thus power supply voltage can be reduced to decrease the power consumption. The voltage noise is inversely proportional to dc operating current whereas the current noise is proportional to dc operating current. Thus current-mode circuits can achieve low noise under low power consumption.

Several current-mode circuits [6], [7] have been proposed for amplifier applications. In [6], a CMOS front-end amplifier for photo-current acquisition is presented with a feedback loop consisted of a sample-and-hold stage, an error amplifier, and a sinking device to bypass the flowing-out dc current. In [7], a trans impedance amplifier (TIA) consisted of an integrator followed by a differentiator is proposed to amplify the current signals of nanodevices. The dc offset current flows into the low-frequency feedback path and is rejected without affecting the in-band signal. However, the high-pass cutoff frequency (100 Hz–1 kHz) is too high for neural signals. The power dissipation is 45 mW which is not suitable for low-power FEAs.

In this paper, a new low-power current-mode front-end amplifier (CMFEA) for neural signal recording is proposed. In

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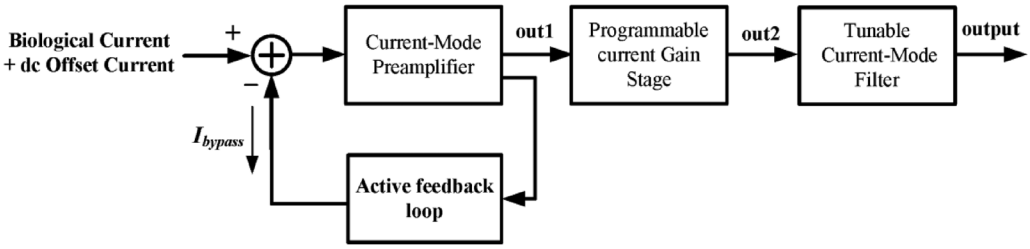


Fig. 1. Block diagram of the proposed current-mode front-end amplifier (CMFEA).

the proposed CMFEA, the biological signal current flowing in the input electrode-tissue interface as generated by the biopotential signal, is sensed and amplified. The proposed CMFEA can retain the advantages of low power consumption and low power supply in current-mode circuits. It also has a good noise rejection capability. As compared to the voltage-mode amplifiers, neither ultra-high value pseudo resistors with reset signals nor external large capacitors are required. Moreover, the current preamplifier with the cancellation feedback loop is designed to bypass the dc offset current generated by the electrode-tissue interface so that the dc offset current does not affect the amplifier operation.

The proposed CMFEA is designed and fabricated in 0.18-μm CMOS technology. The measurement results show that the high-pass cutoff frequency of 0.3 Hz can be achieved whereas the low-pass cutoff frequency can be adjusted from 1 kHz to 10 kHz. The measured input-referred current noise density is 153 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$. The power dissipation is 13 μW at 1-V power supply. The chip area is 0.576 mm^2 with 0.076 mm^2 of the core CMFEA circuit. The animal test on the ECoG signal recording of epileptic Long-Evan rats is demonstrated. These experimental results have verified that the proposed CMFEA is a potential solution for neural signal recording systems.

II. Circuit Design

The architecture of the proposed CMFEA is shown in Fig. 1 which consists of a current-mode preamplifier with an active feedback loop, a programmable current gain stage, and a tunable current-mode filter. The first stage is the current-mode preamplifier designed to amplify the in-band current signals. The incorporated active feedback loop is operated at a very low frequency to bypass the dc offset current generated from the electrode-tissue interface. The second stage is the programmable current amplifier which provides further amplification and adjustable signal gain for different neural signals. The third stage is a tunable current-mode filter. Its low-pass cutoff frequency is adjustable from 1 kHz to 10 kHz. A TIA is designed to convert the output current signal to voltage for measurement.

A. Current-Mode Preamplifier

Since the noise of the first stage is the dominate noise source, a current-mode preamplifier with low dc current is used as the first stage to suppress the noise contributed by this stage [8]. The structure of the current-mode preamplifier with low dc current is shown in Fig. 2(a) [8]. The operational amplifier $\mathrm{OP_1}$ is designed with a two-stage topology as shown in Fig. 2(b) where the aspect ratio of $\mathrm{M_1(M_3)}$ is identical to that of $\mathrm{M_2(M_4)}$. In

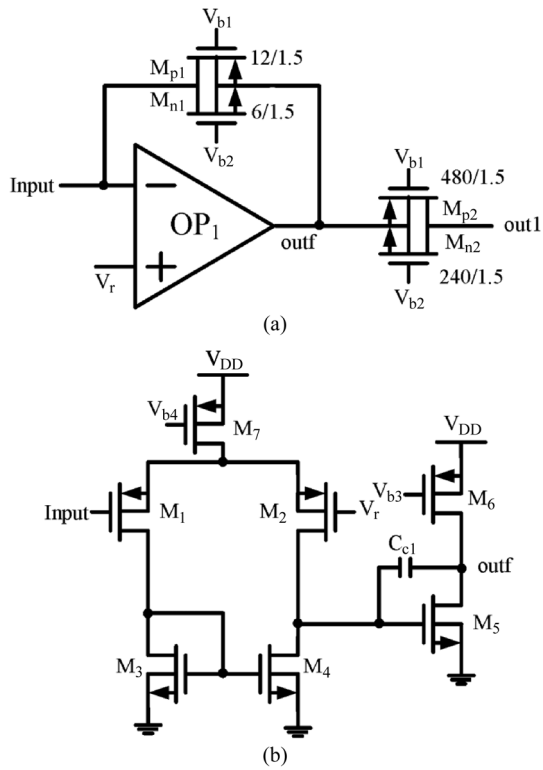


Fig. 2. (a) Structure of current-mode preamplifier. (b) Circuit schematic of $\mathrm{OP_1}$.

Fig. 2(a), the dc voltages of the input node and the node outf are set to $\mathrm{V_r = 1/2\ V_{DD}(0.5\ V)}$ via the negative feedback loop of $\mathrm{OP_1}$. The voltage of out1 is also set to $\mathrm{V_r}$ via the negative feedback loop in the next stage. As a result, the dc drain-source voltages of $\mathrm{M_{n1}}$, $\mathrm{M_{n2}}$, $\mathrm{M_{p1}}$, and $\mathrm{M_{p2}}$ are kept at 0 V. With $\mathrm{V_{b1} = 0.3\ V}$ and $\mathrm{V_{b2} = 0.7\ V}$, all devices are operated at a very low dc current in the linear subthreshold region as resistors. Since the channel lengths of $\mathrm{M_{p1}(M_{n1})}$ and $\mathrm{M_{p2}(M_{n2})}$ are the same, the resistance ratio of $\mathrm{M_{p2}(M_{n2})}$ to $\mathrm{M_{p1}(M_{n1})}$ is equal to the channel width ratio of $\mathrm{M_{p2}(M_{n2})}$ to $\mathrm{M_{p1}(M_{n1})}$ which is designed to be 40. With a small-signal input current $\mathrm{i_1}$ flowing on $\mathrm{M_{p1}/M_{n1}}$, the small-signal voltage across $\mathrm{M_{p1}/M_{n1}}$ is the same as that of $\mathrm{M_{p2}/M_{n2}}$. Thus the current $\mathrm{i_2}$ on $\mathrm{M_{p2}/M_{n2}}$ is equal to 40 $\mathrm{i_1}$ and a current gain of 40 can be obtained. The current-mode preamplifier in Fig. 2(a) has low input impedance and distortion.

In the $\mathrm{OP_1}$ circuit of Fig. 2(b), $\mathrm{M_1 - M_2}$ form an amplifier with the current-mirror load $\mathrm{M_3 - M_4}$. Using PMOS as input devices can reduce the flicker noise. The $\mathrm{OP_1}$ is designed

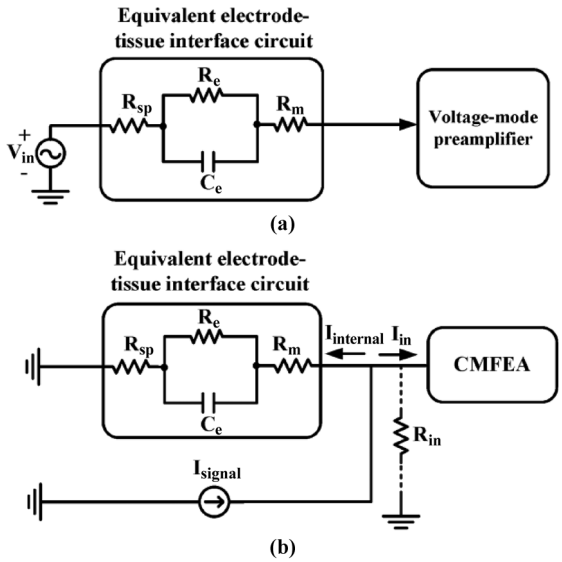


Fig. 3. (a) The equivalent electrode-tissue interface circuit with the voltage-mode preamplifier. (b) Norton equivalent circuit of the electrode-tissue interface circuit with the CMFEA.

to achieve low offset voltage with suitable gain. Therefore, the sizes of $\mathrm{M}_1 - \mathrm{M}_4$ which are the main contributions of offset are enlarged to decrease the offset caused by device mismatch.

The equivalent electrode-tissue interface circuit with the voltage-mode preamplifier is shown as Fig. 3(a). Its Norton equivalent circuit with the CMFEA is shown as Fig. 3(b). In Fig. 3, $\mathrm{R_{sp}}$ is the spreading resistance between electrolyte and tissue, $\mathrm{R_e}$ and $\mathrm{C_e}$ are the resistance and capacitance of the electrode-tissue interface, respectively, $\mathrm{R_m}$ is the resistance of the electrode, $\mathrm{V_{in}}$ is the neural potential signal, $\mathrm{R_{in}}$ is the input impedance of the CMFEA, $\mathrm{I_{in}}$ is the current signal injecting into the current-mode preamplifier, and $\mathrm{I_{internal}}$ is the internal signal current flowing through the interface circuit in Fig. 3(b). Unlike voltage-mode preamplifiers whose input impedance should be designed as high as possible, the input impedance of current-mode preamplifier should be designed as low as possible to sense the input current signal. Thus the current signal generated by the neural signal on the input electrode-tissue interface can flow into the current-mode preamplifier with less degradation as can be seen from Fig. 3(b).

Note that the recorded current signal is generated by the neural potential signal on the input electrode-tissue interface and dependent on interface impedance. It can be used directly to extract physiological features like epileptic seizure occurrence. The recorded current signal can also be converted into the corresponding neural potential signal by using an analog TIA with the transimpedance equivalent to the electrode interface impedance.

Since the measured equivalent impedance of electrode is about 1 MΩ at dc and 100 kΩ at 10 kHz, the input resistance of the current-mode preamplifier is designed to be 4.6 kΩ which is determined by R_{Mn1}, R_{Mp1}, and the gain of $\mathrm{OP_1}$ as

$$R_{in} = \frac{R_{Mn1} \| R_{Mp1}}{A_{OP1}} \tag{1}$$

where R_{Mn1} and R_{Mp1} are the turn-on resistance of $\mathrm{M_{n1}}$ and $\mathrm{M_{p1}}$, and A_{OP1} is the gain of $\mathrm{OP_1}$ which is designed to be 60 dB.

In the normal AC coupled voltage-mode preamplifier, the voltage signal in the kHz frequency range generates displacement current flowing in the electrode and input capacitor circuit. The displacement current is in the range of nA when the kHz voltage signal in the range of mV. In the proposed current-mode preamplifier, the input signal current is also in the range of nA when the kHz voltage signal in the range of mV.

The input referred current noise I_n of the current-mode preamplifier can be expressed as [8]

$$\overline{I_n^2} = \left[\frac{kT}{3}(\mathrm{g}_{m\_Mn1} + \mathrm{g}_{m\_Mp1}) + (2\pi f)^2 C_{in}^2 \overline{V_{op}^2}\right] \Delta f \tag{2}$$

where k is the Boltzmann constant, T is the absolute temperature, g_m is the transconductance of MOS device, f is the signal frequency, C_{in} is the input capacitance of $\mathrm{OP_1}$, V_{op} is the input referred voltage noise of $\mathrm{OP_1}$, and Δf is the bandwidth of the preamplifier.

The first term in (2) is mainly contributed by $\mathrm{M_{p1}}/\mathrm{M_{n1}}$ and proportional to the transconductance. Thus, low dc currents in the devices $\mathrm{M_{p1}}/\mathrm{M_{n1}}$ result in a low noise performance. Since $\mathrm{M_{p2}}/\mathrm{M_{n2}}$ are operated at low dc currents and their noise contribution to the equivalent input noise is divided by the gain of 40, the noise influence of $\mathrm{M_{p2}}/\mathrm{M_{n2}}$ is negligible.

In the second term in (2), V_{op} is contributed by the flicker noise $V_{n,op\_flicker}$ and the thermal noise $V_{n,op\_thermal}$ of the devices in $\mathrm{OP_1}$, which can be expressed as

$$\overline{V_{n,op}^2} = \overline{V_{n,op\_thermal}^2 + V_{n,op\_flicker}^2} \tag{3}$$

$$\overline{V_{n,op_{thermal}}^2} = \frac{16kT}{3}\frac{1}{\mathrm{g}_{m1}^2} \times \left[\mathrm{g}_{m1} + \mathrm{g}_{m3} + \frac{\mathrm{g}_{m5} + \mathrm{g}_{m6}}{2\mathrm{g}_{m5}^2 (r_{o2} \| r_{o4})}\right] \tag{4}$$

$$\approx \frac{16kT}{3}\frac{1}{\mathrm{g}_{m1}^2}[\mathrm{g}_{m1} + \mathrm{g}_{m3}] \tag{5}$$

$$\overline{V_{n,op\_flicker}^2} = \frac{2K_p}{W_1 L_1 C_{ox} f} + \frac{2K_n}{W_3 L_3 C_{ox} f}\left(\frac{\mathrm{g}_{m3}}{\mathrm{g}_{m1}}\right)^2 + \frac{1}{\mathrm{g}_{m2}^2 \mathrm{g}_{m5}^2 (r_{o2} \| r_{o4})} \times \left[\frac{\mathrm{g}_{m5}^2 K_n}{W_5 L_5 C_{ox} f} + \frac{\mathrm{g}_{m6}^2 K_p}{W_6 L_6 C_{ox} f}\right] \tag{6}$$

$$\approx \frac{2K_p}{W_1 L_1 C_{ox} f} + \frac{2K_n}{W_3 L_3 C_{ox} f}\left(\frac{\mathrm{g}_{m3}}{\mathrm{g}_{m1}}\right)^2 \tag{7}$$

$$= \frac{2}{C_{ox} f}\left[\frac{K_p}{W_1 L_1} + \frac{\mu_n K_n L_1}{\mu_p W_1 L_3^2}\right] \tag{8}$$

where r_o, W, L, C_{ox}, and μ are the output resistance, width, length, gate capacitance density, and the mobility of the MOS device, respectively, and K is the process-dependent constant of flicker noise. From (5), the thermal noise can be reduced by increasing $\mathrm{g_{m1}}$. Thus, the bias current in the first stage of $\mathrm{OP_1}$ is increased to increase $\mathrm{g_{m1}}$ and reduce the thermal noise contributed to the preamplifier. Since the flicker noise is inversely

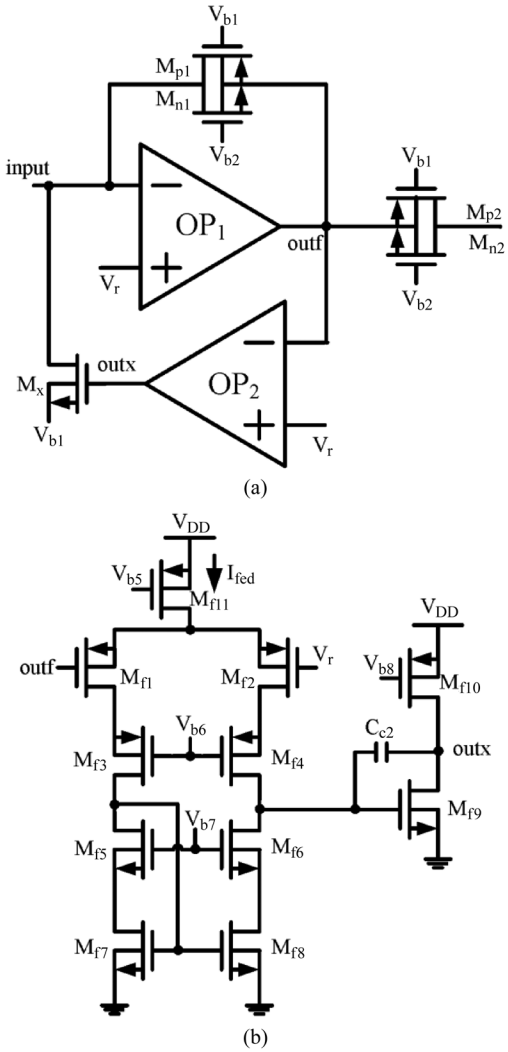


Fig. 4. (a) Structure of the feedback loop. (b) Circuit schematic of OP_2.

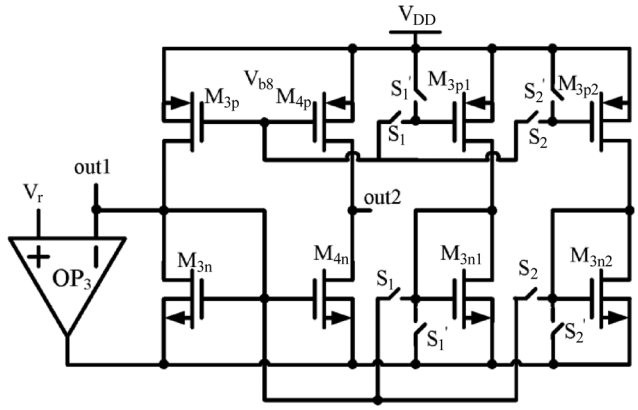


Fig. 5. Circuit structure of the programmable current gain stage.

proportional to L_3^2 in (8), M_3 is designed with a long device channel length to reduce the flicker noise.

To avoid the effect of long length in limiting the signal swings, M_3 is designed with a large device width W_3. Since the input noise is independent of W_3, large W_3 does not increase the noise. W_1 is also designed to be larger to reduce both thermal and flicker noises.

B. Active Feedback Loop

Fig. 4(a) shows the active feedback loop with the current-mode preamplifier. The loop consists of the transistor M_x and the operational amplifier OP_2. The purpose of the feedback loop is to take the flowing-in dc offset current that could exist in the electrode-tissue interface. In the experimental chip design, only one direction of dc offset current is considered. The loop for the flowing-out one can be similarly designed.

In the proposed current-mode preamplifier, the input dc offset current is determined by the resistance of the electrode-tissue interface and the input resistance of the preamplifier as well as the dc offset voltage across of the electrode-tissue interface and the input dc offset voltage of the preamplifier. Thus both dc offset voltages should be kept as small as possible to minimize the input dc offset current. With appropriate op amp design and animal test setup, the total input dc offset voltage can be minimized to tens of uV. The total dc resistance of the preamplifier input loop is in the mega ohm order. Thus, the input dc offset current can be minimized to the pA range to avoid the damage to the tissue or electrodes.

When the input dc offset current flows into the preamplifier, the output voltage of OP_2 is changed to drive M_x which generates a similar dc current to bypass the input dc offset current. The amount of the bypass current I_{bypass} can be derived as

$$I_{bypass} = \frac{R_{M1} g_{mx} A_{fed}}{1 + R_{M1} g_{mx} A_{fed}} I_{OS} \tag{9}$$

where R_{M1} is the resistance of M_{n1} and M_{p1}, g_{mx} is the transconductance of M_x, A_{fed} is the gain of OP_2, and I_{OS} is the input dc offset current. The feedback loop is designed to bypass 99% of input dc offset current.

The amplifier used in the feedback loop is shown in Fig. 4(b) where the telescopic architecture with a common-source second stage is used. High output resistance of telescopic architecture with the miller compensation capacitor C_{c2} can achieve a very low 3-dB cutoff frequency of 0.24 mHz. The high-pass cutoff frequency f_{HP} of the overall preamplifier in Fig. 4(a) can be derived as

$$f_{HP} = R_{M1} g_{mx} A_{fed} f_{fed} = R_{M1} \frac{I_{OS}}{nU_T} \frac{I_{fed}}{2\pi n U_T} \frac{1}{C_{c2}} \tag{10}$$

where f_{fed} is the low 3-dB cutoff frequency of OP_2, I_{fed} is the dc bias current of input stage in OP_2, n is the weak inversion slope factor, and U_T is the thermal voltage. As can be seen from (10), f_{HP} varies with g_{mx} which depends on I_{OS} directly. The f_{HP} variation can be compensated by adjusting I_{fed} to keep the high-pass cutoff frequency fixed for different input dc offset currents.

The output noise of the OP_2 in Fig. 4(a) contributes the noise current to the input node through M_x. But since M_x is designed to be at zero operating current, the generated noise current is very small. Thus, the noise contribution of OP_2 and M_x can be neglected.

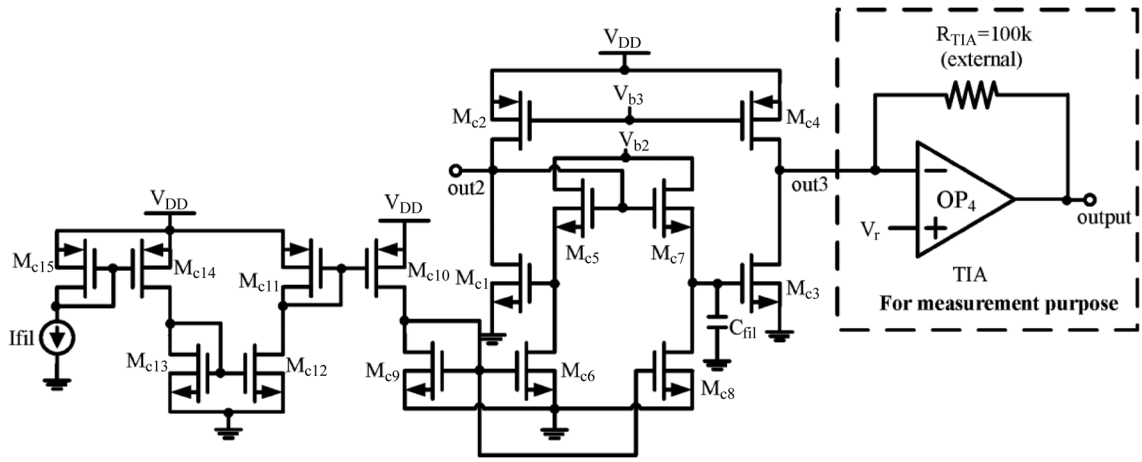


Fig. 6. Schematic of the first-order log-domain current-mode filter.

C. Programmable Current Gain Stage

Since the output dc voltage of out1 in the proposed current preamplifier of Fig. 2(a) has to be clamped to $\mathrm{V_r}$ by the next stage, a programmable current gain stage incorporated with a negative feedback loop is proposed as the second stage. The structure of the programmable current gain stage is shown in Fig. 5. Since the noise of the second stage is not the dominate source, the multi-stage current mirror is designed as the programmable current gain stage. In Fig. 5, $\mathrm{OP_3}$ has a two-stage structure as shown in Fig. 2(b). It is used not only to clamp the voltage of out1, but also to reduce the input impedance of the stage. This also reduces the variations of input impedance with different input signal currents so that the signal distortion can be minimized and the linearity can be improved. The input impedance of the programmable current gain stage can be derived as

$$R_{in2} = \frac{1}{A_{OP3} g_{m3n}} \tag{11}$$

$$= \frac{nU_T}{A_{OP3}(I_{bias} + I_{in})} \tag{12}$$

where A_{OP3} is the gain of $\mathrm{OP_3}$ and $\mathrm{g_{m3n}}$ is the transconductance of $\mathrm{M_{3n}}$. $\mathrm{M_{3n}}$ is operated in the subthreshold region, thus the input impedance can be expressed as (12) where I_{bias} is the dc bias current in $\mathrm{M_{3n}}$, and I_{in} is the input current signal flowing in to the programmable current gain stage. It can be seen from (12) that the input impedance is reduced by a factor of A_{OP3}. Thus the current injection efficiency can be increased.

The current amplification ratio is determined by the MOS size ratio. When $\mathrm{S_1}$ turns on, the parallel-connection number of $\mathrm{M_{3n}}$ and $\mathrm{M_{3p}}$ is increased and the current gain is reduced. On the other hand, when $\mathrm{S_1}$ turns off, the transistors of $\mathrm{M_{3p1}}$ and $\mathrm{M_{3n1}}$ are turned off and the current gain is increased. With digital control signals on the switches $\mathrm{S_1}$ and $\mathrm{S_2}$, the number of parallel-connection transistors is selected to adjust the current gain. The current gain can be adjusted from 12 dB to 24 dB in four steps.

D. Tunable Current-Mode Filter

A first-order log-domain current-mode filter is used as shown in Fig. 6 [9] where the transistors $\mathrm{M_{c1}}$, $\mathrm{M_{c3}}$, $\mathrm{M_{c5}}$, and $\mathrm{M_{c7}}$ are operated in the weak inversion region. The low-pass cutoff frequency f_{LP} is described as

$$f_{LP} = \frac{I_{fil}}{2\pi n U_T C_{fil}} \tag{13}$$

where I_{fil} is the current of $\mathrm{M_{c7}}$ and $\mathrm{M_{c8}}$, and C_{fil} is the capacitor used in the current-mode filter. From (13), the low-pass cutoff frequency of the current-mode filter can be designed at a very low frequency by applying a low I_{fil} without the use of large capacitance. By adjusting I_{fil}, the low-pass cutoff frequency of the CMFEA can be tuned from 1 kHz to 10 kHz.

In Fig. 6, the TIA with a 100 k external resistor is used to convert the output current signal to voltage signal for measurement purpose, since there is no measurement equipment available to measure the current signal directly. In the integration of the proposed CMFEA with ADC, the TIA with the external resistor is not required.

III. Experiment Results

The proposed CMFEA has been designed and fabricated by TSMC 0.18-μm CMOS technology. The chip photograph of the fabricated circuit is shown in Fig. 7. The total chip area is $0.576\,\mathrm{mm^2}$ including the ESD pad. The chip areas of the core circuit are $0.076\ \mathrm{mm^2}$ and $0.135\ \mathrm{mm^2}$ without and with the TIA, respectively.

In the measurement setup for functionality test, the input voltage signal is fed into the discrete circuit which is the same as the equivalent electrode-tissue interface circuit as shown in Fig. 3(a). Thus, the voltage signal can be converted into current signal through the discrete circuit and fed into the CMFEA.

The measured frequency response is shown in Fig. 8 where low-pass and high-pass cutoff frequencies are both tunable. The low-pass cutoff frequency is located in the range of 1 kHz to 10 kHz with $\mathrm{I_{fil}} = 0.1\ \mathrm{nA}$ to 1 nA as shown in Fig. 8(a) and Fig. 8(b), respectively. The high-pass cutoff frequency can be as low as 0.3 Hz when the input dc current is 5 nA. The maximum gain is 55.9 dB. The maximum input dc offset current which can be bypassed by the active feedback loop is 15 nA with the high-pass cutoff frequency remains below 1 Hz.

The measurement result of the THD is shown in Fig. 9 where the input signal has the maximum operation frequency (10 kHz)

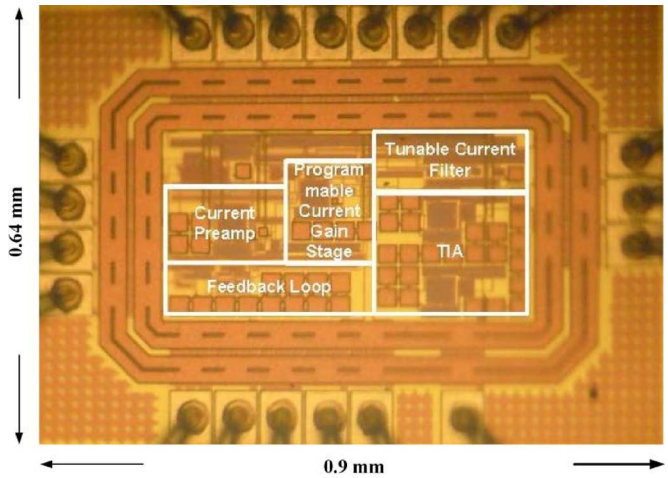


Fig. 7. Chip photograph of the fabricated CMFEA.

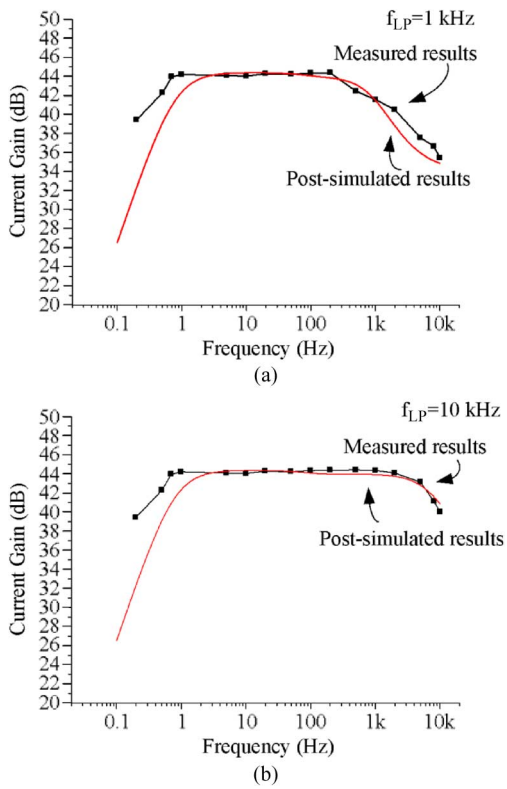


Fig. 8. The measured frequency response with (a) 1 kHz low-pass cutoff frequency and (b) 10 kHz low-pass cutoff frequency.

and 20 nAp-p peak-to-peak amplitude. It can be seen that under the maximum input signal 20 nAp-p which is much higher than the normal neural signal, the THD is 1.03%. Thus the proposed CMFEA has a low THD. The measured output current noise from 1 Hz to 10 kHz is shown in Fig. 10. The measured input-referred current noise is 15.3 $\mathrm{pA_{rms}}$. By using the maximum input current of 7.07 nArms, the SNR or maximum dynamic range of the CMFEA can be calculated as $20\log(7.07\ \mathrm{nA}/15.3\ \mathrm{pA}) = 53.29\ \mathrm{dB}$.

The fabricated CMFEA chip is applied to the measurement of ECoG signals of Long-Evan rats. Fig. 11 shows the measurement setup of the animal test where the recording electrode is

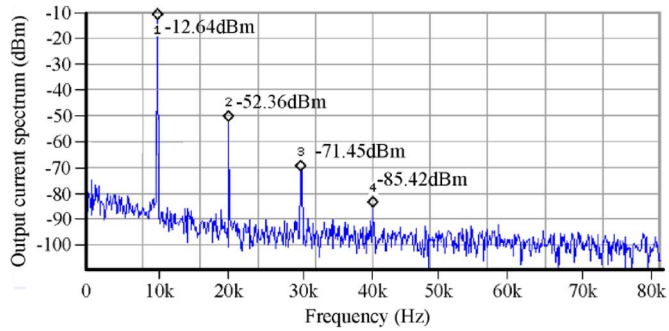


Fig. 9. The measured frequency spectrum of output current when Iin $= 20\ \mathrm{nA_{p-p}}$ at 10 kHz.

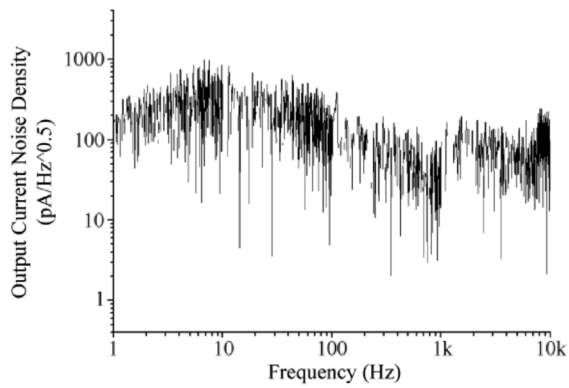


Fig. 10. The measured output current noise from 1 Hz to 10 kHz.

connected to the CMFEA with wire. The ECoG signal is sensed and amplified by the CMFEA and the amplified signal is measured by the oscilloscope.

Figs. 12(a) and (b) show the ECoG measurement results of the animal test in both time and frequency domains with the gain of CMFEA set to 55.9 dB. Fig. 12(a) shows the measured normal ECoG signal. As can been seen from Fig. 12(a) that the amplitude variations of the transient waveform are small and no specific component is shown on the spectrum. Fig. 12(b) shows the measured ECoG signal when the rat has epileptic seizures. In Fig. 12(b), the corresponding input current is around 0.3 nA. As can be seen from the measured spectrum, the main frequency components are around 7.5 Hz and 15 Hz which are identical with the measurement results of voltage-mode amplifiers.

The experimental results are summarized in Table I with the comparisons to other reported voltage-mode FEAs. With the same bandwidth of 7 $\sim$ 10 kHz, the power consumption of the proposed current-mode front-end amplifier is less than other voltage-mode FEAs. The formula of the noise efficiency factor (NEF) is

$$NEF = V_{ni.rms}\sqrt{\frac{2I_{tot}}{4\pi U_T kTBW}} \tag{14}$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total supply current, and BW is the amplifier bandwidth. To calculate the NEF of the proposed CMFEA, the input noise current density referred to the input node of the electrode is converted to the input noise voltage density by multiplying the measured impedance of the electrode with $\mathrm{R_{sp}} = 10\ \mathrm{k\Omega}$, $\mathrm{R_e} =$

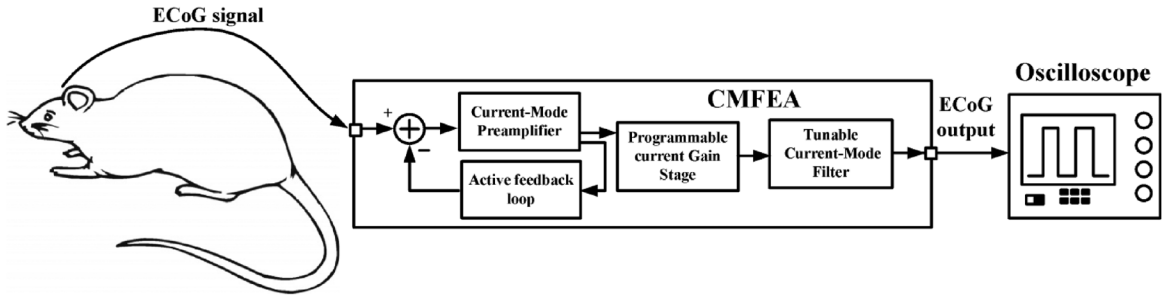
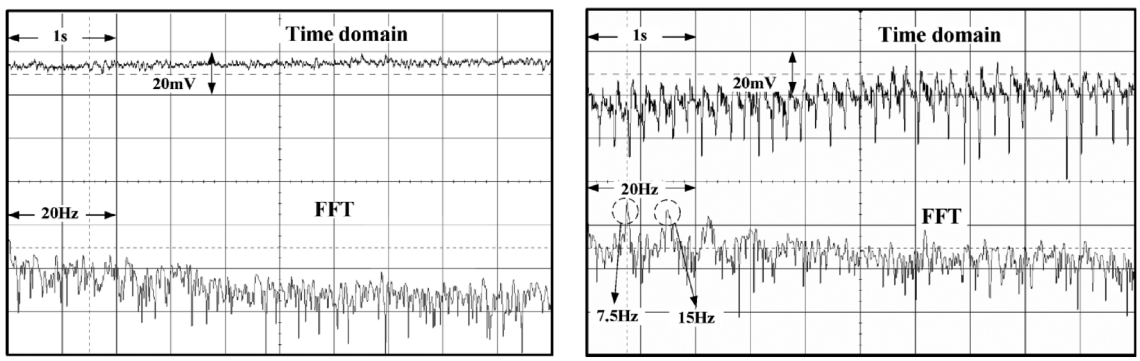


Fig. 11. The measurement setup of the animal test.



(a) (b)

Fig. 12. The measured ECoG signals of the rat when in the (a) normal state and (b) epileptic seizure state.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF FEAS

	This Work	[1]	[5]	[10]	[11]	[12]
Technology	0.18 μm CMOS	1.5 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS
Area[a](mm^2)	0.076[b]/0.135[c]	0.22	0.38	0.3	0.22	0.76
Topology	Current-mode	Voltage-mode	Voltage-mode	Voltage-mode	Voltage-mode	Voltage-mode
Supply Voltage (V)	1	±2.5	1.5	1	1.5	3.3
Power (μW)	13	80	7.5	3.5	26.9	11.5[f]/231[g]
Gain (dB)	44.5/50/55.9[d]	39.5[e]	40.8[e]	60[e]	51.9/57.4/59.9/ 65.6[e]	40~75[e]
Bandwidth (Hz)	0.3~1k-10k	0.025~7.2k	0.5, 10~100-400	0.2~100	1.1~12k	2.6~6.2k
Input-referred Noise (integration bandwidth)	15.3pArms/ 4.4μVrms[i] (10kHz)	2.2 μVrms (50kHz)	1.27μVrms (100Hz)	1.3 μVrms (100Hz)	3.12 μVrms (50kHz)	2.3[f]~2.9[g] Vrms (6kHz)
Large-value Resistor	None	Pseudo resistor	Pseudo resistor	Yes	Pseudo resistor	Pseudo resistor
External Capacitor	None	None	Yes	Yes	None	None
NEF	5.45[i] 0.10[j]	4	6.1	8.6	2.68[h]	5.1

a. Area per channel. b. w/o TIA. c. w/TIA. d. Current gain. e. Voltage gain. f. Bandwidth of 200 Hz. g. Bandwidth of 200–6.2 kHz. h. Only the first stage.
i. Referred to the input node of the electrode. j. Referred to the input node of the CMFEA.

900 kΩ, $C_e = 500$ pF and $R_m = 90$ kΩ as shown in Fig. 3(b). The calculated NEF of the CMFEA is 5.45. For the NEF referred to the input node of the CMFEA which is adopted in voltage-mode FEAs, the input impedance value of 4.6 kΩ and

NEF is 0.10. Unlike voltage-mode FEAs, the CMFEA has low input impedance which leads to low input noise voltage. Thus the calculated NEF of the CMFEA can be as low as 0.10.

IV. Conclusion

In this paper, a new CMOS current-mode front-end amplifier (CMFEA) for neural signal recording is proposed. In the proposed CMFEA, both bandwidth and current gain are all tunable for different neural signals. Through an active feedback loop incorporated with the first-stage current-mode preamplifier, the high-pass cutoff frequency can achieve 0.3 Hz and the dc offset current caused by electrode-tissue interface can be bypassed. No reset signal or ultra-high value pseudo resistor is needed in the CMFEA. The measured input referred current noise density is 153 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ with the bandwidth up to 10 kHz. The power dissipation is 13 μW at 1-V power supply. The proposed CMFEA is also applied to the animal test successfully to measure the epileptic ECoG of rats. The experimental results have demonstrated that the CMFEA is a promising solution for designing low-noise and low-power neural recording amplifiers.

Acknowledgment

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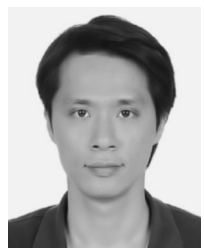

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