NeuroBus - Architecture for an Ultra-Flexible Neural Interface

Markus Sporer, *Graduate Student Member, IEEE*, Ioana-Georgiana Vasilaş, Ahmed Adžemović, Nicolas Graber, *Graduate Student Member, IEEE*, Stefan Reich, *Member, IEEE*, Calogero Gueli, Max Eickenscheidt, Ilka Diester, Thomas Stieglitz, *Fellow, IEEE*, and Maurits Ortmanns, *Senior Member, IEEE*

(Invited Paper)

***Abstract*—This article presents the system architecture for an implant concept called *NeuroBus*. Tiny distributed direct digitizing neural recorder ASICs on an ultra-flexible polyimide substrate are connected in a bus-like structure, allowing short connections between electrode and recording front-end with low wiring effort and high customizability. The small size (344 μm $\times$ 294 μm) of the ASICs and the ultraflexible substrate allow a low bending stiffness, enabling the implant to adapt to the curvature of the brain and achieving high structural biocompatibility. We introduce the architecture, the integrated building blocks, and the post-CMOS processes required to realize a *NeuroBus*, and we characterize the prototyped direct digitizing neural recorder front-end as well as polyimide-based ECoG brain interface. A rodent animal model is further used to validate the joint capability of the recording front-end and thin-film electrode array.**

***Index Terms*—Neural recording, biomedical implant, electrophysiology, direct digitizing neural recorder.**

Manuscript received 6 October 2023; revised 20 December 2023; accepted 8 January 2024. Date of publication 16 January 2024; date of current version 29 March 2024. This work was supported in part by the German National Science Foundation DFG under Grants OR 245/15-1 and EI 1078/1-1 and in part by the European School of Network Neuroscience (euSNN). This paper was recommended by Associate Editor H. Jiang. *(Corresponding author: Markus Sporer.)*

This work involved human subjects or animals in its research. Approval of all ethical and experimental procedures and protocols was granted by the Regierungspräsidium Freiburg under Application No. TVA G-20-65, and performed in line with the 2010/63/EU directive.

Markus Sporer, Nicolas Graber, Stefan Reich, and Maurits Ortmanns are with the Institute of Microelectronics, University of Ulm, 89081 Ulm, Germany (e-mail: markus.sporer@uni-ulm.de; nicolas.graber@uni-ulm.de; stefan.reich@uni-ulm.de; maurits.ortmanns@uni-ulm.de).

Ioana-Georgiana Vasilaş and Thomas Stieglitz are with the BrainLinks-BrainTools//IMBIT, 79110 Freiburg, Germany, and also with the Department of Microsystems Engineering (IMTEK), University of Freiburg, 79110 Freiburg, Germany (e-mail: ioana-georgiana.vasilas@brainlinks-braintools.uni-freiburg.de; thomas.stieglitz@imtek.uni-freiburg.de).

Ahmed Adžemović and Ilka Diester are with the BrainLinks-BrainTools//IMBIT, 79110 Freiburg, Germany, and also with the Faculty of Biology, University of Freiburg, 79110 Freiburg, Germany (e-mail: ahmed.adzemovic@biologie.uni-freiburg.de; ilka.diester@biologie.uni-freiburg.de).

Calogero Gueli is with the BrainLinks-BrainTools//IMBIT, 79110 Freiburg, Germany, and also with the Department of Microsystems Engineering (IMTEK), University of Freiburg, 79110 Freiburg, Germany (e-mail: calogero.gueli@imtek.uni-freiburg.de).

Max Eickenscheidt is with the Department of Microsystems Engineering (IMTEK), University of Freiburg, 79110 Freiburg, Germany (e-mail: meickenscheidt@neuroloop.de).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TBCAS.2024.3354785.

Digital Object Identifier 10.1109/TBCAS.2024.3354785

I. Introduction

THE emergence of integrated neural interfaces significantly facilitated the recording of neural activity, giving researchers detailed insights into brain functions [1] but also contributing to the development of potential bidirectional interfaces for the treatment of neurological disorders [2], [3], [4]. Bidirectional interfaces for complex interactions as in brain-computer-interfaces to control assistive devices are even more challenging [5], especially when transferring the laboratory settings to home-use. Advances in circuit design and technology allow both, to implement power efficient neural recorder front-ends with direct digitization on smallest areas [6], [7], [8] and increasing the channel count [6], [9], [10] in neural implants. While mature CMOS nodes can suffer from increased silicon area and power consumption due to extensive digital circuitry [11], they can be preferable if recorders are potentially co-integrated with stimulation [12] and also offer a significant cost advantage since biomedical implants are often specialized products with a rather low production volume.

A conventional design [12] of an epicortical (ECoG) neural recording interface (Fig. 1(a)) consists of a sealed base unit which connects to one or multiple electrode arrays. The sealed base unit is either implanted in the cranial bone [14] or in the chest as in pacemakers and contains the neural recording interface with digitization as well as additional circuitry for wireless communication/power transfer and power management. A majority of this functionality can be integrated on a single ASIC [9], allowing to share resources for, e. g., power management, digitization and readout of the digitized data between all recording channels. Consequently, integrating all recording channels on one central ASIC is beneficial in terms of power consumption and also allows less strict area constrains since the sealed base unit is typically implanted in regions of the body which are not in direct contact with the brain tissue and the electrode array like the cranial bone. The conventional implant concept typically requires a direct wired connection between electrode and neural recording front-end which is located in

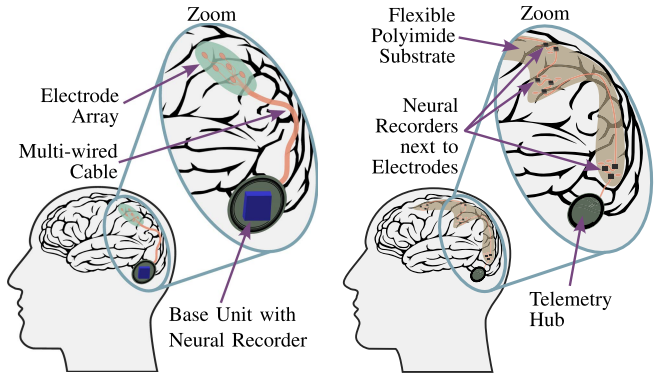
the base unit [12]. These wired connections scale with the total number of channels and are combined into multi-wire cables that increase in diameter and decrease in flexibility as the number of channels increases. These multi-wire cables can be particularly vulnerable for crosstalk between the high impedance electrode connections, especially if the distance between electrode array and base unit is large and a long multi-wire cable is required.

Active neural probe concepts [15], [16], [17] based on silicon technology with integrated CMOS electronics allow direct signal conditioning and digitization close to the recording site, thus drastically lowering the connection length between electrode and signal conditioning circuitry. They are established tools in fundamental neuroscience and use multiplexing techniques to reduce the number of interconnect lines and therefore stay relatively small in their cross-sectional areas and allow high integration densities and channel counts. They however require customized digital circuitry for data readout which can dominate the power consumption per recording site [16]. This concept of miniaturization, however, suffers from a lack of flexibility to distribute the channels to different, application dependent regions of interest. The large mechanical mismatch between the silicon devices and the brain can pose an increased risk of tissue damage and scarring [18], [19], [20], implying poor long-term functionality. These devices are equipped with head mounted connectors [16], [21] since they are rather intended for short to medium term fundamental neuroscience applications [17] than for translational research and chronic use in humans.

Free-floating single-channel neural recording interfaces were proposed in [22], [23], [24] and work wirelessly. Power and data transfer are based on ultrasonic or inductive links, respectively. These types of neural recorders offer superior flexibility since they can be placed directly at the region of interest without preceding customization steps. While the implant itself is freely floating inside the body, a larger implanted resonator coil enclosing the implant is required for inductive power transfer [23], [24]. This limits the free placement of the implant and significant power losses can increase local tissue temperature due to a low power transmission efficiency [23], [24]. Ultrasonic based links bypass the limitations of a resonator coil but transfer the neural signal itself in the analog domain, making it prone to crosstalk and require cumbersome trimming or hardwiring of implants for multichannel recordings with several distributed devices [22].

The encapsulation of many early prototype developments, e. g. [22], [25], relies on parylene and epoxy. While encapsulation with these materials is simple, it limits the longevity of the system and the functionality of the electronics by its non-hermetic nature. Ingress of moisture causes passivation layer degradation and corrosion of conductive parts of standard CMOS electronics. Therefore, CMOS electronics need hermetic encapsulation for long-term function. Multi-layered stacks combining atomic layer deposition (ALD) with inorganic layers are used for hermetic encapsualtion on the die level [24], [26], [27] and ensure longevity of electronics embedded in flexible materials.

A newly proposed implant concept called *NeuroBus* [13] comes with a modular and distributed design (Fig. 1(b)). ASICs which are hermetically sealed on the die level, are embedded into a thin mechanically flexible polyimide (PI) foil in close vicinity to the electrode sites. This modular approach allows customized placement of each ASIC within the post-CMOS process technology, enabling versatile manufacturing of customized application specific neural implants. We aim for a high level of structural biocompatibility, and thus aim towards smallest ASICs that can be embedded into the ultra-flexible PI foil. Separation of one larger into several smaller ASICs (μASICs) results in decreased bending stiffness, reduces the foreign body reaction (FBR) and thus scarring which separates the recorder from the source [28]. Power distribution, communication with the spatially distributed ASICs and wireless data transfer [29] with an extracorporeal receiver is managed by a centralized electronics *Telemetry Hub*. The miniaturization of the *small* μASICs determines how well NeuroBus can be adopted to various sizes and curvature of the target brain region, i. e. the species which is subject of investigation [30]; thus, as long as handling can be realized, the smaller the better.



(a) Common implant concept. (b) NeuroBus implant concept.

Fig. 1. Conventional and proposed *NeuroBus* implant concept based on [13].

The *NeuroBus* concept was briefly introduced [13], where mainly the inter-μASIC communication bus was explained. This work gives a detailed description into the system architecture with its underlying design decisions and presents the prototyped building blocks of the system. The general concept of μASIC placement and encapsulation into application specific designs is given, while details for process engineers can be found in [31]. A validation of the NeuroBus concept has been performed in a hybrid system assembly to prove adequacy of all interface specifications and performance of the neural recoders in an acute rodent model.

II. NeuroBus System Overview

A. System Overview & Requirements

The NeuroBus implant concept aims for long-term implantation and the ability to cover larger areas of the human brain which requires high structural biocompatibility and longevity. We therefore propose the use of a thin mechanically compliant PI substrate material which is able to conform to the curvilinear structures of the brain [30]. Small and distributed application specific integrated circuits (μASICs) will be embedded into this substrate (Fig. 2). The μASICs are manufactured in a 180 nm Si-based CMOS process to achieve much higher integration

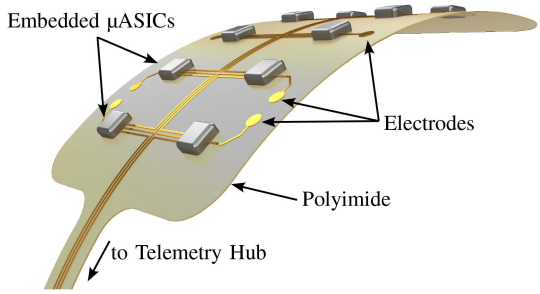


Fig. 2. Visualization of a simplified NeuroBus implant. The shape of the PI substrate and placement of μASICS/electrodes can be customized depending on the application scenario.

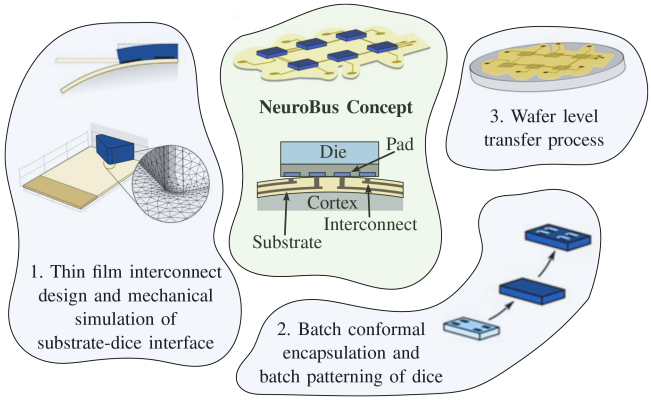


Fig. 3. NeuroBus system considerations, adapted from [31], [35]. Size and orientation of CMOS dice determine interface stress to the substrate. Adequate routing of interconnect lines and contact pads helps to reduce interfacial stress at electrical contact sites.

density compared to foil-based flexible circuits [32]. The miniaturization of the small μASICs determines how well NeuroBus can be adopted to various sizes and curvature of the target brain region, i. e. the species which is subject of investigation [30]; this manifests as conformability, a characteristic enabling the implant to establish intimate proximity to the brain without the need of applying external pressure. Such pressure, if applied through e. g. plugging and unplugging of connectors in case of a conventional implant, could potentially lead to undesired displacement of the neural prosthesis, particularly in conjunction with the pulsatile dynamics of the brain and therefore deliver unreliable signal readouts. It has been shown that thin, ultra-conformable arrays yield superior quality readings, allowing the recording of single-unit activity (spikes) [33] which is especially relevant for clinical application. Nonetheless, the synergistic integration of miniaturization, conformability and other physical attributes of the system such as the weight of external connectors can significantly reduce the stress exerted on the underlying tissue, consequently mitigating the formation of glial scar. In contrast to more rigid, non-conformable implants, such configurations remain stable on the brain's surface even beyond acute scenario [30].

Finite element models were previously described in [31], [34], [35] and are useful tools to derive geometric design considerations for the encapsulated μASIC, interconnect routing and pad distribution on the μASIC for best possible compliance of the whole system. It was therefore highlighted the importance of the edge radius fillet and thickness of the dice to improve the integrity of the structure on the substrate, increase the contact pad area and reduce stress. Consequently, a scalable microfabrication process has been developed to fabricate hybrid implants whereby multiple electrically interconnected μASIC can be batch-wise transferred into conformable PI substrates [31], [34], [35]. Fig. 3 summarizes important aspects of the NeuroBus system that have to be taken into consideration before and during the implementation of the system.

In addition to a high level of biocompatibility, application and patient specific design are key objectives of the NeuroBus implant. Thus, the number and placement of recording channels as well as the outline of the PI substrate can be flexibly chosen for each implant. The tiny μASICs can then be spatially distributed on the PI substrate [13] and embedded on the system level. The pitch of the μASICs is firstly determined by their own physical size. On PI foil, the pitch is rather determined by neuroscientific specifications of electrode diameter, pitch and size of electrodes, and is usually found in the range between 30 μm and 100 μm [30]. With the fact that electrodes can be routed closer to each other even though μASICs are limited in pitch by their own size, local clusters of electrodes can be realized with smallest, technology defined distance. Moreover, in a future version of μASICs multiplexing can be implemented, which will allow several electrodes to be digitized by a single μASIC, thus bringing the whole grid of electrodes to a pitch well below 100 μm.

The target silicon area for the μASICs is very limited in order to achieve structures which are compliant with low bending stiffness (structural biocompatibility) on the complete substrate. Hence all integrated building blocks need design for smallest chip area. While electrostatic discharge (ESD) events are of no concern in the implanted state, proper ESD protection must still be provided to minimize the risk of ESD damage during handling and implantation. Therefore, a low pin count per μASIC is desirable not only to limit the number of pads including naturally large silicon area for ESD protection structures, but also to facilitate alignment during embedding. This implicitly excludes a multi-bit wide data interface for transmission of the digitized neural signals.

B. μASIC Overview & Requirements

The functional block diagram of a μASIC is shown in Fig. 4. A μASIC is able to record neural signals from one electrode with an oversampled direct digitizing neural recorder. DC-coupling allows to avoid the typically large AC-coupling capacitors. The μASIC uses passive ground referencing [36] due to its simplicity and very limited area overhead. With an intended analog bandwidth of 7.5 kHz and a resolution in the range of 12 bits, a Nyquist data rate of 180 kbit/s per μASIC is targeted. A serial bus interface is used to transfer the digitized neural signals to the Telemetry Hub. The μASIC is clocked via a single

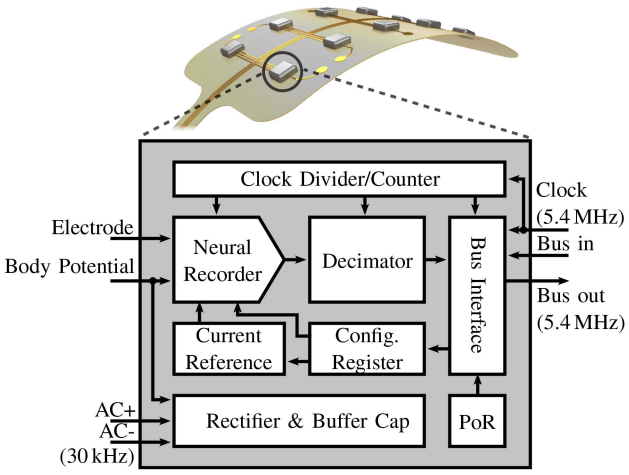


Fig. 4. Block diagram of a single μASIC. A power-on reset (PoR) module is used to initialize the digital logic after power-on.

externally supplied bus clock. All other required clocks and control signals are derived on-chip via a clock divider/counter. Power is supplied by a differential AC signal rectified on-chip. Since direct voltages (DC voltage) tend to drive electrochemical reactions like hydrolysis of water (if they exceed the water window determined by the thermodynamic properties of water, the surrounding electrolyte and voltage carrying materials) and corrosion, we designed the system such that DC voltages only occur on μASICs passivated by hermetic coatings [37], [38], [39], [40]. Off-chip interconnection lines which are embedded in PI as non-hermetic packaging material do not see any DC voltages due to the μASIC concept. This design measure minimized the risk of electrochemical reactions with possible gas evolution on these interconnection lines. A configuration register allows custom programmability of each μASIC by the Telemetry Hub via the serial bus.

The maximum number of μASICs along a single serial bus is only limited by the maximum clock rate which can be delivered via the substrate embedded gold trace on the PI substrate. With an estimate of an approximately 5 cm long 10 μm wide trace, this was experimentally found to be about 20 MHz [41] in buffer solution (PBS). This translates into a maximum of about 100 μASICs connected over a single serial bus, when a net data rate of 180 kbit/s is targeted. Note that a single telemetry hub could still connect several NeuroBus sub-systems, such that larger number of μASICs could be realized.

C. Encapsulation & Packaging

Major goals of NeuroBus include reducing FBR at tissue level and corrosive reactions at the implant level, the latter being caused by the harsh biological conditions in the body. These criteria can be fulfilled through the use of biocompatible materials and a system design which increases the structural biocompatibility and technical reliability by minimizing mechanical stresses inside the system and in forces between the system and the target tissue. In addition, CMOS dice will be protected against humidity and ions by a conformal hermetic coating. This conformal encapsulation of the CMOS dice is prior to transferring them to the PI substrate ensuring void free packaging of the overall encapsulation, therefore minimizing water penetration [42]. Integration of μASICs within the foil includes connection of the contact pads to integrated interconnects in a physical vapor deposition (PVD) process without further materials than the interconnect line metal [31]. The surface materials of the chip-in-foils system are the same than in (passive) ECoG electrode arrays [30] which proved to be biocompatible in chronic studies.

Using plasma-enhanced chemical vapor deposition (PECVD) of non-polymeric materials such as silicon-carbide (SiC) (amorphous state) has been shown to have positive results as thin-film encapsulation technique for in-plane microelectrode arrays [43] and even as reinforcement layers for stimulation and recording neural electrodes [44]. Moreover, SiC has good capabilities of adhering to PI and was used as adhesion promotion layer in polyimide-based electrode arrays, improving their stability both in-vitro and in-vivo [45]. Long-term stable encapsulation of single dice can thus benefit from this method. Further studies have to be conducted to optimize PECVD parameters and lower material stress that could allow water vapor intrusion. This can be made by adapting deposition parameters such as precursor gas ratio, annealing temperature [46], plasma power and pressure. Second, mimicking the biological environment through inserting the samples in different aging solutions (e. g. to correlate to the enzymatic activity) can predict potential failure mechanisms. Accordingly, bovine serum or diverse oxidative species such as artificial cerebrospinal fluid or the widely used hydrogen peroxide and alternating temperature and timeframes can bring more understanding than the standard phosphate buffered saline (PBS) immersion as aging agent [35]. Understanding and considering the different mechanical and chemical boundary conditions during the use case of the implants is mandatory to choose adequate design rules to develop a reliable device compatible to the available manufacturing processes.

III. Electronic Components & Building Block Prototypes for μASICs

Next, the electronic building blocks intended for the realization of the μASICs from Fig. 4 are explained.

A. Direct Digitizing Neural Recorder

A traditional method for neural recorder designs is to use an analog front-end [12], [47] that amplifies and filters the neural signals so that they can be digitized by a standard analog-to-digital converter (ADC). Direct digitizing neural recorders [48] combine the analog front-end and signal conditioning with a data converter. Delta-Sigma-Modulators (DSMs) are a popular choice for direct digitizing neural recorders [11], [49], [50], [51], [52], [53] since they can provide good power efficiency and high resolution especially within the neural signal bandwidth. While the Delta-Sigma-Modulator (DSM) based neural front-ends are heavily researched and can achieve impressive performance [49], [50], [51], the mandatory decimation filter

is often neglected and is therefore also not included in the published area and power consumption. While this is of less concern for modulators designed in highly scaled CMOS technology, where a power- and area efficient digital filter could be argued, this is not the case for a miniaturized recorder in a mature technology node since the digital filter can dominate the total silicon area [54].

Incremental $\Delta\Sigma$ analog-to-digital converters (I-ADCs) intrinsically require a significantly less complex decimation filter, while their power efficiency is usually worse compared to a DSM based ADC with same order and oversampling ratio (OSR) [55]. Since the NeuroBus system is designed in a 180 nm CMOS technology and minimized silicon area is of utmost importance for structural biocompatibility, an I-ADC based direct digitizing neural recorder is employed. It is implemented as a 2nd order continuous-time (CT) I-ADC with a sample rate $f_s = 15$ kHz at OSR of 180, allowing the NeuroBus system to record neural signals both in the local field potential (LFP) band (1 Hz–200 Hz) and action potential (AP) band (200 Hz–7.5 kHz). Although the current single-channel recorder prototype is used for ECoG recordings, where a bandwidth of 500 Hz is typical, the recording of AP signals with conformable ECoG arrays has been demonstrated in [33], [56]. Hence, the neural recorder is specified with a 7.5 kHz bandwidth to not limit the implants potential AP recording capabilities. Moreover, although the current prototype uses only a single electrode per recording channel, the I-ADC within the recorder could be easily extended for multiplexed operation and distribute its available bandwidth among multiple channels if no AP recording is intended and a multiplexer is implemented at the input to periodically connect several electrodes.

A Gm-based input stage with small input devices ($W = 28\ \mu$m, $L = 0.6\ \mu$m) allow chopping of the input stage at $f_{chop} = 30$ kHz while maintaining a sufficiently large input impedance without the need for additional input impedance boosting. The neural recorder is DC-coupled, which avoids the need for large AC-coupling capacitors. Potential electrode offset (EDO) is canceled with a body-induced offset based DC servo loop (DSL), which was described in detail in a previously presented recorder [57]. However, this recorder was unsuitable for use in a μASIC because it is based on a free-running CT DSM, which is not architecturally capable of supporting the possible need for channel multiplexing in future design iterations, it did not include digital filtering for proper decimation, and possible decimation filter implementations would violate the strict area constraints for μASICs [54]. While cascade of integrator (COI) reconstruction filters are the most popular choice for higher-order I-ADC due to their simple implementation and superior performance compared to other filter structures [55], [58], [59], [60], they suffer from poor out-of-band suppression. To avoid folding of strong chopping artifacts, we implemented a 2nd order cascaded integrator-comb (CIC) decimation filter [61]. While this reconstruction filter results in worse signal-to-quantization-noise ratio (SQNR) than a COI filter of the same order at the same OSR on I-ADCs, its frequency response features notches offering significant suppression at dedicated out-of-band frequencies. This enables significant filtering of chopping artifacts if the chopping frequency aligns with the notches of the filter.

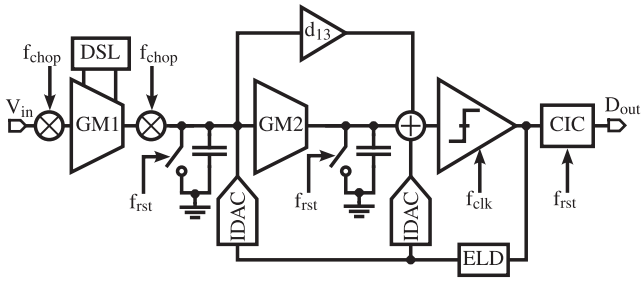


Fig. 5. Block diagram of the direct digitizing neural recorder based on a 2nd order incremental DSM and a CIC based reconstruction filter. EDO is suppressed by a DSL-controlled body-bias induced offset in the chopped input stage.

The use of chopping in CT modulators can result in noise folding into the in-band. This issue can be mitigated by increasing the chopping frequency to f_S [62], significantly reducing the input impedance of the neural recorder, or utilizing FIR feedback [63] with a large number of taps. In our implementation of the direct digitizing neural recorder (Fig. 5), the feedback digital-to-analog converter (DAC) is fed back to the first integration capacitor, bypassing the chopped Gm-based input stage and hence avoiding noise folding. By implementing a negative edge triggered flip-flop into the feedback path, a constant excess loop delay (ELD) of $0.5 \cdot T_s$ can be achieved. The noise transfer function of the modulator is restored with a fast feedback path around the quantizer [64].

CT DSMs can be very sensitive to clock jitter [65], resulting in increased inband noise. Since the presented neural recorder will use a clock provided through a bus system by the Telemetry Hub, considerably more clock jitter can occur compared to benchtop measurements with high precision equipment. To estimate the jitter sensitivity of this recorder, the clock jitter induced inband noise for CT DSM can be calculated [66, Eq. 4.25] for a given input clock jitter and multiplied with the noise penalty factor of 1.3 for an incremental ADC using a 2nd order CIC decimator. For an RMS clock jitter of 50 ps, which is plausible for simple clock generators, the induced input referred noise increases by only approximately 0.27 μV_{rms} for a 7.5 kHz bandwidth. This demonstrates good jitter immunity for the intended application.

1) Chip Prototyping and Measurement Setup: A prototype of the chopped direct digitizing neural recorder based on the I-ADC with CIC reconstruction filter was realized in a 180 nm CMOS technology with 1.8 V rated devices. The I-ADC consumes 24.7 μW of power from a 1.8 V supply with about half of the power (12.8 μW) attributed to the CIC decimation filter. The chip photo is shown in Fig. 6. The prototype occupies a core area of 0.03 mm^2, from which about 1/3 is consumed by the digital reconstruction filter. Please note that the decimation filter for a similarly performing, but-free running DSM recorder front-end [54] consumed 11 times more area and 10% more power.

The packaged chip was placed inside a QFN48 socket on a measurement board. The board contains voltage regulators (LT3045 & LT3094, Analog Devices) to generate a dual supply (± 0.9 V). The chip is configured and read out via a MicroZed

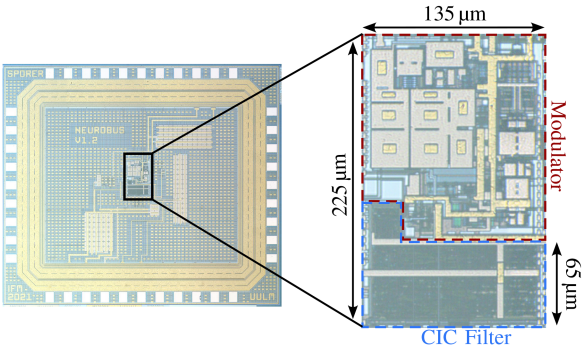


Fig. 6. Chip micrograph of the direct digitizing neural recorder prototype.

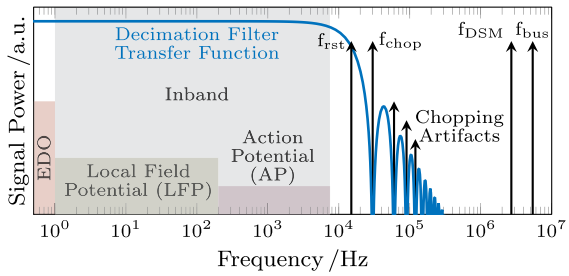


Fig. 7. Summary of all important frequency bands, transfer functions and clock frequencies for the direct digitizing neural recorder.

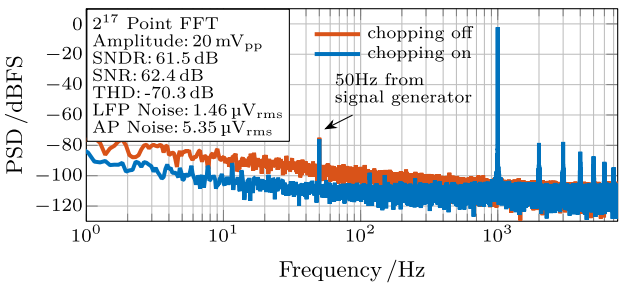


Fig. 8. Measured output spectrum after on-chip decimation with and without chopping.

7020 module; digital signals are buffered via digital isolator ICs (ADN4650 & ADUM141, Analog Devices) to achieve galvanic isolation between the MicroZed 7020 module and the measurement PCB. A Stanford Research DS360 function generator is used for input signal generation, an Agilent 81150 A generates the 2.7 MHz modulator clock (f_{DSM}) as well as a Nyquist rate (15 kHz) reset pulse (f_{rst}) and an Agilent 33250 A is used to supply a 30 kHz chopping clock (f_{chop}). An on-chip flip-flop synchronizes the reset pulse with the modulator clock. Fig. 7 summarizes all important signal bands, the transfer function of the decimator and clock signals regarding the direct digitizing neural recorder.

2) Measurement Results: Fig. 8 shows the measured output spectrum of the direct digitizing neural recorder for a maximum input amplitude of 20 mV_{pp} with chopping activated and the achieved noise floor with chopping deactivated. The power supply tone at 50 Hz generated by the signal generator is excluded

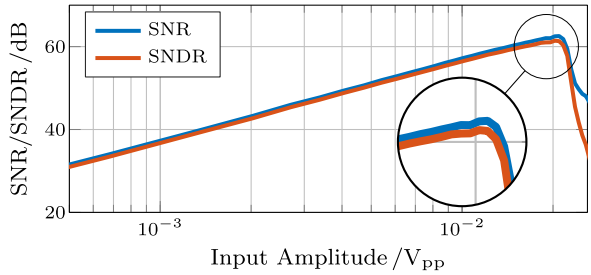


Fig. 9. SNR/SNDR measured versus input amplitude.

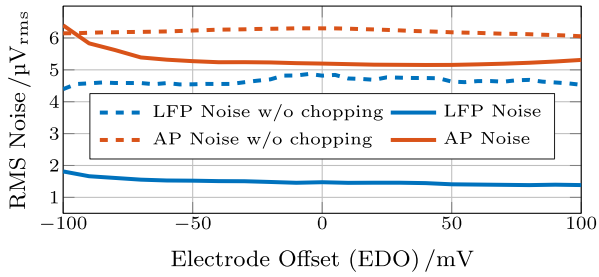


Fig. 10. RMS noise for the LFP and AP band measured over an EDO range of ±100 mV with and without chopping.

from the SN(D)R and RMS noise. The neural recorder achieves an AP noise of 5.35 μV_{rms} and an LFP noise of 1.46 μV_{rms}, respectively. While the majority of 1/f noise is removed due to chopping, unchopped components such as the DSL and the feedback DAC contribute to residual 1/f noise. Deactivating chopping leads to a strong increase in 1/f noise, resulting in an AP noise of 6.43 μV_{rms} and an LFP noise of 5.44 μV_{rms}, respectively.

The measured SNR/SNDR versus input amplitude (Fig. 9) indicate the designed maximum-stable-amplitude (MSA) of 20 mV_{pp}. The EDO cancellation is validated by adding a tunable DC offset to a 18 mV_{pp} input signal with activated chopping. A second measurement shows the noise performance over EDO without chopping. The chopped LFP and AP noise performance are stable over an EDO range from −100 mV to 100 mV with a slight increase for large negative EDO (Fig. 10). This increase can be explained by the fact that an input signal close to the recorder's MSA was applied and residual EDO started to overload the modulator. The measurement with deactivated chopping does not show this effect since the input signal amplitude was set below the MSA. The input impedance is measured with 216 MΩ.

Table I presents a summary of the direct digitizing neural recorder's performance and compares it with state-of-the-art recorders including on-chip decimation. The presented prototype achieves state-of-the-art LFP noise performance and the best AP noise performance compared to neural recorders without external circuitry. The increased area, when compared to [8], [16], [67], can be attributed to the on-chip implementation of the DSL, which was implemented off-chip in [8], [67] and completely omitted in [16]. The front-end in [6] was designed in a highly scaled CMOS technology and has a technological advantage for the implementation of digital circuitry in terms

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART DIRECT DIGITIZING NEURAL RECORDERS

	This work	JSSC'23 [67]	JSSC'23 [6]	JSSC'19 [11]	TBCAS'19 [68]	JSSC'18 [16]	JSSC'12 [8]
Technology	**180 nm**	180 nm	22 nm	180 nm	130 nm	180 nm	65 nm
Supply /V	**1.8**	1.8	0.8	1.8	1.2	1.8	0.5
Area /mm^2	**0.03**	0.0046	0.0045	0.694	0.035	0.0049	0.013
Power /Ch. /µW	**24.7**	14.62	6.02	122	48.7	39.14	5.04
Architecture	**I-ADC+DSL**	2-step I-ADC	Δ-ΔΣ	IA+ΔΣ-ADC	IA+SAR-ADC	I-ADC	split dual-loop
Coupling	DC	DC	AC	DC	AC	DC	DC
EDO Tolerance /mV	**±100**	±60	±400	±104	±600	±11.25	±50
External Circuitry	**No**	Yes[b]	No	No	No	No	Yes[c]
THD /dB	**-70.3 @20mV$_{pp}$**	-62.2/-38.2[a] @10mV$_{pp}$	-56.5 @21.5mV$_{pp}$	-77 @26mV$_{pp}$	-55 @10mV$_{pp}$	-53 @10mV$_{pp}$	-34 @0.57mV$_{pp}$
LFP Noise /µV$_{rms}$	**1.46**	2.51/9.21[a]	11.9	3.5	7.65	6.02	4.3
NIB /Hz	**1 - 200**	0.5 - 1000	0.5 - 1000	1 - 1250	0.5 - 1000	1 - 300	1 - 300
AP Noise /µV$_{rms}$	**5.35**	4.46/11.83[a]	7.71	7.3	7.44	10.46	4.9
NIB /kHz	**0.2 - 7.5**	0.3 - 10	0.3 - 10	0.001 - 5	0.3 - 10	0.3 - 10	0.3 - 10
NEF	**9.1**	13.42[*,a]	8.26[*]	14.2	18.87[*]	19.42[*]	5.99
PEF	**149**	324[*,a]	54.55	363[*]	427[*]	679[*]	17.96

[*] calculated [a] for a ±60 mV EDO [b] EDO cancellation level is set off-chip [c] loop is closed off-chip on FPGA

of area and power. However, despite operating from a 0.8 V supply, which reduces digital circuit power consumption fivefold compared to a 1.8 V supply - but which also would need to be additionally generated on the μASIC - , the achieved power efficiency factor (PEF) is only 2.7 times lower compared to the herein presented design. Furthermore, it shows 1.5 times more noise power density within the AP band and inferior low-frequency noise performance. The input impedance of the presented neural recorder remains constantly high for the complete bandwidth while the input impedance of [6], [21] drops to a few MΩ at the band edge. In summary this direct digitizing neural recorder prototype has demonstrated the ability to combine good low frequency noise performance, chopping and power supply artifact rejection and on-chip EDO cancellation on a small area with low power consumption.

B. Digital Communication Bus

As the number of channels in neural implants increases, efficient data readout becomes increasingly important. Single-chip implants can rely on standardized protocols such as SPI or I^{2}C [6], [12] where the area and power consumption is shared between all integrated channels, hence having only a minor impact on the total power budget and area. The NeuroBus implant consists of dozens of spatially distributed μASICs that need to transfer data to the Telemetry Hub (cf. Fig. 2), where it is transmitted via a conventional transcutaneous data link. Standardized protocols cannot meet the specific requirements for pin count, power consumption and size for this custom application. While there are some approaches for in-body wireline communication [68], [69], [70], these concepts are not suitable for NeuroBus due to their complex architecture and large storage capacitor. Thus, a custom communication interface is implemented. Although simplex communication would allow a very simple communication interface, programming capabilities for each μASIC are preferable.

In [13], we compared two different communication bus architectures for NeuroBus. While a typical serial bus architecture

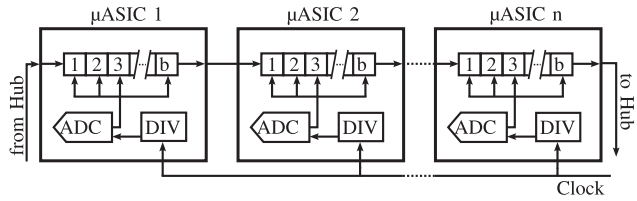


Fig. 11. Basic concept of the daisy-chained bus interface for NeuroBus, based on [13].

allows great flexibility and enables to address single μASICs in a custom manner, it also generates noticeable protocol overhead. This could be mitigated with a larger payload per transaction, requiring on-chip buffering of data which is contradictory to the tiny μASICs approach with low power and area consumption.

1) Daisy-Chained NeuroBus: To avoid the drawbacks of a serial bus interface, we implement a lightweight daisy-chained bus interface to achieve data readout with basic programming capabilities on a small area and power budget. Fig. 11 shows the basic concept of the bus interface. μASICs are daisy chained and act similar as a distributed shift register, clocking their data through the μASIC-chain until it arrives at the Telemetry Hub. Data order is inherently given by the position of the μASIC in the chain, eliminating the need for unique chip IDs. All clocks that are required for the μASIC (oversampled I-ADC clock, chopping clock, Nyquist clock) are generated from the externally supplied bus clock via a divider. The internal data register of each μASIC is loaded with a new sample on the clock edge of the Nyquist clock. Assuming a daisy chained bus of n μASICs with a sample width of b bit, the required bus clock frequency f_{clk} can be written as

$$f_{\mathrm{clk}} = b \cdot f_{\mathrm{nyq}} \cdot n. \tag{1}$$

Regarding the sample rate and bitwidth of the direct digitizing neural recorder (f_{nyq}= 15 kHz, b = 12), (1) results in f_{clk} = 18 MHz for n = 100 μASICs. While a clock frequency of 18 MHz is below the maximum allowable clock rate for the

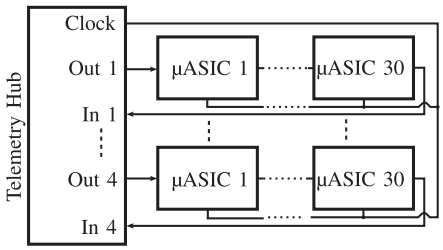


Fig. 12. Example of the split daisy-chain approach with 4 daisy-chains operated in parallel, based on [13].

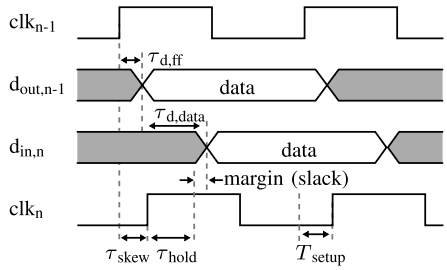


Fig. 13. Timing diagram illustrating the hold time constraints of the daisy-chained NeuroBus expressed with (2).

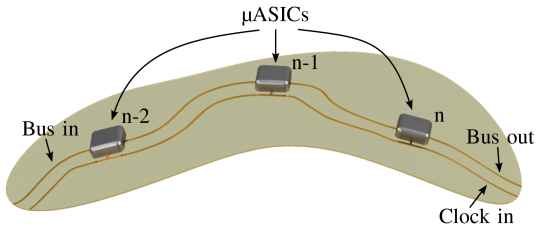


Fig. 14. Clock patch routing for negative clock skew, based on [13].

PI substrate, bus timing requirements and register width for the on-chip clock divider increase with clock rate, requiring more and stronger driver cells and increase dynamic power consumption. We therefore limit the length of the bus to a fraction of the original and choose the number of daisy chained μASICs ($n = 30$) in such a way that the bus clock frequency is exactly twice the incremental $\Delta\Sigma$ modulator (I-DSM) clock; simplifying internal clock generation/division and the bus clock can be lowered to 5.4 MHz. The NeuroBus system also allows to increase total channel count by connecting multiple daisy-chained buses to the Telemetry Hub. It must however be noted that each bus requires its dedicated data in/data out pad at the Telemetry Hub (Fig. 12), increasing wiring effort and Telemetry Hub chip size. Also, the capacitive load of the shared clock line must be considered and adequate drivers need to be employed.

The primary function of the communication bus is to transfer digitized neural signals to the Telemetry Hub, though initial programming for each μASIC must be carried out. After power-on reset (PoR) initialized the μASIC logic the Telemetry Hub can shift 30 times 12 b of configuration data into the bus. The shifting direction of the configuration data is identical to the direction of the conventional ADC data. After $30 \cdot 12$ clock cycles, the first Nyquist clock is counted, triggering the μASIC to copy the currently available data into the configuration register. This procedure is repeated until 2x12 b of configuration data are received by each μASIC.

2) Design for Bus and µASIC Timing: The on-chip digital logic is verified with state-of-the-art tools for timing analysis, ensuring proper implementation. Although these tools can verify timing for on-chip logic and also off-chip traces with a known, constant ϵ_r, they are not intended to be used for the off-chip traces of the NeuroBus implant. This is due to the connection of several spatially distributed μASICs via traces embedded into a PI substrate, whose actual impedance even varies from dry to implanted wet state. Due to the thin PI substrate, the effective relative permittivity $\epsilon_{r,eff}$ is affected by the surrounding tissue. As the ϵ_r of biological tissue can vary significantly with tissue type [71], we use the relative permittivity of water ($\epsilon_r \approx 80$) as a worst case estimation.

In [13] we presented a design methodology where the daisy-chained μASICs are considered as a distributed shift register. Typically shift registers have sufficient setup time for low clock speeds but can suffer from hold time violations if the relation

$$\tau_{d,data} + \tau_{d,ff} > \tau_{hold} + \tau_{skew} \quad (2)$$

is violated. In (2) $\tau_{d,data}$ and $\tau_{d,ff}$ are the propagation delays of the data trace and transmitting register, respectively, τ_{skew} is the clock skew between transmitting and receiving register and τ_{hold} denotes the hold time of the receiving register.

Digital implementation tools can adjust the digital on-chip logic to guarantee valid timing for $\tau_{skew} = 0$ and $\tau_{d,data} = 0$ by keeping the hold time τ_{hold} smaller than the propagation delay $\tau_{d,ff}$ of the register. Fig. 13 visualizes (2) for positive clock skew where n-1 denotes the transmitting register and n denotes the receiving register. As long as (2) is met, the slack is positive and the hold timing is valid. Valid hold timing can be further guaranteed with arbitrary embedded μASIC arrangements if negative clock skew routing as shown in Fig. 14 is applied since the first μASIC receiving the data is the last μASIC to receive the clock, increasing hold slack at the cost of reduced setup slack; this concept is also applicable on the initial programming where configuration data is shifted in the same direction as the conventional ADC data.

To meet setup timing, the following relation must be met:

$$\tau_{d,data} + \tau_{d,ff} + T_{setup} \leq T_{clk} + \tau_{skew} \quad (3)$$

where $\tau_{d,data}$ and $\tau_{d,ff}$ are the propagation delays of the data trace and transmitting register,respectively, T_{setup} is the setup time of the receiving register, T_{clk} is the clock period, and τ_{skew} denotes the clock skew between receiving and transmitting μASIC. Fig. 15 visualizes (3) for negative clock skew where n-1 denotes the transmitting register and n denotes the receiving register. The setup timing is met as long as the setup slack shown in Fig. 15 is positive.

When $T_{clk} \gg \tau_{d,ff} | \tau_{setup}$, (3) simplifies to

$$\tau_{d,data} - \tau_{skew} \leq T_{clk} \quad (4)$$

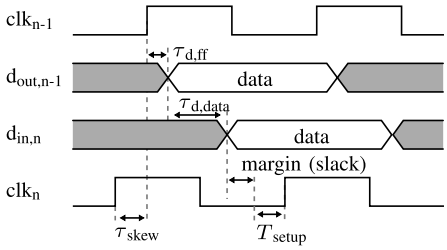


Fig. 15. Timing diagram illustrating the setup time constraints of the daisy-chained NeuroBus expressed with (3).

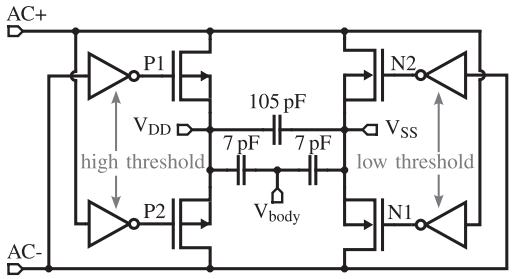


Fig. 16. Schematic of the square-wave rectifier.

Thus, only if the data delay, which equals the negative skew of the clock ($\tau_{d,data} = -\tau_{skew}$), becomes approximately as large as half clock period, setup timing violations could appear.

With

$$\tau_{d,data} = -\tau_{skew} = \frac{\sqrt{\epsilon_{r,eff}}}{c} \cdot L_{trace} \tag{5}$$

the maximum trace length can be expressed as

$$L_{trace} \leq c \cdot \frac{T_{clk}}{2 \cdot \sqrt{\epsilon_{r,eff}}} \tag{6}$$

where L_{trace} is the physical trace length and c the speed of light. If $\epsilon_{r,eff}$ is pessimistically estimated as 80 and the previously specified bus clock frequency of 5.4 MHz is assumed, an uncritical and unrealistically large trace length of around 300 cm is received. This shows that propagation delay induced setup violations are of no concern for the NeuroBus implant.

Parasitic resistance of a 10 μm wide gold trace embedded into the PI substrate is measured with approximately 60 Ω per 10 mm [41]. Coupling capacitance to neighboring traces with 100 μm distance is about 25 fF/mm [72] and the parasitic capacitance to surrounding phosphate buffered saline (PBS) is 10 fF/mm.

The daisy-chain interface can drive loads up to 10 pF, easily allowing a targeted maximum trace length between μASICs of 5 cm since the bus input of the μASIC adds only a parasitic capacitance of 305 fF to the bus. While this buffer strength is oversized for connections between μASICs, it is useful for the last μASIC in the chain to drive the input of the Telemetry Hub. Although the data trace length between two adjacent μASICs can easily be several centimeters long, the constraint on the total bus length is stricter. Parasitic elements such as trace resistance, trace capacitance and μASIC pad capacitance form a multi-segmented RC filter on the clock trace. Assuming a daisy chain with 30 equally spaced μASICs and that frequency components up to the third harmonic of the clock frequency are required to ensure proper clock delivery, the total bus length must not exceed 22 cm.

3) Implementation of the Communication Interface: The presented NeuroBus communication interface was implemented in an 180 nm CMOS process with a 1.8 V nominal supply voltage as a building block on the final μASIC which is currently under manufacturing. The simple architecture of the communication interface requires only 40 standard cells, including 32 flip-flops, 6 combinatorial logic cells and 2 buffers/inverters. The low number of flip-flops is achieved since only 17 b of the transmitted 24 b configuration data are stored. The total area consumption is 2600 μm^2 and the post-layout simulated power consumption is 18.7 μW and includes the power required to drive a 1 pF load on the bus line, which corresponds to a bus wire to be driven by a single μASIC as long as 2 cm. The current implementation of this daisy-chained bus does not include any mechanisms to detect or correct potential bit errors during transmission. While a bit error can damage a single ADC sample within the daisy chain, the independently counting μASICs prevent misalignment of the entire chain. The bit error rate (BER) of the communication bus needs to be evaluated in-vitro and in-vivo and depending on the achieved BER a potential parity bit could be implemented for future design iterations.

C. Power Management for μASIC

Implants intended for long-term implantation must consider and prevent harmful electrochemical reactions which can damage the implant itself and endanger the safety of the patient. Although all off-chip connections and traces for the NeuroBus implant are embedded into PI, it is considered a non-hermetic sealing and moisture penetration over the long implant lifetime cannot be ruled out. To prevent any gas evolution due to hydrolysis, no DC voltages are applied to any off-chip connection. Instead, the μASICs are AC powered and an on-chip square-wave rectifier with MOS switches is used to generate an on-chip DC supply; the original square wave rectifier with self-driven switches was published in [73], though it required an additional external control signal to disconnect the buffer capacitor from the rectifier during switching. To minimize the pin count, our rectifier is based on [74] where large capacitors and inverters with modified thresholds are used to disconnect the buffer capacitor during switching (Fig. 16).

The four inverters are sized to achieve a high and low threshold, respectively. This allows to disconnect the rectifier early from the AC lines during their polarity change and reconnects it afterwards as shown in Fig. 17. This drastically reduces buffer capacitor discharge during switching. Simulation showed that the rectifier performance is also stable over process corners. To prevent performance degradation in the neural recorder due to ripples in the supply voltage, the frequency of the AC supply is chosen to match the notches of the CIC decimation filter [59]. We did not implement the large capacitors between the AC lines and inverter outputs as introduced in [74] due to their

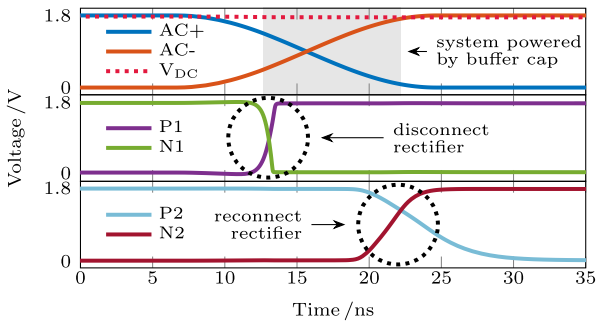


Fig. 17. Post-layout simulated rectifier control signals. Buffer capacitor and rectifier are disconnected from the AC lines when polarity change occurs.

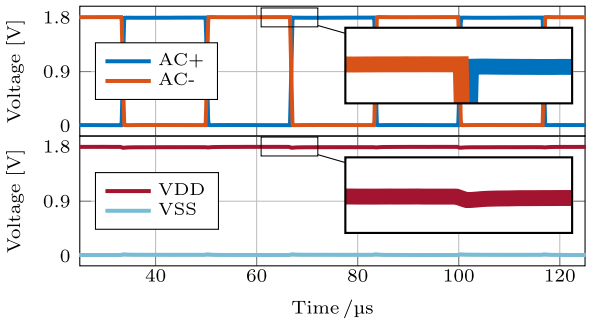


Fig. 18. Measured AC signals for μASIC power delivery and rectified supply voltages. The amplitude mismatch of the AC signals translates into ripples in the rectified supply voltages.

minor influence on the rectifier performance for light loads. Instead, they generate capacitive load on the AC lines, causing noticeable switching losses for the Telemetry Hub. The rectifier also includes a pin which connects to the global body potential V_{body}. This connection ensures that the internal supplies of each μASIC are referenced to the same potential, resulting in the same logic level on the serial bus. The global body potential is also supplied to the Telemetry Hub, which centers the AC supply around it. The tissue potential can slightly differ locally from V_{body}, creating a small DC voltage between the V_{body} centered AC line and tissue. This is however of no concern since these local variations are typically small and within the water window. This rectifier was prototyped in the same 180 nm CMOS technology (chip photo of the prototype not shown). Fig. 18 shows the measured rectifier output as well as the measured AC supply signals of frequency $f_{rect} = 30$ kHz and $t_{rise/fall} = 18$ ns which are fed into the rectifier. These AC signals exhibit a slight amplitude mismatch of approximately 8 mV, which produces a ripple of similar amplitude on the rectified signal. By matching the frequency of the AC supply (f_{rect}) to the notches of the decimation filter, sufficient ripple rejection can be realized and further allows to relax the amplitude mismatch constrains for the Telemetry Hub. The voltage efficiency of the rectifier was measured with 97% for a 68 k Ω load and a 77 pF buffer capacitor. For the final μASIC integration, the buffer capacitor size was increased to 105 pF since area above the implemented digital

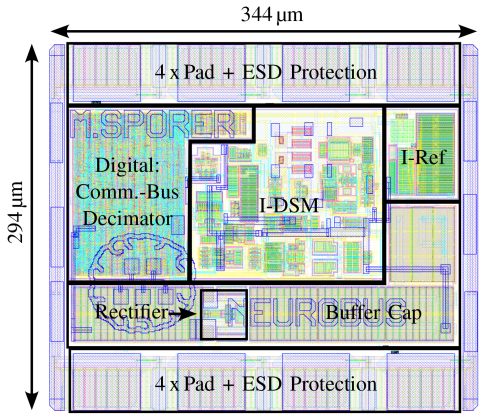


Fig. 19. Layout of the complete μASIC.

logic could be used for additional metal-insulator-metal (MIM) capacitors. The total area consumption of the rectifier including a 105 pF buffer capacitor is 18400 μm^2.

D. μASIC Integration

All electronic components were recently integrated onto a single chip to create the μASIC, which is currently in production in a 180 nm CMOS process. The layout of the μASIC is shown in Fig. 19. It achieves a small size of 344 μm x 294 μm and requires only 7 pads. An additional eighth pad can be used for verification of the on-chip current reference. All pads include grounded-gate NMOS based single protection structures which are standard cells in the used technology design kit and are rated for a 2 kV human-body-model (HBM) ESD protection. Due to their extensive area requirements, comparatively large pads (54 μm x 64 μm) can be realized on top of the ESD protection structures, facilitating the alignment during embedding and allowing simple chip verification with needle probing. Although amplitude mismatch between recording channels on different μASICs can also be corrected by digital post-processing, the μASIC includes trimming bits in the configuration register for the neural recorder and the on-chip reference current, allowing to mitigate amplitude mismatch directly on-chip.

The digital logic requires a silicon area of 12700 μm^2 whereas 57% of the area is required by the CIC filter, 30% by the clock generator and 14% by the communication interface. The post-layout simulated digital power is 35 μW including a 1 pF bus load, which corresponds to a bus wire to be driven by a single μASIC as long as 2 cm. The current μASIC implementation records a single channel with 15 kSps, limiting each daisy chain to 30 channels. Future implementations could be extended by a multiplexer as described in Section III-A, allowing to use a maximum channel count of 450 per daisy chain if 15 channels with 500 Hz bandwidth would be multiplexed to a single μASIC.

Table II compares the NeuroBus concept against other neural implant systems. It should be noted that the values given for the NeuroBus concept were derived from the measured prototypes, the μASIC and the system specifications. Prototyped full assembly of NeuroBus has not yet been performed, but

TABLE II
COMPARISON OF THE NEUROBUS CONCEPT WITH OTHER NEURAL IMPLANT SYSTEMS

	NeuroBus[a]	Conventional Concept [12]	Neuropixels [76]	Neurograin [24]	Neural Dust [22]
Concept	Distributed µASICs embedded into a PI substrate	Passive electrode array, connected to a base unit	Active silicon based probe with implantable shank	Wireless powered ASICs placed inside an implanted coil	ASIC and piezo-ceramic on a substrate, ultrasonic powered
Application	ECoG recording	Neuromodulation	fundamental neuroscience	ECoG recording	peripheral and central nervous system recording
intended long-term implantation	Yes	Yes	No	Yes	Yes
ASIC technology	180 nm	180 nm	130 nm	65 nm	65 nm
ASIC area/ch. /mm^2	0.10	0.46	0.12	0.25	0.25
Power/ch. /µW	46.9[a]	115 (LNA+ADC)	49.1	≈40	37.7
ASIC readout	custom digital bus	SPI	4 x SPI	wireless	ultrasonic
Channels	n · 30[a,b]	32	384	64, up to 1000[*]	-
ASIC pitch	≥350 µm[a]	NA	NA	≥ 500 µm	3.8 mm[‡]
Electrode pitch	≥30 µm[c]	-	20 µm	≥ 500 µm[†]	2 mm
Telemetry	centralized	centralized	NA	individual ASIC	individual implant

[*] estimated [†] determined by ASIC edge length [‡] determined by implant length [a] estimated from system specifications, building block prototypes and µASIC. [b] n = number of parallelized daisy chains [c] local clusters of electrodes

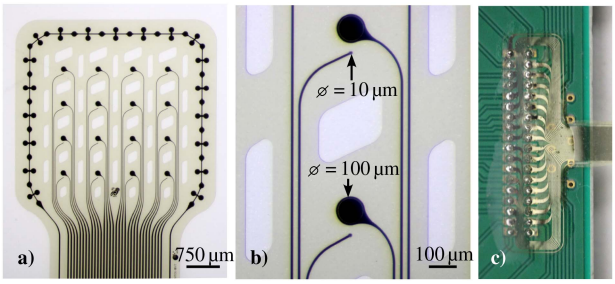


Fig. 20. ECoG array. (a) Electrode site consisting in a total of 32 Pt electrodes. (b) Magnified picture of closely positioned small and large electrodes. (c) Corresponding pads soldered on PCB with epoxy encapsulation to avoid water penetration and unwanted mechanical interactions

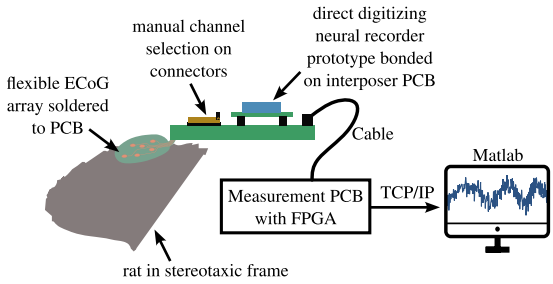


Fig. 21. Sketch of the measurement setup for the in-vivo concept validation. The direct digitizing neural recorder prototype is connected to a flexible ECoG array via a custom PCB.

encapsulation tests and the functionality of system components were first evaluated and validated by in-vivo measurement, cf. Section IV.

IV. NEUROBUS SYSTEM VALIDATION

As a final step, after having discussed the system concept, the encapsulation procedure, and the electronic sub-system implementation, we aimed to preliminarily demonstrate the performance of all components within a joined ECoG-chip system in a hybrid assembly as proof of concept step before fully integrating the system. Therefore, the direct digitizing neural recorder IC was connected to the ECoG array via an interposed printed circuit board (PCB) that allows us to manually select the channel of interest by connecting the chip to the recording electrode. The readout and clock generation was managed via an field-programmable gate-array (FPGA) (MicroZed 7020 module).

A. Materials and Methods

In brief, a PI-based ECoG array consisting of 16 large ($\phi = 100\,\mu$m) and 16 small ($\phi = 10\,\mu$m) platinum (Pt) electrodes was used (Fig. 20). To meet the requirements of the NeuroBus system, conformability was one of the pre-requisites of the chosen device, therefore an 8 μm thick array with highly distributed substrate fenestration was preferred [30]. The ECoG array [30] has been manufactured with the materials and technology which is used to integrate the μASICs into the flexible substrate with electrodes [31]. The ECoG array was soldered to a previously custom-made PCB, which allows stable fixation to the stereotaxic manipulator during surgical procedure and substantially reduces the potential artifacts caused by vibration. The direct digitizing neural recorder prototype was bonded onto a thin interposer PCB and then connected to the custom-made PCB as shown in Fig. 21. The recording channel was manually selected from the 32 electrodes using a jumper-connector.

The measured RMS noise per electrode channel was calculated by determining the power spectral densitiy (PSD) of the recorded signal, integrating all the bins located within the band of interest (LFP: 1Hz-200 Hz, AP: 200Hz-7.5 kHz), and then taking the square root of the received noise power. A Hann window was applied during the PSD calculation and all calculations were performed with MATLAB.

B. In-Vitro Characterization of Arrays

Electrochemical impedance spectroscopy (EIS) was performed in PBS (pH 7.4, Sigma-Aldrich, Missouri, USA) to verify the functionality of the recording channels (Fig. 22). A potentiostat (Metrohm, Autolab, Filderstadt, Germany) was used in a 3-electrode setup with an Ag/AgCl reference electrode,

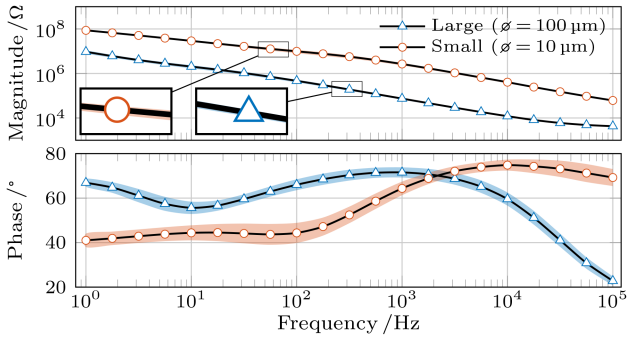


Fig. 22. Impedance of small (circles) and large (triangle) μECoGs Pt electrodes from 1 Hz to 100 kHz. Mean value (solid line) and standard deviation (filled area) calculated for n = 14(large) and n = 11 (small) electrodes. Negative phase angles are displayed on the positive y-axis according to standards in electrochemistry of electrodes.

TABLE III
MEAN AND STANDARD DEVIATION OF THE MEASURED ELECTRODE IMPEDANCES FROM FIG. 22

Small Electrodes				Large Electrodes			
Magnitude (Ω)		Phase (°)		Magnitude (Ω)		Phase (°)	
mean	σ	mean	σ	mean	σ	mean	σ
2.7 M	486.6 k	-64.4	3.3	74.4k	11.6k	-71.5	2.5

a standard Pt counter electrode and individually selected ECoG channels as working electrodes. An excitation voltage of 100 mV was applied, and the signal frequency was swept between 1 Hz and 100 kHz. All measurements were conducted in a Faraday cage to reduce electromagnetic interference. The mean and standard deviation of the measured electrode impedances from Fig. 22 are shown in Table III. Non-functional electrodes were excluded from the measurement.

C. NeuroBus Concept Validation In-Vivo

1) Ethical Statement: Animal procedures were approved by the Regierungspräsidium Freiburg (TVA G-20-65) and in accordance with the 2010/63/EU directive.

2) Stereotaxic Surgeries: In total, two rats (female, Sprague-Dawley, weeks 15-20) underwent surgical procedures under anesthesia. Only one animal was used for achieving cortical recordings with the described ECoG-chip system, whereas the other was part of an in-vivo experiment not related to our work and therefore only used for post-mortem data collection. The animals were briefly anesthetized with 5% isoflurane inhalant. After induction, a mixture of 80 mg/kg ketamine (Serumwerk Bernburg, Germany) and 0.06 mg/kg medetomidine (Dextomidor, Zoetis Deutschland GmbH, Germany) was administered intraperitoneally (i.p.). The animals were quickly transferred to the stereotaxic frame, head-fixed and allowed to breathe normally through the rodent mask. A mixture of oxygen and isoflurane (<1%) was delivered through the mask to maintain anesthesia. The animal was administered with 4 ml of 0.9% saline (NaCl, B.Braun Melsungen AG, Germany) solution subcutaneously (s.c.) approximately every 2 hours. Animal breathing and heart rate were tracked with a heart monitor and their temperature

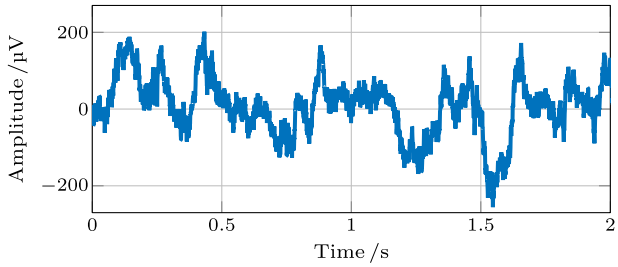


Fig. 23. Spontaneous cortical activity measured over one electrode of the ECoG array. The recording was post-processed with a low-pass filter (f_c = 500 Hz).

maintained at 37 °C with a heating-pad. Prior to incision, lidocaine (2% xylocaine gel, Aspen Pharma Trading Limited, Ireland) was applied topically over the skin around the incision site, which was further disinfected with Braunol (B. Braun Melsungen AG, Germany) and Kodan (Schülke, Germany). A single incision was made (up to 2 cm) above the skull and roughly along the midline. The subcutaneous tissue was removed with a bone scraper and any persistent bleeding from skull blood vessels stopped with a cautery pen. The skin was gripped in place with 5-6 bulldog clamps and the surface of the skull cleaned from debris with 3% hydrogen peroxide. The animal head was then leveled in the frontal, horizontal and sagittal planes.

A large (6 mm x 6 mm) craniotomy was made using a microdrill over the left barrel cortex, spanning (0.5 mm, 6.5 mm) medio-lateral (m.l.) and (−0.5 mm, −6.5 mm) antero-posterior (a.p.) from bregma. The dura was removed and the ECoG array placed over the exposed brain surface, centered at 3.5 mm m.l., −3.5 mm a.p. from bregma. The anesthesia was maintained with additional i.p. injections of ketamine/medetomidine as required. After 4 hours of surgery, the animals were injected s.c. with 2 ml of 5% glucose solution (B. Braun Melsungen AG). After completing the measurements, the animals were transcardially perfused with an i.p. injection of ketamine (min. 100 mg/kg) and xylazine (min. 10 mg/kg).

3) Electrophysiology: Electrocorticographical recordings were conducted in a unipolar configuration with a single reference/ground electrode tied together (Fig. 23). A silver wire was soldered to a gold pin on one side, and the ground pin on the measurement PCB on the other side. The gold pin was inserted through an additional craniotomy over the frontal lobe and stabilized with dental cement. We made sure the pin achieved contact with the brain/cerebrospinal fluid. Initial measurements were conducted on the dead brain tissue of a rodent to validate the setup and eliminate any potential artifacts or interferences. The noise floor of 4 small (S4, S13, S14, S16) and 5 large (L1, L2, L3, L4, L6) electrodes was measured and evaluated. The noise floor of channel L1 was evaluated with similar noise levels than channels L2, L3, L4 and L6 but is not shown in Fig. 24 to achieve a reasonable figure layout. For all four electrodes with small diameters, larger noise levels were measured compared to large electrode diameters. (Fig. 24). This behavior was expected due to increased impedance for smaller electrodes (Fig. 22). While the AP-band of the neural recorder

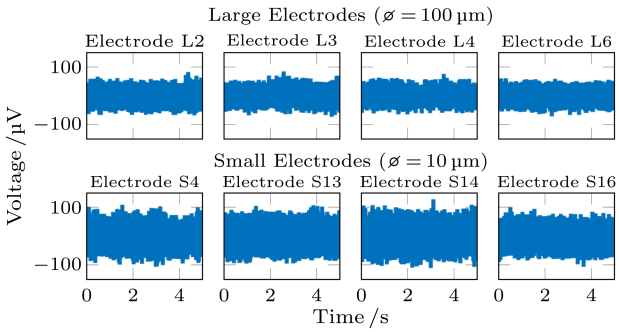


Fig. 24. Measured noise for different electrode diameters on nervous tissue for a 7.5 kHz bandwidth after the death of the animal. The recordings show no bio-electrical activity any longer and reflect noise and artifacts of the measurement setup and the environment in the surgical room.

has a benchtop measured input referred noise of about 5 μV_{rms}, using the large and small electrodes on tissue, the measured AP band noise of the recorder-electrode system is in the range of 12–18 μV_{rms} in the conducted experiments. LFP-band noise was affected by the electrodes only at a minor value, and using the small electrodes, an LFP noise of 3–5 μV_{rms} could be achieved.

V. Conclusion

Technological advancements in neuroprosthetics and circuit design are resulting in considerable enhancements in neural interfaces. Frequently, the focus is placed on optimizing parameters like integration density (channel count) and recording performance in terms of SNR/SNDR, while other essential factors for chronically implanted neural interfaces, such as structural biocompatibility, receive less attention at the die level. Distributing the functionality of a single high-channel count ASIC on several spatially distributed tiny μASICs which in turn are embedded into an ultra-flexible and thin polyimide substrate is a promising concept not only to achieve a highly conformable implant with a low bending stiffness but also allows application dependent placement of electrodes and μASICs. In this work we presented the overall architecture of this new neural interface concept called *NeuroBus* and discussed the building blocks of the μASIC as well as the post-CMOS processing for encapsulation and packaging. The prototypes of the system's direct digitizing neural recorder and ECoG array underwent individual benchtop measurements to assess their performance. Components were combined in hybrid assembly for an acute proof of concept in-vivo study to validate the system concept and adequacy of the interfaces between sensors (electrodes) and electronics. The system showed satisfactory performance and allowed proper recording of brain data in-vivo. This hybrid system assembly approach is employed to technically de-risk the NeuroBus concept by ensuring that the final integration occurs only after all crucial components prove satisfactory performance. It also serves as a means of reducing and refining animal experiments. The obtained results are prerequisite to fully integrate all components into a chip-in-foil system for applications scenarios on the brain.

References

[1] A. K. Engel, C. K. E. Moll, I. Fried, and G. A. Ojemann, "Invasive recordings from the human brain: Clinical insights and beyond," *Nature Rev. Neurosci.*, vol. 6, no. 1, pp. 35–47, Jan. 2005.
[2] T. L. Skarpaas and M. J. Morrell, "Intracranial stimulation therapy for epilepsy," *Neurotherapeutics*, vol. 6, no. 2, pp. 238–243, Apr. 2009.
[3] F. T. Sun, M. J. Morrell, and R. E. Wharen, "Responsive cortical stimulation for the treatment of epilepsy," *Neurotherapeutics*, vol. 5, no. 1, pp. 68–74, Jan. 2008.
[4] H. Kassiri, N. Soltani, M. T. Salam, J. L. P. Velazquez, and R. Genov, "Battery-less modular responsive neurostimulator for prediction and abortion of epileptic seizures," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2016, pp. 1298–1301.
[5] A. B. Ajiboye et al., "Restoration of reaching and grasping movements through brain-controlled muscle stimulation in a person with tetraplegia: A proof-of-concept demonstration," *Lancet*, vol. 389, no. 10081, pp. 1821–1830, May 2017.
[6] X. Yang et al., "An AC-Coupled 1st-Order Δ-$\Delta\Sigma$readout IC for area-efficient neural signal acquisition," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 949–960, Apr. 2023.
[7] J. Huang et al., "A 0.01-mm2 mostly digital capacitor-less AFE for distributed autonomous neural sensor nodes," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 7, pp. 162–165, Jul. 2018.
[8] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2, 5 μW, DC-Coupled neural signal acquisition IC with 0.5 v. supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.
[9] B. C. Johnson et al., "An implantable 700 μW 64-channel neuromodulation IC for simultaneous recording and stimulation with rapid artifact recovery," in *Proc. Symp. VLSI Circuits*, 2017, pp. C48–C49.
[10] H. Kassiri et al., "Rail-to-rail-Input dual-radio 64-channel closed-loop neurostimulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2793–2810, Nov. 2017.
[11] A. Nikas, S. Jambunathan, L. Klein, M. Voelker, and M. Ortmanns, "A continuous-time delta-sigma modulator using a modified instrumentation amplifier and current reuse DAC for neural recording," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2879–2891, Oct. 2019.
[12] S. Reich, M. Sporer, M. Haas, J. Becker, M. Schüttler, and M. Ortmanns, "A high-voltage compliance, 32-Channel digitally interfaced neuromodulation system on chip," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2476–2487, Aug. 2021.
[13] M. Sporer et al., "NeuroBus architecture and communication bus for an ultra-flexible neural interface," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2023, pp. 1–5.
[14] T. L. Skarpaas, B. Jarosiewicz, and M. J. Morrell, "Brain-responsive neurostimulation for epilepsy (RNS system)," *Epilepsy Res.*, vol. 153, pp. 68–70, Jul. 2019.
[15] K. Najafi and K. Wise, "An implantable multielectrode array with on-chip signal processing," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1035–1044, Dec. 1986.
[16] D. D. Dorigo et al., "Fully immersible subcortical neural probes with modular architecture and a delta-sigma ADC integrated under each electrode for parallel readout of 144 recording sites," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3111–3125, Nov. 2018.
[17] N. A. Steinmetz et al., "Neuropixels 2.0: A miniaturized high-density probe for stable, long-term brain recordings," *Science*, vol. 372, no. 6539, Apr. 2021, Art. no. eabf4588.
[18] A. Ersen, S. Elkabes, D. S. Freedman, and M. Sahin, "Chronic tissue response to untethered microelectrode implants in the rat brain and spinal cord," *J. Neural Eng.*, vol. 12, no. 1, Jan. 2015, Art. no. 016019.
[19] J. C. Barrese et al., "Failure mode analysis of silicon-based intracortical microelectrode arrays in non-human primates," *J. Neural Eng.*, vol. 10, no. 6, Nov. 2013, Art. no. 066014.
[20] V. S. Polikov, P. A. Tresco, and W. M. Reichert, "Response of brain tissue to chronically implanted neural electrodes," *J. Neurosci. Methods*, vol. 148, no. 1, pp. 1–18, Oct. 2005.
[21] S. Wang et al., "A compact quad-shank CMOS neural probe with 5,120 addressable recording sites and 384 fully differential parallel channels," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1625–1634, Dec. 2019.
[22] M. M. Ghanbari et al., "A Sub-mm3 ultrasonic free-floating implant for multi-mote neural recording," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3017–3030, Nov. 2019.
[23] S. A. Mirbozorgi, P. Yeon, and M. Ghovanloo, "Robust wireless power transmission to mm-sized free-floating distributed implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 692–702, Jun. 2017.

[24] J. Lee et al., "An implantable wireless network of distributed microscale sensors for neural applications," in *Proc. 9th Int. IEEE/EMBS Conf. Neural Eng.*, 2019, pp. 871–874.

[25] D. Seo et al., "Wireless recording in the peripheral nervous system with ultrasonic neural dust," *Neuron*, vol. 91, no. 3, pp. 529–539, Aug. 2016.

[26] J. Jeong et al., "Conformal hermetic sealing of wireless microelectronic implantable chiplets by multilayered atomic layer deposition (ALD)," *Adv. Funct. Mater.*, vol. 29, no. 5, 2019, Art. no. 1806440.

[27] U. Passlack, N. Simon, V. Bucher, C. Harendt, T. Stieglitz, and J. N. Burghartz, "Flexible ultrathin chip-film patch for electronic component integration and encapsulation using atomic layer-deposited Al2O3TiO2 nanolaminates," *ACS Appl. Mater. Interfaces*, vol. 15, no. 12, pp. 16221–16231, Mar. 2023.

[28] P. Moshayedi et al., "The relationship between glial cell mechanosensitivity and foreign body reactions in the central nervous system," *Biomaterials*, vol. 35, no. 13, pp. 3919–3925, Apr. 2014.

[29] R. Ritter, J. Handwerker, T. Liu, and M. Ortmanns, "Telemetry for implantable medical devices: Part 1 - media properties and standards," *IEEE Solid-State Circuits Mag.*, vol. 6, no. 2, pp. 47–51, Spring 2014.

[30] M. Vomero et al., "Conformable polyimide-based μECoGs: Bringing the electrodes closer to the signal source," *Biomaterials*, vol. 255, Oct. 2020, Art. no. 120178.

[31] T. Stieglitz et al., "Highly conformable chip-in-foil implants for neural applications," *Microsystems Nanoeng.*, vol. 9, no. 1, May 2023, Art. no. 54.

[32] D. Ji, T. Li, W. Hu, and H. Fuchs, "Recent progress in aromatic polyimide dielectrics for organic electronic devices and circuits," *Adv. Mater.*, vol. 31, no. 15, 2019, Art. no. 1806070.

[33] D. Khodagholy et al., "NeuroGrid: Recording action potentials from the surface of the brain," *Nature Neurosci.*, vol. 18, no. 2, pp. 310–315, Feb. 2015.

[34] C. Gueli, J. Martens, M. Eickenscheidt, and T. Stieglitz, "Scalable batch transfer of individual silicon dice for ultra-flexible polyimide-based bioelectronic devices," in *Proc. IEEE 43rd Annu. Int. Conf. Eng. Med. Biol. Soc.*, 2021, pp. 6880–6883.

[35] C. Gueli, "Towards a chip-in-foil implant for neural applications," Ph.D. dissertation, Albert-Ludwigs-Universität Freiburg im Breisgau, Freiburg im Breisgau, Germany, 2023.

[36] D. Haci, Y. Liu, S. S. Ghoreishizadeh, and T. G. Constandinou, "Design considerations for ground referencing in multi - module neural implants," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2018, pp. 1–4.

[37] S. F. Cogan, "Neural stimulation and recording electrodes," *Annu. Rev. Biomed. Eng.*, vol. 10, no. 1, pp. 275–309, 2008.

[38] D. R. Merrill, M. Bikson, and J. G. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, no. 2, pp. 171–198, Feb. 2005.

[39] T. Stieglitz, "Implantable device fabrication and packaging," in *Handbook of Neuroengineering*, N. V. Thakor, ed. Singapore: Springer Nature Singapore, 2023, pp. 289–337.

[40] S. Lange et al., "An AC-powered optical receiver consuming 270 μW for transcutaneous 2 Mb/s data transfer," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 304–306.

[41] B. Szabo, C. Gueli, M. Eickenscheidt, and T. Stieglitz, "Polyimide-based thin film conductors for high frequency data transmission in ultra-conformable implants," *Curr. Directions Biomed. Eng.*, vol. 6, no. 3, pp. 481–485, Sep. 2020.

[42] S.-H. Ahn, J. Jeong, and S. J. Kim, "Emerging encapsulation technologies for long-term reliability of microfabricated implantable devices," *Micromachines*, vol. 10, no. 8, Aug. 2019, Art. no. 508.

[43] M. Beygi et al., "Fabrication of a monolithic implantable neural interface from cubic silicon carbide," *Micromachines*, vol. 10, no. 7, Jul. 2019, Art. no. 430.

[44] F. Deku, Y. Cohen, A. Joshi-Imre, A. Kanneganti, T. J. Gardner, and S. F. Cogan, "Amorphous silicon carbide ultramicroelectrode arrays for neural stimulation and recording," *J. Neural Eng.*, vol. 15, no. 1, Jan. 2018, Art. no. 016007.

[45] M. Vomero et al., "Incorporation of silicon carbide and diamond-like carbon as adhesion promoters improves in vitro and in vivo stability of thin-film glassy carbon electrocorticography arrays," *Adv. Biosyst.*, vol. 2, no. 1, 2018, Art. no. 1700081.

[46] L. Tong, M. Mehregany, and W. Tang, "Amorphous silicon carbide films by plasma-enhanced chemical vapor deposition," in *Proc. IEEE Micro Electro Mech. Syst.*, 1993, pp. 242–247.

[47] R. Harrison, "A low-power, low-noise CMOS amplifier for neural recording applications," in *Proc. IEEE Int. Symp. Circuits Syst. Proc.*, 2002, vol. 5, pp. 197–200.

[48] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub- μ vrms-noise sub- μ w/channel ADC-Direct neural recording with 200-mV/ms transient recovery through predictive digital autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018.

[49] C. Lee et al., "A 6.5-μW 10-kHz BW 80.4-dB SNDR gm-c-based CT $\Delta\Sigma$ modulator with a feedback-assisted gm linearization for artifact-tolerant neural recording," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2889–2901, Nov. 2020.

[50] H. Chandrakumar and D. Marković, "A 15.2-ENOB 5-kHz BW 4.5- μw chopped CT $\Delta\Sigma$ -ADC for artifact-tolerant neural recording front ends," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, Dec. 2018.

[51] C. Pochet, J. Huang, P. Mercier, and D. Hall, "A 174.7-dB FoM, 2nd-order VCO-based ExG-to-Digital front-end using a multi-phase gated-inverted ring oscillator quantizer," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1283–1294, Dec. 2021.

[52] L. Somappa and M. S. Baghini, "A 400 mV 160 nW/Ch compact energy efficient $\Delta\Sigma$ modulator for multichannel biopotential signal acquisition system," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 4, pp. 765–776, Aug. 2021.

[53] W. Zhou, W. L. Goh, Y. Chen, T. Zhang, and Y. Gao, "A 100-mVpp input range 10-kHz BW VCO-based CT-DSM neuro-recording IC in 40-nm CMOS," in *Proc. IEEE 32nd Int. Syst.-on-Chip Conf.*, 2019, pp. 466–470.

[54] M. Sporer, N. Graber, S. Moll, S. Reich, and M. Ortmanns, "Implementation of a low power decimation filter in a 180 nm HV-CMOS technology for a neural recording front-end," in *Proc. SMACD/PRIME 2021; Int. Conf. SMACD 16th Conf. PRIME*, 2021, pp. 1–4.

[55] Z. Tan, C.-H. Chen, Y. Chae, and G. C. Temes, "Incremental delta-sigma ADCs: A tutorial review," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 67, no. 12, pp. 4161–4173, Dec. 2020.

[56] T. Bockhorst, F. Pieper, G. Engler, T. Stieglitz, E. Galindo-Leon, and A. K. Engel, "Synchrony surfacing: Epicortical recording of correlated action potentials," *Eur. J. Neurosci.*, vol. 48, no. 12, pp. 3583–3596, 2018.

[57] M. Sporer, S. Reich, J. G. Kauffman, and M. Ortmanns, "A direct digitizing chopped neural recorder using a body-induced offset based DC servo loop," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 3, pp. 409–418, Jun. 2022.

[58] M. A. Mokhtar, P. Vogelmann, M. Haas, and M. Ortmanns, "A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT incremental DeltaSigma modulator with differentially reset FIR feedback," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 87–90, Sep. 2019.

[59] J. Markus, J. Silva, and G. Temes, "Design theory for high-order incremental converters," in *Proc. IEEE Int. Symp. Intell. Signal Process.*, 2003, 2003, pp. 3–8.

[60] J. Markus, P. Deval, V. Quiquempoix, J. Silva, and G. C. Temes, "Incremental delta-sigma structures for DC measurement: An overview," in *Proc. IEEE Custom Integr. Circuits Conf.*2006, 2006, pp. 41–48.

[61] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 29, no. 2, pp. 155–162, Apr. 1981.

[62] D. R. Welland, B. P. D. Signore, and D. A. Kerth, "Delta-sigma analog-to-digital converter with chopper stabilization at the sampling frequency," US Patent US5039989A, Aug. 13, 1991.

[63] S. Pavan, "Improved chopping in continuous-time delta-sigma converters using FIR feedback and N -path techniques," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 65, no. 5, pp. 552–556, May 2018.

[64] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A comparative study on excess-loop-delay compensation techniques for continuous-time SigmaDelta modulators," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 55, no. 11, pp. 3480–3487, Dec. 2008.

[65] J. Cherry and W. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 661–676, Jun. 1999.

[66] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*, 1st ed, (Advanced Microelectronics Series), vol. 21. Berlin, Germany:Springer, 2006.

[67] D. Wendler et al., "A 0.0046-mm2 two-step incremental DeltaSigma analog-to-digital converter neuronal recording front end with 120-mVpp offset compensation," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 439–450, Feb. 2023.

[68] D. Haci, A. Mifsud, Y. Liu, S. S. Ghoreishizadeh, and T. G. Constandinou, "In-body wireline interfacing platform for multi-module implantable microsystems," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2019, pp. 1–4.

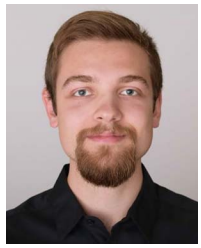
[69] S. S. Ghoreishizadeh, D. Haci, Y. Liu, N. Donaldson, and T. G. Constandinou, "Four-wire interface ASIC for a multi-implant link," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 64, no. 12, pp. 3056–3067, Dec. 2017.

[70] C. Eder, V. Valente, N. Donaldson, and A. Demosthenous, "A 1-Wire communication interface between a control hub and locally powered epidural stimulators," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2013, pp. 214–217.
[71] C. Gabriel, S. Gabriel, and E. Corthout, "The dielectric properties of biological tissues: I. Literature survey," *Phys. Med. Biol.*, vol. 41, no. 11, pp. 2231–2249, Nov. 1996.
[72] M. F. P. Cruz, *Conformable Epicortical Implants Brain Mapping: A Technological Perspective Neural Recordings*, (Biomedical Microtechnologies), vol. 20, Munich, Germany: Verlag Dr.Hut, 2021.
[73] A. Rothermel et al., "A CMOS chip with active pixel array and specific test features for subretinal implantation," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 290–300, Jan. 2009.
[74] H. Kaim, C. Brendler, V. Rieger, and A. Rothermel, "Capacitive coupled full-wave rectifier for rectangular power signals," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2015, pp. 1–4.
[75] C. M. Lopez et al., "A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13 Mm SOI CMOS," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 510–522, Jun. 2017.

Markus Sporer (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering in 2015 and 2018, respectively, from the University of Ulm, Ulm, Germany, where he is currently working toward the Ph.D. degree with the Institute of Microelectronics, under the supervision of Prof. Dr.-Ing. M. Ortmanns, with a focus on analog and mixed-signal circuits for biomedical applications. From 2016 to 2017, he interned with the IC Group at the Robert Bosch Research and Technology Center in Palo Alto, CA, USA. In 2019, he joined the Institute of Microelectronics, the University of Ulm.

Ioana-Georgiana Vasilaş received the B.Sc. degree in bioengineering from the University of Medicine and Pharmacy Gr.T.Popa Iasi, Romania, in 2017, and the M.Sc. degree in neuroscience from the University of Strasbourg, Strasbourg, France, in 2019. She is currently working toward the Ph.D. degree under the supervision of Prof. Dr.-Ing. T.Stieglitz at the Laboratory for Biomedical Microtechnology, Department of Microsystems Engineering, University of Freiburg, Freiburg, Germany. Her research interests include the study of tissue-electrode interface with special emphasis on ECoG arrays and polyimide substrates.

Ahmed Adžemović received the B.Sc. degree in genetics and bioengineering from the International University of Sarajevo, Bosnia and Herzegovina, in 2018, and the M.Sc. degree in innovative medicine from the University of Groningen, The Netherlands, and Uppsala University, Uppsala, Sweden, in 2020. He is currently working toward the Ph.D. degree with the Institute of Biology III, University of Freiburg, Freiburg im Breisgau, Germany, under the supervision of Prof. Dr. Ilka Diester, and as part of the European School of Network Neuroscience Innovative Training Network. His research focuses on the role of prefrontal cortex in the control of movements in rodents.



Nicolas Graber (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering in 2021 from the University of Ulm, Ulm, Germany, where he is currently working toward the M.Sc. degree in electrical engineering and information technology. In 2023, he interned at the Analog and Mixed-Signal Department, Qualcomm Technologies Inc., Cork, Ireland.

Stefan Reich (Member, IEEE) received the B.Sc., M.Sc., and Dr.-Ing. degrees in electrical engineering from the University of Ulm, Ulm, Germany, in 2015, 2018 and 2023, respectively. His research in the Group of Prof. Dr.-Ing. M. Ortmanns focuses on integrated analog and mixed-signal circuits for biomedical application and brain-machine interfaces. In 2016, he completed an eight month internship with the Robert Bosch Research and Technology Center in Palo Alto, CA, USA, where he worked on integrated circuits and digital synthesis. Mr. Reich was the recipient of the VDE award for his bachelor thesis in 2016 and the VDI award for his master thesis in 2019.

Calogero Gueli received the B.Sc. and M.Sc. degrees in microsystems engineering from the University of Freiburg, Freiburg, Germany, in 2016 and 2018, and the Ph.D. degree in 2023 from the Department of Microsystems Engineering, under the supervision of Prof. Dr.-Ing. T. Stieglitz, with a focus on development of novel processes for microfabrication of neural interfaces. In 2016 he interned with the MEMS Research Laboratory, the San Diego State University, San Diego, CA, USA, in a collaborative project between Freiburg and San Diego.

Max Eickenscheidt received the master's and Ph.D. degrees in biophysics from Technical University Munich, Munich, Germany, in 2006 and 2010, respectively. During this time he was a Research Fellow with the Max-Planck Institute for Biochemistry, Martinsried, Germany. His work focused mainly on capacitive bi-directional coupling of high-density CMOS chips for neuronal recording and especially retinal stimulation. He continued his work on neural interfaces a Senior Scientist with the Natural and Medical Institute Reutlingen and Max-Planck Institute for Intelligent Systems, Stuttgart, Germany. In 2015, he became a Group Leader with the Department of Microsystems Engineering (IMTEK), University of Freiburg, Freiburg im Breisgau, Germany, where he focused on novel interfacing materials on polymer based neural probes for in-vivo applications. Since 2020, he has been the team leader and Project Manager with neuroloop GmbH, Germany.

Ilka Diester received the Ph.D. degree about the "Representations of numerical formats in the monkey association cortex". She spent three years as a Postdoctoral Fellow with the labs of Karl Deisseroth and Krishna Shenoy, Stanford University, Stanford, CA, USA, where she established optogenetics in monkeys. In 2011 she established her own lab at the Ernst Strüngmann Institute for Neuroscience in Cooperation with Max Planck Society. Her Ph.D. work was awarded with the Academy Prize for Biology of the Academy of Science of Göttingen in 2009. For her work, she was the recipient of the Boehringer-Ingelheim Award in 2012 and the TILL Photonics Technology Prize 2013. She also was the recipient of the Bernstein Award for Computational Neuroscience in 2012, and the ERC Starting Grant in 2013. Since 2014, she has been a full Professor of optophysiology with the University of Freiburg, Freiburg im Breisgau, Germany, working on local and distributed processing of movement preparation and generation in the motor cortex as well as higher order structures, e. g. prefrontal cortex. She is currently the Managing Director of the IMBIT and Spokesperson of the BrainLinks-BrainTools Center.

Thomas Stieglitz (Fellow, IEEE) received the Dr.-Ing. degree from the University of Saarland, Saarbrücken, Germany, in 1998. He was with the Fraunhofer Institute for Biomedical Engineering, St. Ingbert, Germany, from 1993 to 2004, where he established the section of neural engineering. He is currently a Full Professor for biomedical microtechnology with the Laboratory for Biomedical Microtechnology, which he founded in 2004, with the Department of Microsystems Engineering (IMTEK), University of Freiburg, Freiburg im Breisgau, Germany. He is currently the Managing Director of the IMTEK and Spokesperson of the BrainLinks-BrainTools Center. Thomas Stieglitz is the Co-Founder of two Neurotechnology Companies, CorTec GmbH and Neuroloop GmbH, holds about 30 patents and has coauthored about 500 peer-reviewed papers and conference proceedings in the field of neural prostheses.His research interests include the design and development of flexible neural microimplants to interface with the nervous system as well as on biocompatible assembly and packaging.

Maurits Ortmanns (Senior Member, IEEE) received the Dr.-Ing. degree from the University of Freiburg, Breisgau, Germany, in 2004. From 2004 to 2005, he was with Sci-Worx GmbH, Hannover, Germany, working in the field of mixed-signal circuits for biomedical implants. In 2006, he joined the University of Freiburg, as an Assistant Professor. Since 2008, he has been a Full Professor with the University of Ulm, Ulm, Germany, where he is currently the Head of the Institute of Microelectronics. He has authored the textbook *Continuous-Time Sigma-Delta A/D Conversion*, authored or co-authored several other book chapters, and more than 250 IEEE journal and conference papers. He holds several patents. His current research interests include mixed-signal integrated circuit design with special emphasis on data converters and biomedical applications.