Impedance-Readout Integrated Circuits for Electrical Impedance Spectroscopy: Methodological Review

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***Abstract*—This review article provides a comprehensive overview of impedance-readout integrated circuits (ICs) for electrical impedance spectroscopy (EIS) applications. The readout IC, a crucial component of on-chip EIS systems, significantly affects key performance metrics of the entire system, such as frequency range, power consumption, accuracy, detection range, and throughput. With the growing demand for portable, wearable, and implantable EIS systems in the Internet-of-Things (IoT) era, achieving high energy efficiency while maintaining a wide frequency range, high accuracy, wide dynamic range, and high throughput has become a focus of research. Furthermore, to enhance the miniaturization and convenience of EIS systems, many emerging systems utilize two-electrode or dry electrode configurations instead of the conventional four-electrode configuration with wet electrodes for impedance measurement. In response to these trends, various technologies have been developed to ensure reliable operations even at two- or dry-electrode interfaces. This article reviews the principles, advantages, and disadvantages of techniques employed in state-of-the-art impedance-readout ICs, aiming to achieve high energy efficiency, wide frequency range, high accuracy, wide dynamic range, low noise, high throughput, and/or high input impedance. The thorough review of these advancements will provide valuable insights into the future development of impedance-readout ICs and systems for IoT and biomedical applications.**

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I. Introduction

In RECENT years, there has been a growing interest in real-time monitoring of physiological signals, facilitated by advancements in wearable devices. This technology enables continuous assessment of the health status and early detection of abnormalities, leading to improved healthcare outcomes. One technique that has gained prominence in this field is electrical impedance spectroscopy (EIS), which offers a versatile and non-invasive measurement of bio-impedances [1], [2], commonly referred to as bioZ.

Impedance measurements can be used to assess the electrical properties of biological tissues [3], providing valuable insights into the body composition [4], fluid distribution [5], and/or tissue health [6]. It can also be applied to monitoring cardiovascular parameters like heart rate variability and cardiac output [7]. In respiratory monitoring, lung impedance measurements offer valuable information on lung functions and pulmonary health [1], [6], [7]. Moreover, impedance measurement techniques have shown promise in cancer detections by detecting tissue abnormalities and characterizing tumor progression [8], [9], [10], [11].

The utilization of frequency sweeping in bioZ measurements allows for a more thorough assessment of the bioZ, as the electrical current pathways in the tissues vary depending on the frequency of the injected signal [3]. This impedance measurement technique over frequency, referred to as EIS, enables to implement the aforementioned applications in the form of wearable systems [2]. Each of those applications requires the impedance measurement circuit to have distinct performance parameters, driving continuous advancement in the structure and building blocks to meet the specific demands. Fig. 1 presents an overall block diagram of impedance-readout integrated circuits (ICs), featuring five specialized parameters specifically tailored for diverse applications. Structures and techniques of impedance-readout ICs to improve each of the performance parameters are discussed from Sections III to VII, as shown in Fig. 1. While all the applications need suitable performances in all the parameters, here are some application examples which demand specific parameters more.

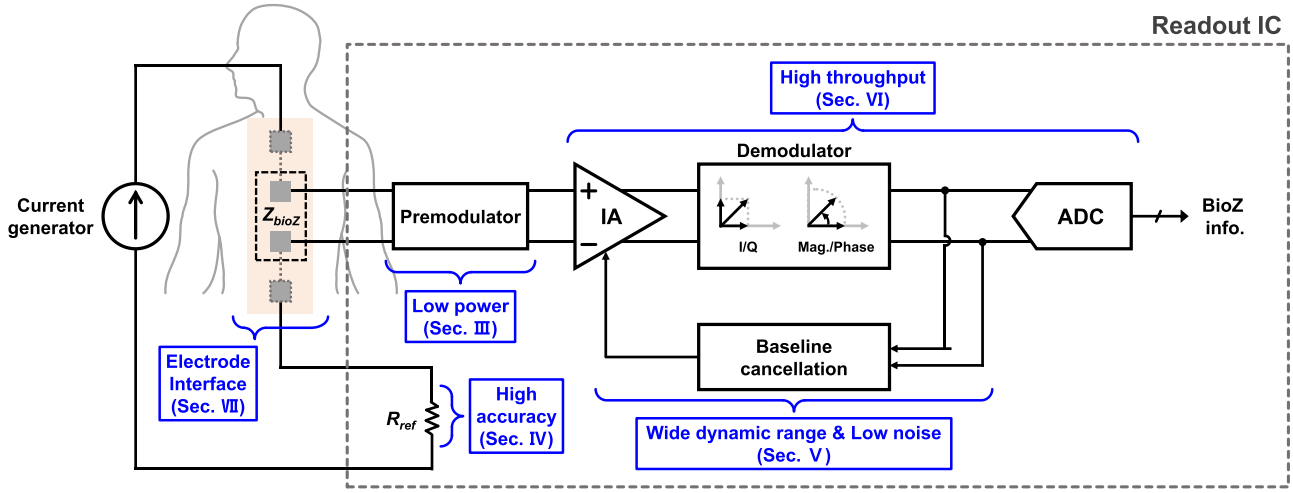

Fig. 1. Overall block diagram of general impedance-readout ICs with relevant building blocks to improve major performance parameters.

First, for effective distinction of various types of cancer cells, impedance measurements of the tissue need to be conducted over a frequency range spanning from 100 Hz to several MHz [10], [12], while the absolute accuracy being of paramount importance. This requirement also applies to the body composition analysis [13], [14]. Various techniques have been proposed to achieve higher accuracy while keeping the power consumption low. Some of these structures involve the addition of reference resistors [15] or modifications in the demodulation method, as illustrated in the Fig. 1. These approaches prioritize the accuracy and low-power consumption, potentially sacrificing the throughput and dynamic range, which are less important for the specific applications [16].

Second, there are applications which require to measure the time-varying impedance, such as monitoring of cardiovasculator signals [7], which vary over time, and respiration for lung function and pulmonary health [1], [6]. These applications typically require measurements in the frequency range of 5 Hz to 250 kHz [17]. More importantly, the impedance variation is approximately 3000 times smaller than the constant baseline impedance [18]. As a result, a dynamic range of 100 dB or higher is demanded [17]. To achieve such a high dynamic range, baseline cancellation techniques are commonly employed [17]. These techniques often entail subtracting the calculated baseline value from the received signal at the amplifier [18], [19], [20], as depicted in the Fig. 1. These techniques often involve utilizing square signals [18], [19], [20], for the ease of noise cancellation, while potentially compromising the accuracy to attain the higher dynamic range.

There are also some applications which demand fast measurement throughput. One of such applications is neural electrical impedance tomography (EIT) where the neural activities of nerves are monitored using multi-channel impedance measurements and image reconstruction [2]. Although this application's measurement frequencies are relatively low, typically ranging from 4 to 18 kHz [21], [22], a large number of measurements is needed to obtain a single tomographic image of the nerve. Therefore, the throughput performance of the readout IC is crucial in consideration of the frame rate required for image visualization. To address this, some advancements have been made, including direct ADC sampling [23], which can enhance the throughput performance of the system by skipping the analog I/Q demodulation. These advancements may result in a slight increase in power consumption but are crucial for enabling real-time image visualization in EIT applications. Additionally, in neural applications, the signal generator and the readout IC often share the same electrodes for signal excitation and sensing to reduce the total number of electrodes [24]. To facilitate this electrode configuration, dedicated techniques and practical considerations are required to ensure reliable operation.

Several review papers on EIS systems have already been published. Some of them focus on signal generators [25], [26] or sensors [27], [28] while other review papers discuss specific types of readout ICs associated with particular applications [2], [17]. In this article, we mainly focus on impedance-readout ICs, exploring circuit structures and techniques to improve main performance parameters for a variety of applications. We delve into various circuits and techniques to achieve low power consumption, high frequency range, high accuracy, wide dynamic range, and high throughput. Dedicated techniques for interfacing specialized electrode configurations are also explored. Additionally, this article includes newly presented structures that have emerged after the publication of those review papers.

The primary objective of this article is to present representative circuit structures and techniques specialized for enhancing specific performance parameters. We offer a comprehensive range of choices for further research, thus allowing circuit designers to apply design techniques optimized for each application. This article covers all the performance parameters shown in Fig. 1. and related circuit techniques.

Detailed discussions on circuits for accuracy and wide dynamic range can be found in [2] and [17], respectively. An in-depth review of EIT and related techniques is available in [2]. Please refer to [17] to obtain insights and more detailed discussion on electrode placements.

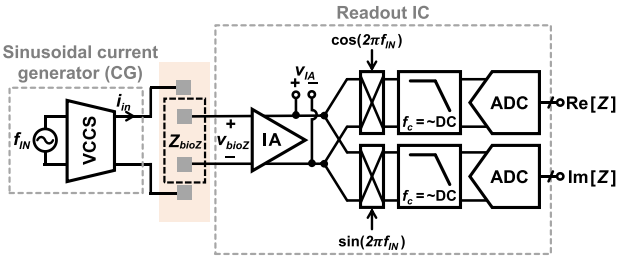

Fig. 2. Conventional EIS system.

The remainder of this article is organized as follows. Before introducing new techniques, Section II presents the conventional structure of readout ICs, offering an overview of its components, functionality, and limitations. Then, Section III focuses on the pre-demodulation technique, primarily employed for low-power operation. Section IV examines the utilization of reference resistors, magnitude/phase detection architecture, and digital calibration methods, all of which play a crucial role in achieving high accuracy in EIS systems. Section V discusses specialized structures for wide dynamic range and low noise, while Section VI explores architectures tailored for high throughputs. Lastly, Section VII reviews additional techniques specifically designed for the two- and dry-electrode interface, including practical considerations in actual measurements. Finally, Section VIII offers a comprehensive summary and comparison of the discussed structures and techniques, and Section IX provides a conclusion for the article.

II. Conventional Architectures

This section introduces the most conventional and basic structure. As depicted in Fig. 2, this structure is based on an I/Q demodulator that is used to measure the real and imaginary components of the target impedance. The I/Q demodulation structure can be implemented with analog blocks, but it can also be implemented in the digital domain by oversampling the signal with an ADC and using digital multiplexers and filters [29]. The current signal generated by the sinusoidal current generator ($i_{in}(t)$) can be represented as follows:

$$i_{in}(t) = I_0 \cos(2\pi f_{IN} t), \tag{1}$$

where I_0 and f_{IN} are the amplitude and frequency of the injected current signal, respectively. The current signal flows through the bioZ, and the voltage generated across the bioZ ($v_{bioZ}(t)$), which is the input of the instrumentation amplifier (IA), can be represented as follows:

$$v_{bioZ}(t) = I_0 |Z_{bio}| \times \cos(2\pi f_{IN} t + \theta_{bio}), \tag{2}$$

where $|Z_{bio}|$ and θ_{bio} are the magnitude and phase of the bioZ, respectively. The received signal $v_{bioZ}(t)$ is first amplified by the IA. Subsequently, when the amplified $v_{bioZ}(t)$ signal (v_{IA}) is multiplied by the in-phase and quadrature-phase signals, denoted as $\cos(2\pi f_{IN} t)$ and $\sin(2\pi f_{IN} t)$, the resulting voltages ($v_{Re}(t)$ and $v_{Im}(t)$) are as follows:

$$\begin{aligned} v_{Re}(t) &= A \times I_0 |Z_{bio}| \times \cos(2\pi f_{IN} t + \theta_{bio}) \times \cos(2\pi f_{IN} t) \\ &= \frac{1}{2} A I_0 |Z_{bio}| (\cos(\theta_{bio}) + \cos(2\pi 2 f_{IN} t + \theta_{bio})), \\ v_{Im}(t) &= A \times I_0 |Z_{bio}| \times \cos(2\pi f_{IN} t + \theta_{bio}) \times \sin(2\pi f_{IN} t) \\ &= \frac{1}{2} A I_0 |Z_{bio}| (\sin(\theta_{bio}) + \sin(2\pi 2 f_{IN} t + \theta_{bio})), \end{aligned} \tag{3}$$

where A is the IA gain. The high-frequency components, $\cos(2\pi 2 f_{IN} t + \theta_{bio})$ and $\sin(2\pi 2 f_{IN} t + \theta_{bio})$, which are located at $2f_{IN}$ or above, can be filtered out easily by the subsequent low-pass filters (LPFs).

In practical circuit implementations, the direct multiplication of analog sinusoidal values poses significant challenges due to its inherent circuit complexity and high power consumption [30], [31]. To address this issue, the chopping technique with a square-wave clock is commonly employed. In this scenario, the square signals of the in-phase and quadrature-phase can be represented with a combination of a Fourier series of odd-number harmonic tones. These harmonic tones are multiplied by $v_{IA}(t)$ of frequency f_{IN} at the chopper and converted into frequencies of $2Nf_{IN}$ (where N is positive integers from 1). If $i_{in}(t)$ consists solely of a pure sinusoidal waveform at the precise frequency f_{IN}, there will be no harmonic-tone folding to the DC level. In such a case, it is possible to eliminate all the high-frequency terms caused by the harmonic tones of the demodulation clocks by using a LPF. Consequently, the real value of $|Z_{bio}|\cos(\theta_{bio})$ and the imaginary value of $|Z_{bio}|\sin(\theta_{bio})$ are obtained, and these values can be used to calculate the target impedance's amplitude and phase.

Due to limitations in generating a perfect sinusoidal signal across a wide frequency range, alternative waveforms such as pseudo-sinusoids with small harmonics or even simplified square-wave can be used as $i_{in}(t)$. The pseudo-sinusoid is a waveform that has a sinusoidal pattern with quantization levels, generated by a digital-to-analog converter (DAC), rather than an oscillator which can produce a continuous sinusoidal signal. When using such waveforms, frequencies that align with the harmonics of the chopping clock are converted to DC, resulting in errors in the measurement results [30], [32], [33]. These current signals are commonly employed when the measurement of the absolute impedance value is not a critical factor, but rather when there is a need to track the impedance changes with minimized power consumption and complexity. They are often used with calibration methods to achieve higher levels of accuracy, which will be discussed in Section IV.

III. Techniques for High-Frequency Range With Low Power

In EIS systems, measurements of the bioZ at multiple frequencies are needed to acquire more complete impedance information of the target, and they can also be used to generate a Cole-Cole plot [34]. It becomes in high demand to extend the frequency range of the measurement to 1 MHz or even beyond to support applications like blood characterization, fingerprint sensing, and cancer diagnosis [12], [35], [36].

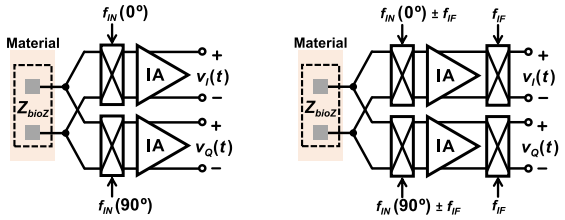

Fig. 3. Low-power EIS systems with pre-demodulation to (a) DC and (b) intermediate frequency.

In the conventional architecture for EIS measurements, a wide-bandwidth IA is typically used to amplify the high-frequency input signal measured from the bioZ [10], [12], [37], [38], [39], as depicted in Fig. 2. After amplification, the amplified signal undergoes the I/Q demodulation. In this widely-used architecture, the IA requires a power consumption that is proportional to the signal frequency. Thus, the higher the EIS frequency range gets, the higher power consumption the IA requires to consume, making it difficult to extend the frequency range with low power.

To address this issue, pre-demodulation techniques, which are based on frequency shifting of the input signal from a high frequency to a lower frequency in front of IA, have been proposed. In this section, two representative pre-demodulation methods are reviewed. These techniques help the readout IC relax its bandwidth requirements and allow it to measure the impedance at high frequencies with much lower power consumption.

A. Pre-Demodulation to DC

The impedance-readout system in [1] conducts the I/Q demodulation in front of the IA to minimize the power consumption, as shown in Fig. 3(a). In contrast to the conventional approach, where the demodulation is performed after the IA, this pre-demodulation technique performs the signal demodulation to DC in front of the IA. Thus, the IA's bandwidth does not need to be higher than the input signal frequency (f_{IN}), leading to the low power consumption of the IA. In addition, the intrinsic low-pass characteristics of the subsequent stages, i.e., the IA, programmable gain amplifier (PGA), and buffer, can contribute to the removal of the high-frequency components, eliminating the need for additional high-order LPFs. Moreover, this early I/Q demodulation process up-converts the DC electrode offset and motion artifacts to higher frequencies, avoiding the use of circuits like a high-pass filter (HPF) and thus saving associated areas. The subsequent stages in the system can effectively eliminate these up-converted DC electrode offsets and demodulated harmonics.

However, this pre-demodulation technique is severely affected by the IA's noise, particularly by the flicker noise. A common approach to mitigating flicker noise involves increasing the size of the noise-contributing transistors. However, despite adopting this approach [1], the system continues to exhibit significant input-referred noise of 112 nV/$\sqrt{Hz}$ across the 0 – 2 kHz frequency range. Moreover, this approach can significantly increase the area to decrease the corner frequency of flicker noise [40] and degrade the input impedance [2].

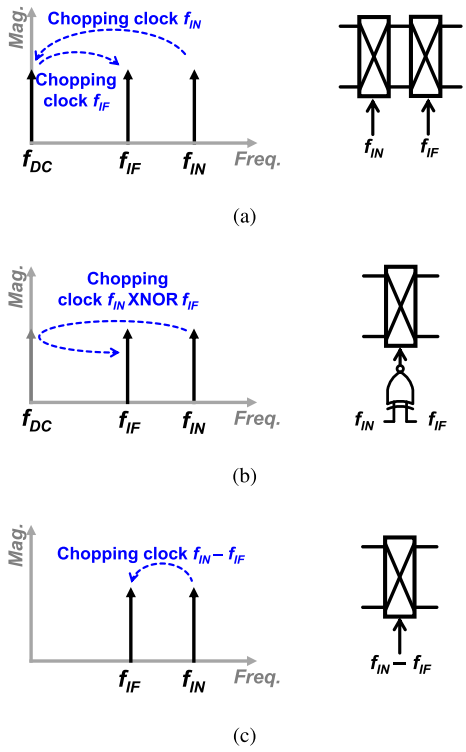

Fig. 4. Frequency-domain illustration, and block diagram of IF demodulation techniques using (a) two choppers and two chopping clocks, (b) one chopper and one XNOR-merged clock, and (c) a single chopping clock of $f_{IN} - f_{IF}$.

B. Pre-Demodulation to IF

As an alternative strategy for achieving a wide excitation frequency bandwidth without increasing power consumption, the pre-demodulation can be conducted to down-convert the signal to an intermediate frequency (IF), f_{IF}, rather than to DC, as depicted in Fig. 3(b) [18], [41], [42], [43], [44], [45], [46], [47]. Compared to the pre-demodulation technique that down-converts to DC, pre-demodulation to IF can avoid placing the signal on the bandwidth of the flicker noise of the IA [43]. This results in significantly lower the input-referred noise compared to the pre-demodulation to DC method. As demonstrated in [46], the input-referred noise was measured to be 36.2 nV/$\sqrt{Hz}$ over the 0 – 7.8125 kHz band. To achieve effective signal amplification at f_{IF}, the IA's bandwidth must cover the IF band, but this requirement may lead to just a slight increase in power dissipation compared to the method using pre-demodulation to DC.

In the conventional IF demodulation, the input signal undergoes two chopping steps, as depicted in Fig. 4(a). The signal at the injected high frequency, f_{IN}, is initially demodulated to DC and then modulated to f_{IF}. After amplification by the subsequent IA, the signal at IF is demodulated back to DC. To implement this IF demodulation, two series-connected choppers

can be used [41], [42]. The first chopper demodulates the signal to DC, and the second chopper modulates the signal to the IF. Alternatively, the XNOR-based chopper method [18], [43], [44], [45] merges the two processes into one by using a single input chopper, as depicted in Fig. 4(b).

This single chopper can effectively replace the two series-connected choppers by using an XNOR-based clock which is generated by the XNOR operation between the f_{IN} and f_{IF} clocks [43]. In addition to the circuit simplicity, this method using the single chopper with XNOR reduces the input leakage current from 0.312 nA to 0.280 nA (7.4%) and the standard deviation of the IA input offset from 11.4 nV to 8.6 nV (24.5%) when compared to the series-connected double-chopper method [43].

Unlike the method shown in Fig. 4(a) and (b), the proposed method in [46], [47] directly demodulates the signal to the IF. Fig. 4(c) illustrates the frequency modulation achieved through the direct IF demodulation. It employs a chopping clock with a frequency of $f_{IN} - f_{IF}$. This direct IF demodulation preserves phase information by modulating the signal directly to the IF and eliminates the need for early I/Q demodulation. Additionally, it prevents potential harmonic folding during up-conversion, which would otherwise require additional filtering [46].

The IF demodulation can be utilized in applications that require an RF excitation signal in the MHz-to-GHz range [48], [49]. This technique involves down-converting the RF excitation frequency to IF using an active mixer, relieving the bandwidth and power consumption constraints for the subsequent amplification stage. In addition, by employing the IF demodulation, the DC offset and noise generated by the active mixer can be avoided.

IV. Techniques for High Accuracy

In conventional IQ demodulator structures, the measurement accuracy is largely impacted by the clock timing mismatch between the excitation signal and the demodulation signals of the readout IC. This timing mismatch can happen from two main sources. The first error source is the time delay at the voltage-controlled current source (VCCS) in the signal generator. To extract the imaginary value from an I/Q demodulator, it is necessary to have a clock that has a 90° phase shift compared to the reference in-phase of the excitation signal. However, generating a clock with a reference in-phase within the readout IC itself is a challenging task due to the intricacies involved in performing a 90° phase shift for each frequency of the excitation signal's frequency range [16]. As a result, it is more common to take the voltage clock signal before the VCCS in the signal generator and utilize it for generating the I/Q demodulation clocks for mixing at the readout IC [12], [41], [50]. However, the VCCS intrinsically has a time delay from its input and output, and this creates a timing error between the excitation current signal and the I/Q demodulation clocks. Moreover, this time delay varies over frequency. The second source of error is the time delay introduced by the IA in the readout IC. The IA also has a time delay between its input and output, and this delay gets worse as the frequency increases. This IA delay creates a time mismatch with the I/Q demodulation clocks, directly affecting the phase measurement result.

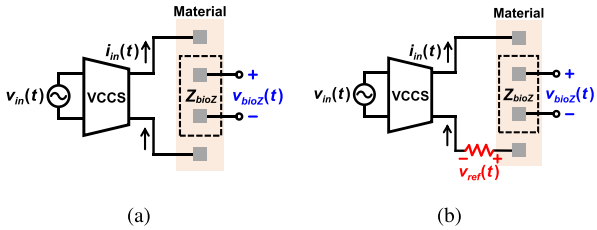

Fig. 5. Simplified bioZ measurement configurations: (a) without and (b) with the reference resistor.

This section reviews the reference resistor structure, which can address the errors caused by signal generator delays. It also delves into the magnitude/phase detection architectures that utilize this approach. Additionally, the discussion covers error-compensation techniques for reducing signal harmonic errors.

A. Reference Resistor

To mitigate the errors caused by the VCCS delay in the signal generator, a reference resistor can be added in series with the bioZ. Fig. 5 illustrates two configurations for bioZ measurements: one with a reference resistor and the other without. Both structures utilize a VCCS to convert the input voltage signal, $v_{in}(t)$, into a current signal, $i_{in}(t)$. This current is then applied to the bioZ, and the resulting voltage, $v_{bioZ}(t)$, is measured. In the conventional structure depicted in Fig. 5(a), the current, $i_{in}(t)$, only passes through the bioZ. In this structure, the delays and non-linearities of the VCCS affect the final measurement results. To address this issue, a reference resistor is inserted in series with the bioZ, as shown in Fig. 5(b) [15]. In this configuration, the same current, $i_{in}(t)$, flows through both the bioZ and the reference resistor, producing two voltages, $v_{bioZ}(t)$ and $v_{ref}(t)$. As resistors have a zero-phase impedance, the voltage signal across the reference resistor, $v_{ref}(t)$, exhibits the same phase as $i_{in}(t)$. Hence, $v_{ref}(t)$ can serve as a reference for the magnitude and phase measurements, mitigating the effects of the VCCS delays and non-linearities [16], [51].

Nevertheless, in the conventional I/Q structure where a 90°-shifted clock is necessary for the quadrature-phase demodulation, effectively utilizing the reference resistor becomes problematic. The difficulty arises from the need to shift the clock received through the reference resistor by 90° for each frequency over the given frequency range [16]. In this section below, alternative architectures that capitalize on the reference resistor to measure the phase directly instead of extracting the imaginary component are reviewed. By doing so, they can eliminate the requirement for a 90°-shifted clock and overcome the limitations of the previous structures.

B. Magnitude/phase Detection

The polar structure, which directly detects the magnitude and phase, unlike the conventional I/Q demodulator, often utilizes a reference resistor to ensure the synchronization between the

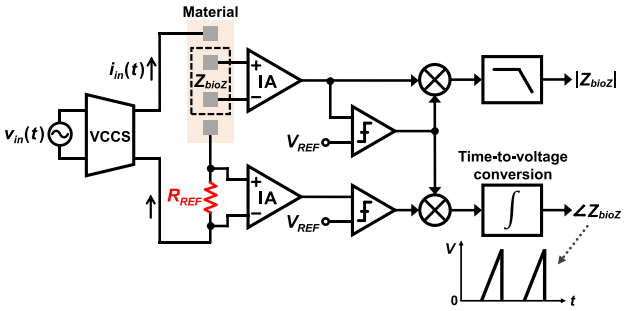

Fig. 6. Magnitude and phase measurement IC with a reference resistor [15].

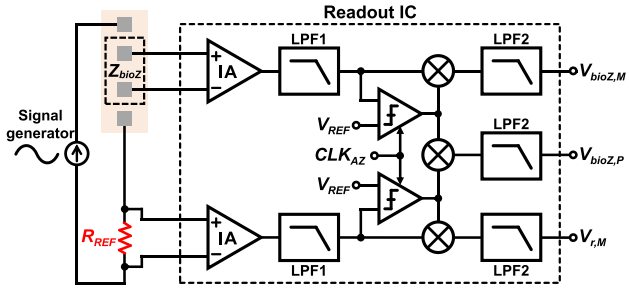

Fig. 7. Magnitude and phase measurement IC with a reference resistor and an additional reference-magnitude measurement path [51].

excitation signal and other clocks in the demodulator. Various methods have been proposed for measuring the magnitude, such as those employing a self-mixing full-wave rectifier [15], [51], an adaptive-sampling scheme [52], a received-signal-strength indicator [53], and a time-stamp scheme [54]. Among them, the following works incorporate the reference resistor in their designs: [15], [51], [52].

In [52], a clock generated from the reference resistor is utilized to detect the peak time of the measured bioZ signal and obtain magnitude values at the peak times. This process involves a 90° phase shift of the reference clock. Unlike the I/Q demodulator, this structure can extract the delay information of the 90°-shifted clock by using the signal generated from the reference resistor. By utilizing the found delay information, it is possible to compensate for the errors arising from the comparator delay and clock generator for each frequency. This compensation allows to achieve a magnitude error of 1% and a phase error of less than 2°. However, the circuit complexity of this approach is likely to be vulnerable to mismatches caused by parasitic elements. Additionally, current and capacitor-based integrators are required to generate the 90°-shifted clock, which requires an additional comparator in the high-frequency range, resulting in higher power consumption.

As an alternative simpler method for measuring the magnitude, a self-mixing full-wave rectifier is used, as depicted in Fig. 6 [15]. Here the bioZ signal amplified by the IA is converted into a clock signal using a zero-crossing comparator. The clock is used for self-mixing with the bioZ signal itself, generating a rectified bioZ signal, which is then low-pass-filtered to the final magnitude measurement value. This clock is also used to be mixed with the clock generated from the zero-crossing comparator, which receives the signal from the reference resistor. Both of these two clocks go through the IA, respectively, and a similar delay is added. Thanks to this process, the inherent delay of the IA and the delay caused by the signal generator are compensated, generating more accurate phase results. Nevertheless, errors may still arise due to the nonlinearity of the IA or the delay introduced by the comparators, resulting in magnitude and phase errors of approximately 2% and 4°, respectively.

Fig. 7 presents a structure designed to mitigate these errors [51]. It introduces an additional magnitude measurement path for the reference signal from the reference resistor. Because both paths use the same blocks, i.e., the IA, LPF1, chopper, and LPF2, their non-linearity and comparator delay are similar. By comparing the results from the two paths, these non-idealities are canceled each other in their measurement of the magnitude and phase. Consequently, this approach achieves small magnitude and phase errors of less than 1.1% and of less than 2°, respectively. However, when the size difference between the reference resistor and the bioZ becomes large, the two paths get more different, inducing larger mismatches in the amplitude-dependent comparator delays and the IA's non-linearity variations. To address this issue, the size of the reference resistor can be varied to have a similar size to the bioZ.

The phase measurement in the polar structure can be achieved by utilizing zero-crossing comparators to convert the voltage signals into square-wave signals. These square-wave signals are then processed using simple logic circuits like an XOR/XNOR gate or latches [51], [52]. The width of the resulting output signal corresponds to the phase of bioZ, so it can be easily translated to the measurement of the phase by using an LPF. By employing this structure, it becomes possible to effectively mitigate the errors introduced by the VCCS and the IA because the clocks generated from the bioZ and reference resistors are made after the IA. To improve its power efficiency further, the frequency-shifting technique discussed in Section III is utilized in conjunction with the polar structure described above [51]. By combining these techniques, the polar structure can achieve reduced power consumption while maintaining high measurement accuracy.

The polar structure with a reference resistor can improve the accuracy by reducing the timing error, especially caused by VCCS. Nevertheless, this polar structure requires the use of an additional measurement path compared to the conventional I/Q demodulator, resulting in increased power and area consumption. Moreover, this configuration requires the VCCS to support a wider output liner range and a higher output impedance due to the reference resistor being connected in series with bioZ. The polar structure in [54] resolves the timing error caused by VCCS through minimizing the time delay of VCCS. That is, rather than measuring the time delay through the reference resistor, it minimizes the time delay of a VCCS itself. This approach mitigates the requirements in multi-channel and high output impedance of current driver, achieving magnitude and phase errors of 3% and 0.51°, respectively. However, a VCCS based on closed-loop structure is required to obtain the minimized time

delay, which results in higher power consumption compared to general open-loop current driver [26].

C. Digital Calibration

There are also some calibration techniques available to reduce the errors without altering the existing structure. In the I/Q architecture, the delays caused by the 90° phase shift or synchronization mismatch can be calibrated by measuring a known impedance additionally [55]. By leveraging this information, compensation for the delays can be applied to achieve sufficient accuracy in impedance measurements. However, this method requires additional measurement with a known impedance at each frequency, which is a huge overhead.

Besides, when the excitation signal from the signal generator is not a perfect sinusoid, it includes harmonic tones. These tones can cause errors in the impedance measurement through the frequency-mixing demodulation process. In the case of using a square waveform as the excitation signal, phase-measurement errors of more than 10° can arise due to its huge harmonics [32]. Moreover, due to frequency-varying bioZ values, it is not easy to identify and cancel the errors caused by such multiple high-frequency harmonic tones.

Certain harmonics can be avoided by adjusting the duty cycle of the clocks [33]. By having specific different duty cycles for the input excitation signal and the demodulation signal, the major harmonics can be avoided at the output of the mixer. This method allows the achieving of an error range of 5–6%, which is relatively large, when using a square-wave signal. Moreover, this method needs accurate control of the duty cycle, requiring a 60 times higher frequency of the excitation signal.

[56] proposes an algorithm that involves measurements at three different frequencies to determine the specific values of R and C in an RC model. When using this method, the measurement errors can be reduced to within 3%. However, this algorithm has a limitation: it can be applied to one- or two-pole RC models only. Alternatively, a more reliable harmonic cancellation technique is proposed in [30]. It is based on the fact that the square-wave clock's harmonics are known. Using the measured I/Q measurement results at higher frequencies, the folded error from the harmonics can be canceled as post-processing in the digital domain. This method allows using square-wave clocks instead of pseudo- or pure sinusoids as the excitation signal for impedance measurements, thus simplifying the measurement process and saving energy. However, it requires measurements at frequencies beyond the target range.

V. Techniques for Wide Dynamic Range and Low Noise

In some applications of EIS, like heartbeat or respiration monitoring [57] and impedance pneumography [58], the measurement target impedance is composed of a large baseline impedance that remains relatively constant and a varying impedance that changes over time. The presence of the baseline impedance of bioZ, typically in the kΩ range [59], may cause saturation of the impedance-readout IC when a high-amplitude excitation current is applied by the current generator (CG) to enhance the signal-to-noise ratio (SNR). Moreover, when a

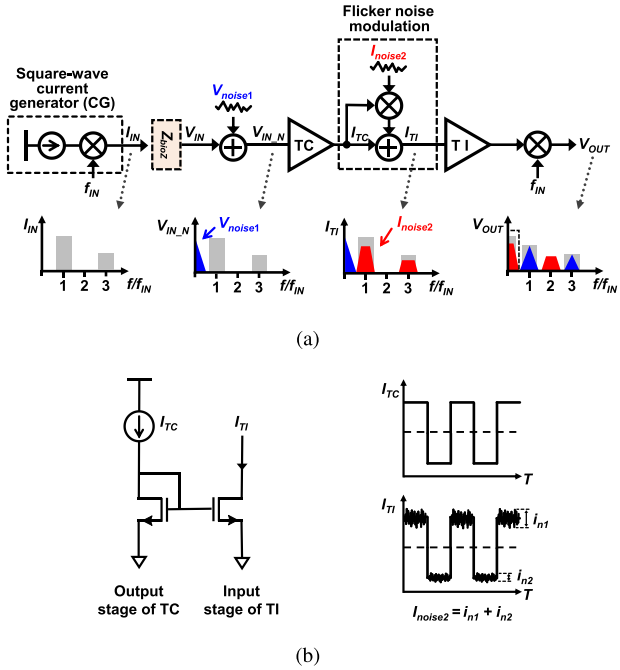

Fig. 8. The flicker noise modulation in the impedance-readout IC using CBIA [40]. (a) Conceptual block diagram and spectrum diagrams. (b) Simplified operation of CBIA's current mirroring and time-domain noise behavior with a large square-wave input.

two-electrode configuration is used for impedance measurements, the baseline impedance is significantly increased by the electrode-tissue impedance (ETI), worsening the issues of saturation and SNR. Therefore, impedance-readout ICs require i) a large dynamic range (DR) to accommodate a large baseline and ii) a large SNR to effectively resolve small impedance variations in the presence of a large baseline.

To elaborate these issues more in detail, an example impedance-readout structure is shown in Fig. 8(a), where a current-balancing instrumentation amplifier (CBIA) is used. The CBIA is widely used in EIS systems due to its high input impedance and good power efficiency [18], [43], [60], [61]. The CBIA comprises transconductance (TC) and transimpedance (TI) stages, which are interconnected through a current mirror. Because the excitation signal is located at f_{IN}, which is typically higher than the flicker noise range, the flicker noise (V_{noise1}) can be avoided thanks to the demodulation of the signal after the TI stage, similar to the chopping techniques. However, when I_{IN} is applied for bioZ measurements, the flicker noise of its current mirror (I_{noise2}) is modulated at the same frequency (f_{IN}). This modulated flicker noise is demodulated along with the signal, directly affecting the measurement result and thus degrading the SNR [40].

Fig. 8(b) depicts a schematic of a simplified CBIA's current mirror and illustrates the flicker noise modulation effect within the CBIA in the time domain. When an AC current from I_{TC}, which is the output current of the TC stage, is applied to the current mirror, the noise magnitude of I_{TI}, which is the input current of the TI stage, also varies accordingly. This variation in noise magnitude occurs due to the direct proportionality between

the noise power of the current mirror and its current. As the input amplitude increases, the flicker noise also increases. It results in different amplitudes of flicker noise (i_{n1} and i_{n2}) in the current mirror. For instance, when the input voltage of the CBIA is increased from 0 mV to 20 mV, the contribution of flicker noise significantly increases from 51.6 nV/$\sqrt{Hz}$ to 337.1 nV/$\sqrt{Hz}$ at 1 Hz [40]. Consequently, this flicker noise modulation in the CBIA significantly impacts the overall noise performance of the system, especially when the input signal includes a large baseline impedance. To mitigate this noise modulation, it is essential to maintain a small input to the CBIA.

A. Baseline Cancellation

To address these aforementioned challenges, BioZ readout ICs have recently adopted baseline cancellation techniques. Similar to a DC-servo loop (DSL), which removes the DC offset, the baseline cancellation techniques cancel out the baseline impedance by subtracting it from the input signal. Thanks to this removal of baseline, small bioZ variations can be more easily detected while increasing the readout IC's DR. Additionally, the flicker noise modulation in CBIA can be mitigated by reducing the signal swing of the current mirror.

Representative impedance-readout ICs with baseline cancellation are shown in Fig. 9. [18] proposes a digital-assist baseline cancellation, which continuously extracts the baseline impedance from the digital output and subtracts it from the input signal. As shown in Fig. 9(a), the digitized baseline impedance is subtracted from the signal at the TC amplifier stage of the CBIA using a current-steering digital-to-analog converter (IDAC). By removing most of the baseline impedance, only a small time-varying impedance remains as the effective input to the CBIA's TI stage. This reduction of the amplitude significantly reduces the input-dependent noise of the IA and enhances the input DR, which enables accurate measurement even in a two-electrode configuration. Furthermore, this approach ensures robustness against saturation even when employing a high gain stage. However, the residual current resulting from the limited resolution of the IDAC still remains, inducing input-dependent noises yet.

To minimize this residual current, a direct digitization bioZ readout architecture in [19] is proposed. As illustrated in Fig. 9(b), the proposed architecture adopts a first-order delta-sigma modulator with an IIR-based digital loop filter (DLF). The DLF enables precisely tracking the input signal while eliminating input-dependent 1/f noise and minimizing the residual current.

A mixed-mode baseline cancellation is another approach to minimize residual current noise, as illustrated in Fig. 9(c) [20]. This mixed-mode approach combines analog and digital methods for baseline cancellation within the TC stage. The analog baseline cancellation is achieved using an analog Gm cell, continuous-time RC integrator, and attenuator. It cancels the baseline signal by copying and reflecting the baseline opposite to the input current. If the baseline current is too large for the analog cancellation to handle alone, the digital baseline cancellation is activated. It uses a comparator to monitor the output voltage of the analog integrator, generating up/down signals to control

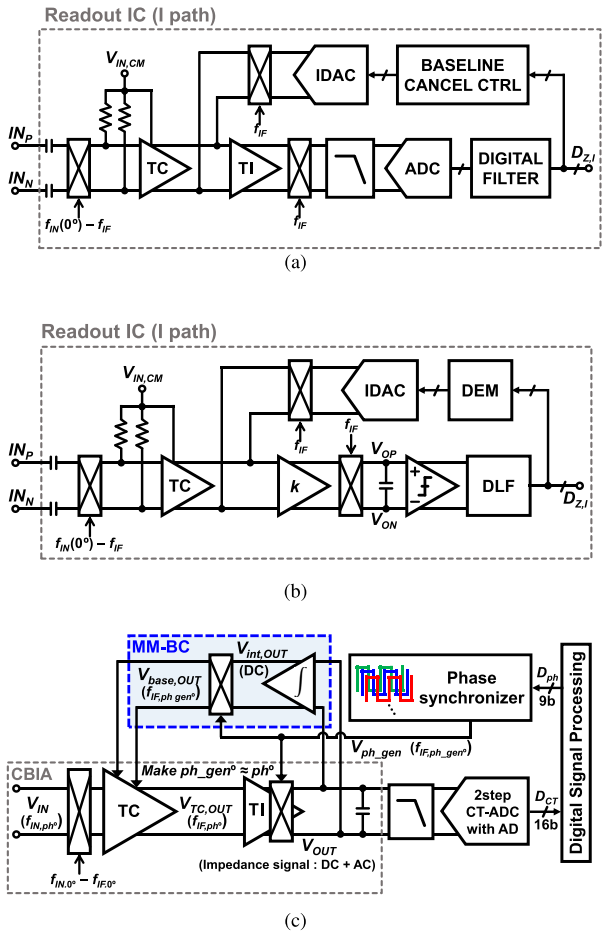

Fig. 9. Block diagrams of readout IC with (a) digital-assisted baseline cancellation [18], (b) direct digitization [19], and (c) mixed-mode baseline cancellation [20].

a counter. This counter adjusts the digital cancellation current using IDACs. By combining both approaches, this technique improves the dynamic range and reduces modulated 1/f noises by compensating for baseline signals.

However, the process of these baseline cancellation techniques takes a long time to settle, especially when dealing with large baseline impedances or large artifacts. [23] adopts successive approximation (SA) for its baseline tracking, offering significantly faster settling time. This SA-based approach provides a rapid and efficient solution for tracking baseline variations and mitigating unwanted motion artifacts or baseline drifts. A two-step conversion process is adopted for the digital conversion of the input, which involves generating coarse bits that control a current-based baseline cancellation circuit, followed by obtaining fine bits through a SAR ADC. This two-step conversion can cancel the baseline variations effectively and fast.

B. Correlated Noise Cancellation

In addition to achieving a wide dynamic range and addressing the input-dependent noise, the baseline cancellation can also be utilized to reject the reference noise, which comes from the reference current source of the CG. Fig. 10 illustrates a

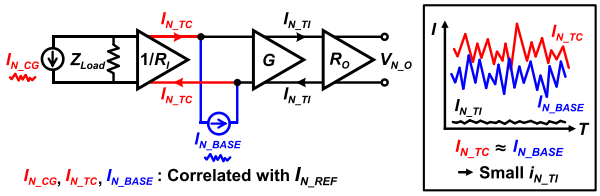

Fig. 10. Principle of the correlated noise cancellation in CBIA [18].

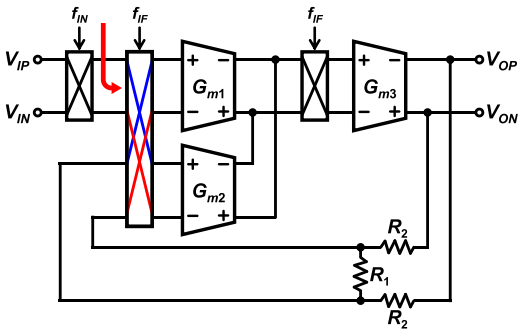

Fig. 11. Block diagram of current-feedback instrumentation amplifier with quiet chopping [62].

technique for the correlated reference noise cancellation. Even with the utilization of dynamic element matching (DEM) to mitigate the noises in the CG [44], the noise of the reference current, which is typically derived from the bandgap reference (BGR), remains within the signal band. By sharing the reference current between the CG and the IDAC of the readout IC, a strong correlation is established between them [18], [19], [20]. This means that when the magnitudes of the CG current (I_{CG}) and the baseline current (I_{BASE}) are identical, the reference current noise (I_{N_REF}) is amplified by the same factor in both. In the CBIA, I_{TC} is determined by I_{CG}, along with the input impedance (Z_{LOAD}) and the transconductance of the TC stage ($1/R_1$). Through the baseline cancellation, I_{BASE} and I_{TC} are approximately equal and can be effectively canceled out by subtracting I_{BASE} from I_{TC}. The difference between I_{TC} and I_{BASE} is replicated through a current mirror, resulting in a significant reduction in the current noise of the TI stage (I_{N_TI}). Therefore, it can effectively eliminate I_{N_REF}'s contribution to the overall system noise.

C. Quiet Chopping

The Quiet chopping (QC) is an alternative method for reducing the input-dependent noise [42]. The QC current-feedback instrumentation amplifier (CFIA) has been proposed to overcome the limitation of the normal chopping CFIA [63]. While the normal chopping CFIA offers 1/f noise removal and common-mode (CM) isolation of the input stage, it suffers from its reduced input impedance due to the chopping and also from gain errors caused by the mismatch of the input Gm stage. To address this issue, the QC CFIA, as illustrated in Fig. 11, can achieve higher input impedance and ensures dynamic matching between the two input Gm cells by changing how the choppers switch the inputs. By synchronously swapping the two input Gm cells during each QC cycle, the CFIA achieves high input impedance comparable to a non-chopped CFIA while effectively demodulating the input signal to the baseband. Furthermore, the QC technique effectively eliminates signal-dependent noises by ensuring that the input signals observed by the swapping Gm1 and Gm2 cells are nearly identical even for high-magnitude inputs.

VI. Techniques for High Throughput

EIS systems measure the magnitude and phase of complex bio-impedance over a range of frequencies, not a specific frequency, thereby obtaining valuable insights into the characteristics of biological tissues. One of the widely used methods for obtaining the impedance spectrum involves injecting a sinusoidal excitation current at a specific frequency and measuring the resulting voltage's phase shift and amplitude for measuring the impedance. This process can be repeated by sweeping the excitation frequency across the desired frequency range. This single-frequency measurement method offers a high SNR but suffers from long measurement time due to the extended data acquisition time required for capturing the complete impedance spectrum [64]. Therefore, achieving high throughput with fast settling is crucial to ensure efficient and rapid transitions between frequencies in EIS systems, reducing the overall measurement time.

Moreover, in applications of EIT and real-time impedance monitoring, this requirement becomes particularly critical to track physiological activities in real-time. An EIT measurement setup typically requires multiple electrodes placed around the human body to enable real-time impedance imaging for monitoring and diagnosing medical conditions. If the settling time exceeds the impedance measurement time of an electrode, it can lead to a decreased image frame rate, compromising the effectiveness of EIT [65]. Therefore, it is crucial to design a readout IC to settle quickly between electrode switching while maintaining a high frame rate.

A. Analog Filter Control

One conventional architecture of impedance-readout ICs in EIS systems includes down-conversion of the impedance-modulated signal to DC after the IA, as explained in Section III. Because the signal's bandwidth is typically less than 10 Hz, the LPF's cut-off frequency is less than 100 Hz to reject the higher-frequency chopping ripples. Such a low cut-off frequency of the LPF to extract the DC output severely limits the achievable measurement throughput and causes long measurement times.

The method in [6] uses a passive LPF with PMOS pseudo-resistors and capacitors to dynamically control the cut-off frequency to improve the settling time. The resistance of the pseudo-resistor (R_{PR}) can be controlled by adjusting the gate voltage. Initially, R_{PR} is set to be low to increase the LPF's corner frequency and speed up the signal settling. Subsequently, R_{PR} is increased to have the targeted corner frequency for filtering out the tones other than the signal at DC. However, R_{PR} is highly dependent on the input signal, so it can introduce unwanted signal distortions. To address this, [66] proposes a

voltage-controlled pseudo-resistor (VCPR) that maintains a high resistance with low distortions. The VCPR utilizes a switched-capacitor circuit to generate the gate voltage. The VCPR in the LPF enables two operating modes (settling and attenuation) to effectively control the cut-off frequency without signal distortion and attenuate the demodulation-induced ripples.

Alternatively, the settling time of the analog filter can be reduced at the system level. The work in [16] addresses the LPF-induced settling-time issue by modifying the system's architecture. Here both the magnitude and real (in-phase) values are measured using identical LPFs with the same cut-off frequency. The settling time is determined by two factors: the rising time, which is mainly determined by the slew rate, and the linear settling time, which is determined by the cut-off frequency. Due to the limited slew rate of the system, both magnitude and real values exhibit the same slope during the rising phase. On the other hand, the linear settling time depends on the cut-off frequency (f_c) and is proportional to the final value (V_{DC}). It can be expressed as $V_{DC} \times (1 - e^{-2\pi f_c t})$. When the ratio of the magnitude and real values is found, the term dependent on the cut-off frequency $(1 - e^{-2\pi f_c t})$ cancels out each other. Thus, accurate measurement results can be obtained immediately after the rising phase without the need to wait for the long settling.

Besides the LPF, the HPF, which is used to remove the DC offset at the electrode-tissue interface, is also a time-consuming block due to its large time constant. It can slow down the system's overall response time when the input signal from the impedance changes abruptly [66], [67]. In particular, the settling time of HPF poses a tough challenge in EIT operations which have frequent switching between sensing and excitation electrodes. In [45], two analog buffers connected in parallel with the resistors of the HPF are used to overcome the issue of large settling time. These buffers assist in charging the capacitor of HPF, reducing the time constant. This configuration enables fast settling within a few hundred milliseconds. Alternatively, the settling time of HPF is reduced by using a switch to hold the output node of HPF at a reference voltage for half the period of the excitation frequency [66]. To achieve such precise turn-off timing at the zero-crossing point, a digital controller generates synchronized on-off signals for the switch based on the timing of the excitation current. This method effectively reduces the settling time of the HPF to just 5 μs for an excitation signal frequency of 100 kHz, while the conventional passive HPF with a similar setup typically requires over 300 μs for settling.

B. Direct Sampling

The direct sampling technique directly quantizes the impedance-modulated signal, skipping the down-conversion of the signal to DC in the analog domain [68], [69], [70]. Fig. 12 depicts a block diagram of an impedance-readout IC utilizing the direct sampling. This approach offers several advantages over conventional analog demodulation, which involves down-conversion. One advantage is that it eliminates the need for a 90°-phase-shifted analog signal, simplifying the system design. Additionally, the direct sampling allows for the use of a wider-bandwidth LPF, which can readily meet the anti-aliasing

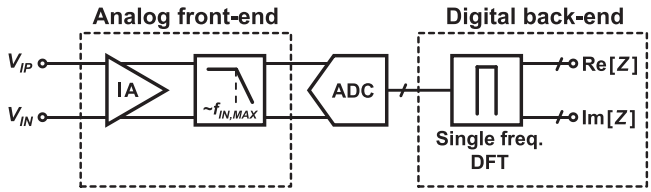

Fig. 12. Block diagrams of impedance-readout IC with direct sampling.

requirements of the ADC. The cut-off frequency of the LPF can be high enough to be easily implemented with small-sized passive components and also lead to a fast settling time. By eliminating the need for down-conversion and reducing the settling time of the LPF, the direct sampling improves the overall system's measurement throughput. However, it does come with some trade-offs. The direct sampling requires a high-speed ADC, which leads to increased power consumption and a limited measurement frequency range.

There is another direct sampling technique called synchronous sampling [23]. In this method, a square-wave signal is injected to the target impedance, and the input impedance signal is amplified. Then, the amplified signal is sampled and quantized at the end of each period of the excitation current injection. This approach offers a significantly high throughput over the conventional I/Q demodulation for impedance measurements. This makes the synchronous sampling well suited for applications like neural EIT [22], allowing fast capture and analysis of neural activity.

In a comparative study shown in [29], it has been found that the analog demodulation typically requires a higher-resolution ADC and a more complex low-pass filter to achieve the same SNR within the same processing time than digital demodulation methods utilizing direct sampling. The analog demodulation is cost-effective and area-efficient at low SNR levels, but its power consumption surpasses the digital demodulation as the required SNR level increases. Therefore, the choice between analog and digital demodulation necessitates careful considerations of SNR, power consumption, and processing time.

C. IF Sampling

The IF demodulation is a technique that performs down-conversion to IF before IA, as discussed in Section III. By using the IF demodulation, the IA's bandwidth and also power consumption do not need to increase as the excitation frequency increases. To reduce the channel settling time in this architecture using IF demodulation, the signal can be quantized at the IF by an ADC with a fast sampling rate [18], [44]. Instead of having a very low cut-off frequency, the filter can be designed to have a relatively high cut-off frequency in the order of f_{IF}. This relaxation in the design constraints of the anti-aliasing filter allows for a faster settling time at the cost of the marginal increase in the ADC power consumption. This IF sampling technique bypasses the demodulation process in the analog domain and directly digitizes the signal in the IF domain, leading to an improvement in the measurement throughput.

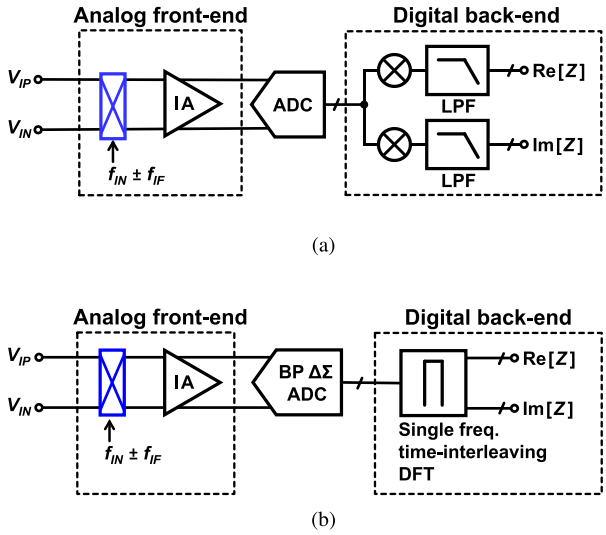

Fig. 13. Block diagrams of impedance-readout ICs using IF demodulation with (a) digital demodulation [47], and (b) band-pass $\Delta\Sigma$ ADC and digital FFT [71].

The work in [47] adopts the IF sampling to enhance the system throughput, as depicted in Fig. 13(a). The architecture effectively addresses the bandwidth and power limitations by employing direct IF sampling without demodulating the signal to DC. The I/Q demodulation is performed in the digital domain. Such digital demodulation eliminates the need for analog demodulation and narrow-bandwidth low-pass filters, enhancing the throughput and enabling faster data rates. Furthermore, a digital switched ratiometric dual-phase (SRDP) demodulation technique is proposed to address the impact of signal fluctuations and chip-to-chip variations. The digital SRDP demodulation module on the FPGA hub compares the demodulated signals with a reference signal to detect small impedance values and eliminate the measurement fluctuations from the analog front-end. On the other hand, an alternative approach in [71] is proposed. It adopts a single-sideband (SSB) mixer for direct IF sampling without the distortion caused by odd-order harmonics. As shown in Fig. 13(b), a band-pass $\Delta\Sigma$ ADC is used to directly quantize the signal in the IF domain, eliminating the need for the LPF and thus enabling a faster throughput. The time-interleaving DFT is performed in the digital domain to enhance the overall throughput further. By interleaving the data from four channels, the system can process them simultaneously to extract impedance information, resulting in a fourfold increase in the throughput.

VII. Practical Consideration for Electrode Interface

In the EIS systems, it is crucial to consider not only the circuitry and the bioZ's characteristics but also the measurement environments and user convenience. Among these considerations, the electrode interface for measurements, such as the placement, location, number, and type of electrodes, plays a paramount role.

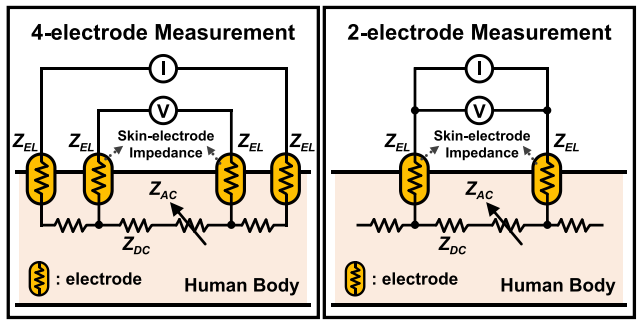

Fig. 14. Comparison of four-electrode and two-electrode configurations of EIS measurements.

The placement of electrodes on the body can influence on the quantity of BioZ and the tolerance of measurement. For instance, according to the impedance plethysmogram (IPG) measurement using electrodes on the neck [20], the longer the distance between electrodes gets, the larger the IPG amplitude becomes. At the maximum distance, the maximum IPG amplitude of $0.08\,\Omega_{pp}$ is observed. According to the mental healthcare system based on multi-modal bio-signals including BioZ, motion artifacts can be mitigated by measuring bio-signals through electrodes behind the ear [72].

Recently, there has been a rising demand for reducing the number of electrodes for small form factor devices and user convenience [18], [19]. By reducing the number of electrodes from four to two, the baseline impedance gets much larger, and it gets more difficult to effectively eliminate the common-mode interference. In addition, dry electrodes are preferred over wet electrodes for long-term monitoring due to their user convenience [73], [74]. However, the impedance of dry electrodes can be easily compared to the input impedance of the readout IC, leading to the degradation of the input signal. Additionally, the impedance of dry electrodes varies more than wet electrodes, making the system more vulnerable to motion artifacts.

This section focuses on reviewing circuit structures specifically designed to tackle the challenges associated with the electrode interface. These specialized circuit configurations aim to optimize the performance of the electrode interface, striking a delicate balance between accuracy and user convenience in EIS measurements.

A. Two-Electrode Configuration

Fig. 14 illustrates impedance measurement configurations using four and two electrodes. In the case with four electrodes, two electrodes are used to apply current signals to the bioZ by the signal generator, while the readout IC measures the voltage signals across the other two electrodes. If the input impedance of the readout IC is sufficiently large, the electrode impedance connected to the readout IC does not significantly influence the voltage signal caused by the bioZ. Consequently, the readout IC can capture only the voltage difference across the bioZ.

On the other hand, when using two electrodes, the signal generator and the readout IC share the same two electrodes

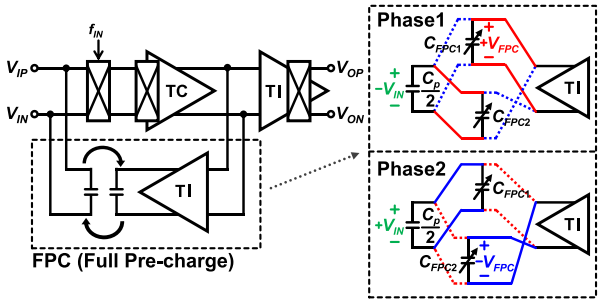

Fig. 15. Input-impedance boosting technique using the pre-charging technique [42].

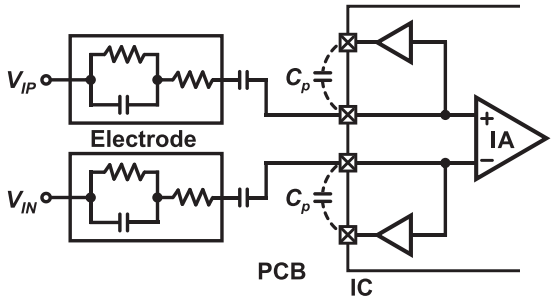

Fig. 16. Input-impedance boosting technique using active shielding [75].

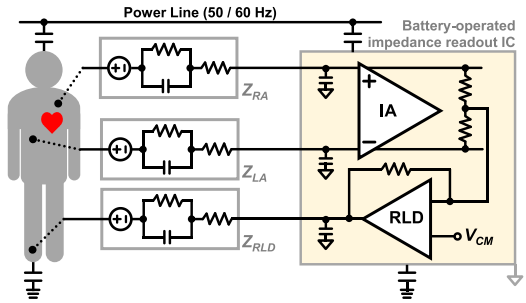

Fig. 17. Block diagram of the driven-right-leg (DRL) or right-leg-drive (RDL) configuration for body biasing and common-mode voltage control.

for signal transmission and measurement. In this configuration, it is not possible to differentiate between the electrode impedance and the bioZ. The excitation current flows through the electrodes and bioZ. As a result, the voltage received by the readout IC is contributed from the combined impedance, i.e., $Z_{DC} + Z_{AC} + 2 \times Z_{EL}$, where Z_{DC} is the constant baseline portion of the target impedance and Z_{AC} is the time-varying portion of the target impedance. Because of the reduced number of electrodes, this setup allows for a smaller form factor of the system [18]. However, to accurately measure Z_{AC} the temporal variations of bioZ in this configuration, the input impedance of the readout IC should be significantly larger than $Z_{DC} + Z_{AC} + 2 \times Z_{EL}$. Moreover, it should have a wide dynamic range to deal with the large baseline increased by the electrode impedance. Precisely knowing the size of Z_{EL} is also required to extract $Z_{DC} + Z_{AC}$ accurately. Nevertheless, in applications where only the variation of impedance (Z_{AC}) is required, such as ECG and respiration monitoring, the two-electrode configuration can be used. In such cases, precise measurement of Z_{DC} and Z_{EL} is not necessary, and they can be effectively eliminated by the baseline cancellation techniques discussed in Section V.

B. Dry Electrode

EIS is well-suited for continuous monitoring of physiological signals due to its low power consumption and small form factor. However, the use of wet electrodes is not ideal as it can lead to discomfort for the user and a decrease in signal quality over time due to dehydration of the conductive gel. Alternatively, dry electrodes can be used for better user convenience. Dry electrodes typically have a higher electrode-tissue impedance in the range of several hundred kΩ, but their impedance decreases and stabilizes over time due to sweat [73]. To facilitate the application of dry electrodes, the input impedance of impedance-readout ICs should be high enough [42], [61], [75], [76], [77].

Fig. 15 shows an impedance-boosting technique that utilizes pre-charging of the parasitic capacitance between the input pad and the printed circuit board (PCB). The charge that would charge or discharge this parasitic capacitance is stored in a pre-charged capacitor (C_{FPC}), which is then used for pre-charging the input nodes. Since this work uses a square waveform, two capacitors (C_{FPC1} and C_{FPC2}) are used. They alternate between charging and connecting to the input to achieve continuous input impedance boosting synchronized with the clock from the signal generator. Through this method, the input impedance is boosted to the GΩ range.

Another input-impedance boosting technique shown in Fig. 16 uses active shielding for the input of the readout circuit [75]. In this technique, the dominant factor lowering the input impedance, which is the parasitic capacitance on the PCB level, is compensated by using unit-gain buffers. To cancel out this capacitance, the buffer's output is connected to the input pad of the main IA on the PCB domain. Thanks to this, the same voltage is made to both sides of the parasitic capacitor, resulting in a boosting effect on the input impedance. However, the noise generated by the buffer can be added to the input, but with a ratio of.

C. Body Biasing

To fully utilize the readout circuit's dynamic range, the common-mode voltage of the differential voltage inputs of the readout circuit would better be set around the middle of the supply voltage (V_{DD}/2). However, ensuring an exact common-mode voltage in the body is challenging. Moreover, there may be large common-mode interference (CMI), and it should be addressed as well [78].

To address these, two common approaches have been employed. The first approach involves the direct application of a reference voltage to the body [20]. By doing so, the common-mode voltage is fixed to a known value, helping reduce the impact of CMI. Another approach, illustrated in Fig. 17 [44], establishes a feedback loop to match the IA output's common-mode voltage

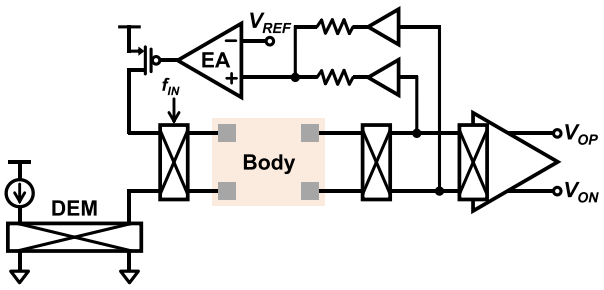

Fig. 18. Bias control loop for body biasing and common-mode voltage control [42].

with a fixed voltage V_{CM}. This technique, known as driven right leg (DRL) or right-leg drive (RDL), effectively mitigates the CMI signal.

However, relying solely on these techniques is insufficient for accurately establishing the common-mode DC voltage at the front-end of the IA. Electrode-induced offsets of voltages up to approximately ± 300 mV may occur [17], necessitating additional measures for removing such offsets. One option is to incorporate a passive HPF in front of the front-end of the readout IC [20], [51]. When utilizing dry electrodes, however, it can be challenging to achieve a high resistance with such HPF. In this case, the HPF is likely to be the dominant factor that lowers the input impedance.

To accommodate the use of dry electrodes, a structure called the bias control loop, shown in Fig. 18, has been proposed. It eliminates the effect of electrode-induced offsets without relying on an HPF. The bias control loop controls the current source of the signal generator to ensure that the incoming common-mode voltage matches the reference voltage. This effectively maintains the common-mode voltage of the input signal. In conjunction with this bias control loop, [42] also employs the full pre-charge technique, enabling the utilization of dry electrodes.

VIII. Summary and Discussion

This article presents a methodological review of impedance-readout ICs for EIS systems, with a specific focus on circuit design aspects. By discussing various circuit design techniques for optimizing parameter metrics, it aims to improve the comprehension of the trade-offs involved in the design process. Table I provides a comparison of impedance-readout ICs, categorized by the circuit design techniques to optimize each parameter.

As shown in the table, impedance-readout ICs for high-frequency ranges usually support a frequency range over hundreds of kHz with low power consumption. In general, impedance-readout ICs to support EIT face trade-offs between frame rate, power budget, and system complexity, and these trade-offs become more pronounced with increased frequency range. The pre-demodulation techniques, which down-convert the input signal to an intermediate frequency or DC before the IA, can alleviate these trade-offs to some extent. The pre-demodulation techniques reduce the frequency range that the readout IC needs to cover, resulting in decreased power dissipation. By doing so, [1], [46] show a significantly low power consumption (< 1 mW) while maintaining the frame rate and SNR, compared to [6]. Just like EIT systems based on impedance measurement, the same trend can be found in wearable EIS systems [18], [19], [20], [42], [43]. By utilizing advanced CMOS technologies and employing lower supply voltages along with pre-demodulation techniques, the power dissipation has been dramatically reduced to only a few tens of μW.

For high accuracy, the utilization of reference resistors and magnitude/phase architectures is instrumental. Eliminating the need for a 90°-shifting clock in magnitude/phase detection removes the synchronization requirements over frequency, leading to improved accuracy. Nevertheless, the polar structure, which measures the magnitude and phase directly rather than the real and imaginary term, requires additional comparators with short delays, which leads to increased power and area consumption. Despite this drawback, the utilization of reference resistors and magnitude/phase architectures allows impedance-readout ICs to achieve superior accuracy with magnitude errors below 1.1% and phase errors below 2° [51], [52].

Recent studies demonstrate the potential of EIS in extracting prognostic medical parameters, offering enhanced clinical diagnosis [79], [80]. [80] demonstrates that the impedance difference between frequencies in the beta dispersion region (i.e., 15 kHz and 307 kHz in this case) differs between healthy individuals and those with various medical conditions by evaluating. For example, the average phase difference in the bioZ exhibits a significantly higher value of 12.20° for healthy individuals when compared to those with emphysema (9.95°), fibrosis (5.42°), and pneumonia (5.85°). These findings highlight the potential of EIS in differentiating lung tissues and improving medical diagnostics. However, current EIS systems struggle with accuracy, particularly in phase detection, leading to challenges in precise disease differentiation. Future studies are needed to refine the tissue differentiation further and develop EIS systems with even higher accuracy to detect phase errors of 1° or less.

In wearable EIS systems used for vital signal measurements, such as monitoring respiration and heart rate, the square waveform is widely used as their excitation current. The utilization of square-wave signals simplifies hardware design by directly injecting a current into bioZ without a current DAC and an extra current driver [26]. However, this approach can lead to significant magnitude and phase errors exceeding 23% and 6°, mainly due to the presence of low-frequency odd-harmonic terms [30]. Despite these challenges, absolute magnitude and phase errors can be tolerated in these applications. This is because the primary objective is to accurately measure small variations of the bioZ, not the absolute value. Therefore, by injecting square-wave signals, it becomes possible to cover a wide frequency range while maintaining power efficiency at the expense of accuracy [18], [19], [20], [42], [43]. Moreover, the implementation of pre-demodulation techniques reduces the bandwidth that the readout IC is required to cover, resulting in exceptionally low power consumption [18], [19], [20], [42], [43]. Moreover, achieving a high SNR in impedance-readout ICs becomes crucial for the precise monitoring of these subtle bioZ variations in addition to reducing the system's form factor and simplifying complexity.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF IMPEDANCE-READOUT ICS

	Tech. [nm]	Supply [V]	Excitation Waveform	Readout power /channel [W]	Frequency range [Hz]	Mag. | Phase error [% | °]	DR[a] [dB]	SNR [dB]	Frame rate [fps]
Impedance-readout ICs with high-frequency range and low power consumption									
[1]	130	1.0	Pseudo-sinusoid	990μ	15.625k – 125k	N/A	N/A	53.3[c]	21
[43]	130	1.2	Square	52μ	16k – 1.24M	N/A	97.1	N/A	N/A
[44]	180	1.2/1.8	Square	18.7μ	1k – 1.024M	N/A	104	76.6[b]	N/A
[45]	180	1.2	Square	36μ[d]	1k – 1.024M	N/A	N/A	N/A	N/A
[46]	130	1.0	Pseudo-sinusoid	830μ	50k – 200k	N/A	N/A	55.0[c]	12.0
Impedance-readout ICs with high accuracy									
[15]	350	±2.5	Sinusoid	21m[d]	100 – 10M	1.78 | 3.6	N/A	N/A	N/A
[16]	180	1.8	Sinusoid	513μ[d,e]	10 – 1M	0.3 | 2.1[e]	N/A	N/A	N/A
[51]	180	1.8	Sinusoid	756μ[d]	100 – 10M	1.1 | 1.9	N/A	N/A	N/A
[52]	250	2.5	Sinusoid	10.3m[d,e]	1 – 2.048k	1 | 1.3[e]	N/A	N/A	N/A
[54]	180	±1.65	Sinusoid	684μ[d]	10k – 500k	1.19 | 0.51	N/A	N/A	N/A
Impedance-readout ICs with wide dynamic range and low noise									
[18]	55	1.2	Square	18.9μ – 34.9μ	1k – 1.024M	N/A	141	95.7[b]	N/A
[19]	40	0.9/0.6	Square	8.8μ – 16μ	1k – 1.024M	N/A	136.6	101.9[b]	N/A
[20]	180	1.8	Square	60μ – 68.4μ	1k –215k	N/A	145.2	103.5[b]	N/A
[42]	180	1.2	Square	15.84μ[d]	1k – 1.024M	N/A	N/A	106[b,d]	N/A
Impedance-readout ICs with high throughput									
[6]	180	1.8	Pseudo-sinusoid	1.73m[f]	10k – 200k	N/A	N/A	56.3[c]	20
[23]	180	1.8	Square	85.8μ	1k – 18k	N/A	N/A	N/A	500
[47]	180	1.2/1.8	Pseudo-sinusoid	85μ	50k – 1M	N/A	N/A	N/A	100
[69]	350	±9/3.3	Pseudo-sinusoid	250m[f]	45k – 1M	1.1 | 1.8	N/A	54.3[c]	122
[71]	180	1.8/3.3	Pseudo-sinusoid	26.76m[f]	4k – 8M	N/A	N/A	N/A	N/A

[a] $20\times\log(R_{MAX}/2\sqrt{2}\times R_{MIN\_RMS})$, $R_{MIN\_RMS}=MIN(R_{N.DENSITY}\times\sqrt{BW})$ or $MIN(R_{pp}/6.6)$
[b] $MAX(20\times\log(R/2\sqrt{2}\times R_{RMS}))$, $R_{RMS}=R_{N.DENSITY}\times\sqrt{BW}$ or $R_{pp}/6.6$
[c] $20\times\log(|E[m_i]|/\sqrt{Var[m_i]}|)$, m_i represents the measurement of i-th electrode pair, $E[m_i]$, the averge of m_i, $Var[m_i]$, the variance of m_i
[d] excluding ADC
[e] simulation results
[f] including CG

Recently, impedance-readout ICs for wearable EIS systems have shown a noticeable trend. First, there is a growing preference for adopting a two-electrode configuration, accompanied by a demand for a high dynamic range in impedance-readout ICs. To meet this requirement, techniques like baseline cancellation are employed. These methods allow to achieve dynamic ranges exceeding 100 dB and avoid the saturation effect even when impedance measurements are required in the range of tens of kΩ [18], [19], [20]. Second, special attention to noise needs to be paid for these systems, particularly the noise originating from the signal generator. By correlating the noise from the readout IC with the signal generator, overall noise can be further reduced. Last, significant efforts are dedicated to reduce the noise that varies with the signal amplitude [18], [19], [20]. Techniques such as baseline cancellation [18], [19], [20] and quiet chopping [42] are employed for this purpose to achieve a high SNR, ensuring more accurate and reliable measurements.

In EIT applications, one common approach to enhance image resolution and accuracy involves increasing the number of electrodes [81]. However, this results in leading to an increased number of measurements as well as a more complicated measurement setup for image reconstruction [81]. As a result, it is necessary to find a delicate balance among competing factors, such as frame rate determined by throughput, power consumption, and circuit complexity. Various approaches have been introduced to enhance the measurement time and throughput of EIS systems, particularly in applications of EIT and real-time impedance monitoring. However, despite the efforts to enhance performance, each of these approaches suffers from trade-offs. For instance, the analog filter control technique with DC sampling maintains a moderate frame rate of 20 fps and improves the settling time [6], but it requires careful circuit design to avoid potential signal distortions. On the other hand, the direct sampling technique achieves a higher frame rate of 122 fps but consumes several hundred mW of power [69]. A promising compromise could be the IF sampling method, which maintains a good balance between power and throughput by reducing the required bandwidth of circuits and maintaining a

fast sampling rate [47], [71]. Recent research shown in [47] demonstrates a high frame rate of 100 fps while consuming only 85 μW of power by using IF sampling.

Furthermore, this article also discusses specialized techniques for electrode interfaces in practical measurements, i.e., the use of high dynamic range structures for two-electrode configurations, high input impedance structures for dry electrodes, and the integration of body-biasing circuits. This emphasizes the critical need for careful consideration in experimental setups to ensure precise and consistent results in impedance measurements.

IX. Conclusion

This review article provides a comprehensive methodological review of impedance readout ICs with the focus on four main design objectives: low power consumption, high accuracy, wide dynamic range and low noise, and high throughput. Depending on the given specific application, there has been a tendency to concentrate heavily on enhancing particular parameters only while disregarding others. For instance, baseline cancellation techniques optimized for square-wave signals have been employed to achieve wide dynamic range and low noise at the expense of accuracy. Conversely, techniques for enhancing the accuracy have often overlooked considerations for achieving wide dynamic range and low noise.

As technologies have been advanced considerably for improving individual parameters, it is clear that more holistic approaches with more balanced performances are needed. For example, BioZ measurement ICs which achieve wide dynamic range and low power also have potentials to incorporate baseline cancellation and pre-demodulation techniques. For more enhanced accuracy, more in-depth researches are required in exploring optimum mixing methods or pseudo-sinusoid excitation. Moreover, the combination of baseline cancellation with direct sampling or IF sampling would be also promising to improve the throughput while maintaining wide dynamic range. Even with these synergic combinations, there are still intrinsic trade-offs between the performance metrics. It would be ideal for an impedance measurement IC to be able to reconfigure each of these performance parameters according to given specifications.

Besides, BioZ measurement ICs have evolved to combine their inherent structural advantages, such as high accuracy and low power consumption, with user-friendly interfaces like dry or two-electrode setups, ensuring reliable operations in diverse usage scenarios. Furthermore, the integration of bioZ measurement into multi-modal sensor interfaces, alongside ExG and PPG signal monitoring, provides not only the monitoring of electrode impedance but also other unique functions, thereby enhancing the overall system robustness and versatility [72]. More advancements in bioZ measurement technology towards better accuracy, power, dynamic range, noise, and throughput will pave the way for more diverse applications of the technology, including electrochemical sensing and portable health monitoring devices.

References

[1] B. Liu et al., "A 13-channel 1.53-mW 11.28-mm^2 electrical impedance tomography SoC based on frequency division multiplexing for lung physiological imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 938–949, Oct. 2019.

[2] Y. Wu, F. F. Hanzaee, D. Jiang, R. H. Bayford, and A. Demosthenous, "Electrical impedance tomography for biomedical applications: Circuits and systems review," *IEEE Open J. Circuits Syst.*, vol. 2, pp. 380–397, 2021.

[3] R. J. Halter, A. Hartov, J. A. Heaney, K. D. Paulsen, and A. R. Schned, "Electrical impedance spectroscopy of the human prostate," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 7, pp. 1321–1327, Jul. 2007.

[4] M. H. Jung et al., "Wrist-wearable bioelectrical impedance analyzer with miniature electrodes for daily obesity management," *Sci. Rep.*, vol. 11, Jan. 2021, Art. no. 1238.

[5] E. Ravagli, M. Crescentini, P. Rovatti, and S. Severi, "Noninvasive estimation of plasma sodium concentration during hemodialysis via capacitively coupled electrical impedance spectroscopy," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 4, pp. 1673–1681, Apr. 2020.

[6] S. Hong, J. Lee, J. Bae, and H.-J. Yoo, "A 10.4 mW electrical impedance tomography SoC for portable real-time lung ventilation monitoring system," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2501–2512, Nov. 2015.

[7] Y. Wu, D. Jiang, A. Bardill, S. D. Gelidi, R. Bayford, and A. Demosthenous, "A high frame rate wearable EIT system using active electrode ASICs for lung respiration and heart rate monitoring," *IEEE Trans. Circuits Syst. I., Regular Papers*, vol. 65, no. 11, pp. 3810–3820, Nov. 2018.

[8] D. Chowdhury and M. Chattopadhyay, "Study and classification of cell bio-impedance signature for identification of malignancy using artificial neural network," *IEEE Trans. Instrum. Meas.*, vol. 70, 2021, Art. no. 2505908.

[9] L. F. E. Huerta-Nuñez et al., "A biosensor capable of identifying low quantities of breast cancer cells by electrical impedance spectroscopy," *Sci. Rep.*, vol. 9, Apr. 2019, Art. no. 6419.

[10] S. Hong et al., "A 4.9 mΩ-sensitivity mobile electrical impedance tomography IC for early breast-cancer detection system," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 245–257, Jan. 2015.

[11] P. Åberg, I. Nicander, J. Hansson, P. Geladi, U. Holmgren, and S. Ollmar, "Skin cancer identification using multifrequency electrical impedance–A potential screening tool," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 12, pp. 2097–2102, Dec. 2004.

[12] J. Lee, S. Gweon, K. Lee, S. Um, K.-R. Lee, and H.-J. Yoo, "A 9.6-mW/ch 10-MHz wide-bandwidth electrical impedance tomography IC with accurate phase compensation for early breast cancer detection," *IEEE J. Solid-State Circuits*, vol. 56, no. 3, pp. 887–898, Mar. 2021.

[13] C. H. Y. Ling et al., "Accuracy of direct segmental multi-frequency bioimpedance analysis in the assessment of total body and segmental body composition in middle-aged adult population," *Clin. Nutr.*, vol. 30, no. 5, pp. 610–615, Oct. 2011.

[14] J. Ferreira, I. Pau, K. Lindecrantz, and F. Seoane, "A handheld and textile-enabled bioimpedance system for ubiquitous body composition aalysis. An initial functional validation," *IEEE J. Biomed. Health Inform.*, vol. 21, no. 5, pp. 1224–1232, Sep. 2017.

[15] P. Kassanos, I. F. Triantis, and A. Demosthenous, "A CMOS magnitude/phase measurement chip for impedance spectroscopy," *IEEE Sensors J.*, vol. 13, no. 6, pp. 2229–2236, Jun. 2013.

[16] S.-I. Cheon, S.-J. Kweon, Y. Kim, J. Koo, S. Ha, and M. Je, "An impedance readout IC with ratio-based measurement techniques for electrical impedance spectroscopy," *Sensors*, vol. 22, no. 4, Feb. 2022, Art. no. 1563.

[17] J. Xu and Z. Hong, "Low power bio-impedance sensor interfaces: Review and electronics design methodology," *IEEE Rev. Biomed. Eng.*, vol. 15, pp. 23–35, 2020.

[18] H. Ha et al., "A bio-impedance readout IC with digital-assisted baseline cancellation for two-electrode measurement," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 2969–2979, Nov. 2019.

[19] T.-T. Zhang, H. Son, J. Zhao, C.-H. Heng, and Y. Gao, "A 26.6–119.3-μW 101.9-dB SNR direct digitization bio-impedance readout IC," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2619–2631, Sep. 2023.

[20] C. S. Park, H. Kim, K. Lee, D. S. Keum, D. P. Jang, and J. J. Kim, "A baseline-tracking single-channel I/Q impedance plethysmogram IC for neckband-based blood pressure and cardiovascular monitoring," *IEEE J. Solid-State Circuits*, vol. 58, no. 7, pp. 2040–2052, Jul. 2023.

[21] J. Hope, Z. Aqrawe, M. Lim, F. Vanholsbeeck, and A. McDaid, "Increasing signal amplitude in electrical impedance tomography of neural activity using a parallel resistor inductor capacitor (RLC) circuit," *J. Neural Eng.*, vol. 16, no. 6, Nov. 2019, Art. no. 066041.

[22] K. Aristovich et al., "Imaging fast neural traffic at fascicular level with electrical impedance tomography: Proof of principle in rat sciatic nerve," *J. Neural Eng.*, vol. 15, no. 5, Aug. 2018, Art. no. 056025.

[23] J.-H. Suh et al., "A 16-channel impedance-readout IC with synchronous sampling and baseline cancelation for fast neural electrical impedance tomography," *IEEE Solid-State Circuits Lett.*, vol. 6, pp. 109–112, 2023.

[24] M. ElAnsary et al., "50 nW opamp-less $\Delta\Sigma$-modulated bioimpedance spectrum analyzer for electrochemical brain interfacing," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1971–1983, Jul. 2020.

[25] N. Neshatvar, P. Langlois, R. Bayford, and A. Demosthenous, "Analog integrated current drivers for bioimpedance applications: A review," *Sensors*, vol. 19, no. 4, Feb. 2019, Art. no. 756.

[26] S.-J. Kweon, A. K. Rafi, S.-I. Cheon, M. Je, and S. Ha, "On-chip sinusoidal signal generators for electrical impedance spectroscopy: Methodological review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 3, pp. 337–360, Jun. 2022.

[27] P. Kassanos, "Bioimpedance sensors: A tutorial," *IEEE Sensors J.*, vol. 21, no. 20, pp. 22190–22219, Oct. 2021.

[28] L. A. Buscaglia, O. N. Oliveira, and J. P. Carmo, "Roadmap for electrical impedance spectroscopy for sensing: A tutorial," *IEEE Sensors J.*, vol. 21, no. 20, pp. 22246–22257, Oct. 2021.

[29] M. Takhti and K. Odame, "Structured design methodology to achieve a high SNR electrical impedance tomography," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 364–375, Apr. 2019.

[30] S. Subhan and S. Ha, "A harmonic error cancellation method for accurate clock-based electrochemical impedance spectroscopy," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 4, pp. 710–724, Aug. 2019.

[31] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2628–2632, Dec. 2005.

[32] S.-I. Cheon, S.-J. Kweon, A. Aberra, M. Je, and S. Ha, "Optimal parameter design of DAC-based sinusoidal signal generators for electrical impedance spectroscopy," *IEEE Trans. Instrum. Meas.*, vol. 72, 2023, Art. no. 2000711.

[33] M. Min and T. Parve, "Improvement of lock-in electrical bio-impedance analyzer for implantable medical devices," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 968–974, Jun. 2007.

[34] S. F. Khalil, M. S. Mohktar, and F. Ibrahim, "The theory and fundamentals of bioimpedance analysis in clinical status monitoring and diagnosis of diseases," *Sensors*, vol. 14, no. 6, pp. 10895–10928, Jun. 2014.

[35] T. Dai and A. Adler, "In vivo blood characterization from bioimpedance spectroscopy of blood pooling," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 11, pp. 3831–3838, Nov. 2009.

[36] W. Kim, W. Hong, T. Kim, D. Kim, and M. Lee, "RF sensor-based liveness detection scheme with loop stability compensation circuit for a capacitive fingerprint system," *IEEE Access*, vol. 7, pp. 152545–152551, 2019.

[37] H. Mazhab-Jafari, L. Soleymani, and R. Genov, "16-channel CMOS impedance spectroscopy DNA analyzer with dual-slope multiplying ADCs," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 5, pp. 468–478, Oct. 2012.

[38] L. Yan et al., "A 13 μA analog signal processing IC for accurate recognition of multiple intra-cardiac signals," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 785–795, Dec. 2013.

[39] S. Rodriguez, S. Ollmar, M. Waqar, and A. Rusu, "A batteryless sensor ASIC for implantable bio-impedance applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 3, pp. 533–544, Jun. 2016.

[40] H. Ha, C. V. Hoof, and N. V. Helleputte, "Measurement and analysis of input-signal dependent flicker noise modulation in chopper stabilized instrumentation amplifier," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 90–93, Apr. 2018.

[41] P. Kassanos, L. Constantinou, I. F. Triantis, and A. Demosthenous, "An integrated analogreadout for multi-frequency bioimpedance measurements," *IEEE Sensors J.*, vol. 14, no. 8, pp. 2792–2800, Aug. 2014.

[42] Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, and J. Xu, "A 0.5-m$\Omega/\sqrt{Hz}$ dry-electrode bioimpedance interface with current mismatch cancellation and input impedance of 100 MΩ at 50 kHz," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1735–1745, Jun. 2023.

[43] H. Ko, T. Lee, J.-H. Kim, J.-A. Park, and J. P. Kim, "Ultralow-power bioimpedance IC with intermediate frequency shifting chopper," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 3, pp. 259–263, Mar. 2016.

[44] H. Ha et al., "A bio-impedance readout IC with frequency sweeping from 1 k-to-1 MHz for electrical impedance tomography," in *Proc. IEEE Symp. VLSI Circuits*, 2017, pp. C174–C175.

[45] J. Xu et al., "A 36 μW 1.1 mm^2 reconfigurable analogfront-end for cardiovascular and respiratory signals recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 4, pp. 774–783, Aug. 2018.

[46] L. Zeng and C.-H. Heng, "An 8-channel 1.76-mW 4.84-mm^2 electrical impedance tomography SoC with direct IF frequency division multiplexing," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 11, pp. 3401–3405, Nov. 2021.

[47] T. Zhou et al., "A 0.63-mm^2/ch 1.3-m$\Omega/\sqrt{Hz}$-sensitivity 1-MHz bandwidth active electrode electrical impedance tomography system," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2022, pp. 1–3.

[48] M. Bakhshiani, M. A. Suster, and P. Mohseni, "A broadband sensor interface IC for miniaturized dielectric spectroscopy from MHz to GHz," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1669–1681, Aug. 2014.

[49] M. Bakhshiani, M. A. Suster, and P. Mohseni, "A 9 MHz–2.4 GHz fully integrated transceiver IC for a microfluidic-CMOS platform dedicated to miniaturized dielectric spectroscopy," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 849–861, Dec. 2015.

[50] I. F. Triantis, A. Demosthenous, M. Rahal, H. Hong, and R. Bayford, "A multi-frequency bioimpedance measurement ASIC for electrical impedance tomography," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, 2011, pp. 331–334.

[51] S.-I. Cheon, S.-J. Kweon, Y. Kim, J. Koo, S. Ha, and M. Je, "A polar-demodulation-based impedance-measurement IC using frequency-shift technique with low power consumption and wide frequency range," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1210–1220, Dec. 2021.

[52] S.-J. Kweon, S. Shin, J.-H. Park, J.-H. Suh, and H.-J. Yoo, "A CMOS low-power polar demodulator for electrical bioimpedance spectroscopy using adaptive self-sampling schemes," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2016, pp. 284–287.

[53] J. Ramos, J. L. Ausín, and G. Torelli, "A 1-MHz analogfront-end for a wireless bioelectrical impedance sensor," in *Proc. Conf. Ph.D. Res. Microelectron. Electron.*, 2010, pp. 1–4.

[54] Y. Wu, D. Jiang, M. Habibollahi, N. Almarri, and A. Demosthenous, "Time stamp–A novel time-to-digital demodulation method for bioimpedance implant applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 5, pp. 997–1007, Oct. 2020.

[55] H. Rezaee-Dehsorkh, N. Ravanshad, A. Shamsaki, M. R. Fakour, and P. Aliparast, "A low-power single-path bio-impedance measurement system using an analog-to-digital converter for I/Q demodulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 6, pp. 1129–1137, Dec. 2022.

[56] R. Kubendran, S. Lee, S. Mitra, and R. F. Yazicioglu, "Error correction algorithm for high accuracy bio-impedance measurement in wearable healthcare applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 196–205, Apr. 2014.

[57] W. Lee and S. Cho, "Integrated all electrical pulse wave velocity and respiration sensors using bio-impedance," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 776–785, Mar. 2015.

[58] V.-P. Seppa, J. Viik, and J. Hyttinen, "Assessment of pulmonary flow using impedance pneumography," *IEEE Trans. Biomed. Eng*, vol. 57, no. 9, pp. 2277–2285, Sep. 2010.

[59] Ø. G. Martinsen, B. Nordbotten, S. Grimnes, H. Fossan, and J. Eilevstjønn, "Bioimpedance-based respiration monitoring with a defibrillator," *IEEE Trans. Biomed. Eng.*, vol. 61, no. 6, pp. 1858–1862, Jun. 2014.

[60] K. Kim, J.-H. Kim, S. Gweon, M. Kim, and H.-J. Yoo, "A 0.5-V sub-10-μW 15.28-m$\Omega/\sqrt{Hz}$ bio-impedance sensor IC with sub-1 phase error," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2161–2173, Aug. 2020.

[61] S. Thanapitak, W. Surakampontorn, and C. Sawigun, "A micropower chopper CBIA with DSL-embedded input stage with 0.4 V EO tolerance for dry-electrode biopotential recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 3, pp. 458–469, Jun. 2023.

[62] Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, and J. Xu, "A 0.5 m$\Omega/\sqrt{Hz}$ 106 dB SNR 0.45 cm^2 dry-electrode bioimpedance interface with current mismatch cancellation and boosted input impedance of 100 MΩ at 50 kHz," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 332–334.

[63] F. Butti, M. Piotto, and P. Bruschi, "A chopper instrumentation amplifier with input resistance boosting by means of synchronous dynamic element matching," *IEEE Trans. Circuits Syst. I., Regular Papers*, vol. 64, no. 4, pp. 753–764, Apr. 2017.

[64] B. Sanchez, G. Vandersteen, R. Bragos, and J. Schoukens, "Basics of broadband impedance spectroscopy measurements using periodic excitations," *Meas. Sci. Technol.*, vol. 23, no. 10, Aug. 2012, Art. no. 105501.

[65] M. Kim et al., "A 1.4-mΩ-sensitivity 94-dB dynamic-range electrical impedance tomography SoC and 48-channel Hub-SoC for 3-D lung ventilation monitoring system," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2829–2842, Nov. 2017.
[66] J. Lee, U. Ha, and H.-J. Yoo, "30-fps SNR equalized electrical impedance tomography IC with fast-settle filter and adaptive current control for lung monitoring," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2016, pp. 109–112.
[67] J. Xu et al., "A wearable 8-channel active-electrode EEG/ETI acquisition system for body area networks," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2005–2016, Sep. 2014.
[68] G. Qu et al., "A 0.28 mΩ-sensitivity 105 dB-dynamic-range electrochemical impedance spectroscopy SoC for electrochemical gas detection," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2018, pp. 286–288.
[69] Y. Wu, D. Jiang, A. Bardill, R. Bayford, and A. Demosthenous, "A 122 fps, 1 MHz bandwidthmulti-frequency wearable EIT belt featuring novel active electrode architecture for neonatal thorax vital sign monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 927–937, Oct. 2019.
[70] M. Rahal, J. Dai, Y. Wu, A. Bardill, R. Bayford, and A. Demosthenous, "High frame rate electrical impedance tomography system for monitoring of regional lung ventilation," in *Proc. IEEE Annu. Int. Conf. Eng. Med. Biol. Soc.*, 2022, pp. 2487–2490.
[71] S.-J. Kweon et al., "An 8 MHz 31.25 kS/s impedance-monitoring IC based on IF-sampling architecture with a band-pass delta-sigma ADC," in *Proc. IEEE Symp. VLSI Circuits*, 2021, pp. 1–2.
[72] H. Kim et al., "32.1 A behind-the-ear patch-type mental healthcare integrated interface with 275-fold input impedance boosting and adaptive multimodal compensation capabilities," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2023, pp. 478–480.
[73] J. Yoo and H.-J. Yoo, "Fabric circuit board-based dry electrode and its characteristics for long-term physiological signal recording," in *Proc. IEEE Annu. Int. Conf. Eng. Med. Biol. Soc.*, 2011, pp. 2497–2500.
[74] A. B. Nigusse, D. A. Mengistie, B. Malengier, G. B. Tseghai, and L. V. Langenhove, "Wearable smart textiles for long-term electrocardiography monitoring–A review," *Sensors*, vol. 21, no. 12, Jun. 2021, Art. no. 4174.
[75] Y.-S. Shu et al., "A 4.5 mm^2 multimodal biosensing SoC for PPG, ECG, BIOZ and GSR acquisition in consumer wearable devices," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2020, pp. 400–402.
[76] N. Koo, H. Kim, and S. Cho, "A 43.3-μW biopotential amplifier with tolerance to common-mode interference of 18 V_{pp} and T-CMRR of 105 dB in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 508–519, Feb. 2023.
[77] N. Koo and S. Cho, "A 24.8-μW biopotential amplifier tolerant to 15-V_{pp} common-mode interference for two-electrode ECG recording in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 591–600, Feb. 2021.
[78] T. Tang et al., "An active concentric electrode for concurrent EEG recording and body-coupled communication (BCC) data transmission," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1253–1262, Dec. 2020.
[79] G. Company-Se et al., "Effect of calibration for tissue differentiation between healthy and neoplasm lung using minimally invasive electrical impedance spectroscopy," *IEEE Access*, vol. 10, pp. 103150–103163, 2022.
[80] G. Company Se et al., "Differentiation using minimally-invasive bioimpedance measurements of healthy and pathological lung tissue through bronchoscopy," *Front. Med.*, vol. 10, Apr. 2023, Art. no. 1108237.
[81] M. Tang, W. Wang, J. Wheeler, M. McCormick, and X. Dong, "The number of electrodes and basis functions in EIT image reconstruction," *Physiol. Meas.*, vol. 23, no. 1, Jan. 2002, Art. no. 129.

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