A CMOS Multi-Electrode Array for Four-Electrode Bioimpedance Measurements

Steffen Nøvik^D, *Member, IEEE*, Magnus Flø Drageseth, Magnus Børresen Grøndalen, Ola Nilsen^D, Stefan Johannes Karl Krauss, Ørjan Grøttem Martinsen, *Senior Member, IEEE*, and Philipp Dominik Häfliger, *Senior Member, IEEE*

Abstract—This work demonstrates how a multi-electrode array (MEA) dedicated to four-electrode bioimpedance measurements can be implemented on a complementary metal-oxidesemiconductor (CMOS) chip. As a proof of concept, an 8×8 pixel array along with dedicated amplifiers was designed and fabricated in the TSMC 180 nm process. Each pixel in the array contains a circular current carrying (CC) electrode that can act as a current source or sink. In order to measure a differential voltage between the pixels, each CC electrode is surrounded by a ring shaped pick up (PU) electrode. The differential voltages can be measured by an on-board instrumentation amplifier, while the currents can be measured with an on-bard transimpedance amplifier. Openings in the passivation layer exposed the aluminum top metal layer, and a metal stack of zinc, nickel and gold was deposited in an electroless plating process. The chips were then wire bonded to a ceramic package and prepared for wet experiments by encapsulating the bonding wires and pads in the photoresist SU-8. Measurements in liquids with different conductivities were performed to demonstrate the functionality of the chip.

Index Terms—Bioimpedance, four-electrode measurements.

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Steffen Nøvik and Philipp Dominik Häfliger are with the Department of Informatics, University of Oslo, 0316 Oslo, Norway (e-mail: steffeno@ifi.uio.no; hafliger@ifi.uio.no).

Magnus Flø Drageseth was with the Department of Physics, University of Oslo, 0316 Oslo, Norway. He is now with the Novelda, 0484 Oslo, Norway (e-mail: magnus.drageseth@fys.uio.no).

Magnus Børresen Grøndalen is with the Department of Physics, University of Oslo, 0316 Oslo, Norway, and also with the Novelda, 0484 Oslo, Norway (e-mail: m.b.grondalen@fys.uio.no).

Ola Nilsen is with the Department of Chemistry, University of Oslo, 0315 Oslo, Norway (e-mail: ola.nilsen@kjemi.uio.no).

Stefan Johannes Karl Krauss is with the Hybrid Technology Hub– Centre of Excellence, Faculty of Medicine, Institute of Basic Medical Sciences, University of Oslo, 0317 Oslo, Norway, and also with the Department of Immunology and Transfusion Medicine, Oslo University Hospital, 0424 Oslo, Norway (e-mail: s.j.k.krauss@medisin.uio.no).

Ørjan Grøttem Martinsen is with the Department of Physics, University of Oslo, 0316 Oslo, Norway, and also with the Department of Clinical and Biomedical Engineering, Oslo University Hospital, 0424 Oslo, Norway (e-mail: o.g.martinsen@fys.uio.no).

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I. INTRODUCTION

ULTI electrode arrays (MEAs) are increasingly used for studying electrically active cells such as neurons and cardiomyocytes. The devices consist of potentially thousands of electrodes that allow for parallel detection of local field potentials endogenously generated by the cells. These potentials can be detected without the need for fluorescent dyes or microscopes tailored for calcium imaging, and the electrodes can also be used for active stimuli and control of neural activities. An additional possibility is to monitor the bioimpedance of cell cultures with the electrodes, but the technique can be considered a niche compared with the traditional modalities on the MEAs. In contrast, bioimpedance is increasingly used in other applications (e.g. lab-on-a-chip (LOC)) for real-time characterization of cells and tissues, and the technique has recently been reviewed by several authors [1], [2], [3], [4], [5]. As opposed to methods usually employed at the end of cell culture assays, such as flow cytometry and live/dead staining, bioimoedance can characterize the cells non-destructively and label-free during the entire experiment. For instance, the technique has been widely used to monitor parameters such as cell motility, death, adhesion, spreading and growth. Another strength is the ability to measure with a high temporal resolution, for instance when monitoring structural changes of beating cardiomyocytes [6]. The technique can also monitor 3D cultures with a high temporal resolution, for instance when studying drug response [7], without the need for fixing the cells. Some spatial resolution can also be achieved by electrical impedance tomography.

A few groups have studied bioimpedance measurements on MEAs as standalone applications [8], [9], but the technique is not widespread compared to traditional MEAs. However, as the complexity of MEAs has increased, several groups have now started to include impedance measurements as an additional module. For instance, in the MEA with the largest active electrode array known to the authors (59.760 electrodes), Dragas et al. [10] implemented six measurement and stimulation modalities including electrical impedance spectroscopy (EIS). However, when characterizing the EIS module [11], they found that the impedance magnitude values of the bright platinum (Pt) electrodes ($3 \times 7.5 \ \mu m^2$) were $2.3 \pm 0.04 \ M\Omega$ at 10 kHz. After depositing Pt-black in order to increase the electrode surface area without increasing the geometrical area, the impedance values

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decreased to $107 \pm 5.2 \,\mathrm{k\Omega}$ when measured in phosphate buffered saline. However, since Pt-black is not mechanically stable, Ptblack had to be re-deposited and the electrode impedance had to be measured before each bio-experiment. In a similar work by Lopez et al. [12], when monitoring the electrode cell interface by EIS, the electrode impedance was found to dominate the frequency spectrum at lower frequencies. Common to all the mentioned MEAs is that they measure the bioimpedance of the biological samples using a so-called two-electrode system. In such a system the impedance from the electrode - solution interface will be included in the measurements. A modern way of omitting the impedance from an electrode - solution interface is to use a so called four-electrode system. This also improves both the sensitivity and the accuracy of the measurements [5]. The first implementation of a four-electrode system on a multi modal chip was recently successfully demonstrated by Jung et al. [16]. In this impressive work with a chip encompassing 21952 pixels, the authors demonstrated holistic cellular characterization where four-electrode impedance measurements proved to be an important module.

In this work, as well as in our conference paper [15], we focus on how a system dedicated to four-electrode transimpedance measurement system can be implemented. In addition to the current carrying (CC) electrode in each pixel, we also incorporate high impedance pick up (PU) electrodes surrounding the CC electrodes. Since there are many properties of an optimally designed four-electrode system that could vary from a multimodal system, such as the important relative placement of the CC and PU electrode pairs, we believe it is essential to investigate how a system dedicated to four-electrode measurements can be designed. This is important both for future dedicated four-electrode systems, as well as for multi-modal chips such as the one demonstrated by Jung et al. [16].

Section II first covers the basics of bioimpedance measurements as well as the impedance contribution from the electrodesolution interface. The four-electrode method, which will be used in this work for minimizing the contribution from the electrode-solution interface, is then described in Section III. The circuit implementation in the TSMC 180 nm CMOS process is presented in Section IV. Initial tests of the the on-board circuits were shown in our conference paper [15], but are excluded here. The current paper extends our conference paper by including fabrication of gold electrodes (Section V), packaging the chips for wet experiments (Section VI), our strategy for dealing with passive PU electrodes (Section VII), data acquisition and filters (Section VIII) and measurements in liquids (IX). Section X concludes the paper.

II. THEORETICAL BACKGROUND

When aiming to measure the impedance of biological samples in electrical impedance spectroscopy experiments, a small alternating current is commonly applied to a working electrode in contact with the sample and measured at an opposite reference electrode. The electrical impedance, $Z(\omega)$, is given by

$$Z(\omega) = \frac{U(\omega)}{I(\omega)} = R + jX(\omega)$$
(1)



Fig. 1. Equivalent circuit model of a two electrode system. The EP of an electrode is modelled by a RC network with a serial resistor R_s . C_{mem} = membrane capacitance, R_{mem} = membrane resistance, R_{cyt} = cytosol resistance, R_{sln} = solution resistance. This model is based on [13] and [14]. The figure was first published in [15].

where the real part of impedance is the resistance R and the imaginary part is the reactance $X(\omega)$. The absolute value is

$$Z| = \sqrt{(R)^2 + (X(\omega))^2}$$
(2)

and phase shift

$$\theta = \arctan\left(\frac{X(\omega)}{R}\right) \tag{3}$$

There is often an unwanted impedance contribution stemming from an electrical double layer formed at the interface between the electrodes and solution in this type of "two electrode measurements". This double layer results in a drop in the electrical potentials across the boundaries, and when current is flowing through the cell this is known as electrode polarization (EP) [17], [18]. The resulting capacitance can dominate the signal at lower frequencies [19], hindering the acquisition of the actual impedance of the biological sample. A simplified model [14] to account for EP in an electrolyte solution is shown in Fig. 1, where the electrode - solution interface is modeled by a parallel RC network with a serial resistor R_s [13]. In bioimpedance experiments we wish to avoid the contributions from EP, and only measure the passive electrical properties of the biological material.

III. FOUR-ELECTRODE METHOD FOR BIOIMPEDANCE

In order to avoid the contribution from EP, two extra electrodes can be added in order to form a so called four-electrode system. These two PU electrodes are responsible for detecting the voltage when a current is applied between the two CC electrodes [5]. The four-electrode system used in this work is illustrated in Fig. 2 along with the prototyped 8×8 MEA and the on-board analog switch matrix and amplifiers. The center electrodes (A and D)



Fig. 2. The 8×8 electrode array designed for four-electrode impedance measurements. Each electrode consists of an inner current carrying electrode (CC) and an outer voltage pick up (PU) electrode. The current between the CC electrodes is routed to an on-board transimpedance amplifier, while the voltage between the PU electrodes is recorded by an on-board instrumentation amplifier. The figure was first published in [15].

are used as CC electrodes, while the ring electrodes (B and C) are implemented as PU electrodes. The influence from polarization impedance on the PU electrodes can be eliminated if the input impedance of the amplifier is sufficiently high. Additionally, the differential voltage measured by the PU electrodes does not include the CC electrode polarization impedance [20]. With the circular and ring shapes of the electrodes, any two pixels on the chip can be utilized while still retaining the symmetry of pixel pairs. For instance, as seen in Fig. 3, both neighbouring pixels (red current streamlines) and diagonal pixels (blue streamlines) can operate as a pixel pair since the PU electrodes sit between the CC electrodes. It is also worth noticing that the distance between the CC electrodes relative to the distance between the PU electrodes is important. A decrease in the distance between the PU electrodes (i.e. with a fixed distance between the CC electrodes) would lead to a decrease in the magnitude of the measured impedance [5]. Moreover, there will also be volumes of negative sensitivity between the CC and PU electrode, which means that an increase in the impedance in these volumes leads to a lower total measured impedance [20]. Designers wishing to



Fig. 3. Electrode pitch and dimensions. The circular PU electrodes ensures that all pairs of electrodes can be utilized, for instance diagonally (blue stream lines).

implement four-terminal systems in multipurpose configurable MEAs (i.e. usually with a fixed distance between the electrodes), should therefore keep this in mind. As seen in Fig. 3, in our design the distances between the CC electrodes and between the PU electrodes are 100 μ m and 75 μ m respectively, with 5 μ m between the CC and PU electrodes. Care should also be taken to ensure that electrical currents do not enter and leave the passive PU electrodes, thereby creating polarization potentials on the electrodes [19]. The net potential of the PU electrodes would then usually be brought closer to the level of the CC electrodes, thus leading to an overestimation of the transfer impedance [20]. This problem can be elegantly avoided by the use of recessed electrodes [19], where the electrodes are moved out of the current field for instance by placing them in the bottom of a trench, as illustrated in Fig. 4.

To the best of our knowledge, no work has previously attempted to model recessed microelectrodes for four-electrode bioimpedance measurements. We therefore performed COM-SOL simulations on a simplified 2D version of our geometry to investigate the amount of current passing through a recessed PU electrode. Two CC and two PE electrodes were positioned at equal distances as in our chip (i.e. pitch of $100 \,\mu\text{m}$), while the recess depth was varied from $0 \,\mu\text{m}$ to $10 \,\mu\text{m}$. A magnified view of a CC and a PU electrode is shown in Fig. 5. The current passing through the PU electrodes (i.e. from the solution into the electrode, and back into the solution again) was found by integrating the current density at the vertical line at the center of the electrode. The current entering the PU electrode depends on the surface impedance, as well as the impedance of the medium and its content (e.g. cells). To generalize, we have not



Fig. 4. (a) Current from the current carrying (CC) electrode entering and leaving the pick up (PU) electrode, thereby creating a net polarization potential. (b) The electrode is moved out of the current field. A fluid coupling establishes contact with the potential to be measured. The figure was first published in [15].



Fig. 5. The current through recessed electrodes at varying depths was simulated in COMSOL. Only one CC- PU-electrode pair is shown. The distance to the corresponding pixel is $100 \,\mu$ m.

included cells, but instead modelled the effect of decreasing the conductivity of the solution. The surface impedance's at 10 kHz $(2 \cdot 10^{-5}\Omega \cdot m^2)$ and 100 kHz $(4 \cdot 10^{-6}\Omega \cdot m^2)$ for circular electrodes with radius $2.5 \,\mu$ m were extracted from Wang et al. [21]. It should be noted that the polarization impedance will in general vary with the conductivity of the solution [22]. The results of the simulations are seen in Fig. 6, where the current through the PU electrode is presented as the percentage of the total current sourced by the CC electrode. The current decreases rapidly for increasing depths of the recess. While the recess depth in our design is $\sim 2 \,\mu$ m, the effect is apparent already from a recess of 1 μ m for a 5 μ m wide structure.

For experiments where the cells are meant to cover the electrode surfaces, there could be an increased risk of a current leakage compared with flat electrodes. This should be kept in mind in the design of the experiment.



Fig. 6. Simulated current through the PU electrode as a function of recess depth. The plot shows different combinations of surface resistance and solution conductivity.

IV. ARCHITECTURE AND CIRCUIT DESIGN

The system consists of the following parts:

- The 8×8 electrode array.
- An addressable signal path from the electrodes to an instrumentation amplifier and a current to voltage converter.
- An off-chip back-end to generate the required inputs, as well as storing the resulting outputs.

The complementary metal–oxide–semiconductor (CMOS) chip was implemented in the TSMC 180 nm CMOS process using a six metal stack. The electrodes were implemented by exposing the top aluminum metal layer through openings in the passivation layer, followed by electroless plating of zinc (Zn), nickel (Ni) and gold (Au).

A block diagram of the chip is seen in Fig. 7. The electrodes are arranged in an addressable $2D \ 8 \times 8$ pixel array, where each pixel contains one inner circular CC electrode and one outer annular PU electrode. An example is seen in Fig. 2, where A-B is implemented as one pixel and C-D as another. The row and column of the A-B pixel and the C-D pixel is addressed by a pair of 3-bit decoders for each pixel.

The current carrying signal path is implemented using transmission gates. One pair of decoders selects a pixel to supply current to, and another pair selects a pixel to drain current from. As an example, the current path for the two leftmost columns on the bottom row is illustrated in Fig. 8. Any pixel can function both as a current source and a current sink. The input is routed directly to a pad where a function generator is used to supply an AC current. The output is connected to the transimpedance amplifier (TIA), converting the current into voltage, which can then be measured.

The voltage signal readout path is controlled by the same decoders as the current readout path. It is implemented using an in-pixel nMOS source follower with a common current source for each column. The signal of the column selected by the



Fig. 7. Top level block diagram of the chip. The amplifiers are tuneable with off-chip potentiometers. The diagram was first published in [15].



Fig. 8. Current carrying path. RS = Row Select, CS = Column Select. The figure was first published in [15].

column decoder is routed by a pMOS source follower to the instrumentation amplifier. Two sets of the readout paths are needed since a differential signal (i.e. both B and C) is required. The circuit is illustrated in Fig. 9. A 7 transistor two-stage operational amplifier [23] was used as a building block for the instrumentation amplifier (IA) as well as the current to voltage converter. The on-board amplifiers are tuneable with off-chip potentiometers. The amplifiers are discussed and illustrated in our conference paper [15]. The PU electrodes are passive, and the potentials can therefore drift toward V_{dd} or Gnd. This could lead to a differential signal on the IA and the signal might fall outside the common mode input range of the amplifier. An option for re-setting the potentials on all PU electrodes with an external reference signal was therefore implemented. The connection to the external reference signal can be switched on or off by in-pixel



Fig. 9. Voltage readout path. RS = Row Select, OB = Out Bias, CS = Column Select, CB = Column Bias. The figure was first published in [15].

transmission gates. Since the PU electrodes are connected to high impedance amplifiers, very little current will be routed away through the PU electrodes during measurements.

A. Back-End

In this work, the Red Pitaya STEMlab 125-14 with an onboard signal generator and oscilloscope was used for measurement and control. The board features high speed RF I/O that were used for generating the input signals and for capturing the resulting outputs. Pixels addressing was performed with the boards digital I/O. A PCB including level shifters and voltage regulators was developed to interface the Red Pitaya board to the chip.

V. ELECTROPLATING GOLD

The microelectrodes received from the foundry are made of aluminum. Since the exposed aluminum quickly oxidizes to Al 2 O₃, a dielectric, it is beneficial to replace the surface of the microelectrodes with another material for impedance measurements. Aluminum compounds are also toxic to cell cultures [24]. Gold is an excellent candidate for impedance measurements since it is biocompatible and has a low ionization tendency [25]. However, gold microelectrodes cannot be included in standard CMOS processes since this may cause serious contamination [26]. An alternative method is to deposit gold in an electroless process called Electroless Nickel Immersion Gold (ENIG), commonly used for manufacturing printed circuit boards, where zinc and nickel are used as adhesion layers for gold, as seen in Fig. 10 i). Several authors have used the ENIG process for plating MEAs with individual differences such as electrode geometry and processing steps. We have based our deposition on the processes described by Niitsu et al. [25] and Bonanno et al. [27], but with different electrode shapes and another gold plating solution.



Fig. 10. Post processing and packaging. i) Zn, Ni and Au are deposited on top of the native Al electrodes and bonding pads by electroless plating, ii) the chip is bonded to a standard ceramic package, iii) SU-8 is applied outside the bonding wires, iv) SU-8 flows through the bonding wires during soft bake, v) the active area of the chip is covered during the UV-exposure, vi) SU-8 covers the bonding wires and pads.

Since handling mm sized chips can be difficult, a strainer was 3D printed in formlabs standard resin for moving the chips between the different chemicals used in the plating process.

Following pre-cleaning in isopropanol (IPA), the chips were dipped in 10% NaOH for 10 seconds to de-oxidize the top aluminum oxide layer, and then de-smuttered in 20% HNO $_3$ for 30 seconds. The electroless gold deposition needs two adhesion layers to be effective [27]. The first layer is a 1 minute zincation treatment (Techni EN Zincate) of the aluminum surface to avoid the formation of Al₂ O₃. To reduce the roughness of the Zn layer, a second zincation step, proceeded by a quick immersion in 20% HNO $_3$ for de-smuttering was also performed. The Ni adhesion layer was then deposited using Technic EN AT 5600 heated to 80 ° C for 10 minutes. Finally, the Au layer was realized by a cyanide-free immersion gold plating solution (Nano3DSystems) heated to 75 °C for 20 minutes. The chips were dipped in DI water at room temperature for 1 minute between each step in the proceess.

Scanning electron microscopy images of pixels before and after the electroless deposition process are seen in Fig. 11. The electroplated gold uniformly covers the aluminum electrodes. Inspection by SEM verified that gold had been successfully deposited on all pixels in the array. The presence of the different materials was also confirmed by Energy-dispersive X-ray spectroscopy (EDS). A cross-section of a pixel verifying the integrity of the metal stack is shown in Fig. 12. The nickel thickness varied between pixels, with an extreme case seen in Fig. 12, where the nickel layer in the ring is about 1 μ m thicker than the inner circle. The impedance of the extra nickel should, however, be very small compared with the impedance in the electrode - solution interface.

It should be noted that after several experiments with different liquids over many days, some electrodes started to disintegrate.

As noted by Jung et al. [16], electroless processes can lead to improper coverage of the underlying electrodes. For electrode stability during long-term cell-based measurements, the group instead deposited Au electrodes by E-beam evaporation. Although the bonding pads were plated as well, no subsequent problems occurred during wire bonding. As calculated by Bonanno et al. [27], with mass- production the ectroless plating process can be performed for less than $1 \in$.

VI. PACKAGING IN SU-8

CMOS chips intended for wet experiments must be packaged to avoid exposing the bonding pads and bonding wires to liquids. Packaging chips for lab-on-a-chip integration still remains a challenge, although several strategies have been developed for different needs and applications, as reviewed by Datta et al. [28] and Khan et al. [29]. For instance, Li et al. [30] developed a multichannel microfluidic microsystem with screen printed interconnects on a custom made epoxy carrier for lab-on-CMOS application, while Zhang et al. [31] developed a flexible package where a liquid metal was used for the electrical interconnects to the IC chip. For many applications, complex solutions such as these are unnecessary. In our application for instance, we first and foremost wish to demonstrate a new sensor concept, and we therefore seek a simple and robust packaging method that effectively shields the IC interconnects. A commonly applied, simple and low-cost solution is to manually cover the bonding wires with epoxy, while simultaneously ensuring that epoxy does not flow onto the active area of the chip. However, this method requires precise control of the amount of epoxy applied, especially with small chips, and there is a high risk of covering the active area of the chip with epoxy. Indeed, Hwang et al. lost several chips during the application of epoxy this way [26].





Fig. 11. (a) Pixel with aluminum electrodes. (b) Pixel after electroless plating of gold.

Fig. 12. (a) FIB cross section of an electroplated pixel. (b) Magnified view of the PU ring in (a). The aluminum, nickel and gold layers can be distinguished.

For improved control, Martin et al. [32] and Dandin et al. [33] patterned a ring structure of SU-8 ($12 \mu m$ high in the work by Martin et al. [32]) between the bonding pads and the active area of the chips to stop the epoxy from flowing onto the active area. While reducing the risk of covering the active area of the chips, the method still depends on precise control of the amount and surface tension of the epoxy applied, as noted by Dandin et al. [33], and the risk of covering the sensor area is therefore still present. Other properties of the epoxy, such as bio-compatibility, must also be considered. Instead of patterning a ring with SU-8 to stop the flow of epoxy, we have focused on developing a robust method that also covers the bonding wires and pads with SU-8. We have briefly described this process previously [34] and in the



present paper we expand upon the method. SU-8 is commonly spun onto a substrate (typically wafers) to achieve precise control of the layer thickness. However, when the bonding wires in a traditional ceramic package are to be covered, a much thicker layer of SU-8 must be cast. This can be be challenging since thicker structures increases the likelihood of unwanted cracks in the resist, which could ultimately lead to leakages. Depending on the desired thickness of the SU-8 film, the photoresist comes with a variety of solvent concentrations. We have tested both SU-8 10 (low viscosity) and SU-8 100 (high viscosity) from MicroChem. Because of solvent evaporation, SU-8 10 had to be applied and soft baked several times in order to cover the bonding





wires. Other authors have found SU-8 10 to shrink about 32% during softbake baking [35]. On the other hand, we have found that SU-8 100 can completely cover the bonding wires after a single application. Additionally, since SU-8 100 has a higher viscosity, the bulk of the resist tends to stop flowing where the bonding wires attaches to the chip, thereby allowing only a small volume to enter the chip surface. A thinner layer of SU-8 on the IC is advantageous since a thinner layer is easier to pattern and develop.

The encapsulation process is shown in Fig. 10 iii) - vi). SU-8 is first placed at the edges of the cavity of the ceramic package with a pipette tip, so that the photoresist can flow towards the chip when heated (i.e. the process does not require spin-coating). For our 84 ceramic pin grid array package (P/N CPG08451 spectrum semiconductor) we applied 130 mg of resist in total. In general, the amount of resist must be tailored to the specific chips and packages. Since the resist is very viscous and sticks to the pipette tip, we have found that the easiest way to control the amount of resist is to place the ceramic package on a weighing scale during the application of the resist. The package is then placed on a hotplate at 125 °C for 30 minutes for the photoresist to flow and cover the bonding wires and pads. Although it is recommended to start soft baking SU-8 at 65 °C, a higher temperature is needed since the package is placed on pins above the hotplate. We have commonly continued baking in a convection oven at 95 °C for 1 h, but this depends on the amount of resist applied. Since a rapid cool down can lead to cracks in SU-8, we let the resist cool down slowly inside the oven when the soft bake is finished. The thickness of the resist requires a long exposure time. For our application we have exposed for 300 seconds (350 W mercury arc lamp). We initially utilized a photomask with sharp corners, as seen in Fig 13 a). However, since the stress in SU-8 often creates cracks in the corners, we now use a photomask with rounded corners (Fig 13 b). A large crack in the photoresist patterned with the square mask is seen in Fig. 13(c)). This crack lead to leakages through the corners. With rounded corners, smaller cracks were formed at the top surface, as seen in Fig. 13(d)), and no leakage was observed. Post exposure baking is done at the same temperatures as the soft bake, still ensuring a slow cool down of the resist. Finally, the resist is developed for 15 min with mr-Dev 600 (Microresist) at room temperature. The SU-8 encapsulated chip is seen in Fig. 14.

VII. RESETTING PASSIVE ELECTRODES

Since the electrodes could be drifting, an option for resetting the PU electrodes before subsequent measurement was implemented. The reset is done by opening and closing transmisson gates connecting the PU electrodes to a chosen voltage (common mode voltage (i.e. 900 mV) is practical). The falling edge of this reset signal is used as a trigger for the signal generator on the Red Pitaya feeding the input CC electrode, ensuring the initial voltage swing to be around 900 mV, as seen in Fig. 15. It should be noted that resetting the electrodes could stimulate cells (e.g. cardiomyocytes, neurons), especially if the electrodes have drifted far away from 900 mV. The drift would be largest when the system have gotten time to settle (e.g. when first switching



Fig. 13. Photomasks with (a) square corners, and (b) rounded corners. The resulting SU-8 structures obtained with (c) square masks often had large cracks in the corners of the SU-8 thereby leading to leakages, while those obtained with (d) rounded corner masks had several small cracks distributed at the top of the SU-8, and no observed leakages.



Fig. 14. The final gold electroplated chip encapsulated in SU-8.

the system on), and smaller between subsequent measurements (i.e. just compensating parasitic leakage in the chip).

VIII. DATA ACQUISITION AND FILTERS

The falling edge of the reset signal also triggers and starts the acquisition process. This ensures that the recording begins at the



Fig. 15. A synchronization with the reset signal ensures an initial swing around common mode voltage for the amplifiers (IA top).



Fig. 16. Original differential IA (blue) and TIA (orange) voltage signals, and the lowpass-filtered IA (red) and TIA (green) voltage signals.

exact moment the signal generator starts feeding the source CC electrode.

Both the IA and the TIA outputs had low-frequency and high-frequency noise as well as drift superpositioned onto the signal. Acquisition of the IA and TIA measurements from the Red Pitaya therefore required some post-processing algorithms and filters to extract the peak-to-peak voltages. To reduce the seemingly random high-frequency noise, a low-pass FIR-filter (Savitzky-Golay) was implemented, and the result of this filtering is seen in Fig. 16. A slow drift on the signals was also observed in some cases. A simple solution for this is to split the signal into the number of whole periods and take the peak-to-peak of each period. For some of the TIA measurements in liquid, significant 50 Hz noise (frequency of mains electricity in Europe) was observed superpositioned on the TIA output. To



Fig. 17. Time series measurement.



Fig. 18. Electrical impedance spectroscopy of DI Water and PBS.

reduce the 50 Hz contribution, a numerical high pass (Butterworth) filter was added to the post-processing algorithms. This high-pass filter also helps reducing signal drift.

IX. LIQUID TESTS

The electrode impedance for miniaturized electrodes can be large (several M Ω) [21], thus requiring a high gain from the TIA to amplify the current. In Fig. 16, a $300 \text{ k}\Omega$ resistor (gain = 300 k) was utilized by the TIA to amplify a 6,3 kHz signal in DI water. However, by increasing the TIA gain up $1 M\Omega$ and beyond, substantial noise was added to to the signal. A variation in the conductivity of the solution did not alter the current much, as seen from the time-series experiment in Fig. 17, where DI water, a 95%/5% DI-PBS mixture and PBS was added sequentially for 40 seconds each. This can possibly be explained by the electrode impedance dominating the impedance of the bulk solution. Additionally, a change in conductivity of the solution also alters the electrode impedance [22]. In contrast, a clear difference in the voltages sensed by the PU electrodes can be seen in Fig. 17, thereby showing the benefit of a four-electrode system for miniaturized electrodes. Finally, EIS measurements were performed with DI water and PBS, as seen in Fig. 18. All

electrodes on the chip were addressable, but a varying degree of drift was observed between pixel pairs. The measurements in this article were obtained from single pixel pairs.

X. CONCLUSION

A MEA was developed to investigate the implementation of a four-electrode system for use in bioimpedance studies. Gold was deposited onto the native aluminum electrode pixels with an electroless plating process, and the structure and integrity of the pixels were verified by FIB-SEM. A packaging technique for protecting the bonding wires and pads with SU-8 was developed. DI water was placed on the sensor, and subsequently replaced by diluted PBS and finally PBS. The current did not change significantly between the different liquid. However, decreasing potentials were observed when the liquids with higher conductivity were added, thereby suggesting that a four-electrode system can be a good alternative for impedance measurements on CMOS MEAs. Our work demonstrates how such a system can be implemented. Future work on dedicated chips for four-electrode measurements on CMOS MEAs could focus on varying the electrodes' size and shape, fabricating structures with varying recess depths and improved noise performance. Finally, measurement results from cell cultures should be obtained.

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Steffen Nøvik (Member, IEEE) received the M.Sc. degree in nanotechnology from the Norwegian University of Science and Technology, Trondheim, Norway, in 2012. After the graduation degree, he was with fiber optic sensor installations for Weatherford Norge AS. In 2018, he started the Ph.D. degree with the Department of Informatics, University of Oslo, Oslo, Norway, where he focuses on bioimpedance sensors for Organ-on-Chip applications.



Stefan Johannes Karl Krauss is currently a Professor and the Director of the Centre of Excellence Hybrid Technology Hub, Institute of Medical Biology, University of Oslo, Oslo, Norway, and the Oslo University Hospital. He has a background in developmental biology, developmental signaling, and chemical biology. He is currently focusing on applying morphogenetic signaling to advance organoid development and integration. He has authored or coauthored 106 peer reviewed articles, including in Cell, Nature and Nature Journals, and six patents.

His discovery of the key vertebrate signal Shh was identified as one of the 24 Milestones in Development by the journal *Nature*.



Magnus Flø Drageseth recieved the M.Sc. degree in electrical engineering and computer science from the University of Oslo, Oslo, Norway, in 2020. After the graduation degree, he joined Novelda AS, where he is currently an IC test and validation Engineer.



Magnus Børresen Grøndalen received the B.Sc. degree in physics in 2019 and the second B.Sc. degree in computer science in 2020 from the University of Oslo, Oslo, Norway, where he is currently working toward the M.Sc. degree in electrical engineering and computer science. While studying, he has had summer internships and part-time positions within a variety of fields, such as rocket simulations, full-stack development, machine learning, and electronics engineering. He is also a Hardware Test Engineer with Novelda AS.



Ørjan Grøttem Martinsen (Senior Member, IEEE) received the Ph.D. degree in 1995. He is currently a Professor of electronics with the Department of Physics, University of Oslo, Oslo, Norway. He also has an adjunct position as a Senior Researcher with the Department of Clinical and Biomedical Engineering, Oslo University Hospital, Oslo. He is a co-author of the textbook *Bioimpedance and Bioelectricity Basics*. His research mainly focuses on the passive, electrical properties of biomaterials. He is the Editorin-Chief of the *Journal of Electrical Bioimpedance*.



Ola Nilsen was born in Oslo, Norway, in 1973. He received the Dr. Sci. degree related to deposition of complex oxides by ALD from the University of Oslo, Oslo, in 2003. He was a Postdoc in 2004 and an Associate Professor in 2008 with the University of Oslo, where his focus on ALD/MLD of complex oxides, organic- inorganic hybrid materials, and Li-based materials. Since 2015, he has been a Full Professor. He is teaching several courses related to chemistry, inorganic materials, nanotechnology, and supervised many students at all levels. He has authored or coau-

thored more than 160 papers, ten patent applications, and spun off a company based on his research.



Philipp Dominik Häfliger (Senior Member, IEEE) received the M.Sc. degree in computer science (with astronomy as a minor subject) from the Swiss Federal Institute of Technology (ETH), Zürich, Switzerland, and the Ph.D. degree from the Institute of Neuroinformatics, ETH, in 1995 and 2000, respectively. He then moved for a Postdoctoral position with the Nanoelectronics Group, Department of Informatics, University of Oslo, Oslo, Norway, where he has advanced to Full Professor. In Oslo, his research focuses on shifted gradually from neuromorphic (inspired by the

nervous system) electronics towards mixed-signal ASIC design, in particular for biomedical devices, e.g. wireless microimplants, and more recently for micro-probes for space research. He coordinates the 3D-MUSE Project of the EU's Horizon 2020 Research Programme, that is concerned with high density 3-D sequential integration of CMOS circuits. He was served on various functions for IEEE ISCAS and IEEE BioCAS conferences, and an Associate Editor for IEEE TRANSACTIONS ON BIOCAS.