Switching-Table-Based Direct Torque Control of Six-Phase Drives With $x-y$ Current Regulation

Mohammad Hosein Holakooie, Grzegorz Iwanski, *Senior Member, IEEE*, and Tomasz Miazga

***Abstract*—High harmonic contents of the stator currents due to uncontrolled $x-y$ subspace dramatically overshadow the performance of the switching-table-based direct torque control (ST-DTC) strategy for multiphase drives. The concept of ST-DTC based on virtual voltage vectors (VVs) has been frequently developed to alleviate this problem. However, VVs with fixed duty ratios are incapable of compensating inherent machine/converter asymmetries and dead time harmonics, which are mapped into the $x-y$ subspace. To solve this problem, this article develops a dynamic duty-ratio-based DTC technique for six-phase induction machine drives, where the duty ratios of the selected VVs are not constant anymore. These duty ratios are updated based on the $x-y$ voltage commands arising from the closed-loop $x-y$ current controllers over every sampling period. The attained merits over and above the conventional fixed duty-ratio-based DTC schemes include effective $x-y$ current cancellation without increase in average switching frequency and decrease in dc-link utilization. Experimental results are presented to validate the effectiveness of the proposed control technique.**

***Index Terms*—Current regulation, direct torque control (DTC), multiphase drive, switching table.**

NOMENCLATURE

Acronyms

3-D VV	Three-dimensional virtual voltage vector.
6PIM	Six-phase induction machine.
DTC	Direct torque control.
DDR-DTC	Dynamic duty-ratio-based DTC.
FDR-DTC	Fixed duty-ratio-based DTC.
FCS-MPC	Finite control set-model predictive control.
FOC	Field-oriented control.
ISR	Interrupt service routine.
P-I-R	Proportional-integral-resonant.
PWM	Pulsewidth modulation.
SS	Steady state.
ST-DTC	Switching-table-based DTC.
THD	Total harmonic distortion.
TMVCL	Total maximum voltage compensation level.
VSD	Vector space decomposition.
VSI	Voltage source inverter.
VV	Virtual voltage vector.

Variables

CA, CB	Counter-compare A and B of PWM module.
PRD	Specified period of PWM module.
f_{sw}	Average switching frequency.
i_{uvw}	Stator phase current.
S_h	Switching states of 3-D VVs.
S_{uvw}	Binary sequences of actual voltage vectors.
t_h	Duty ratios of 3-D VVs.
T_1, T_2	PWM action points.
T_e	Electromagnetic torque.
T_s	Sampling period.
$v_{\alpha\beta}$	Normalized $\alpha-\beta$ voltage space vectors.
$\lvert v_{\alpha\beta}\rvert$	Normalized amplitude of $\alpha-\beta$ voltages.
v_{xy}	Normalized $x-y$ voltage space vectors.
$\lvert v_{xy}\rvert$	Normalized amplitude of $x-y$ voltages.
V_{dc}	DC-link voltage.
V_{hx}, v_{hx}	Real and normalized x-components of 3-D VVs.
V_{hy}, v_{hy}	Real and normalized y-components of 3-D VVs.
V_{xy}^*, v_{xy}^*	Real and normalized $x-y$ voltage commands.
η	DC-link utilization.
θ_s	Angular position of stator flux.
ω_r	Rotor speed.

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The authors are with the Institute of Control and Industrial Electronics, Warsaw University of Technology, 00-662 Warszawa, Poland (e-mail: hosein.holakooie@pw.edu.pl; iwanskig@isep.pw.edu.pl; tomasz.miazga@pw.edu.pl).

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ψ_s	Amplitude of stator flux.
Symbols	
L, ML, MS, S	Large, medium large, medium small, and small voltage vectors.
$h = \{1, 2, 3\}$	Vector number within 3-D VVs.
j	Imaginary unit.
$k = \{I, \ldots, XII\}$	Sector number.
N	Normalized quantities.
$u - v - w$ (Two sets)	Normal six-phase system.
$x - y$	Secondary reference frame.
$\alpha - \beta$	Stationary reference frame.
$*$	Command values.

I. Introduction

MULTIPHASE machine drives have been remarkably joining the mainstream of research studies in the recent decades due to their valuable advantages over three-phase ones, e.g., higher reliability, lower rate of phase quantities and converter switches, and lower torque pulsations [1], [2]. Specifically, the need for a higher reliability has popularized the use of multiphase electric drives in some industrial applications, such as electric vehicles, brake-by-wire systems, fuel pumps, electric aircraft, and ships, thanks to their stator-phase redundancy [3]. Although the multiphase drives are not widely used as three-phase drives, their inherent fault-tolerant capability is enough to attract a lot of interests for safety-critical applications [4], [5].

The original idea of DTC strategy was first introduced in mid-1980s [6], for three-phase induction machine. Despite the fact that DTC was introduced more than one decade after FOC, it has found a prestigious place in academic and industrial communities. A fair comparison between DTC and FOC techniques has been well addressed in [7]. In comparison to FOC, DTC proposes an inherent *sensorless drive*, which is more preferable in high-power application because of lower average switching frequency. Furthermore, this method benefits from simple structure, fast dynamics, and robust performance. However, the classical ST-DTC is subject to high torque ripple and variable switching frequency [7]. More importantly, in the case of multiphase drives, this technique is overshadowed by the high THD of the stator currents, when single voltage vector is selected and applied during whole sampling period [8]. The reason is that the applied single voltage vector causes nonzero average volt-seconds (volt-sec) in the secondary subspaces (several $x-y$ orthogonal subspaces in relation with number of machine phases), which do not contribute to electromechanical energy conversion. The excited secondary subspace increases current harmonics and losses [9]. Undoubtedly, integration of all promising features of a drive system into a unified DTC strategy is sophisticated; nevertheless, a large number of papers has been dedicated to alleviate some of previously cited problems, where they have approached the issue from different angles. Modulation-based DTC scheme is a possible solution [10], [11], where the simplicity, fast dynamics, and robustness of ST-DTC are sacrificed to achieve better SS performance and constant switching frequency [7]. The slow dynamic behavior of the modulation-based DTC is mainly due to PI regulators, which has been investigated by a hybrid two-mode DTC scheme [12]. However, the complexity of the modulation-based DTC schemes, especially for multiphase drives, has stimulated a prolific research work to tackle the problems of the ST-DTC strategy [13]–[22].

Definition of VVs is a core idea to decrease unwanted stator current harmonics due to uncontrolled $x-y$ subspaces in multiphase drives, where the VVs are first constructed using appropriate actual voltage vectors; then, their duty ratios are calculated offline in such a way that the average volt-sec in the secondary subspaces to be zero. This context has been frequently highlighted for the nonmodulation-based control techniques, i.e., ST-DTC strategy [13]–[22] and FCS-MPC strategy [22], [23]. In this regard, VVs have been synthesized for three-level and two-level VSIs-fed five-phase induction machine in [13] and [14], respectively. In [16], an ST-DTC scheme with five-level hysteresis torque regulator has been proposed for 6PIM, where it has employed two groups of VVs with different voltage levels to reduce the torque ripples. Experimental implementation of [16] has been discussed in more detail in [20]. Such ST-DTC schemes with a modified three-level [17] and five-level [18] hysteresis torque regulators as well as rearranged VVs, to provide a simpler realization, have been addressed for six-phase permanent magnet synchronous machine. Forming VVs for ST-DTC of seven-phase and nine-phase machines has been reported in [21] and [22], respectively. Despite an inevitable decrease in dc-link utilization and increase in average switching frequency as consequences of using several actual voltage vectors within every sampling period, ST-DTC and FCS-MPC benefit greatly from VVs in terms of lower harmonic content of the stator currents compared with actual voltage vectors. These VVs possess fixed duty ratio, i.e., their duty ratios are precalculated based on a simple principle to make an average volt-sec of zero in the $x-y$ subspace. This situation can be interpreted as zero $x-y$ voltage commands ($v_x^* = v_y^* = 0$) in modulation-based techniques, which clearly cannot fully compensate $x-y$ currents, because there is no control over these currents. Similarly, FDR-DTC strategies cannot perfectly compensate stator current harmonics because of stator winding/converter asymmetries and VSI dead time effect, which are unavoidable in multiphase electric drives, as well as, back-electromotive force distortion [19]. Indeed, the ST-DTC schemes presented in [13]–[22] suppresses the $x-y$ currents due to discrete PWM implementation in a great extent, but $x-y$ currents due to dead band and asymmetry harmonics, because they always maintain zero average $x-y$ voltages during every sampling period using static VVs.

The abovementioned problems, in relation to FDR-DTC, have been well-reported in the modulation-based techniques, such as FOC strategy [24]–[28], where applying different current control strategies in $x-y$ subspace have made it possible to effectively compensate $x-y$ currents. However, circumstances become more involved when it comes to ST-DTC or FCS-MPC due to lack of modulation strategy, where the topic has been rarely studied until now [29]–[31]. In the light of these limitations, the ideas of dynamic VVs and smart VVs have been recently proposed

in [29] and [30], respectively, for FCS-MPC of multiphase drives to enhance the capability of $x-y$ currents compensation. On the other hand, in [31], an ST-DTC with closed-loop $x-y$ current compensation, based on PIR controller, has been proposed, where significant increasing the average switching frequency and remarkable reducing the dc-link utilization besides implementation complexity are the main deficiencies.

Unsatisfactory performance of the multiphase drives under uncontrolled $x-y$ currents (by setting zero $x-y$ voltage commands) has motivated many research efforts to effectively control them [24]–[28]. However, the most significant developments in this field have been limited to the modulation-based techniques, especially FOC. The main goal of this article is to develop an ST-DTC scheme with $x-y$ current regulation for 6PIM. Indeed, static VVs in FDR-DTC schemes can just assure zero $x-y$ voltages, which is not enough to compensate the $x-y$ currents due to destructive effects, such as machine/converter asymmetries, dead time, and back-electromotive force, which are very likely in the multiphase drives. Aiming to overcome these shortcomings, this article proposes an DDR-DTC technique for 6PIM drives, where the virtual voltage vectors can dynamically provide both zero and nonzero $x-y$ voltages within every sampling period depending on the $x-y$ currents. Specifically, developing a feasible solution to add the closed-loop $x-y$ current controllers to the ST-DTC strategy is the main contribution of this article. To this end, in the first step, 3-D VVs based on three actual large voltage vectors are formed. Then, their duty ratios are determined using $x-y$ voltage commands, which come from $x-y$ current control loops. The proposed technique effectively compensates the $x-y$ currents, while it maintains the fast dynamic response of conventional FDR-DTC schemes without increasing the average switching frequency. The proposed DDR-DTC scheme is experimentally validated for an asymmetrical 6PIM with two isolated neutral points, while it can be extended to five-phase drives as well. Nevertheless, extending this method to other multiphase drives, for example, symmetrical 6PIM, to compensate for zero-sequence currents as well, requires a more complicated scheme due to lack of modulation strategy; this is, however, beyond the scope of this article.

II. Proposed DDR-DTC Scheme

A. Virtual Voltage Vectors Selection

Thanks to the VSD technique [9], an asymmetrical 6PIM with near-sinusoidal distribution of stator windings is represented in three orthogonal subspaces (called $\alpha-\beta$, $x-y$, and o_1-o_2), where only $\alpha-\beta$ components contribute toward electromechanical energy conversion, while the $x-y$ and o_1-o_2 components cannot generate a useful rotating magnetomotive force in the air gap. The so-called six-dimensional Clarke transformation, presented in [9], transforms the normal six-phase system ($u_1-u_2-w_1-w_2-v_1-v_2$) into these three orthogonal subspaces. In a two-level dual three-phase VSI-fed 6PIM with two isolated neutral points, there are entirely 64 switching states, consequently 64 voltage vectors, where 60 of them are active and the rest are zero voltage vectors. They are

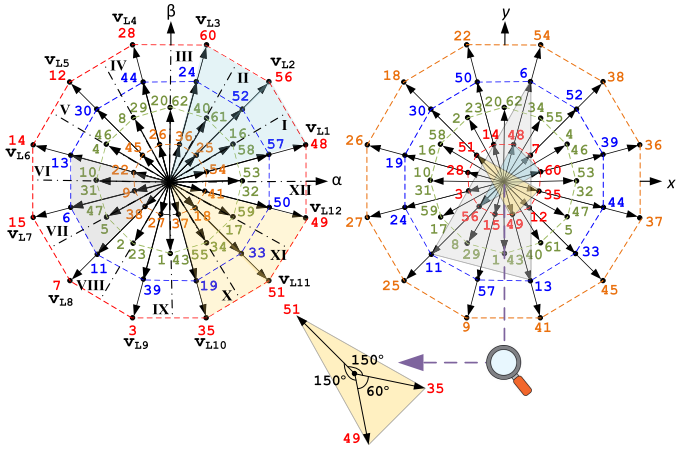

Fig. 1. Voltage vectors of two-level dual three-phase VSI-fed asymmetrical 6PIM in the $\alpha-\beta$ and $x-y$ subspaces.

TABLE I
Actual Voltage Vectors of 6PIM

Group Name	Sample	$\lvert v_{\alpha\beta}\rvert$	$\lvert v_{xy}\rvert$	η (%)
Large (V_L)	48	0.6440	0.1725	100%
Medium large (V_{ML})	57	0.4714	0.4714	73.21%
Medium small (V_{MS})	16(58)	0.3333	0.3333	51.76%
Small (V_S)	54	0.1725	0.6440	26.79%

spatially distributed in the $\alpha-\beta$ and $x-y$ subspaces, which are outlined in Fig. 1. Decimal voltage numbers in Fig. 1 indicate switching states of dual three-phase VSI using binary sequences as $S_{uvw}=[S_{u1}S_{u2}S_{w1}S_{w2}S_{v1}S_{v2}]$, where S_{uvw} is the state of upper VSI's switches. These voltage vectors constitute four voltage levels in the $\alpha-\beta$ or $x-y$ subspace, categorized in large, medium large, medium small, and small groups, which are shown as four nonzero dodecagons in Fig. 1. The specifications of the constructed actual voltage vectors in the $\alpha-\beta$ subspace are listed in Table I, where the normalized amplitude of the voltage vectors with $V_{\rm dc}$ is calculated as

$$|v_{\alpha\beta}|=\sqrt{v_\alpha^2+v_\beta^2} \tag{1}$$

and the percentage of dc-link utilization (η) is given by [17]

$$\eta=\frac{|v_{\alpha\beta}|}{|v_{\alpha\beta}|^L}\times 100 \tag{2}$$

where $v_{\alpha\beta}=v_\alpha+jv_\beta$.

As shown in Fig. 1, each actual voltage vector in the $\alpha-\beta$ subspace is mapped in a different space position in the $x-y$ subspace, where the voltage levels of large and small voltage vectors in the $\alpha-\beta$ subspace are reversed in the $x-y$ subspace, while no change is made to the voltage levels of medium large and medium small voltage vectors. Accordingly, applying single voltage vectors during whole sampling period penalizes nonmodulation-based control techniques by high harmonic content of the stator currents with dominant orders of fifth and seventh in the case of 6PIM with two isolated neutral points [9]. The concept of VVs can solve this problem to a great extent,

where applying multiple actual voltage vectors with their appropriate duty ratios in each sampling period offers the possibility of nullifying average volt-sec in the $x-y$ subspace. However, zero resultant $x-y$ voltages may not ensure zero $x-y$ current flows because of inherent machine/converter asymmetries and dead time effect, which they both often appears simultaneously in 6PIM drives. In order to fully compensate the $x-y$ current harmonics, the VVs should be flexible enough in such a way that they offer the possibility of tracking any $x-y$ voltage commands, which are provided by the closed-loop $x-y$ current controllers. Therefore, forming the suitable VVs with such a capability is a first step in developing the proposed scheme.

A nonflexible option of forming VVs is to use two actual voltage vectors in each sampling period, where medium large voltage vectors should be included within each synthesized VVs because of their opposite direction in the $x-y$ subspace against large or small voltage vectors in each sector k (see Fig. 1). For examples, the sets, such as $V_{48}-V_{57}$ and $V_{54}-V_{57}$ (for $k=I$), from large and medium large groups, and small and medium large groups, respectively, have been frequently used in the literature [16]–[18], where they provide two different voltage levels in the $\alpha-\beta$ subspace, while their exactly opposite direction in the $x-y$ subspace may only offer zero average volt-sec in the $x-y$ subspace, which make them unsuitable for the proposed DDR-DTC scheme. Indeed, the projection of these two actual voltage vectors in x- and y- axes is always two-quadrant, while it should be four-quadrant to be able to reconstruct any $x-y$ voltage commands (as the output of the $x-y$ currents controllers) with arbitrary angular position. To this end, implementation of three consecutive actual voltage vectors is proposed in this paper to construct 3D VVs. The 3D VVs are flexible and four-quadrant to track any $x-y$ voltage commands, where they constitute similar triangles in the $x-y$ subspace, which are shown in Fig. 1 for three cases from large and medium large voltage groups. There are similarities between constructed triangles in the $x-y$ subspace despite the fact that they belong to different voltage levels in the $\alpha-\beta$ subspace. This similarity may offer a generalized ST-DTC scheme, which is straightforward in the experimental realization. All constructed 3-D VVs based on three consecutive actual large voltage vectors are tabulated in Table II. Each VV is described by a decimal sequence as $C=[C_{u1}C_{u2}C_{w1}C_{w2}C_{v1}C_{v2}]$, where $C\in\{0,\ldots,7\}$ is the switching sequence of upper VSI's switches. Obviously, there are totally $2^3=8$ possible switching sequences for each VSI's leg, because three voltage vectors are applied during each sampling period. The procedure of extraction of switching sequences from actual voltage vectors is highlighted in Table II.

TABLE II
3-D VVs Based on Three Consecutive Actual Large Voltage Vectors

k	VVs	DEC Seq.	V_1^k	V_2^k	V_3^k
I	VV_{L1}	771004	V_{L12} 110001	V_{L1} 110000	V_{L2} 111000
II	VV_{L2}	773100	V_{L1} 110000	V_{L2} 111000	V_{L3} 111100
III	VV_{L3}	677300	V_{L2} 111000	V_{L3} 111100	V_{L4} 011100
IV	VV_{L4}	467700	V_{L3} 111100	V_{L4} 011100	V_{L5} 001100
V	VV_{L5}	047710	V_{L4} 011100	V_{L5} 001100	V_{L6} 001110
VI	VV_{L6}	007731	V_{L5} 001100	V_{L6} 001110	V_{L7} 001111
VII	VV_{L7}	006773	V_{L6} 001110	V_{L7} 001111	V_{L8} 000111
VIII	VV_{L8}	004677	V_{L7} 001111	V_{L8} 000111	V_{L9} 000011
IX	VV_{L9}	100477	V_{L8} 000111	V_{L9} 000011	V_{L10} 100011
X	VV_{L10}	310077	V_{L9} 000011	V_{L10} 100011	V_{L11} 110011
XI	VV_{L11}	730067	V_{L10} 100011	V_{L11} 110011	V_{L12} 110001
XII	VV_{L12}	770046	V_{L11} 110011	V_{L12} 110001	V_{L1} 110000

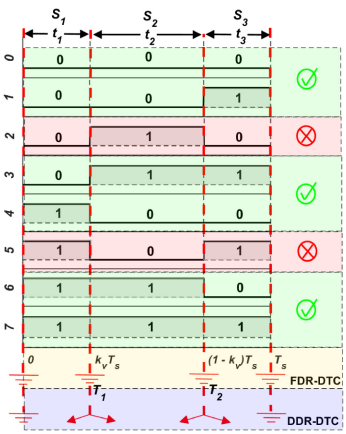

Fig. 2. Possible switching sequences of three consecutive actual voltage vectors.

B. General Overview of the Proposed Technique

The general overview of the proposed DDR-DTC technique can be described by Fig. 2, where the binary strings $\overline{S_1S_2S_3}$ make the switching sequence of each VSI's leg. As mentioned in the preceding section, since that three consecutive actual voltage vectors are applied at every sampling period, there are eight possible switching sequences, which are outlined by decimal numbers 0 to 7 in Fig. 2. However, it can be seen from Table II that the switching sequences of 2 and 5 do not take place when three large voltage vectors are employed, while these sequences also appear for the other voltage groups. Hence, the switching sequences 2 and 5 are distinguished in Fig. 2. This will be to the benefit of the ST-DTC technique from average switching frequency viewpoint, because sequences 2 and 5 impose two switching jumps in each sampling period, while the rest imposes one jump. In the case of conventional FDR-DTC techniques, the duty ratios of the applied voltage vectors are calculated in such a way that make average volt-sec of zero in the $x-y$ subspace. Regarding Fig. 1, solving

$$\begin{cases}\sqrt{3}/2(t_1+t_3)=t_2\\ t_1+t_2+t_3=T_s\\ t_1=t_3\end{cases}\tag{3}$$

ensures zero volt-sec in the $x-y$ subspace for three consecutive actual voltage vectors regardless of the voltage groups, which yields

$$\begin{cases} t_1 = (2-\sqrt{3})T_s \\ t_2 = (2\sqrt{3}-3)T_s \\ t_3 = (2-\sqrt{3})T_s \end{cases}. \tag{4}$$

The duty ratios of t_1, t_2, and t_3 can be experimentally implemented by defining two action points T_1 and T_2 as

$$\begin{cases} T_1 = t_1 = k_v T_s \\ T_2 = t_1 + t_2 = (1-k_v)T_s \end{cases} \tag{5}$$

where $k_v = 2-\sqrt{3}$.

The difference between the conventional FDR-DTC techniques and proposed DDR-DTC technique is schematically shown in the down side of Fig. 2. When the action points T_1 and T_2 are fixed, the average volt-sec of the $x-y$ subspace will be zero during each sampling period. This is indicated by the ground symbol ⏚ in Fig. 2 for the FDR-DTC technique, which is equivalent to a disabled $x-y$ current regulation, because the $x-y$ voltage commands are set to zero ($v_x^* = v_y^* = 0$). Such schemes are incapable of compensating $x-y$ currents due to the machine/converter asymmetries and dead time effect. For this purpose, simultaneous movements of action points T_1 and T_2 during each sampling period is proposed in this article as a feasible solution to reconstruct any desired $x-y$ voltage commands arising from $x-y$ current control loops. The movements may take place in both left and right directions, which are shown by the arrow symbols (↙↘) in Fig. 2. In the next section, the effect of these movements on the produced $x-y$ voltages will be discussed using a quantitative example.

C. Mathematical Derivations

As mentioned previously, VVs made of three consecutive large voltage vectors explore the possibility of compensating $x-y$ currents through reconstructing any desired $x-y$ voltage commands, which are obtained from $x-y$ current control loops. These three voltage vectors for each sector number k in the $x-y$ subspace can be expressed as (see also Table II)

$$\begin{cases} V_{1xy}^k = V_{1x}^k + jV_{1y}^k \\ V_{2xy}^k = V_{2x}^k + jV_{2y}^k \\ V_{3xy}^k = V_{3x}^k + jV_{3y}^k \end{cases}. \tag{6}$$

Defining the $x-y$ voltage commands as V_x^* and V_y^*, the volt-sec equations in $x-y$ subspace are written as

$$\begin{cases} V_{1x}^k.t_1 + V_{2x}^k.t_2 + V_{3x}^k.t_3 = V_x^*.T_s \\ V_{1y}^k.t_1 + V_{2y}^k.t_2 + V_{3y}^k.t_3 = V_y^*.T_s \end{cases} \tag{7}$$

where t_1, t_2, and t_3 are the duty ratios of these three voltage vectors to reconstruct the desired command voltages. After normalization with $V_{\rm dc}$ and T_s, (7) can be derived as

$$\begin{cases} v_{1x}^k.t_1^N + v_{2x}^k.t_2^N + v_{3x}^k.t_3^N = v_x^* \\ v_{1y}^k.t_1^N + v_{2y}^k.t_2^N + v_{3y}^k.t_3^N = v_y^* \end{cases}. \tag{8}$$

Regarding

$$t_1^N + t_2^N + t_3^N = 1 \tag{9}$$

by removing the normalized duty ratio t_3^N from (8), the normalized volt-sec equations can be rewritten as follows:

$$\begin{cases} v_{13x}^k.t_1^N + v_{23x}^k.t_2^N = v_x^* - v_{3x}^k \\ v_{13y}^k.t_1^N + v_{23y}^k.t_2^N = v_y^* - v_{3y}^k \end{cases} \tag{10}$$

where

$$\begin{cases} v_{13x}^k = v_{1x}^k - v_{3x}^k \\ v_{23x}^k = v_{2x}^k - v_{3x}^k \\ v_{13y}^k = v_{1y}^k - v_{3y}^k \\ v_{23y}^k = v_{2y}^k - v_{3y}^k \end{cases}. \tag{11}$$

Accordingly, the duty ratios t_1^N and t_2^N are calculated as

$$\begin{bmatrix} t_1^N \\ t_2^N \end{bmatrix} = \begin{bmatrix} v_{13x}^k & v_{23x}^k \\ v_{13y}^k & v_{23y}^k \end{bmatrix}^{-1} \begin{bmatrix} v_x^* - v_{3x}^k \\ v_y^* - v_{3y}^k \end{bmatrix} = \boldsymbol{\Delta V}_{xy}^{-1} \boldsymbol{V}_{xy}^*. \tag{12}$$

After calculating the determinant of $\boldsymbol{\Delta V}_{xy}$ matrix for all 3-D VVs, it can be proved that it remains the same for all VVs belong to the same voltage groups. This determinant is always $1/18$ for 3-D large VVs (then $1/|\boldsymbol{\Delta V}_{xy}| = 18$ for large voltage vectors). Therefore, (12) can be simplified in the following way:

$$\begin{bmatrix} t_1^N \\ t_2^N \end{bmatrix} = 18 \begin{bmatrix} v_{23y}^k & -v_{23x}^k \\ -v_{13y}^k & v_{13x}^k \end{bmatrix} \begin{bmatrix} v_x^* - v_{3x}^k \\ v_y^* - v_{3y}^k \end{bmatrix}. \tag{13}$$

Equations (9) and (13) can be used for online updating the duty ratios t_1^N, t_2^N, and t_3^N according to the desired $x-y$ voltage commands obtained by $x-y$ currents controllers. If the $x-y$ voltage commands are set to zero, i.e., $v_x^* = v_y^* = 0$, the duty ratios will be fixed at

$$\begin{cases} t_1^N = 2-\sqrt{3} \\ t_2^N = 2\sqrt{3}-3 \\ t_3^N = 2-\sqrt{3} \end{cases} \tag{14}$$

for all VVs, which represents the FDR-DTC technique. However, in the proposed DDR-DTC technique, the $x-y$ voltage commands are continuously adjusted to compensate $x-y$ currents.

A quantitative example helps to clarify how the proposed DDR-DTC scheme can compensate any zero/nonzero $x-y$ voltage commands. For simplicity, let us only consider VV_{L1}, while the conclusions can be extended to other 3-D large VVs as well. According to Table II, VV_{L1} is expressed by a decimal six-digit sequence as [771004] for $u_1-u_2-w_1-w_2-v_1-v_2$ phases, respectively. It means that whenever VV_{L1} is selected according to the switching table, the upper switches of VSI for phase-u_1 and phase-u_2 should be ON during whole sampling period, while they should be OFF for phase-w_2 and phase-v_1. The upper switch of phase-w_1 should take OFF–ON position during each sampling period, while the switch should take ON–OFF position for phase-v_2, where the duty ratios are calculated based on $x-y$ voltage commands. A set of nine different VV_{L1}, constructed based on different $x-y$ voltage commands, is shown

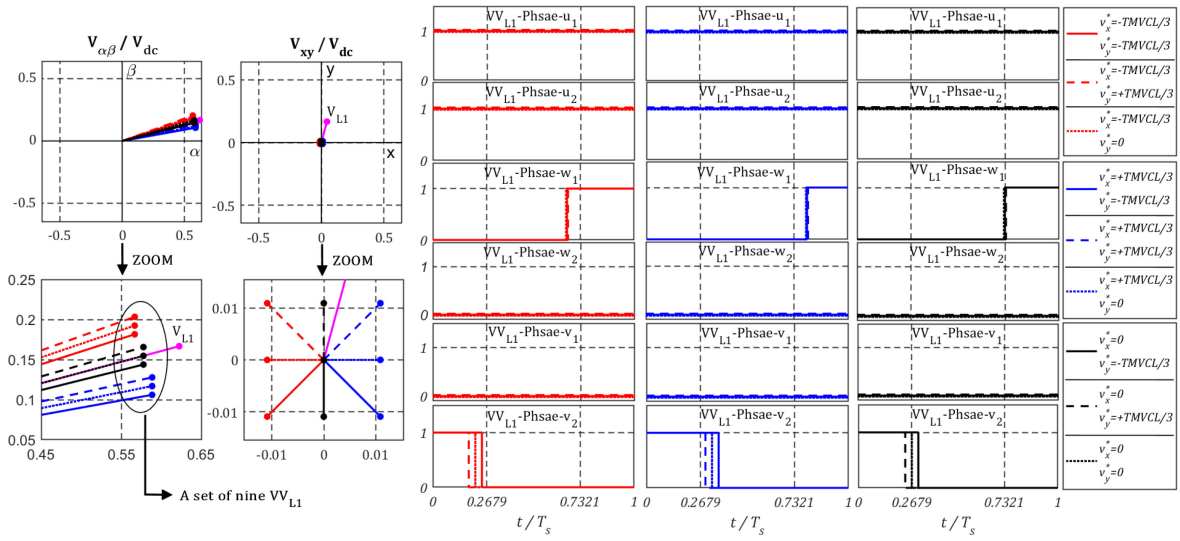

Fig. 3. Set of nine different VV_{L1}, constructed based on different $x-y$ voltage commands with corresponding pulse patterns.

in Fig. 3. The corresponding pulse patterns for every VV_{L1} are also depicted in Fig. 3. The parameter TMVCL of this figure will be defined later. As it can be seen, the constructed VV_{L1} are four-quadrant in the $x-y$ subspace, while they are close together in the $\alpha-\beta$ subspace. It means that all constructed VV_{L1} have the same impact on the torque and stator flux ($\alpha-\beta$ subspace), while they can reconstruct any $x-y$ voltage commands. It should be noted that only nine conditions are shown in Fig. 3, while there are an infinite possibility for each 3-D VVs.

D. $x-y$ Currents Controllers

Generally, additional current harmonics inevitably arise in adjustable ac drives due to, e.g., asymmetries, inverter nonlinearities, and back-electromotive force distortion, where lower order current harmonics are always of more concern because of lower inductive impedance of the circuit at lower frequencies. In the multiphase drives, these current harmonics are mapped in a primary subspace ($\alpha-\beta$ subspace) and several secondary subspaces. The harmonics in the primary subspace cause torque ripples and the stator ohmic losses, while the harmonics of the secondary subspaces only produce losses. Low impedance of the secondary subspaces will exacerbate the content of stator current harmonic flow in the secondary circuits, which causes a significant efficiency decrease [2], [32].

Implementing FDR-DTC technique can compensate the stator current distortion to a great extent in comparison with conventional ST-DTC for multiphase drives. In actual, this method can remarkably reduce the current harmonics due to improper switching sequences, which are adopted in the conventional ST-DTC. However, FDR-DTC techniques may be still penalized by a serious current distortion because of machine/converter asymmetries and dead time effects. As reported in [24] and [26], inherent machine/converter asymmetries of 6PIM drives cause $x-y$ currents with fundamental frequency, which may rotate in the synchronous, antisynchronous, or both directions, depending on the type of asymmetries. Specifically, in [24], a general analysis of machine/converter asymmetry has been presented using the concept of symmetrical components and double-stator modeling, where it was concluded that the $x-y$ currents, due to machine/converter asymmetry, rotate at the fundamental frequency. On the other hand, the dead time effect of 6PIM drives causes $x-y$ currents rather than torque/flux-producing currents, where the dominant harmonic orders are the fifth and seventh harmonics in the case of 6PIM with two isolated neutral points [9].

A variety of current controllers, mainly based on PI and PR terms, have been proposed in the literature for compensating the $x-y$ currents. For examples, parallel dual PI (in the synchronous and antisynchronous frames) and PR (in the antisynchronous frame) controllers [24], generic multiple PR and PI controllers in multiple synchronous frames [25], PR controllers in the stationary frame [26], and PI controllers in the synchronous frame [27], [28] have been developed to compensate the $x-y$ currents due to multiphase drives-specific phenomena, such as machine/converter asymmetries and dead time effect. Anyway, the primary concern of this article is what goes on in the ST-DTC scheme if there are nonzero $x-y$ voltage commands, not how these voltage commands can be generated, while the later problem has been well addressed in the literature [24]–[28]. Thanks to the capability of synchronous PI controllers for compensating the fifth and the seventh harmonics of 6PIM's stator phase currents (mapped into the $x-y$ subspace), to an extent limited by the PI controllers' bandwidth [24], [27], [28], as well as, PI controllers in the antisynchronous frames in parallel with it to fully compensate the inherent machine/converter asymmetries [24], a dual PI controller in the synchronous and antisynchronous reference frames is adopted in this article. The block diagram of this controller is shown in the down side of Fig. 4. Undoubtedly, $x-y$ currents can be fully compensated using some generic multiple resonant-based current controllers [25], but they may overshadow the simplicity of ST-DTC, as well.

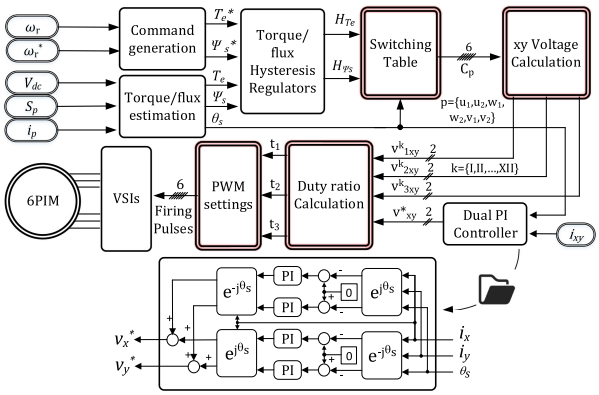

Fig. 4. Block diagram of the proposed DDR-DTC scheme.

E. Block Diagram and Hardware Implementation

Fig. 4 depicts the block diagram of the proposed DDR-DTC technique. The outputs of the switching table represent six switching sequences, in relation to the six legs of dual three-phase VSI by decimal numbers from 0 to 7 (except 2 and 5 in the case of 3-D large VVs), which the possible pulse patterns were demonstrated in Fig. 2. It should be noted that a sequence of these decimal numbers describe 3-D large VVs. In the proposed DDR-DTC method, the switching table functions, such as the classical switching table, which can be found in the literature [8]. The difference between the switching table of the classical ST-DTC and DDR-DTC schemes is the outputs of the switching table, while the rules for selecting these outputs are the same according to the hysteresis flux and torque regulators and the sector number. Using these switching sequences, dual three-phase VSI normalized model as

$$\begin{bmatrix} v_{u1} \\ v_{w1} \\ v_{v1} \\ v_{u2} \\ v_{w2} \\ v_{v2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 & 0 & 0 & 0 \\ -1 & 2 & -1 & 0 & 0 & 0 \\ -1 & -1 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & -1 & -1 \\ 0 & 0 & 0 & -1 & 2 & -1 \\ 0 & 0 & 0 & -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_{u1} \\ S_{w1} \\ S_{v1} \\ S_{u2} \\ S_{w2} \\ S_{v2} \end{bmatrix} \tag{15}$$

and 6-D Clarke transformation, six $x-y$ voltage components should be calculated during each sampling period, i.e., v_{1xy}^k, v_{2xy}^k, and v_{3xy}^k. These voltage components besides the $x-y$ voltage commands, as the outputs of the $x-y$ current controllers, provide the appropriate duty ratios according to (9) and (13).

The duty ratios of t_1^N, t_2^N, and t_3^N can be experimentally realized by defining two adjustable action points in the proposed DDR-DTC (see also down side of Fig. 2) as follows:

$$\begin{cases} T_1^N = t_1^N \\ T_2^N = t_1^N + t_2^N \end{cases}. \tag{16}$$

The modified switching sequences, based on dynamic changes of the action points T_1^N and T_2^N in every sampling period to conform to the desired $x-y$ voltage commands, can be implemented using the PWM module in the most microcontroller platforms. For this purpose, the PWM module can be initialized to an asymmetrical counting mode, for example, count-up mode in this article. Moreover, two counter-compare registers are required, which they should be updated at each sampling period according to the action points T_1^N and T_2^N as follows [20]:

$$\text{CA} = T_1^N \text{PRD} + (1 - T_1^N)(\overline{S_1 \oplus S_2})\text{PRD} + M(\overline{S_1 \oplus S_2}) \tag{17}$$

$$\text{CB} = T_2^N \text{PRD} + (1 - T_2^N)(\overline{S_2 \oplus S_3})\text{PRD} + M(\overline{S_2 \oplus S_3}) \tag{18}$$

where $M \geq 1$ is an integer constant and $\oplus$ indicates the XOR logical operation. The switching states S_1, S_2, and S_3 can be easily extracted from switching sequences. The switching state S_1 determines the output state of the PWM module when the counter starts at the beginning of every sampling period. These settings, besides (17) and (18), have been pictured as the *PWM settings block* in Fig. 4. It is worth mentioning that in the conventional FDR-DTC schemes, the values of CA and CB are fixed, while they are continuously changed in line with the $x-y$ voltage commands over each sampling period in the proposed DDR-DTC scheme.

F. Further Details About the Proposed Technique

1) Average Switching Frequency (f_{sw}): It is obtained by counting total number of switches' jumps during a certain time period. Obviously, an increase in f_{sw} is inevitable when VVs are used instead of actual ones. This increase is more visible when symmetrical middle-high pulse patterns are used, where the justification is to simplify the hardware implementation [18]. Although the proposed DDR-DTC scheme employs three large voltage vectors over each sampling period, the f_{sw} will not theoretically increase compared to the conventional FDR-DTC schemes [14], [20], because a maximum of one switch's jump take places at each sampling period for each VSI's leg. In actual, the difference between the proposed DDR-DTC and the conventional FDR-DTC schemes is in the time of occurrence of these switches' jumps, not in the number of jumps.

2) Total Maximum Voltage Compensation Limit (TMVCL): It is the absolute value of maximum $x-y$ voltage commands that can be injected by the 3-D VVs without erroneous calculation of duty ratios. TMVCL specifies the minimum and maximum allowable values of the dual PI current controller outputs. It is defined as follows:

$$\text{TMVCL} = \min\{\max(v_{xy}^*)\}^k; \qquad k = \{\text{I}, \text{II}, \ldots, \text{XII}\} \tag{19}$$

where the maximum voltage compensation level of each VVs should be firstly calculated, then a minimum of these values determines TMVCL. TMVCL can be proved as

$$\text{TMVCL} = \sqrt{2}\left(1 - \frac{\sqrt{3}}{2}\right)|v_{xy}|. \tag{20}$$

For 3-D VVs based on three consecutive large voltage vectors, the normalized amplitude of the voltage vectors in the $x-y$ subspace is calculated as

$$|v_{xy}| = (2/3)\cos(5\pi/12). \tag{21}$$

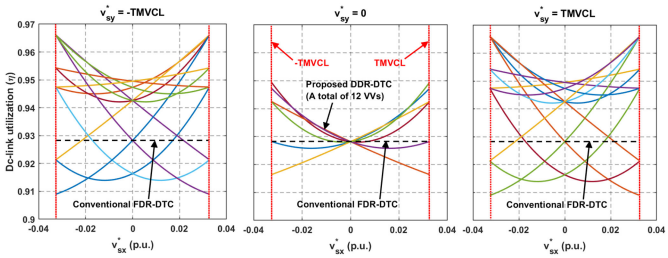

Fig. 5. DC-link utilization of different 3-D VVs for the proposed DDR-DTC technique.

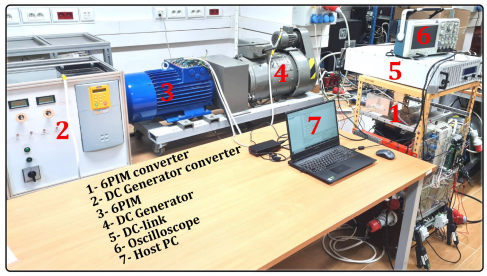

Fig. 6. Experimental setup for dual three-phase VSI-fed 6PIM.

Hence, TMVCL is about 3.27% for 3-D large VVs.

3) DC-Link Utilization: In order to calculate the dc-link utilization of 3-D VVs, the $\alpha-\beta$ voltages aligned with V_2^k are written as

$$v_\alpha = \frac{\sqrt{3}}{2}t_1V_1^k + t_2V_2^k + \frac{\sqrt{3}}{2}t_3V_3^k \tag{22}$$

$$v_\beta = \frac{1}{2}t_3V_3^k - \frac{1}{2}t_1V_1^k. \tag{23}$$

Thanks to (2), a general form of η for 3-D VVs can be simplified as follows:

$$\eta = \sqrt{\left(\frac{\sqrt{3}}{2}t_1 + t_2 + \frac{\sqrt{3}}{2}t_3\right)^2 + \left(\frac{1}{2}t_3 - \frac{1}{2}t_1\right)^2}. \tag{24}$$

In the case of conventional FDR-DTC technique, using duty ratios presented in (4), dc-link utilization is

$$\eta = \sqrt{3}t_1 + t_2 = 4\sqrt{3} - 6 = 0.9282. \tag{25}$$

However, η is not constant anymore for the proposed DDR-DTC technique, where it depends on the $x-y$ voltage commands and the selected VVs according to the torque and flux demands. Fig. 5 shows the changes in η relative to v_x^* for all 3-D VVs (a total of 12 VVs) for three different v_y^* values. Furthermore, η is shown with dash line for the conventional FDR-DTC method, which is a constant value for all VVs. It is obvious that η converges to 0.9282 for all VVs when $v_x^* = v_y^* = 0$. It can be seen in Fig. 5 that the proposed DDR-DTC method offers dc-link utilization close to the conventional FDR-DTC method, while there is a high probability that η in the proposed method will be usually more than the conventional method depending on the selected VVs and the $x-y$ voltage commands.

4) Increasing TMVCL: As discussed earlier, VVs based on three consecutive large vectors obtain a voltage compensation up to a maximum of 0.0327 per unit (p.u.), which it seems to be enough to compensate for the inherent machine/converter asymmetries and dead time effect, as the experimental results of this article also confirm it. Nevertheless, the proposed DDR-DTC technique is flexible enough to increase TMVCL by changing the voltage group from large level to medium large level, without extensive changes in the hardware implementation. It should be noted that although this substitution increases TMVCL, it increases f_{sw} as well, because the switching sequences of 2 and 5 (see Fig. 2) may also appear at VSI's legs. Moreover, using such a VVs decreases dc-link utilization. According to (20), TMVCL for VVs based on three consecutive medium large voltage vectors is given by

$$\begin{aligned}\text{TMVCL}^{ML} &= \sqrt{2}\left(1 - \frac{\sqrt{3}}{2}\right)(2/3)\cos(3\pi/12) \\ &= 0.0893 \text{ p.u.}\end{aligned} \tag{26}$$

and the ratio of TMVCL for medium large group to large group is

$$\frac{\text{TMVCL}^{ML}}{\text{TMVCL}^{L}} = \frac{\cos(3\pi/12)}{\cos(5\pi/12)} = 2.7321 \tag{27}$$

which means that VVs based on medium large voltage vectors can increase TMVCL more than twice.

III. Experimental Results

A. Hardware Description

Fig. 6 shows a photograph of the laboratory test stand. This is composed of a four-pole asymmetrical 6PIM with two isolated neural points, which is fed by two commercial three-phase Semikron SKiiP VSI connected to a 250-V dc power supply, as well as, it is mechanically coupled with a separately excited dc generator controlled by a Parker dc digital drive to apply the load torque. 6PIM converters are controlled by a 32-bit floating point TMS320F28335 digital processor, which is programmed through code composer studio development environment. The main control algorithm is periodically called through a PWM ISR with 10 kHz frequency, where the dead time is about 2.3 μs, and the speed controller and calculation are called by a timer interrupt with 100 Hz frequency. An incremental shaft encoder with 2048 pulses per revolution (PPR), LEM LV25-P voltage transducers, and LEM LA55-P current transducers are employed to measure the rotor pulse train, dc-link voltage, and phase currents, respectively. The required parameters for implementing the proposed control scheme are listed in Table III, where the rated torque of 10 N $\cdot$ m, the rated speed of 1350 r/min, and the rated stator flux of 0.6 Wb are considered for the laboratory setup.

B. Experimental Results

The theoretical investigations are supported by the experimental results, where this article makes a comparison between

TABLE III
REQUIRED PARAMETERS OF THE LABORATORY SETUP

Symbol	Value	Description
T_n	10 Nm	Rrated torque
ω_n	1350 rpm	Rated speed
ψ_{sn}	0.6 Wb	Rated stator flux
P	2	Pole pairs
B_T	5%	Torque hysteresis band
B_ψ	2%	Stator flux hysteresis band
R_s	1.8 Ω	Stator resistance
K_{pxy},K_{ixy}	0.1, 2.5	$x-y$ current controller's gain
$K_{p\omega}$,$K_{i\omega}$	0.4, 0.2	Speed controller's gains
f_s	10 kHz	PWM ISR frequency
f_m	100 Hz	Speed controller ISR frequency

the proposed DDR-DTC and the conventional FDR-DTC techniques in different test scenarios to demonstrate the validity of the proposed scheme. The PI controller gains of the speed control loop and the $x-y$ current control loops are tuned using trial-error method. The maximum and minimum allowable outputs of the current controllers are specified using TMVCL. A two-level hysteresis flux regulator and a three-level hysteresis torque regulator are employed in the DDR-DTC and FDR-DTC schemes. Fig. 7 shows the SS performance results of the conventional FDR-DTC and the proposed DDR-DTC techniques under no-load condition at 100 r/min. The stator flux command for this test and subsequent tests is 0.6 Wb. The harmonic spectra of $x-y$ and u_1-u_2 currents are also shown in this figure. From top to bottom, the x-, y-, u_1-, and u_2-currents are presented in each oscillogram. The results are captured, then a zoom of two cycles after passing through a low-pass filter with the cutoff frequency of 1 kHz is plotted in the down side of each oscillogram. From Fig. 7, it can be seen that the inherent machine/converter asymmetries cause $x-y$ currents with fundamental frequency, in turns, unequal amplitudes of the stator phase current, which the conventional FDR-DTC is unable to compensate it. However, the proposed DDR-DTC scheme effectively compensate these asymmetries, which the $x-y$ currents spectra confirm the effectiveness of the proposed control strategy. Moreover, the fifth and seventh current harmonics in the $x-y$ subspace, mainly due to dead time effect, are appropriately compensated by the proposed DDR-DTC technique. The phase current THD with the proposed method is clearly superior to those with the conventional FDR-DTC. Fig. 8 depicts the SS experimental results with harmonic spectra of x-axis and phase-u_1 currents for FDR-DTC and DDR-DTC schemes at 1350 r/min speed and rated load torque. The rotor speed, electromagnetic torque, phase-u_1, and x-axis currents are shown in each oscillogram. The merits of the proposed scheme in reduction of the current harmonics under the rated conditions can be clearly observed from this test scenario as well.

In the next test, the 6PIM-drive system is allowed to work with the proposed DDR-DTC technique at 400 r/min without load torque. The control algorithm switches from the proposed DDR-DTC to FDR-DTC by applying $v_x^* = v_y^* = 0$ at $t = 0.5$ s. The experimental results for the $x-y$ currents, u_1-u_2 currents, and $x-y$ voltages are shown in Fig. 9. It is seen that the $x-y$ currents with a visible fundamental frequency emerge

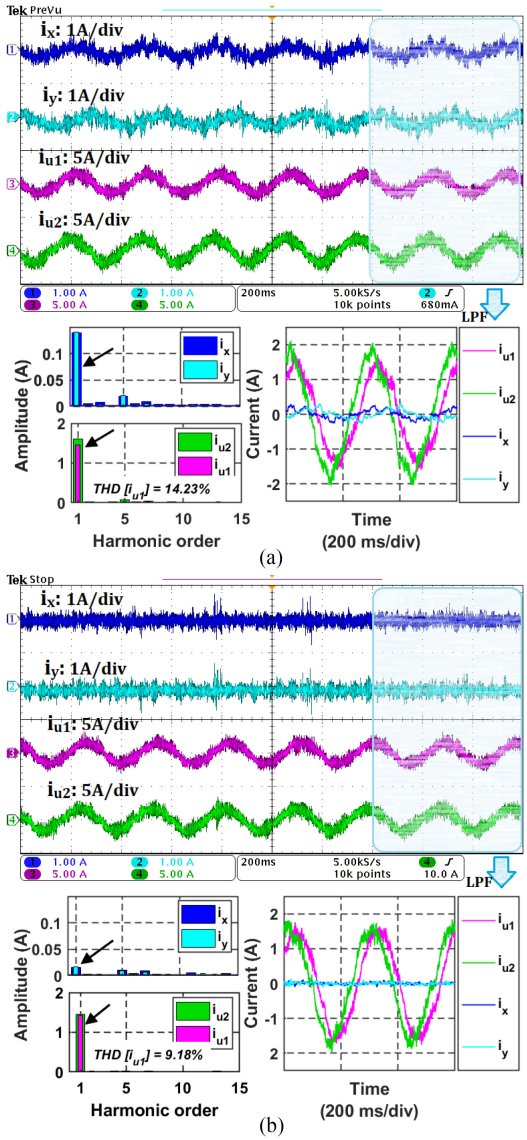

Fig. 7. Experimental results with harmonic spectra of $x-y$ and u_1-u_2 currents for no-load condition at 100 r/min. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

after deactivation of the proposed technique at $t = 0.5$ s, where the $x-y$ voltages are zero. Such a test scenario is repeated for speed command of $\omega_r^* = 100$ r/min at rated load condition. Fig. 10 shows the traces of the measured $x-y$, u_1-u_2, and $\alpha-\beta$ currents in addition to $x-y$ voltages for this test. The harmonic spectra of x-axis and phase-u_1 currents as well as the measured THD of phase current are also included in Fig. 10. It should be mentioned that this test as well as the prior one are performed twice to capture all needed traces using a four-channel oscilloscope. It can be seen from Fig. 10 that the proposed DDR-DTC effectively compensates the $x-y$ currents through proper injecting the $x-y$ voltage commands, which yields lower THD of phase current. However, considerable asymmetries and dead time harmonics appear after deactivating the proposed algorithm at $t = 1$ s. Taking a detailed look at the stator phase currents (i_{u1} and i_{u2}) in Figs. 9 and 10, within the frame that the

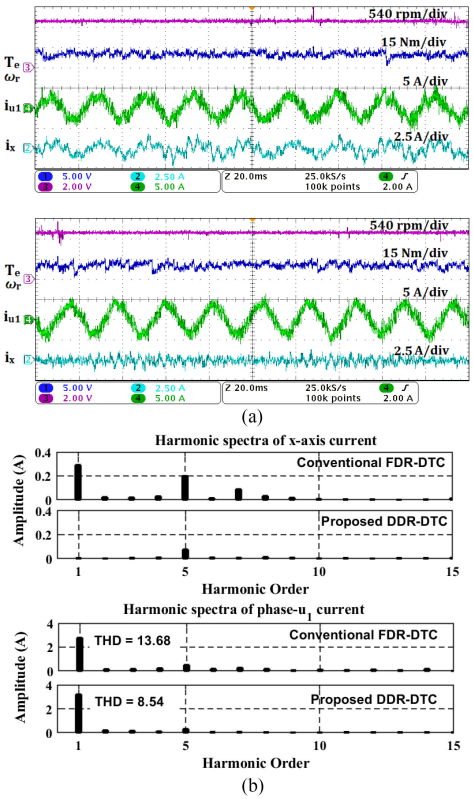

Fig. 8. Experimental results with harmonic spectra of x-axis and phase-u_1 currents for rated load condition at 1350 r/min. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

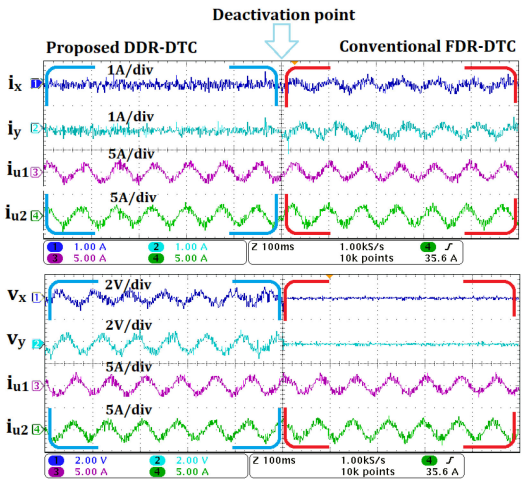

Fig. 9. Experimental results for no-load condition at 400 r/min with online deactivation of proposed DDR-DTC.

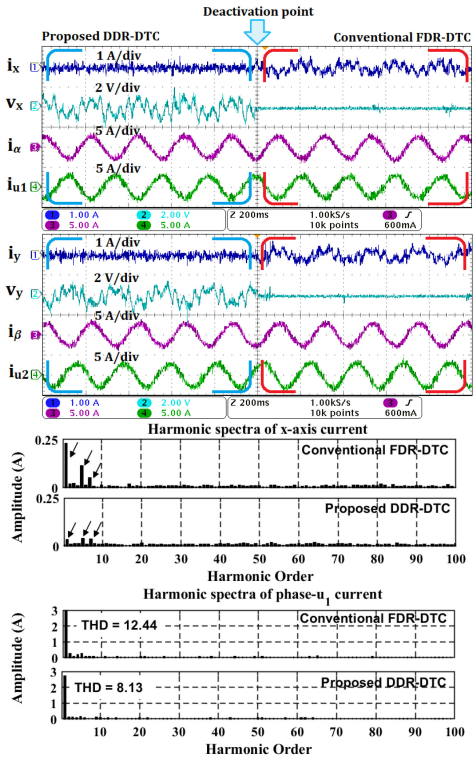

Fig. 10. Experimental results with harmonic spectra of x-axis and phase-u_1 currents for rated load condition at 100 r/min with online deactivation of proposed DDR-DTC.

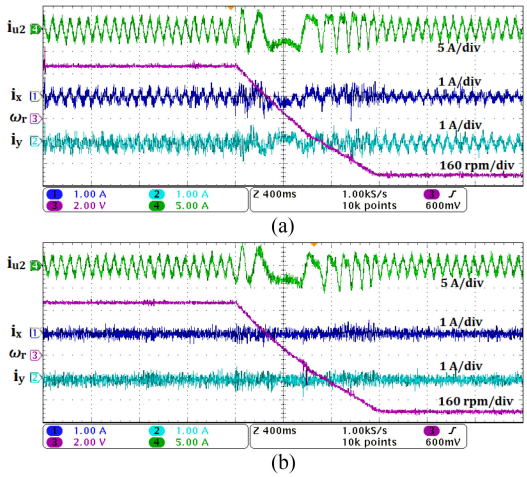

Fig. 11. Experimental results for speed reversal maneuver (±400 r/min) at no-load condition. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

FDR-DTC is active, reveals an unequal amplitude of phase currents due to inherent machine/converter asymmetry, which it appears as $x-y$ currents at fundamental frequency. However, this fundamental harmonic besides dead band harmonics are effectively suppressed in the case of the proposed DDR-DTC.

In addition to SS tests shown in Figs. 7–10, some experiments are carried out to confirm the valid dynamic performance of the proposed technique. The experimental results for the speed reversal maneuver from +400 to −400 r/min at no-load condition are shown in Fig. 11(a) and (b) for the conventional FDR-DTC and the proposed DDR-DTC, respectively. Each oscillogram contains the measured traces of the $x-y-u_2$ currents and the rotor speed. Moreover, Fig. 12 shows the measured traces of speed, electromagnetic torque, phase-u_1, and x-axis currents for speed reversal test from −400 to +400 r/min at 75% rated load torque condition. The experimental results for the sudden loading scenario, with an amount of 75% rated load torque, for the conventional and proposed techniques are shown

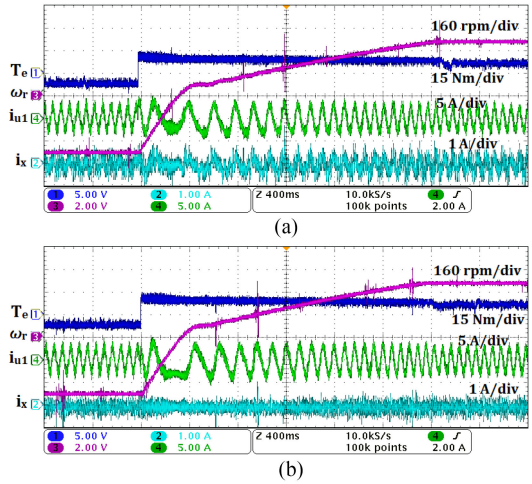

Fig. 12. Experimental results for speed reversal maneuver (∓400 r/min) at 75% rated load torque. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

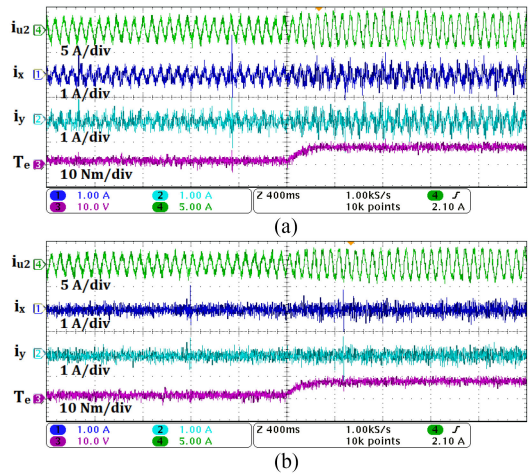

Fig. 13. Experimental results for sudden loading (75% rated load torque) at 400 r/min. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

in Fig. 13(a) and (b), respectively. The speed command is 400 r/min in this test, where the traces of $x-y-u_2$ currents and the electromagnetic torque are captured in each oscillogram. Finally, the recorded experimental results for sudden unloading test scenario under rated conditions are shown in Fig. 14. In this test, the drive system is initially commanded by the rated speed and load torque, then the load torque is suddenly removed at $t = 0.3$ s. From Figs. 11 to 14, it is seen that the proposed scheme effectively compensates both asymmetry and dead time harmonics, while adding dual PI controller does not affect speed/torque control in comparison with FDR-DTC. From these dynamic test results, it can be concluded that the proposed DDR-DTC technique does not impose negative effects (for example, degrading transient behavior of the torque and speed or increasing the torque ripples) on the electromechanical characteristics of the drive system during dynamic tests compared with conventional FDR-DTC. Indeed, the proposed DDR-DTC technique offers a comparable dynamic

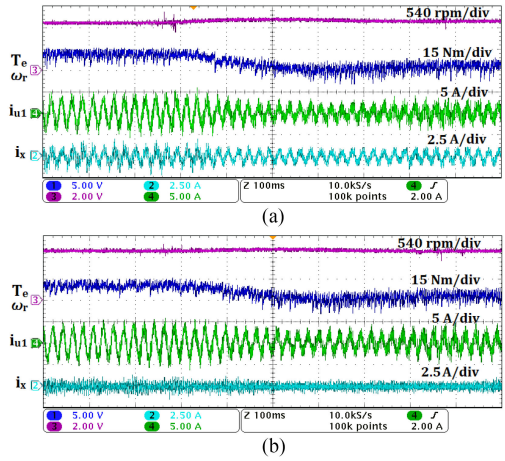

Fig. 14. Experimental results for sudden unloading (rated load torque) at 1350 r/min. (a) Conventional FDR-DTC. (b) Proposed DDR-DTC.

TABLE IV
QUANTITATIVE/QUALITATIVE COMPARISON BETWEEN FDR-DTC AND DDR-DTC

Items	FDR-DTC	DDR-DTC	Note
CPU utilization (%)	20.15	39.27	—
f_{sw} (kHz)	2.45	2.48	Ref.: Fig. 10
THD $[i_{u1}]$ (%)	12.44	8.13	Ref.: Fig. 10
ΔI_{u1u2} (A)	0.2366	0.0309	Ref.: Fig. 10
η (%)	92.82	90.91 ∼ 96.61	Ref.: Fig. 5
Parameter dependency	R_s	R_s	—
Torque/flux ripples	Same level	Same level	—
Transient response	Same level	Same level	—

performance with conventional FDR-DTC technique, but with lower harmonic contents of the $x-y$ currents.

C. Quantitative and Qualitative Analysis

A quantitative/qualitative comparison of the proposed DDR-DTC and conventional FDR-DTC can reveal the superiority of the proposed scheme as well as its limitation. The comparison items and results are summarized in Table IV. The findings of this comparison will be further described in the following.

1) Computational Burden: To evaluate the software complexity of the proposed DDR-DTC, its average execution time over 500 calls of PWM ISR is monitored, then it is compared with the FDR-DTC scheme presented in [16]. The scheme of [16] has employed a modified hysteresis torque regulator. To obtain a fair comparison, the same hysteresis flux and torque regulators are considered in both schemes. It should be noted that since the execution time is hardware dependent and programming dependent, same programming style makes such a comparison fair. For more clarification, the computational burden is reported as a percentage of central processing unit (CPU) utilization @150 MHz operating speed. The percentage of CPU utilization is listed in Table IV. As expected, the proposed DDR-DTC scheme imposes more computational burden on the CPU, because of dual-PI controller, $x-y$ voltages, and duty ratios calculations. Therefore, implementation of the proposed method in the low-cost electric drives may be challenging.

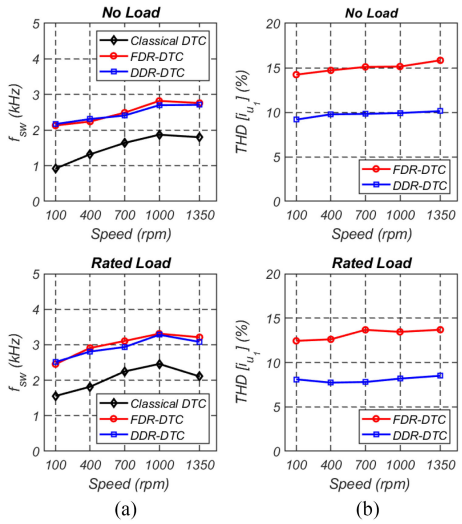

Fig. 15. Comparison between FDR-DTC and DDR-DTC. (a) Average switching frequency. (b) THD of phase-u_1 current.

Anyway, microprocessor market size is growing so fast that such a computational burden may marginally overshadow the modern and high-speed microprocessors. It is worth mentioning here that another FDR-DTC scheme with symmetrical pulse patterns has been presented in [17], where the CPU utilization of this scheme is about 15.68% but with higher f_{sw}. Indeed, f_{sw} and execution time are the main differences between asymmetrical and symmetrical switching sequences presented in [16] and [17], respectively.

2) Average Switching Frequency: The average switching frequency of the classical DTC, FDR-DTC, and DDR-DTC for different speeds at no load and rated load conditions is shown in Fig. 15(a). In this comparison, the FDR-DTC scheme of [16] is considered. As frequently mentioned in the literature, by implementing the FDR-DTC scheme, the $x-y$ currents due to discrete PWM are suppressed in a great extent in comparison with the classical DTC method, but at the expense of sacrificing f_{sw}. This is a very reasonable compromise, because the classical DTC of multiphase drives is dramatically penalized by the current harmonics. As shown in Table IV and Fig. 15(a), the proposed DDR-DTC scheme maintains f_{sw} at the same level as FDR-DTC, which the reason was described earlier. The sample pulse patterns of Fig. 3 can also justify the issue, where it can be observed that all constructed 3-D large VVs have the same effect on f_{sw}.

3) Current Harmonics: Io order to assess the capability of the proposed DDR-DTC in reduction of the $x-y$ currents, two indices are considered, i.e., THD of phase-u_1 current and ΔI_{u1u2}. The later index is defined as the absolute difference between magnitude of phase-u_1 and phase-u_2 currents at the fundamental frequency, which is significant in the studied test bench due to inherent machine/converter asymmetry when static VVs or actual voltage vectors are employed. The THD of phase-u_1 current for the FDR-DTC and DDR-DTC schemes at different machine speeds under no load and rated load torque conditions is depicted in Fig. 15(b). It is clear that the proposed DDR-DTC scheme can effectively reduce the THD of phase currents under a wide speed range due to a dual PI controller. Moreover, it can be seen from Table IV that ΔI_{u1u2} is significantly reduced for the proposed DDR-DTC scheme, which means that the proposed method properly removes asymmetries.

4) Other Items and Overall Analysis: As listed in Table IV, the proposed DDR-DTC obtains a variable η in the range of 90.91–96.61% depending on the selected 3-D VVs and $x-y$ voltage commands (see Fig. 5), which is in close proximity to FDR-DTC scheme. On the other hand, the proposed DDR-DTC is just like classical DTC from parameter dependency viewpoint. Therefore, it does not overshadow the robustness of the classical DTC method. Moreover, the SS torque/flux ripples and transient response of the both DDR-DTC and FDR-DTC schemes are at the same level, mainly due to the same level of η with similar switching table. The overall result is that the proposed DDR-DTC, in comparison with FDR-DTC, can significantly reduce the $x-y$ harmonics just at the expense of relative increasing the software complexity.

IV. Conclusion

This article was aimed at compensating $x-y$ currents due to machine/converter asymmetries and dead time effect for ST-DTC of 6PIM drives. For this, a DDR-DTC scheme was proposed, where the $x-y$ currents were compensated through a dual PI current controller embedded in the ST-DTC technique. First, 3-D VVs based on three actual large voltage vectors were arranged; then, the duty ratios of these vectors were optimally selected according to the $x-y$ voltage commands as the outputs of the $x-y$ current control loops. Some experiments were carried out to validate the theoretical investigations. The experimental results showed that the proposed method effectively compensates $x-y$ currents in comparison with the conventional FDR-DTC, while it maintains the fast dynamic response because the firing pulses are still determined using the switching table. In addition, the proposed method does not cause an increase or a decrease in f_{sw} and dc-link realization, respectively, compared to the conventional FDR-DTC.

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Mohammad Hosein Holakooie received the M.Sc. degree from Tabriz University, Tabriz, Iran, in 2013, and the Ph.D. degree from Zanjan University, Zanjan, Iran, in 2018, both in electrical engineering.

He is currently a Researcher with the Institute of Control and Industrial Electronics, Warsaw University of Technology, Warsaw, Poland, within the Ulam Programme supported by the Polish National Agency for Academic Exchange. His research focuses on the control of electric drives.

Grzegorz Iwanski (Senior Member, IEEE) received the M.Sc. degree in automatic control and robotics and the Ph.D. degree in electrical engineering from the Faculty of Electrical Engineering, Warsaw University of Technology (WUT), Warsaw, Poland, in 2003 and 2005, respectively.

From January 2006 to December 2008, he was a Research Worker involved in an international project within the Sixth Framework Programme of the European Union. Since 2009, he has been an Assistant Professor with the Institute of Control and Industrial Electronics, WUT, where he became an Associate Professor in 2019. In 2012/2013, he joined the Renewable Electrical Energy System Team, Universitat Politecnica de Catalunya, Barcelona, Spain, within the framework of the scholarship of Polish Minister of Science and Higher Education. He teaches courses on power electronics, drives, and power conversion systems. He is a coauthor of one monograph, three book chapters, and about 70 journal articles and conference papers. His research interests include variable and adjustable speed power generation systems, photovoltaic and energy storage systems, and automotive power electronics and drives.

Dr. Iwanski provided two plenary lectures on IEEE technically sponsored international conferences: *Ecological Vehicles and Renewable Energies* (EVER 15) and *Joint International Conference on Optimization of Electrical and Electronic Equipment and Aegean Conference on Electrical Machines and Power* (OPTIM-ACEMP 17).

Tomasz Miazga received the B.Sc. and M.Sc. degrees in electrical engineering, in 2012 and 2013, respectively, from the Warsaw University of Technology, Warsaw, Poland, where he is currently working toward the Ph.D. degree in electrical engineering

His research interests mainly include energy processing, renewable energy conversion systems, and dc–dc converters.