An Isolated Soft-Switched High-Power-Factor Rectifier Based on the Asymmetrical Half-Bridge Flyback Converter

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***Abstract*—This article presents the analysis and design of a high-power-factor rectifier that integrates a discontinuous conduction mode operated Boost input cell with an asymmetrical half-bridge flyback converter (AHBFC). The particular connection of the dc–dc stage with the boost cell makes the dc link voltage decrease at light load, thus naturally limiting the switches' voltage stress. A suitable design procedure is described that accounts for the resonant nature of the AHBFC, and allows to calculate all converter parameters to meet the design specifications and to achieve zero-voltage turn-ON for the switches in any operating condition, considering both input voltage and load variations. The theoretical analysis is validated by experimental results taken on a 160 W rated prototype, working at the nominal switching frequency $f_s = 400$ kHz, with a line voltage rms value ranging from 85 to 135 V.**

***Index Terms*—High power factor rectifier, isolated Power Factor Corrector (PFC), soft-switching..**

I. Introduction

ISOLATED high-power-factor rectifiers are usually obtained by cascading a Boost input stage with an isolated dc–dc converter. Such combination yields a very good input power factor, while providing a fast output voltage regulation. The two converters are controlled independently, using the respective degrees of freedom. In the attempt to reduce the number of components and the cost, especially for low–medium power applications, many integrated solutions are proposed in literature that combine a Buck, Boost or a Buck–Boost input cell with an isolated dc–dc stage, sharing the switches. For example, in [1] and [2], a Boost rectifier, operating in *discontinuous conduction mode* (DCM), is combined with a two-switch forward converter. In [1], the input current discharging subinterval is affected by the forward transformer magnetizing current, thus worsening the power factor, while in [2] a ripple-steering concept is applied to the output inductive filter, to smooth the output current. Examples of boost+flyback combinations can be found in [3]–[6], where passive loss-less snubbers and/or auxiliary windings are used to deal with the transformer leakage inductance. However, all these solutions are hard-switching, with the exception of [4], where an auxiliary winding is employed to achieve soft commutations at the cost of a higher input current distortion.

Better performing solutions are those that combine a Boost input stage with a resonant converter, that is exploited to achieve a zero-voltage-switching (ZVS) condition for all switches. This is, in our opinion, the most significant advantage with respect to the cascade configuration, where the boost switch usually operates in hard-switching, unless DCM/CCM borderline operation at variable switching frequency is chosen, and, in any case, with an output voltage higher than twice the peak of the line voltage. Among the different resonant topologies, the most widely adopted is the *LLC* one, combined with an input stage with a standard diode bridge rectifier, as in [7]–[10], or in a bridgeless configuration, like in [11] and [12]. Interleaved boost stages, aimed at reducing the input current high-frequency content, are proposed in [13] and [14], while *continuous conduction mode* (CCM) of the boost stage is also exploited in [15]. Excluding the latter, all the other solutions operate at constant duty-cycle, fixed at 50%, with a variable switching frequency. The main drawback of the *LLC* converter is that, when designed to work in its inductive region to achieve ZVS, its voltage gain decreases when the switching frequency increases. Thus, at light-load, when the switching frequency must be increased to reduce the power drawn from the line, the dc link voltage increases, because of the reduced *LLC* gain, making it very hard to keep the switch voltage stress within acceptable limits. An attempt to solve the problem is found in [16], where a combined pulse frequency/interleaved asymmetric pulsewidth modulation is used to keep the dc link voltage below 500 V with an universal input voltage range. However, it requires the use of a full-bridge *LLC* structure with an interleaved boost cell (three magnetic elements are needed).

Other dc–dc topologies have been proposed, like in [17] and [18], where the DCM boost rectifier (with interleaved configuration as in [17], or bridgeless, like in [18]) is combined with an asymmetrical half-bridge buck topology, where the transformer magnetizing inductance is exploited to achieve ZVS. However, the dc–dc stage has a parabolic gain curve that limits the duty-cycle variation range. A similar topology is proposed in [19], where, compared to [18], the dc–dc stage employs a half-wave rectifier, instead of a full-wave one. A constant line rms voltage was considered and results are reported only at nominal power.

Manuscript received 11 May 2021; revised 2 July 2021; accepted 21 July 2021. Date of publication 10 August 2021; date of current version 9 February 2022. *(Corresponding author: Giorgio Spiazzi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2021.3100975.

Digital Object Identifier 10.1109/TIE.2021.3100975

Both papers neglect the transformer leakage inductance. A resonant converter with a modified input impedance was presented in [20], that operates at discrete switching frequencies, with a variable duty-cycle. The aim was to reduce the dc link voltage variation, with the drawback of an asymmetrical operation of the resonant converter. Other input stage topologies were proposed as well, as in [21] and [22], where a buck-type rectifier was combined with an isolated flyback dc–dc stage. The buck-type input stage facilitates the design for universal input voltage, and the typical dead zone in the line current can be removed with a series-connected energy buffer, as in [22]. However, the transformer leakage inductance and the hard-switching condition severely limit the applicability of these configurations. A buck–boost input stage was exploited in [23]–[25], combined with a flyback, *LLC* and *CLCL* dc–dc topologies, respectively. Only the last two papers, that employ resonant dc–dc converters, are able to achieve soft-switching, but at the expense of a more complicated structure ([25] needs four magnetic elements).

The asymmetrical half-bridge flyback converter (AHBFC) has been proposed in [26], combined with coupled input inductors and two filter capacitors connected to the switching node. An improved version of the abovementioned topology appeared in [27], including an additional input inductance, besides the coupled input inductors, and synchronous rectification at the output of the dc–dc stage. Both solutions achieve a continuous input current, but with a parabolic input power function that limits the maximum duty-cycle to 50%, impeding the full exploitation of the dc–dc stage. Moreover, the resonant nature of the dc–dc stage is neglected. Another application of the AHBFC, integrated with a DCM-operated Buck-type rectifier, was proposed in [28] and [29] for high power factor ac–dc applications. While the solution in [28] presents the typical dead zone in the line current of buck-type rectifiers, the circuit proposed in [29] achieves a better power factor by introducing a series-connected energy buffer, as was done in [22]. However, both schemes present high conduction losses of the input stage, being the input current forced to flow through the series combination of a diode and a switch, besides the two input bridge diodes. Obviously, this adversely affects the overall conversion efficiency that, despite the achieved soft switching, remains below 85% in the whole input voltage and load range.

This article proposes a high-power-factor rectifier built combining a DCM-operated Boost input stage with an AHBFC. Its main outcomes include: 1) a detailed converter design procedure that, taking advantage of the resonant nature of the AHBFC, guarantees the ZVS for both switches in the whole input voltage and load range; 2) a simple feed-forward control of the switching frequency, based on the line rms voltage, to reduce the needed duty-cycle variation; 3) the experimental proof of a high power factor obtained keeping a constant switching frequency and duty-cycle in the line half period, with a limited and well controlled maximum dc link voltage, over the whole load range.

The article is organized as follows. Section II describes the converter operation, while the design procedure is outlined in Section III. Experimental results, from a 160 W prototype, are discussed in Section V and shown to confirm the theoretical analysis, reaching the expected performance. Section VI concludes this article.

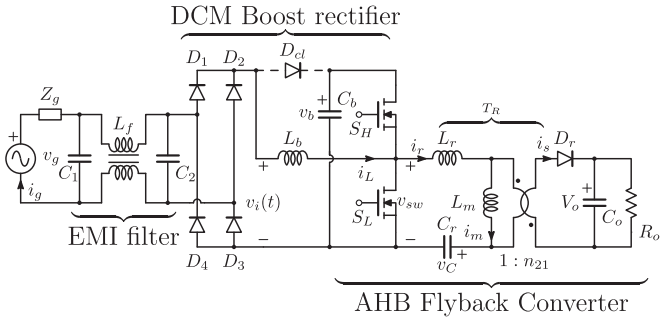

Fig. 1. Schematic of the high quality rectifier built integrating a boost cell with an AHBFC.

II. Description of Converter Operation

The proposed isolated PFC is shown in Fig. 1. The input voltage is $v_g(\theta) = V_{g_{pk}} \sin(\theta) = \sqrt{2} V_g \sin(\theta)$, with $\theta = \omega_g t$. The particular connection of the AHBFC cell makes its duty-cycle d_c, which refers to the turn-ON interval of the upper switch S_H, equal to the complement of the boost cell duty-cycle d_b, i.e., $d_c = 1 - d_b$. The reason of such connection will become clear during the explanation of the converter behavior. As well known, in order to obtain a reasonable power factor at a constant duty-cycle and switching frequency, the boost cell must be designed to operate in DCM. The main converter waveforms in a switching period, taken around the peak of the line voltage, are reported in Fig. 2 for two different AHBFC operating regions. As a result of the chosen design criteria, that aim to fully exploit the resonant nature of the dc–dc stage, DCM operation happens at the minimum line rms voltage, while CCM characterizes the operation at the maximum line rms voltage, both at nominal power (here, CCM means that the rectifier diode D_r conducts at least for the entire $(1 - d_c)T_s$ subinterval). As we will see in the converter analysis, CCM operation is likely to occur at light-load too. This converter, in a switching period, cycles through the subtopologies illustrated in Fig. 3. The sequence depends on the operating mode of the AHBFC stage: for the DCM example of Fig. 2(a) the cycled subtopologies are *b–c–d–e–d*; for the CCM example of Fig. 2(b) the cycled subtopologies are *a–b–c–e*.

A. DCM Boost Analysis

Considering a generic switching period inside the line half-cycle and assuming a constant dc link voltage $v_b(t) \approx V_b$, the inductor current has a triangular waveshape (see Fig. 2), with $I_{L_{pk}} = \frac{|v_g|}{L_b} d_b T_s$. With respect to the boost cell only, three subintervals can be identified. It is important to observe that the subinterval $(1 - d_b - d_b')T_s$ is caused by the turn-OFF of the input bridge diodes, since the boost cell operates with a synchronous rectification (thanks to the upper switch S_H). This fact has important practical consequences, besides forcing the use of fast input diodes (please, refer to Section V for further discussion of this point).

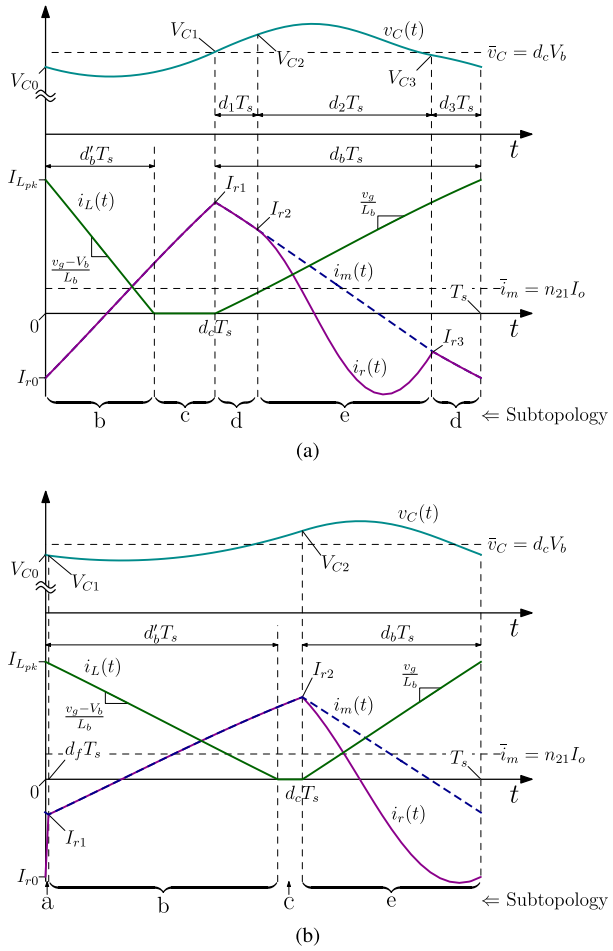

Fig. 2. Main converter waveforms in a switching period taken around the peak of the line voltage: (a) example of DCM operating mode ($V_{g\min}$); (b) example of CCM operating mode ($V_{g\max}$).

Indicating with $m_B = V_b/V_{g_{pk}}$ the boost voltage gain, it is easy to recognize that, for a correct DCM operation of the boost cell, the following condition must be satisfied at any time:

$$m_B = \frac{V_b}{\sqrt{2}V_g} > \frac{1}{1-d_b}. \tag{1}$$

Now, considering the inductor *flux balance* for which $|v_g|d_b = (V_b - |v_g|)d_b'$, the average inductor current in a switching period is given by:

$$\bar{i}_L(\theta) = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt = \frac{d_b^2}{2L_b f_s}\frac{m_B V_{g_{pk}}|\sin(\theta)|}{m_B - |\sin(\theta)|}. \tag{2}$$

Only if $m_B \to \infty$ the average inductor current becomes proportional to the input voltage, thus achieving, in principle, a unity power factor. In all the other cases, low-frequency distortion appears, and the power factor is lower than one.

The average input power is given by

$$P_g = \frac{1}{\pi}\int_0^{\pi} v_g(\theta)\bar{i}_L(\theta)d\theta = \frac{d_b^2 V_{g_{pk}}^2}{2\pi f_s L_b}\int_0^{\pi}\frac{m_B \sin^2(\theta)}{m_B - |\sin(\theta)|}d\theta = \frac{d_b^2 V_g^2}{f_s L_b} f(m_B) \tag{3}$$

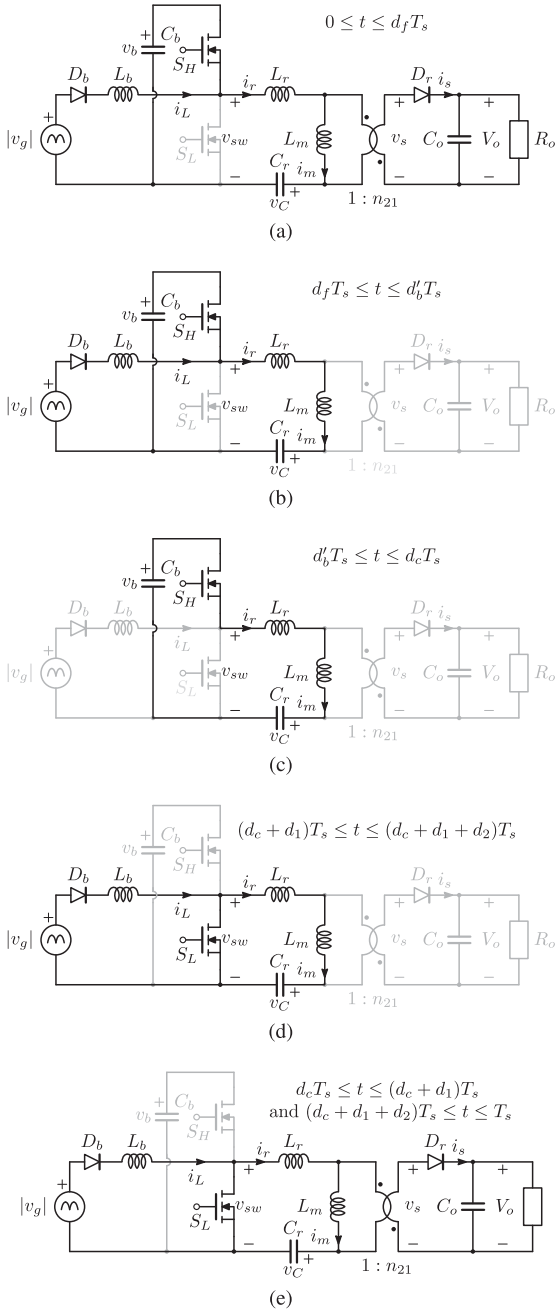

Fig. 3. Subtopologies in a switching period: (a) interval $0 \le t \le d_fT_s$; (b) interval $d_fT_s \le t \le d_b'T_s$; (c) interval $d_b'T_s \le t \le d_cT_s$; (d) intervals $d_cT_s \le t \le (d_c + d_1)T_s$ and $(d_c + d_1 + d_2)T_s \le t \le T_s$; (e) interval $(d_c + d_1)T_s \le t \le (d_c + d_1 + d_2)T_s$.

with

$$f(m_B) = \frac{m_B^3}{\sqrt{m_B^2 - 1}}\left[1 + \frac{2}{\pi}\arctan\left(\frac{1}{\sqrt{m_B^2 - 1}}\right)\right] - \frac{2}{\pi}m_B - m_B^2. \tag{4}$$

Analyzing (3), we see that, when the output power reduces, the duty-cycle must be reduced and/or the switching frequency must be increased in order to maintain the input/output power

balance. An alternative would be to increase the boost inductance L_b, by using a variable inductor arrangement, but at the cost of a much more complex inductor construction. When the boost cell is integrated with a dc–dc stage, no matter which topology is used, it shares the same control variables, i.e., duty-cycle and switching frequency. However, these control variables are now used to regulate the output voltage of the dc–dc stage, leaving the dc link voltage V_b uncontrolled, i.e., a function of the converter operating point. If $m_{DC} = V_o/V_b = g(d_c, P_o, f_s)$ is the voltage gain of the dc–dc stage, that can be, in general, a function of duty-cycle, load, and switching frequency, the combined Boost+dc–dc stage must obey the following system of equations:

$$\begin{cases} \dfrac{d_b^2 V_g^2}{f_s L_b} f\left(\dfrac{V_o}{\sqrt{2}V_g m_{DC}}\right) - \dfrac{P_o}{\eta} = 0 \\ m_{DC} = g(1-d_b, P_o, f_s) \end{cases} \tag{5}$$

where η is the estimated overall conversion efficiency, and the relation $d_c = 1 - d_b$ was used. For a given set of parameters P_o, V_g, and f_s, (5) allows to find the corresponding boost duty-cycle d_b, as well as the dc link voltage V_b.

Differently from the *LLC* converter, the voltage gain of the AHBFC increases with its control variable, i.e., with duty-cycle d_c.[1] At light-load, the boost duty-cycle d_b must decrease, to account for the reduced transferred power: the consequent increase of the AHBFC duty-cycle $d_c = 1 - d_b$, forces a reduction of the dc link voltage ($V_b = V_o/m_{DC}$). This is the reason why the AHBFC cell was connected in parallel to the bottom switch in Fig. 1 and not to the upper switch. The opposite choice would indeed lead to an unacceptable increase of the dc link voltage at light-load. At the same time, the decrease of d_b at light-load makes it easier to satisfy constraint (1).

B. AHBFC Analysis

As stated in the previous section, the solution of (5) requires the knowledge of the voltage gain expression of the dc–dc stage. The analysis of the AHBFC, taking into account its resonant behavior, was recently proposed in [30]. Here, only the main outcomes of such analysis are reported. Considering a *steady-state* condition, the inductors' *volt–second* balance and the capacitors' *charge* balance yield the following relations:

$$\begin{cases} \bar{v}_C = \bar{v}_{sw} = d_c V_b & \text{inductor flux-balance} \\ \bar{i}_r = 0 & \text{resonant capacitor charge-balance} \\ \bar{i}_m = n_{21}\bar{i}_s = n_{21} I_o & \text{capacitors charge-balance} \end{cases} \tag{6}$$

The third equation is a unique property of the proposed topology, consequence of the half-wave rectification, which makes the switched current values load-dependent, thus affecting the switches' ZVS condition. Two different resonant tanks are involved, depending on the rectifier diode D_r state, whose parameters are as follows:

$$\begin{cases} Z_r = \sqrt{\dfrac{L_r}{C_r}},\ \omega_r = \dfrac{1}{\sqrt{L_r C_r}} & D_r \text{ is ON}, \\ Z_{ro} = \sqrt{\dfrac{L_r + L_m}{C_r}},\ \omega_{ro} = \dfrac{1}{\sqrt{(L_r + L_m) C_r}} & D_r \text{ is OFF}. \end{cases} \tag{7}$$

The inductance ratio $\lambda = L_r/L_m$ will also be used in the following. If the voltage across capacitor C_r has a negligible ripple, piece-wise linear current waveforms are obtained, and the converter is likely to operate in CCM. In this case, the AHBFC behaves essentially like an isolated Buck converter, showing a voltage gain proportional to the duty-cycle. In fact, neglecting the small subinterval $d_f T_s$ in Fig. 2(b), the *volt–second* balance of the magnetizing inductance yields

$$\frac{(1-d_c)V_b}{1+\lambda} d_c \approx \frac{V_o}{n_{21}}(1-d_c) \quad \rightarrow \quad m_{DC}^{ideal} = \frac{V_o}{V_b} = \frac{n_{21}}{1+\lambda} d_c. \tag{8}$$

However, as demonstrated in [30], when the resonant voltage $v_C(t)$ has a non-negligible ripple, as for the case of Fig. 2, the above relation fails to correctly predict the converter behavior. A more precise equation, valid for CCM operation [i.e., for the waveforms of Fig. 2(b)], is

$$m_{DC}^{(CCM)} = \frac{V_o}{V_b} = m_{DC}^{ideal} \left(\frac{1}{\dfrac{d_c(1-d_c)}{k_1} + m_{DC}^{ideal} \dfrac{k_2}{n_{21}}} \right) \tag{9}$$

with coefficients k_1 and k_2 given by

$$k_1 = \frac{f_s}{\omega_{ro}} \frac{\sin(\beta)(1-\cos(\alpha))}{1-\cos(\alpha)\cos(\beta)} \tag{10}$$

$$k_2 = 1 + \frac{n_{21}^2 Z_r}{R_o}\left[1 + R_N(1-d_c)\right] \frac{\sin(\alpha)}{1-\cos(\alpha)} + \frac{n_{21}^2 Z_{ro}}{R_o}\left[1 - R_N(1-d_c)\right] \frac{(1+\cos(\alpha))\,(1-\cos(\beta))}{\sin(\beta)\,(1-\cos(\alpha))}. \tag{11}$$

In these expressions, $R_N = \frac{R_o}{2 n_{21}^2 L_m f_s}$ is the normalized load resistance, $\alpha = \omega_r(1-d_c)T_s$, and $\beta = \omega_{ro} d_c T_s$. Only two approximations have been used in the derivation of (9): subinterval $d_f T_s$ in Fig. 2(b) is neglected, and the magnetizing current waveform is assumed to be perfectly triangular.

The comparison of (9) with simulation and experimental measurements shows a good match. With respect to the ideal voltage gain m_{DC}^{ideal}, the resonant operation increases the gain and shows a nonmonotonic behavior that limits the maximum duty-cycle the converter can work with.[2] This limit increases when the load resistance is reduced.

Far from this maximum duty-cycle value, the voltage gain turns out to be practically independent of the load. However, it shows some dependency on the switching frequency and, in particular, it decreases when the switching frequency increases.

[1] This is true up to a maximum duty-cycle value, above which the voltage gain starts decreasing, exhibiting a non monotonic behavior. However, as will be shown in the following, duty-cycle d_c can be limited within the monotonic region with no performance penalization.

[2] The limitation is effective only when the duty-cycle is closed loop regulated, because, in that case, the inversion of the gain slope determines a positive feedback effect, which destabilizes any controller.

TABLE I
CONVERTER SPECIFICATIONS

Parameter	Symbol	Value	
Minimum line RMS voltage	$V_{g_{min}}$	85	V
Nominal line RMS voltage	V_g	110	V
Maximum line RMS voltage	$V_{g_{max}}$	135	V
Nominal output voltage	V_o	160	V
Nominal output power	P_o	160	W
Minimum output power	$P_{o_{min}}$	40	W
Switching frequency	f_s	$400 \pm 25\%$	kHz

TABLE II
AHBFC PARAMETERS

Parameter	Symbol	Value	
Resonant inductance	L_r	6.2	μH
Magnetizing inductance	L_m	55.4	μH
Resonant capacitor	C_r	2×8.2	nF
DC link capacitor	C_b	2×10	μF
Transformer turns ratio	$n_{21} = N_2/N_1$	18/23	
Output capacitor	C_o	680	μF

We will exploit this property to reduce the duty-cycle variation needed to cope with the input voltage variation in the specified range (see Table I).

III. PROPOSED DESIGN PROCEDURE

In this section, we describe the converter design procedure, that is carried on referring to the specifications listed in Table I and derived from a line-fed, solid-state lamp driver test-case.The design objectives are as follows:

1) Guaranteeing DCM operation of the boost cell in any condition (⇒ the minimum dc link voltage is bounded).
2) Limiting the maximum switch voltage stress (⇒ the maximum dc link voltage is bounded).
3) Limiting the switching frequency variation.
4) Guaranteeing a ZVS turn-ON for both switches in any condition, while minimizing the conduction losses.

1) Selection of the Nominal Operating Point: The first step involves the selection of the nominal operating point in terms of input and dc link voltage, output power, and Boost duty-cycle. While the first and the third parameters come from the converter specifications of Table I, the other two affect all the design outcomes, as it will become clear shortly. Selecting the nominal Boost duty-cycle at $d_b = 0.5$, the minimum dc link voltage for DCM operation of the boost cell, from (1)), is 311 V. We select $V_b = 370$ V, to keep enough margin also in different operating points.

2) Calculation of the Boost Inductance: The boost inductor is calculated based on the desired output power, i.e., from the power balance $\eta P_g = P_o$, where η is the estimated conversion efficiency. Using the nominal operating point in (3), assuming $\eta = 0.94$, the required inductance is $L_b = 35$ μH.

3) Calculation of the DC Link Capacitance: The value of the dc link capacitor C_b can be estimated based on the desired residual low-frequency ripple. To this purpose, the integrated Boost+AHBFC can be considered equivalent to the cascade connection of a Boost stage and a dc–dc stage, for which the dc link capacitance is in charge of filtering the twice-the-line frequency power fluctuation caused by an almost sinusoidal input current absorption. The average current absorbed by the dc–dc stage can be approximated as $I_{in}^{\mathrm{DC}} \approx P_o/V_b = 0.43$ A, at the nominal operating point, with $V_b = 370$ V. Consequently, imposing a desired peak-to-peak voltage ripple of $\Delta V_b = 60$ V, the needed capacitance value turns out to be $C_b = \frac{I_{in}^{\mathrm{DC}}}{\omega_g \Delta V_b} = 23$ μF. The selected value was $C_b = 2 \times 10$ μF, so as to have the possibility of using two paralleled film capacitors instead of an electrolytic one.

4) Calculation of the AHBFC Parameters: This is the key point in the design phase. The resonant tank parameters L_r, L_m, C_r and the transformer turns ratio n_{21}, are derived by imposing the DCM/CCM boundary condition at the nominal operating point. This is the most favorable operating point for the AHBFC, with minimum devices' rms current and soft rectifier diode turn-off. At this boundary condition, each switching period contains only two topological states $d_c T_s$, and $(1 - d_c)T_s$, i.e. $I_{r0} = I_{r1}$, $V_{C0} = V_{C1}$, in Fig. 2(b). The solution is found numerically, building a system of seven equations made-up by four relations exploiting the continuity property of state variables $i_r(t)$ and $v_C(t)$, plus the three constraints (6). However, there are eight unknowns, i.e., the four state variable values V_{C1}, V_{C2}, I_{r1}, I_{r2}, and the four converter parameters L_r, L_m, C_r, n_{21}. Thus, we can use one of the two current values, that affect the ZVS turn-ON of the switches, to set an additional constraint. Please note that, while the ZVS turn-ON of the upper switch S_H is facilitated by the Boost inductor peak current $I_{L_{pk}}$, which sums with $I_{r0} = I_{r1}$, the ZVS turn-ON of the bottom switch S_L depends entirely on I_{r2} [see Fig. 2(b)], since, at the end of the upper switch conduction interval, the boost current $i_L(t)$ is always zero, if the boost cell is correctly operating in DCM. For this reason, the current value I_{r2} can be imposed as a constraint. However, the nominal operating point is not the worst case scenario for S_L ZVS condition, which happens at light load. In fact, assuming an almost triangular current waveform, the peak magnetizing current is estimated as

$$I_{r2} \approx \bar{i}_m + \frac{\Delta i_{m_{pp}}}{2} = n_{21}\frac{V_o}{R_o} + \frac{V_o}{2n_{21}L_m f_s} d_b. \tag{12}$$

At light load, both I_o and d_b are at minimum [d_b decreases to reduce the power drawn from the line, see (3)]. This is to explain why the selected I_{r2} value at the nominal operating point must be much higher than the minimum value that guarantees the ZVS condition for the bottom switch. The initial guessed values for the seven unknowns were calculated according to the procedure described in [30]. The solver returned the following values: $L_r = 6.17$ μH, $L_m = 55$ μH, $C_r = 16.1$ μF, $n_{21} = 0.806$. The values used in the experimental prototype, are listed in Table II, and are pretty close to the calculated ones.The simulation of the AHBFC, at the nominal operating point, shows a condition quite close to the DCM/CCM boundary, with $d_f = d_3 = 0$, but with a small $d_1 T_s \approx 160$ns, which is less than 7% of the switching period.

5) Check for the Boost DCM Condition at the Maximum Line rms Voltage: The calculation of the Boost duty-cycle and the dc link voltage at $V_{g\max}$ requires to find a solution for the system (5). Since d_b becomes lower than 50%, i.e., the value corresponding to the nominal input voltage, $d_c = 1 - d_b$ will increase, thus making the AHBFC enter the CCM region. In order to limit the maximum d_c value in this condition, and avoid working too close to the maximum of the AHBFC voltage gain curve, we decided to increase the switching frequency to $f_{s\max} = 500\,\text{kHz}$. Using (9) into (5), and solving numerically the system, we found $d_b = 0.413$, and $V_b = 350$ V, higher than the minimum value required for DCM operation of the Boost cell ($V_{blim} = 325$ V).

6) Check for the Boost DCM Condition at the Minimum Line rms Voltage: At the minimum line rms voltage, the Boost duty-cycle increases above 50%, causing the AHBFC to operate in DCM, where (9) is no longer valid. To solve this problem, the voltage gain in the DCM region was investigated following the same approach used in [30]. Essentially, a brute-force approach was used, consisting in numerically solving, in a MATLAB™ script, a nonlinear system of 11 equations with unknowns $[V_{C0}, V_{C1}, V_{C3}, I_{r0}, I_{r1}, I_{r2}, I_{r3}, d_1, d_2, f_s, V_o]$, for a given dc link voltage V_b and load resistance. The value of V_{C2} is not listed in the unknowns as it is a function of the output voltage only, being equal to the voltage at which D_r becomes forward polarized. The equations come from the continuity property of state variables $v_C(t)$ and $i_r(t)$ [four equations each, for the four subintervals in Fig. 2(a)], plus the three steady-state equations in (6). The convergence was assured by starting with guessed values obtained in the design phase considering the boundary DCM/CCM operating point, and then reducing the duty-cycle in small steps assigning, as guessed values for a new iteration, the values obtained from the previous one. Once again, to limit the duty-cycle variation, the switching frequency was reduced to $f_{s\min} = 300\,\text{kHz}$. Then, a quadratic equation was used to fit the curve obtained with the procedure outlined above, with the following coefficients $m_{DC}^{(DCM)} = -0.58d_c^2 + 0.13d_c - 0.025$. This equation has been used in (5), yielding $d_b = 0.606$, and $V_b = 403$ V (with $\eta = 0.94$). A simulation of the whole converter gave $d_b = 0.605$, with $V_b = 383$ V. The minimum dc link voltage for DCM operation of the boost stage is 305 V.

7) Check for the ZVS Condition at the Minimum Power and Maximum Line rms Voltage: At a reduced output power, the boost duty-cycle must decrease to maintain the input/output power balance, and the reduction is deeper at the maximum line rms voltage. Once again, we decided to increase the switching frequency to $f_{s\max} = 500\,\text{kHz}$ in order to mitigate the duty-cycle variation. Solving (5) for the minimum power, we obtained $d_b = 0.17$, with $V_b = 322$ V. The values obtained in simulation, in the same operating point, are $d_b = 0.2$, with $V_b = 296$ V. The DCM operation of the Boost stage is still satisfied, being the minimum dc link voltage, from (1), equal to 230 V.

If one of the checks about the DCM operation of the boost cell fails, the nominal dc link voltage V_b that was chosen at the beginning of the procedure, should be increased. Similarly, if the switched current at light load is not sufficient to guarantee a correct ZVS condition for all the switches, the constraint I_{r2} selected at step 3 should be increased, yielding a consequent reduction of the magnetizing inductance.

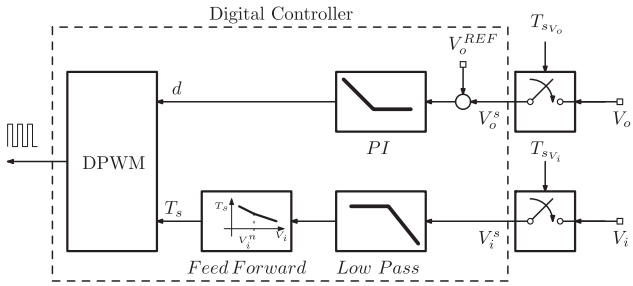

Fig. 4. Block scheme of the implemented digital controller. Rectified input voltage and output voltage are sampled and used to regulate duty-cycle and switching period, respectively.

It is important to observe that, with the proposed topology, it is not possible to handle a universal input voltage range, because that would require a too wide variation of both the control parameters, namely duty-cycle and switching frequency, with consequent difficulties in guaranteeing the ZVS condition for all the operating points.

Finally, we would like to clarify that the choice of varying the switching frequency to accommodate more easily input voltage and load variations was done to exploit all possible degrees of freedom of this topology, but is not strictly necessary. One could first try to design the converter keeping the switching frequency constant, if the required duty-cycle variation is acceptable.

IV. Control Implementation

The rectifier circuit is digitally controlled by a low-cost microcontroller (STM32F334R8), following the scheme illustrated by Fig. 4. As can be seen, two control parameters are simultaneously used to steer the converter operating point: the duty-cycle d and the switching period T_s. The former is regulated by a standard proportional-integral (PI) controller, designed to achieve the target control bandwidth, $\ll 100$Hz, so as to minimize the input current distortion, with an adequate phase margin $> 60°$. The sampling period of the output voltage is set to $T_{sV_o} = T_s/20$. The switching period, instead, is slowly adjusted to the measured value of the rectified input voltage (iteration frequency is in the $15 - 250$Hz range, i.e. $T_{sV_i} = T_{sV_o}/1000$), in a feed-forward manner. This requires a piece-wise linear map to be implemented in the microcontroller firmware, whose parameters are then iteratively tuned to compensate the undesired effect of input voltage variations on voltage V_b. As will be shown in Section V, this organization allows to effectively minimize the variation of voltage V_b in the considered input voltage range.

V. Experimental Results

The schematic of the implemented prototype is illustrated in Fig. 1, where Z_g models the line impedance. It employs four bridge diodes STTH803 and two MOSFETs STB26N60M2, all from STMicroelectronics™, while the rectifier SiC diode is the model IDD03SG60 C from Infineon™. A silicon device could be used as well but, in any case, the voltage rating needs to be

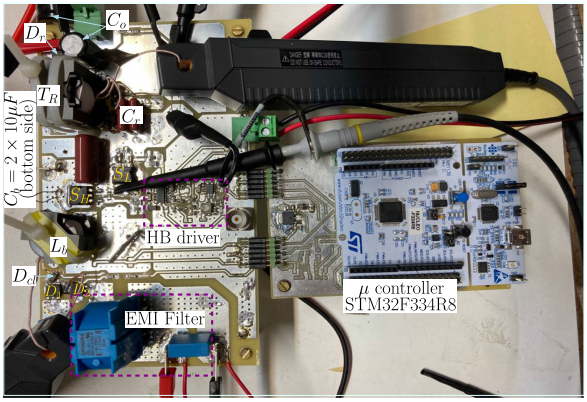

Fig. 5. Photo of the implemented prototype where the main components are highlighted.

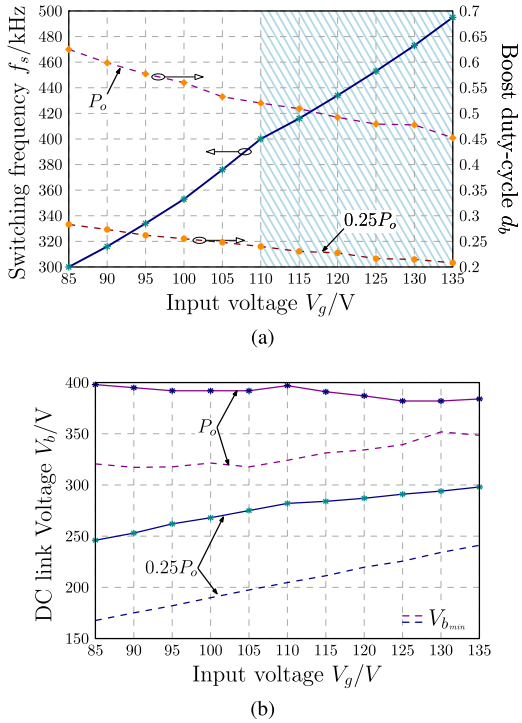

Fig. 6. Steady-state converter characterization as a function of the input rms voltage for minimum and nominal output power values: (a) switching frequency and boost duty-cycle d_b; (b) dc link voltage variation and minimum value given by (1) (dashed lines).

higher than the theoretical diode voltage stress because of the ringing that occurs at its turn OFF when the converter operates in CCM. In fact, the high di/dt the rectifier diode experiences, during subinterval $d_f T_s$ in Fig. 2(b), is likely to excite high frequency oscillations between the device's parasitic capacitance and the transformer secondary leakage inductance, with a consequent increase of the diode voltage stress (see Fig. 9 in [30]). The transformer has been realized with a PQ 26/25 magnetic core (material N49), with primary and secondary windings made by 23 and 18 turns, respectively, both using a Litz wire (bundle of 200 strands, having each a diameter of 50 μm). The values obtained for the magnetizing inductance and the total primary side leakage inductance are reported in Table II, measured at 400 kHz with the Agilent 4294 A precision impedance analyzer. Please note that no additional external inductor has been used, the only resonant element being the transformer leakage inductance. The input inductor was built on an RM10 core (material N49), using 20 turns of the same Litz wire. The obtained value was $L_b = 38.8$ μH, slightly higher than the calculated one. A simple EMI filter was used, that includes a common mode choke (2×3.3mH), having a leakage inductance of roughly 33 μH, and two capacitors ($C_1 = 100$ nF, $C_2 = 0.92$ μF). The dc link capacitor was selected as $C_b = 2 \times 10$ μF, film type. The output filter capacitor is $C_o = 680$ μF. This value was selected to attenuate the unavoidable line frequency ripple in the output voltage for testing the converter with an equivalent resistive load. However, if the final application is for solid-state street lamps, electrolytic capacitors should be avoided. This can be obtained by allowing a higher line-frequency ripple that will be attenuated by the LED current controller stage, like in [12], where a Twin-Bus Buck output stage was employed. The photo of the implemented prototype is visible in Fig. 5: the main passive/active components are highlighted. The converter was initially tested to verify the proposed deign procedure: Fig. 6(a) shows the implemented feedforward variation of the switching frequency and the corresponding range of the boost duty-cycle, as a function of the input rms voltage and for minimum and nominal output power values. The corresponding variation of the dc link voltage is visible in Fig. 6(b): the maximum voltage results bounded below 400V, and reduces at light load, as expected. Moreover, the measured value is well above the minimum value given by (1) (see dashed lines), so that DCM operation of the boost cell is always guaranteed.

Fig. 7(a) displays the line voltage and current taken at the nominal operating point ($V_g = 110$ V_{rms}, $V_o = 160$ V, $R_o = 160$ Ω, $f_s = 400$ kHz, $d_b = 0.52$,). The dc link voltage is also visible, its ripple being around $\Delta v_b \approx 55$ V, with an average value $V_b = \bar{v}_b \approx 380$ V. These values are quite close to the outcomes of the proposed design procedure, with minor discrepancies caused by the converter losses. The details of main converter waveforms recorded at the peak of the line voltage are visible in Fig. 7(b): the AHBFC is operating nearly at the DCM/CCM boundary, in agreement with the design choice, and ZVS is easily achieved, considering the 200 ns dead-time in the driving signals. The line current crossover distortion, visible in Fig. 7(a), deserves a deeper discussion, and it is related to the clamping diode D_{cl}, visible in Fig. 1 with dashed connections. As mentioned in Section II, the discontinuous boost current is caused by the turn-OFF of the two bridge diodes that are conducting in the considered line half cycle. When they turn OFF, after interval $d_b' T_s$ in Fig. 2, the bridge diodes' parasitic capacitance resonates with the boost inductor, causing voltage $v_i(t)$ to oscillate around the dc link voltage. Since this resonant tank has virtually no damping, the peak voltage reaches almost twice the dc link value, increasing the diode voltage stress and causing EMI problems (the measured resonance frequency was 3.3 MHz). Diode $D_{\rm cl}$ solves the problem by clamping the voltage $v_i(t)$ to the dc link voltage V_b, with two consequences:

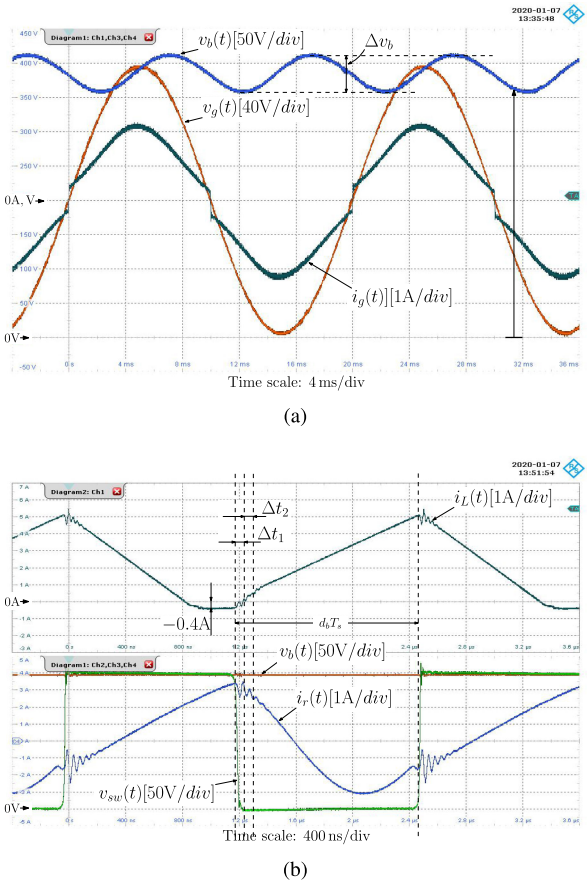

Fig. 7. Main waveforms at the nominal operating point ($f_s = 400$ kHz): (a) line voltage and current; (b) detail of converter waveforms at the peak of the line voltage.

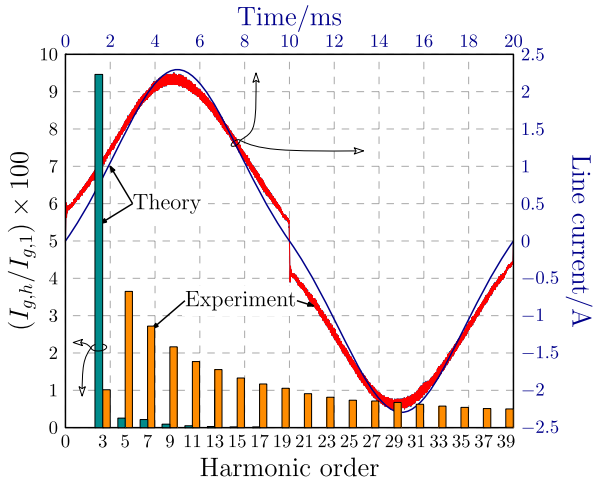

Fig. 8. Analysis of the measured line current at the nominal operating point, compared with the theoretical expression (2): time domain waveforms (upper/right axes in blue); harmonic content, in percentage of the fundamental component (bottom/left axes in black).

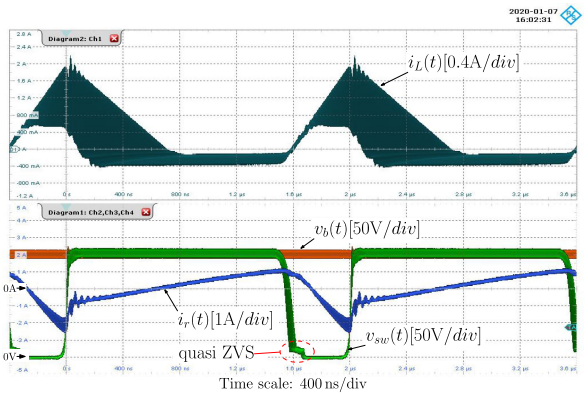

Fig. 9. Main waveforms at $V_{g_{\max}}$ and $P_o = 40$ W. Please note that the inductor current waveform is amplitude modulated at twice the line frequency.

the first is a slightly negative (roughly 400 mA) boost inductor current during subinterval $(1 - d_b - d'_b)T_s$, that flows through D_{cl} and S_H sustained by the small voltage drop across these two components [see Fig. 7(b)]; the second effect causes the mentioned crossover distortion in the input current. In fact, when the bottom switch S_L turns ON, the inductor current starts to rise, initially, with a higher slope because the clamping diode is still *on*. When $i_L(t)$ becomes positive, after the small interval Δt_1 in Fig. 7(b), D_{cl} turns OFF, and the resonance between L_b and the bridge diodes' parasitic capacitance discharges the latter. Only when voltage $v_i(t)$ drops below $|v_g(t)|$, after another small interval Δt_2, two bridge diodes turn ON and the current slope becomes $|v_g(t)|/L_b$, as it should be. This initial transient is independent of the line voltage instantaneous value, meaning that the inductor current is nonzero even during the line voltage zero crossing, which causes the distortion visible in Fig. 7(a).

It is interesting to analyze the effect of this crossover distortion on the input current harmonic content. In Fig. 8, we can see the comparison between the measured and the theoretical line current, in terms of waveform and harmonic content. The waveforms reveal a slight shift of the measured current peak due to the nonnegligible ripple of the dc link voltage $v_b(t)$ [see Fig. 7(a)], while the harmonic content shows that the crossover distortion is almost entirely canceling the third harmonic component, while increasing the higher order harmonics, compared with the theoretical expectations. In any case, the harmonic content is well below the IEC 61 000-3-2 limits, relative to *Class C* (lighting equipment).

The light-load condition at the maximum line rms voltage was tested as well, and Fig. 9 shows the main converter waveforms taken in two switching periods ($f_s = 500$ kHz): the dc link voltage is around 300 V, with $d_b = 0.24$, once again values well predicted in the design phase. Quasi ZVS is achieved for the bottom switch, because the switched current, which is around 1 A, is able to discharge almost completely the switching node capacitance (down to ≈ 20 V). This behavior reflects the strong nonlinearity of the MOSFETs' output capacitance of the chosen devices, that increases more than two orders of magnitude when their V_{DS} voltage approaches zero. As expected, at light-load, the AHBFC operates deeply in CCM.

The comparison of the proposed rectifier with state-of-the-art Boost+*LLC* solutions (refs. [11] and [12]) and with the recent rectifier application [29] of the AHBFC is shown in Table III.

TABLE III
COMPARISON WITH STATE-OF-THE-ART INTEGRATED AC–DC TOPOLOGIES WITH SIMILAR COMPLEXITY

Condition	V_g	V_o	$P_{o_{nom}}$	f_s @$P_{o_{nom}}$	PF	THD	η @$P_{o_{nom}}$	ΔV_b @$P_{o_{nom}}$	ΔV_b @$0.25P_{o_{nom}}$	Magnetics N°/Vol
Paper	[V_{RMS}]	[V]	[W]	[W]		[%]		[V]	[V]	mm^3
Ref [11]	$100-120$	36	144	$120\pm?$	>0.99	$\approx 6-8$	$92.4-92.9$	$216-340$	not given	3/?
Ref. [12]	$90-135$	50	100	$62-125$	>0.99	$5.5-7$	$92.8-94.5$	$256-450$	not given	3/23240
Ref. [29]	$90-264$	19	100	100	0.97	not given	<85	<260	<260	2/20880
Proposed	$85-135$	160	160	$300-500$	0.997	$\approx 6-7$	$87-90$	$380-400$	$246-300$	2/10850

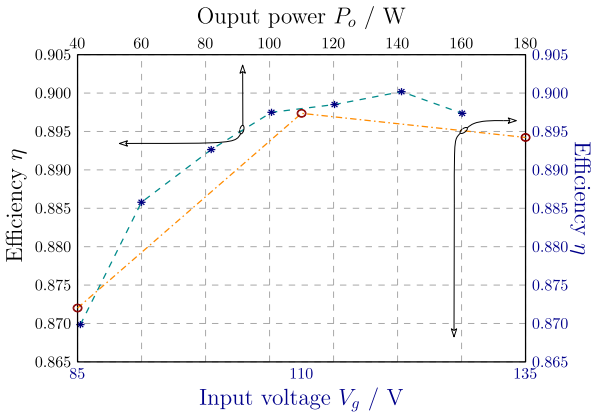

Fig. 10. Measured power stage efficiency: at nominal input/output voltage values for variable output power (top/left axes); at nominal output power for different input voltage rms values (bottom/right axes).

Based on these data, we can make the following considerations: 1) for fixed load applications, the Boost+*LLC* converter operating at constant 50% duty-cycle and variable switching frequency is probably the best solution, mainly because of the possibility to employ a bridgeless configuration, with a significant reduction of the input stage losses; 2) universal input voltage range can best be handled by a buck-type input rectifier, as in [29], with a penalty in the overall efficiency mainly caused by the need for the input energy buffer to get rid of the input current dead zone. However, as far as the Boost+*LLC* rectifiers are concerned, even at nominal load, in order to cope with the considered input voltage variation, the switching frequency needs to change by a factor higher than 2, with a significant variation of the dc link voltage. In both refs. [11] and [12] no information is given in terms of switching frequency and dc link voltage variation when the output power is reduced (ref. [12] reports only the efficiency curve as a function of the output power for $V_g = 120\,V_{rms}$). It is important to consider that the ZVS condition must be ensured at the maximum switching frequency (where, unluckily, the maximum dc link voltage occurs).

The measured power stage efficiency of the proposed topology is reported in Fig. 10: as we can see, it reflects the higher conduction losses of the input bridge rectifier, compared with bridgeless solutions, and the chosen switching frequency, much higher than in similar prototypes presented in literature. Please note that, despite the measured efficiency is lower than the guessed value used in the converter design (see point 2 in Section III), the prototype proved to be able to achieve the desired nominal output power, with no need for further design iterations.

On the other hand, we believe that the major advantage of these integrated rectifiers, compared with a cascade configuration, relies exactly on the possibility to reduce the overall magnetic volume (EMI filter included) by increasing the switching frequency, while maintaining the ZVS condition, i.e., a reasonable efficiency. From this standpoint, let us compare the number and the total volume of the magnetic components (EMI filter not considered) reported in the last column of Table III: [11] does not give information about the magnetic core used, but it employs three magnetic elements, just like in [12], where the inductors of the twin-bus buck LED current controllers were not considered, for a fair comparison. Huang *et al.* [29] employed only two magnetic elements, like our proposal, but the magnetic volume is almost twice, due to the much lower switching frequency.

As a last comment, Table III shows that load variations are better managed by the proposed topology, for which the dc link voltage decreases at light load.

VI. CONCLUSION

In this article, a high-power-factor rectifier combining a DCM operated Boost input cell with an AHBFC was proposed and analyzed in detail. The main contributions are: 1) a detailed design procedure that, by exploiting the resonant nature of the AHBFC stage, allows to calculate all converter parameters, while ensuring zero-voltage-switching turn-ON for the switches, in the specified input voltage and load ranges; 2) a combined feedforward-feedback digital control strategy that exploit both duty-cycle and switching frequency control parameters; and 3) the investigation of a particular type of input current crossover distortion caused by the DCM operation of the boost input cell. The theoretical analysis is validated by experimental results taken on a 160 W rated prototype, working at the nominal switching frequency of $f_s = 400\,\text{kHz}$.

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