





Improved MIMO Modeling and Enhanced Transient Performance of Phase-Locked Loop During Grid Fault

Kanakesh Vatta Kkuni , Graduate Student Member, IEEE, Guangya Yang , Senior Member, IEEE, Qiteng Hong , Member, IEEE, and Campbell Booth 

Abstract—A phase-locked loop (PLL) is commonly used in grid-connected power converter for synchronization. A single input single output (SISO) linear model of PLL with the phase angle of the point of common coupling (PCC) voltage as input and the estimated phase angle as the output is generally used in the PLL analysis and design. However, an undesirable coupling between the magnitude and phase of the input voltage is present when a filtering stage is incorporated before the control loop, which a SISO model cannot capture, and could result in a significant disturbance in the PLL estimated phase during grid faults. This paper proposes a generalized multi-input multi-output (MIMO) linear model that captures the complete PLL dynamics during symmetrical faults for a PLL equipped with any prefilter. Furthermore, a compensation method that decouples the magnitude dynamics of the input voltage from the phase dynamics is proposed in this paper. The proposed compensation improves the PLL's phase tracking performance by ensuring that the prefiltered PLL acts only on the PCC voltage phase changes. A vital application of the proposed compensation method for PLL is during a grid fault case, wherein the converters are expected to contribute to the fault current, which requires an accurate measurement of the PCC voltage phase. The compensation method's effectiveness is demonstrated using power hardware in the loop simulation of a hardware voltage source converter interfaced to a distribution system simulated in real-time.

Index Terms—Phase-locked loop (PLL), power system faults.

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Kanakesh Vatta Kkuni and Guangya Yang are with the Center for Electric Power and Energy, Department of Electrical Engineering, Technical University of Denmark, 2800Kgs. Lyngby, Denmark (e-mail: kvkhu@elektro.dtu.dk; gyy@elektro.dtu.dk).

Qiteng Hong and Campbell Booth are with the Department of Electronic and Electrical Engineering, University of Strathclyde, G1 1XQ Glasgow, UK. (e-mail: q.hong@strath.ac.uk; campbell.d.booth@strath.ac.uk).

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I. INTRODUCTION

THE proliferation of power electronics (PE) based resources into the power system brings immense challenges and well-known benefits. Challenges arise, mainly because it is harder to describe the PE resources' response. It is driven by embedded control, unlike the synchronous machine, where physical parameters primarily drive their response. The difference in response is apparent in the case of fault current contribution, as the response from a synchronous machine is well described and predictable but it is not the same in the case of a PE-based generation and compensation [1]–[3]. There are several different control strategies for PE-based generation proposed in the literature [4], which introduces diverse fault current characteristics and grid voltage support. An improper response current to grid fault from a converter could also result in currents from different converters to offset the reactive power contribution from rest of the components [5]. The grid codes expect that the PE resources quickly inject fast fault reactive current to the system to ensure the satisfactory protective relay system operation [6], [7]. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system.

Central to the requirement for a fast fault current contribution is accurate detection of the phase of the point of common coupling (PCC) voltage, typically achieved by a phase-locked loop (PLL) based synchronization unit [8]. During the fault event, both the magnitude and phase of the PCC voltage are disturbed, making it challenging to estimate the phase of PCC voltage using PLL. A comprehensive modeling of the PLL is necessary in the fault scenario to design the control parameters to meet the strict time-domain performance requirements, such as a rise time for reactive fault current injection in tens of milliseconds as specified in the grid codes. Several variations of PLL's for power converters were proposed over recent years [9], [10]. Despite the differences in their names, most of them are structurally similar and are derived from a conventional synchronous reference frame PLL (SRF-PLL) shown in Fig. 1. These differences between PLL types are mainly due to the different types of filtering incorporated in the PLL. These filtering of the PCC voltages are implemented in mainly three stages: digital filters in the stationary reference frame [prefilter, $PF2(s)$], the digital filters embedded in the PLL control loop [in loop filters, $IF(s)$],

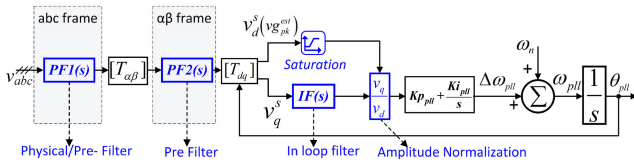


Fig. 1. Common structure of three Phase SRF-PLL with disturbance rejection capabilities.

and the physical filtering [PF1(s)] present due to antialiasing filter, as well as transducers and its associated circuits as shown in Fig. 1, [9]. Both prefilter and in-loop filters are incorporated in the PLL structure to enhance the disturbance rejection capability of PLL during nonideal grid voltage conditions, such as in the case of harmonics and unbalance in the PCC voltages. The classification of the most advanced PLL's is done based on the presence, absence, and types of prefilter and in-loop used in the PLL design. The PLL's with prefilter include, but not limited to, dual second-order generalized integrator based PLL (DSOGI-PLL) [8] multiple complex coefficient filters [8] based PLL both used to extract the positive sequence components of three-phase ac voltage before the PLL control loop. Further, even a simple lowpass or a BPF implemented in the stationary reference frame can also be considered a prefiltered type PLL. Several PLL's and frequency-locked loops (FLL) with prefiltering has been proposed in the literature to estimate the phase of distorted PCC voltages with unbalances in both amplitudes and phase angles [11], [12].

For PLL controller parameter design, most of the past work utilizes a linear time-invariant single input single output (SISO) PLL model with the phase angle ($\theta_g(t)$) of the PCC voltage as input and its estimated phase angle ($\theta_{pll}(t)$) as its output [13]. Extension of such a model is straightforward for the PLL's with in-loop filters [13], [14]. However, obtaining a SISO model is not a trivial task for a prefiltered PLL since the filtering takes place in a stationary frame with time-varying sinusoidal voltages. When analysis PLL's with sudden large disturbance in voltage magnitude it is important to consider the PCC voltage magnitude change as in input in PLL modeling. An extended SISO model that consider the harmonic components of the PCC voltage as a disturbance input is presented by [14]. While such a model is sufficient to capture PLL dynamics during small disturbances and control design, this article shows that for PLL's equipped with additional filters for disturbances and harmonics elimination, the SISO modeling is inadequate. For studying large disturbances like power system faults, a multi-input multi-output (MIMO) dynamic model of the PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs is necessary to improve the modeling and control design. Such a MIMO model of the PLL could also improve synchronization stability assessment accuracy improvement during severe grid faults [15], [16]. Several recent studies have presented linear time-periodic MIMO models of specific types of PLL's and FLL. These MIMO models can account for the presence of harmonics and/or imbalance [17], [18]. In [12], modeling and an improvement in transient response and harmonic response for

a second-order generalized integrator based FLL is presented. However, these MIMO models are specific to PLL/FLL types and cannot be generalized for prefiltered PLL types. In [19], a generalized method for converting the prefiltered section of the PLL's implemented in the stationary frame to a rotating reference frame is presented. Such a method could be used as the basis for establishing a generalized (MIMO) dynamic model of the prefiltered PLL with both phase angle and instantaneous magnitude of the PCC voltage as inputs.

In this article, a generalized MIMO model for prefiltered PLL, which captures the complete dynamics of prefiltered PLL during faults, is proposed. From the developed nonlinear MIMO model, it is readily observable that unlike a PLL with in-loop filters, for the PLL's with prefilters implemented in the stationary frame (including physical filters), there exists a coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. Such a coupling is not a desirable attribute to a PLL as it is intended to only respond to the change in phase of the terminal ac voltage and could result in wrong estimates of frequency and phase during faults. Based on the derived nonlinear MIMO model, a linearized model is developed to aid the controller design. A supplementary control loop is proposed in this article to reduce the coupling effect of the instantaneous peak of the ac voltage to the estimated phase. Overall the contributions of this article are as follows.

- 1) Develop a MIMO model of a prefiltered PLL, which captures the complete dynamics of prefiltered PLL during faults. The model is useful in enforcing a strict time-domain requirement for converter response during fault cased. Further, the model can be used for converter control design as well as synchronization stability analysis.
- 2) A supplementary control loop is proposed for a prefiltered PLL, which not only reduces the transients in the estimated phase and frequency during fault, but also eliminates the steady-state phase lag introduced by prefilters

The modeling and analysis in this article is generalizable for all types of prefiltered PLL. However, for the sake of brevity, the analysis presented in this article is restricted to three of the commonly used types of prefilters, 1) PLL with first-order lowpass filter as prefilter (LPF-PLL), 2) PLL with bandpass filter as prefilter (BPF-PLL), 3) PLL with DSOGI as prefilter (DSOGI-PLL). Additionally, to show the effectiveness of the proposed model and supplementary control on a cascaded prefilter as an example application of a PLL with both physical filter and a prefilter, a PLL with DSOGI as prefilter and a first-order LPF as a physical filter (LPF-DSOGI-PLL) is also studied in this article.

II. OVERVIEW OF PLL OPERATIONS AND MOTIVATION

In SRF-PLL with prefilter is shown in Fig. 1. The three phase instantaneous PCC voltages (v_{abc}) are first filtered and transformed into a rotating reference frame (dq frame) using estimated phase angle θ_{pll} . The q -axis voltage (v_q^s) of the transformed voltages is then driven to zero in steady state by a Proportional Integral (PI) controller with a proportional gain Kp_{pll} , and integral gain Ki_{pll} . In steady state, the magnitude of

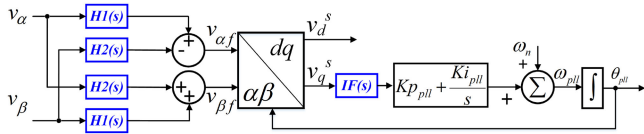


Fig. 2. Generalized representation of prefiltered SRF PLL.

the d -axis voltage (v_d^s) is equal to the magnitude of the input PCC voltage (v_{gpk}), hence the v_d^s is also termed as estimated peak voltage of the PCC voltage (v_{gpk}^{est}). The PLL estimated frequency ω_{pll} is the sum of the nominal frequency (ω_n) and output of the PI controller ($\Delta\omega_{pll}$). A dynamic amplitude normalization is implemented in all the PLL's considered to ensure the loop gain of the PLL remain the same for all magnitude of the grid voltages. The $[T_{\alpha\beta}]$ and $[T_{dq}]$ in Fig. 1 are the Clarke (abc to $\alpha\beta$) and park ($\alpha\beta$ to dq) transformation matrices.

$$[T_{\alpha\beta}] = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \quad (1)$$

$$[T_{dq}] = \begin{bmatrix} \cos(\theta_{pll}(t)) & \sin(\theta_{pll}(t)) \\ -\sin(\theta_{pll}(t)) & \cos(\theta_{pll}(t)) \end{bmatrix}. \quad (2)$$

In a PLL, the physical filtering stage ($PF1(s)$) and prefilter stage ($PF2(s)$) could be present in abc frame or $\alpha\beta$ frame. However, most filtering action in the abc frame can also be represented in an equivalent $\alpha\beta$ frame model. For instance, a LPF or a BPF implemented in abc frame is similar to the same filters implemented in $\alpha\beta$ frame [19]. Hence the PLL's with a filtering stage (both $PF1(s)$, $PF2(s)$) present in the stationary reference frame (abc and $\alpha\beta$), can be represented in a convenient generalized form as shown in Fig. 2 with no distinction between a prefilter or physical filter. The transfer functions $H1(s)$, $H2(2)$ shown in Fig. 2, acts on the $\alpha\beta$ frame value of the terminal voltages (v_α, v_β) to give the filtered $\alpha\beta$ frame terminal voltages ($v_{\alpha_f}, v_{\beta_f}$). The transfer functions $H1(s)$, $H2(2)$ could include

- 1) The 2×2 MIMO transfer function of a prefilter implemented in $\alpha\beta$ frame, which could include a DSOGI [14], a standard complex coefficient filter [20], or any other prefilter implemented in $\alpha\beta$ frame.
- 2) $\alpha\beta$ frame equivalent of the filtering action caused due to physical filter or antialiasing filter in abc frame.
- 3) A cascaded combination of the physical filter and prefilter in $\alpha\beta$ frame.

In order to emphasize the main motivation of this article, the four types of prefiltered PLL's under consideration; LPF-PLL, BPF-PLL, DSOGI-PLL, LPF-DSOGI-PLL along with a PLL with no prefilter but a LPF placed inside the control loop (LPF-Inloop-PLL), are subjected to symmetrical grid voltage sag to about 0.1 p.u. and recovery. The parameters for the prefilters are typical to 50 Hz supply and is shown in Table I. The PLL control parameters Kp_{pll} and Ki_{pll} are designed such that all the PLL's time-domain performances are equal for a change in the terminal voltage phase. The response of the considered PLL's to the sudden dip in PCC voltage is depicted in Fig. 3. The symmetrical voltage sag is of magnitude 0.1 p.u. lasting for 0.1

TABLE I
TRANSFER FUNCTIONS AND PARAMETERS OF THE FILTERS USED

Prefilter type	Transfer Function	Parameters
Bandpass prefilter	$H1(s) = \frac{2\omega_n s \zeta}{s^2 + 2\omega_n \zeta s + \omega_n^2}$ $H2(s) = 0$	$\zeta = 0.707$ $\omega_n = 2\pi 50 \text{ rad/sec}$
Lowpass prefilter	$H1(s) = \frac{\tau}{s + \tau}$ $H2(s) = 0$	$\tau = 0.0005$
DSOGI prefilter	$H1(s) = \frac{k s}{\omega_n^2 + s^2 + 2\omega_p s}$ $H2(s) = \frac{\omega_n k}{\omega_n^2 + s^2 + 2\omega_p s}$	$\omega_n = 2\pi 50 \text{ rad/sec}$ $k = \sqrt{2}$
Lowpass Inloop	$IF(s) = \frac{\tau}{s + \tau}$	$\tau = 0.0005$

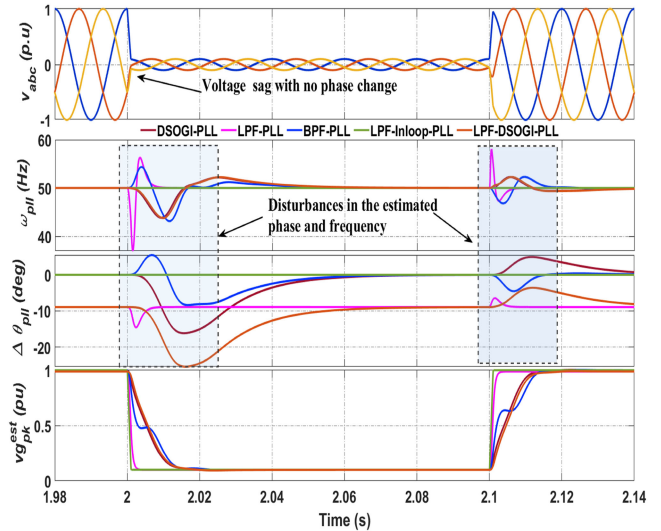


Fig. 3. Comparative simulation results of different prefiltered and in-loop filtered PLL under grid voltage magnitude change while keeping the phase constant.

s and a subsequent recovery to 1 p.u., the terminal voltages' phases unchanged for the whole duration.

Ideally, as the name suggests, a PLL is only supposed to respond to a change in the terminal voltage phase. However, as seen from Fig. 3, except for the PLL with a filter placed inside the control loop (LPF-inloop-PLL), all the other three PLL's with prefilters show disturbances in the estimated phase ($\Delta\theta_{pll}$) and frequency (ω_{pll}), with varying degree of differences in performance. Moreover, for the case of a LPF in the prefilter stage as in LPF-DSOGI-PLL and LPF-PLL, there is also a steady-state phase error of approximately 10° as seen in Fig. 3. Such responses of the prefiltered PLL during grid faults cannot be explained or accounted for by a conventional linear SISO model. Therefore, to design the PLL's with prefilters and to capture and subsequently reduce the coupling effect of the instantaneous peak voltages and the estimated phase, an improved PLL model has to be developed.

III. PLL MODELING

A small signal model of a basic SRF-PLL without filters is well explained in literature [9], [14]. All the variable in the PLL is transformed to rotating reference frame for ease of analysis due to existence of dc steady state. One must note that the

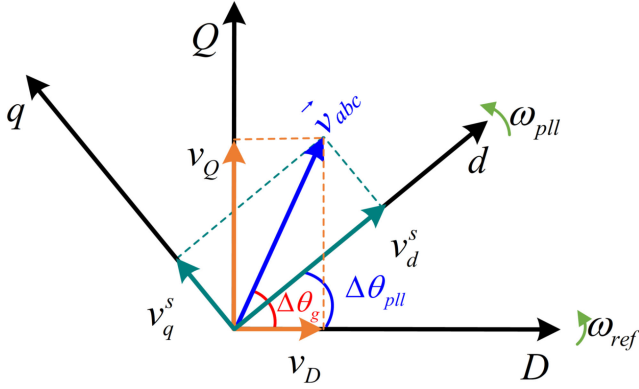


Fig. 4. Phasor relationship between the variables for SRF-PLL without prefilter.

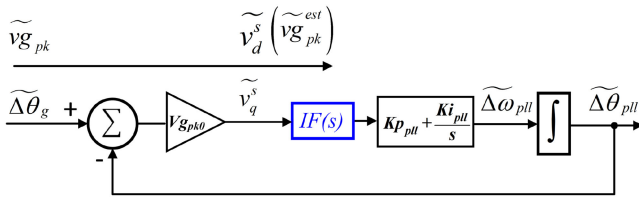


Fig. 5. Linear model of SRF PLL with an in loop filter.

inverter system has two rotating reference frames; a controller d - q frame (dq frame), which is defined by PLL angular velocity ω_{pll} and a system d - q frame (DQ frame) defined by ω_{ref} , which in this article is the nominal system frequency ω_n . At steady-state condition, both frames rotate in synchronization, but during small-signal perturbations the frames can rotate at different speeds depending on the PLL's tracked angle and speed. The phasor relationship between the variables defined in DQ and dq domain are depicted in Fig. 4. Assuming the voltages are balanced, the PCC voltage can be represented as a vector \vec{v}_{abc} with a magnitude V_{gpk} and phase of $\Delta\theta_g$ in DQ frame. The $\Delta\theta_{pll}$ is the difference in phase of the PLL dq frame and system DQ frame. Henceforth in this article, variables with the symbol \sim represents small perturbed form of the respective variables, also variable with appended 0 represents its steady-state value.

A. PLL's With Only Inloop Filter [IF(s)]

The PLL with only inloop filter without a prefilter does not technically exist because there is almost always a physical prefilter present for signal processing [PF1(s)], however, if the bandwidth of the prefilters is very high, the dynamics of these can be neglected and approximated as a unity gain. Therefore, among the three possible filtering positions in Fig. 1 only IF(s) needs to be considered. Using the phasor diagram shown in Fig. 4 and the Fig. 1, the linearized model of the three phase PLL with an inloop filter around an operating point V_{gpk0} , $\Delta\theta_{g0}$ can be derived and is shown in Fig. 5. The inputs of this model are $v_{gpk}^{\tilde{}}$ and $\Delta\tilde{\theta}_g$, and outputs are the estimated phase of the terminal voltage ($\Delta\tilde{\theta}_{pll}$) and $v_{gpk}^{\tilde{est}}$.

TABLE II
SFE TRANSFER FUNCTIONS OF $H1(s)$ AND $H2(s)$

Synchronous frame equivalent transfer function	
Band pass	
$H1_{DQ}(s)$	$\frac{2\omega_n \zeta (2\zeta \omega_n^3 + 2\omega_n^2 s + 2\zeta \omega_n s^2 + s^3)}{4\omega_n^4 \zeta^2 + 8\omega_n^3 \zeta s + 4\omega_n^2 s^2 + 4\omega_n s^3 + s^4}$
$H2_{DQ}(s)$	$\frac{2\omega_n^2 s^2 \zeta}{4\omega_n^4 \zeta^2 + 8\omega_n^3 \zeta s + 4\omega_n^2 s^2 + 4\omega_n s^3 + s^4}$
Lowpass	
$H1_{DQ}(s)$	$\frac{\tau(s+\tau)}{\omega_n^2 + s^2 + 2s\tau + \tau^2}$
$H2_{DQ}(s)$	$\frac{-\omega_n \tau}{\omega_n^2 + s^2 + 2s\tau + \tau^2}$
DSOGI	
$H1_{DQ}(s)$	$\frac{k\omega_n(2k\omega_n^3 + 4\omega_n^2 s + k\omega_n s^2 + s^3)}{2k^2\omega_n^4 + 2k^2\omega_n^2 s^2 + 8k\omega_n^3 s + 4k\omega_n s^3 + 8\omega_n^2 s^2 + 2s^4}$
$H2_{DQ}(s)$	$\frac{k^2\omega_n^3 s}{2k^2\omega_n^4 + 2k^2\omega_n^2 s^2 + 8k\omega_n^3 s + 4k\omega_n s^3 + 8\omega_n^2 s^2 + 2s^4}$

As seen from Fig. 5, the linear small signal model of a SRF-PLL with an in loop filter is decoupled for the dynamics of $v_{gpk}^{\tilde{}}$ and $\Delta\tilde{\theta}_g$. The model is simply an extension of the conventional SISO SRF-PLL linear model. The important point to note is that any disturbance in the instantaneous peak voltage will not have an impact on the estimated phase θ_{pll} , this conclusion is also confirmed from the simulation results shown in Fig. 3.

B. PLL's With Prefilters [PF1(s) and PF2(s)]

In the generalized model of prefiltered SRF-PLL is depicted in Fig. 2. The major challenge in modeling the prefilter PLL is that the control/filter action on the voltages occurs in stationary reference frame as well as SRF. This imposes challenges on developing a linear time invariant model, as there is no dc steady state in the stationary reference frame, which is required for modeling the equations in dq reference frame. The methods shown in [21] and [22] is used to transform the prefilters represented in frequency domain [$H1(s)$, $H2(s)$] shown in Fig. 2 to its equivalent transfer function [$H1_{DQ}(s)$, $H2_{DQ}(s)$] in the system synchronous rotating reference frame (DQ frame). The synchronous frame equivalent (SFE) transfer function matrix of the prefilter is given by $H_{DQ}(s)$

$$[H_{DQ}(s)] = \begin{bmatrix} H1_{DQ}(s) & -H2_{DQ}(s) \\ H2_{DQ}(s) & H1_{DQ}(s) \end{bmatrix} \quad (3)$$

where

$$H1_{DQ}(s) = \frac{H1(s-j\omega_{ref})}{2} + \frac{H1(s+j\omega_{ref})}{2} - j\frac{H2(s-j\omega_{ref})}{2} + j\frac{H2(s+j\omega_{ref})}{2} \quad (4)$$

$$H2_{DQ}(s) = j\frac{H1(s-j\omega_{ref})}{2} - j\frac{H1(s+j\omega_{ref})}{2} + \frac{H2(s-j\omega_{ref})}{2} + \frac{H2(s+j\omega_{ref})}{2} \quad (5)$$

The elements of SFE transfer function matrix of the prefilters considered in this article are given in Table II. For cascaded prefilters such as the LPF-DSOGI-PLL considered in this article, the SFE can be found by first obtaining the individual SFE transfer function matrix for each prefilter separately and then multiplying to get the final SFE transfer function matrix.

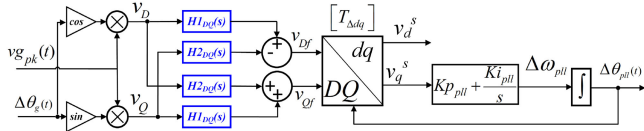


Fig. 6. Nonlinear model of a general prefiltered PLL in rotating reference frame.

The variables defined in system DQ frame can be rotated to the control frame (dq frame) using transformation matrix $[T_{\Delta dq}]$, for instance

$$[v_{dq}] = [T_{\Delta dq}][v_{DQ}] \quad (6)$$

where

$$[T_{\Delta dq}] = \begin{bmatrix} \cos(\Delta\theta_{pll}(t)) & \sin(\Delta\theta_{pll}(t)) \\ -\sin(\Delta\theta_{pll}(t)) & \cos(\Delta\theta_{pll}(t)) \end{bmatrix} \quad (7)$$

The nonlinear model of prefiltered PLL in rotating reference frame by utilizing the SFE transfer function matrix is shown in Fig. 6, the DQ frame voltage of terminal voltages (v_{DQ}) v_D , v_Q are given as input signals to the DQ frame transfer function of the prefilter. The nonlinear model has the inputs as terminal voltage phase $\Delta\theta_g$ and instantaneous peak $vg_{pk}(t)$, and outputs are the estimated phase of the terminal voltage $\Delta\theta_{pll}$ and estimated magnitude v_d^{est} . This nonlinear model can also be used to extend the loss of synchronization study power converter dominated power systems [15], [23], [24].

The time domain equation of $v_{DQ}(t)$ and subsequently of $v_{dq}(t)$ (vector of v_d^s , v_q^s) can be written as

$$[v_{DQ}(t)] = \begin{bmatrix} vg_{pk}(t) \cos(\Delta\theta_g(t)) \\ vg_{pk}(t) \sin(\Delta\theta_g(t)) \end{bmatrix} \quad (8)$$

$$[v_{dq}^s(t)] = [T_{\Delta dq}] \cdot [[H_{DQ}(t)] * [v_{DQ}(t)]] \quad (9)$$

where the asterisk $*$ denotes the convolution operation, and dot \cdot denotes multiplication. The linearized model can be derived by finding the first order approximation of (9) around an operating point V_{gpk0} , $\Delta\theta_{g0}$, $\Delta\theta_{pll0}$.

$$[\tilde{v}_d^s \ \tilde{v}_q^s]^T = [Cl(s)] [\tilde{v}_{gpk} \ \Delta\tilde{\theta}_g \ \Delta\tilde{\theta}_{pll}]^T \quad (10)$$

where

$$Cl(s) = \begin{bmatrix} H1_{DQ}(s) & -V_{gpk0}H2_{DQ}(s) & 0 \\ H1_{DQ}(s) & V_{gpk0}H2_{DQ}(s) & V_{gpk0} \end{bmatrix}. \quad (11)$$

Using (10) and the nonlinear model shown in Fig. 6, the linearized model of the prefiltered PLL as shown in Fig. 7 can be derived. Unlike a PLL with only inloop filter, where \tilde{v}_q was decoupled from vg_{pk} , in prefiltered PLL, vg_{pk} is coupled to v_q^s via $[H2_{DQ}(s)]$ as shown in Fig. 7. This coupling effect can be significant during the large disturbances in PCC voltage for some PLL's with prefilter, but it is usually ignored in the existing PLL models. It is also important for controller design as the underlying couplings is evident as opposed to a SISO model of the PLL. The MIMO model helps us in designing an efficient controller and thus ensures a better time domain performance,

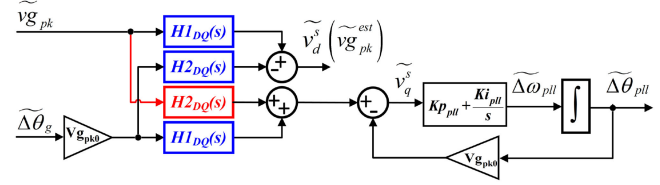


Fig. 7. Linear model of SRF PLL with prefilter.

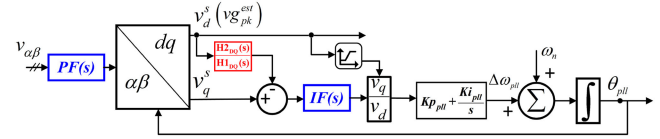


Fig. 8. General implementation of compensator for a prefiltered PLL.

especially when there is a simultaneous large disturbances in both terminal voltage magnitude and phase as in the case of power system faults. The MIMO model also allow us to capture the disturbances in estimated phase of prefiltered PLL's for a symmetrical disturbance in the PCC voltage.

IV. PROPOSED CONTROL TO REDUCE COUPLING

In this section, a supplementary control structure is proposed to reduce the coupling between the phase and instantaneous peak of the terminal voltage. The coupling effect is highlighted in Fig. 7, the obvious choice for a perfect decoupling would be to include a inverse based controller, which inverts the plant dynamics, which in this case is the transfer function matrix $H_{DQ}(s)$. However, the computational burden associated with such a controller can be extremely high as it involves inverting the MIMO transfer function matrix. Moreover, such controls will also overturn the advantages of using a prefilter such as harmonic. Hence, for practical purpose, a pure inverse based controller may not be desirable in this case.

Based on the insights derived from the linearized model and also from the characteristics of DQ equivalent frequency response of the common prefilters, a compensator of the same order as the respective prefilter transfer functions shown in Table I is proposed. The approach followed is to make the forward path gain from \tilde{v}_{gpk} to the input of the PI control to zero, which is achieved with the addition of a compensator $(\frac{H2_{DQ}(s)}{H1_{DQ}(s)})$ as shown in Fig. 8. The compensator is realizable for any filter type as long as the filter types have no nonminimum phase behavior. The decoupling effect of the addition of compensator can be clearly seen from Fig. 9, which depicts the linearized model of the PLL with prefilter. The compensator types for the prefilters considered in this article is shown in Table III. To test the effectiveness of the compensator, the study shown in Fig. 3 is repeated with added compensator, the parameters of the prefilter remained the same as in Table I. As anticipated, the disturbance in peak voltage did not have any effect on the estimated phase and frequency of the PLL with prefilter as shown

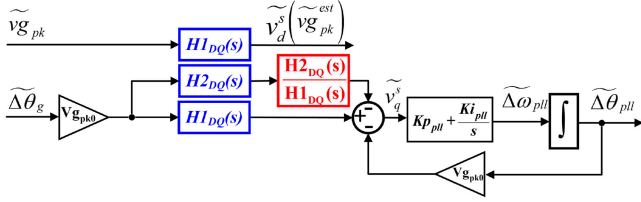


Fig. 9. Simplified linear model of prefiltered PLL, including the proposed compensator.

TABLE III
TRANSFER FUNCTIONS OF THE PROPOSED COMPENSATORS

PrefilterType	Compensator
Bandpass	$-\frac{\omega_n s^2}{2\zeta\omega_n^3 + 2\omega_n^2 s + 2\zeta\omega_n s^2 + s^3}$
Lowpass	$-\frac{\omega_n}{s + \tau}$
DSOGI	$\frac{k\omega_n^2 s}{2k\omega_n^3 + 4\omega_n^2 s + k\omega_n s^2 + s^3}$

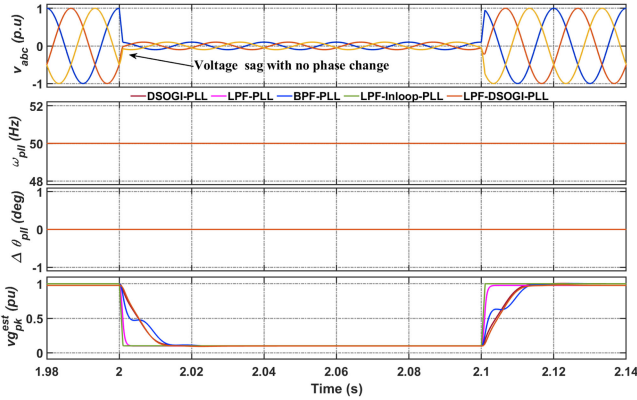


Fig. 10. Simulation results of prefiltered PLLs with the proposed supplementary compensator for grid voltage magnitude change while keeping the phase constant.

in Fig. 10. Furthermore, the steady-state phase offset caused due to a first-order LPF as the prefilter is also eliminated by the use of compensator.

This article focus is on PLL response and compensation for balanced voltage dips and phase jump. Nevertheless, the feasibility of the proposed compensator is also investigated in an unbalanced sag case. Among the considered PLL, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the negative sequence voltage generated by unbalanced sag [9]. Therefore, the results for unbalanced cases are only demonstrated on those two PLL's against PCC voltage sag typical for double line to ground fault while keeping the phase constant. The results of the unbalanced sag study are shown in Fig. 11. It can be seen that the compensation reduces the disturbance in estimated phase and frequency of the PLL as well as it removes any steady-state error caused due to LPF in LPF-DSOGI-PLL.

The procedure for obtaining the compensator for any prefiltered PLL is summarized below for readers convenience

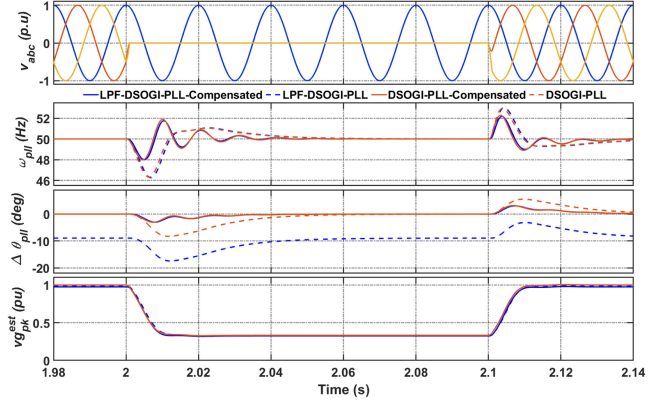


Fig. 11. Simulation results of DSOGI-PLL and LPF-DSOGI-PLL with and without compensation for unbalanced grid voltage sag while keeping the phase constant.

- 1) Convert to generalized representation as in Fig. 2 and obtain transfer functions $H1(s)$, $H2(s)$.
- 2) Obtain the (SFE) transfer function matrix components $H1_{DQ}(s)$, $H2_{DQ}(s)$ using algebraic combination of frequency shifted $H1(s)$, $H2(s)$ as shown in (4) and (5)
- 3) The compensator is $\frac{H2_{DQ}(s)}{H1_{DQ}(s)}$ and its generalized implementation is shown in Fig. 8.

V. SIMULATION RESULTS

A simulation study of the three prefilter types and its compensation was carried out to verify the advantages of the proposed compensation. To ensure a fair design, all the three PLL's were designed to have two cycle settling time while limiting the overshoot to 10%. The design was carried out using the linear model derived in the previous section. The control parameters of a PLL type was retained when compensation was added. It should be noted that, as the PLLs as the PLL input voltage magnitude coupling is eliminated with the proposed compensator, control performance can be improved. To simulate symmetrical fault, we considered a positive sequence voltage sag to 0.3 p.u. for 100 ms duration accompanied by a positive phase jump of 15° . The positive effects of compensation is evident from the results shown in Fig. 12. The net error in estimated angle of the PLL and the actual angle ($\Delta\theta_{error} = \theta_{pll} - \theta_g$) is reduced. To further quantify the impact of compensation, a normalized root mean square (NRMS) of $\Delta\theta_{error}$ is computed for all the PLL types considered with varying level of voltage dip and phase jump. The NRMS of $\Delta\theta_{error}$ for a PLL under a input phase jump of θ_{fault} during the period of fault related dynamics is defined by

$$NRMS\Delta\theta_{error} = \frac{\sqrt{\frac{1}{T2-T1} \int_{T1}^{T2} \Delta\theta_{error}(t)^2}}{\theta_{fault}} \quad (12)$$

where T1 is the fault initiation time and T2 is two cycles after the fault clearing time when all dynamics of induced by the fault is settled. The NRMS of $\Delta\theta_{error}$ is computed by running the time domain simulation for a dip in positive sequence voltages for

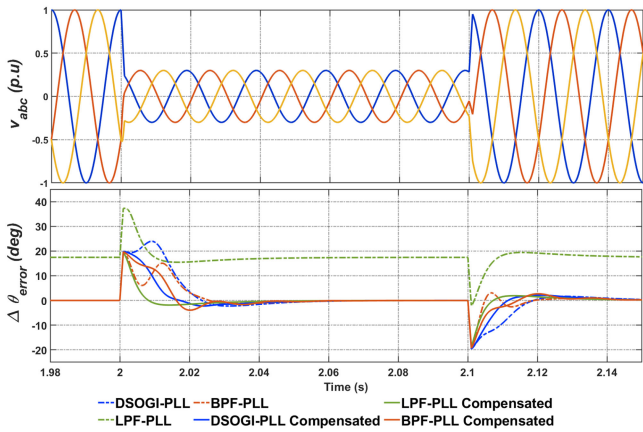


Fig. 12. Simulation results for a dip in positive sequence voltage magnitude for 100 ms duration accompanied by a positive phase jump of 15° .

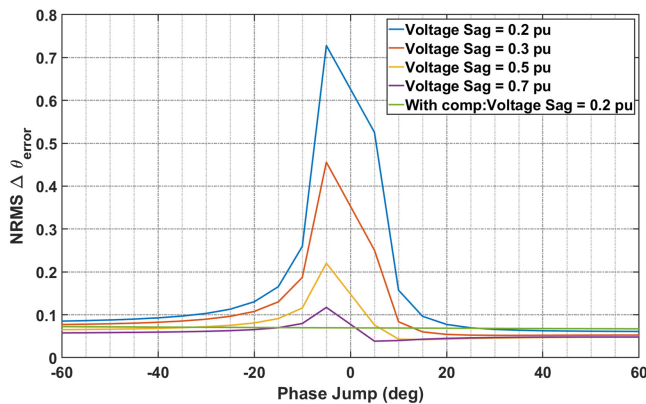


Fig. 13. NRMS of $\Delta\theta_{\text{error}}(\text{deg})$ during variable voltage sag and simultaneous phase jump for 100 ms period for BPF PLL.

a period of 100 ms, a phase jump is also accompanied with this dip. It can be seen from Figs. 13–15 that the net error in estimated phase for all uncompensated PLL's is dependent on the magnitude of dip in voltage, whereas a compensation makes NRMS of $\Delta\theta_{\text{error}}$ independent of the voltage dip. The NRMS is not relevant for LPF prefilter as the phase shift introduced is constant regardless of the dip in voltage.

VI. PHIL RESULTS

The proposed compensation and MIMO modeling can be applied in any grid-connected converter system, which employs a prefiltered PLL for grid frequency and phase detection for protection and control. One of the applications, where the advantage of the PLL compensation is inherently visible is to enable fast fault current injection effectively. The grid codes expect that the PE resources quickly inject as much reactive current to the system to ensure the satisfactory protective relay system operation [6], [7]. The protection system in the high voltage grid requires a sufficient amplitude of fault current in the first 20–30 ms after the fault to operate correctly. Further, the

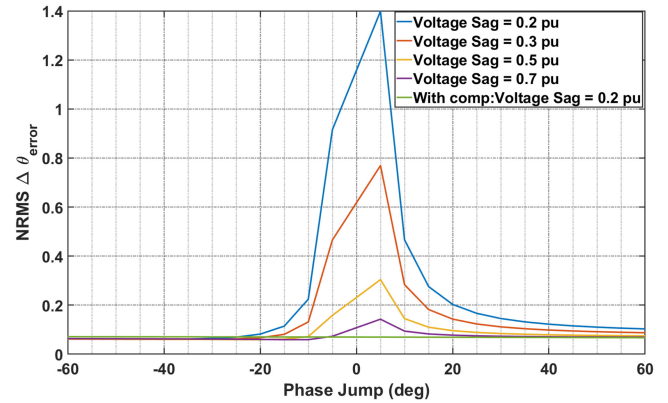


Fig. 14. NRMS of $\Delta\theta_{\text{error}}(\text{deg})$ during variable voltage sag and simultaneous phase jump for 100 ms period for DSOGI PLL.

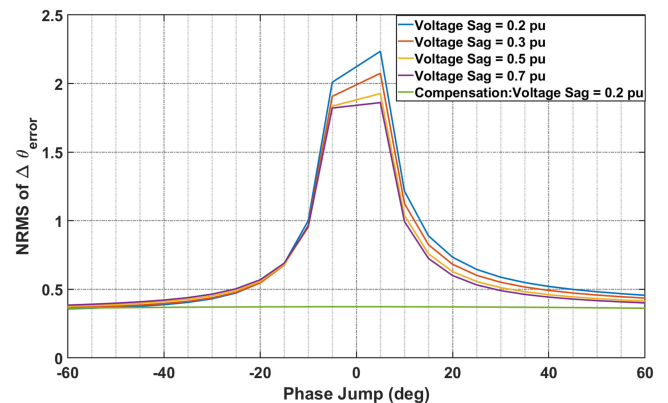


Fig. 15. NRMS of $\Delta\theta_{\text{error}}(\text{deg})$ during variable voltage sag and simultaneous phase jump for 100 ms period for LPF-DSOGI-PLL.

fault level contribution from PEIPS (PE connected equipment) mitigates the severity of maximum voltage depression seen by other assets (especially more distant from the fault). It can prevent tripping due to under-voltage protection and help keep the power system stable. Standards on fault current injection are anticipated to become even stringent with more PE-based generation connected to the power system.

The advantages of using proposed compensation for prefiltered PLL is confirmed through power hardware in the loop (PHIL) simulation. The PHIL test setup is shown in Fig. 16. The setup includes a simplified power system model implemented in real-time digital simulator (RTDS), RTDS *I/O* cards, two-level VSC hardware, which is a SEMIKRON SkiiP stack with inductive filter, and current and voltage sensors, a 2.5 kVA SPITZENBERGER & SPIES PAS 2500 linear amplifier. The VSC switching frequency is set to 10 kHz, and the inductive filter for the VSC stack is 8 mH. The *I/O* cards exchange the PCC voltage from RTDS and current coming into the RTDS between the amplifier and the PCC. This exchange ensures that the VSC is part of the power system network. The voltage and current signal between the RTDS and the hardware is scaled, and the scaling is shown in Table IV. The current feedback signal is

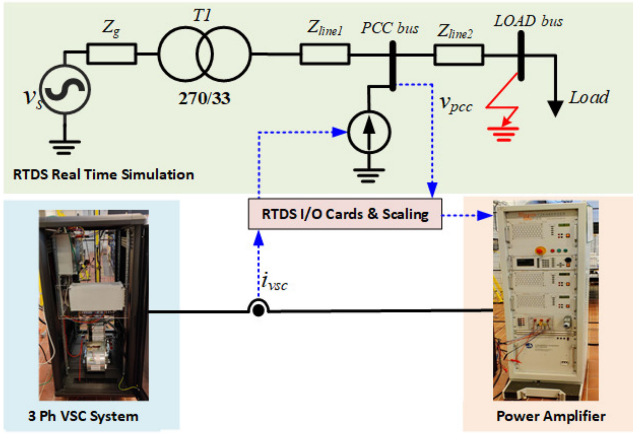


Fig. 16. PHIL test.

TABLE IV
PHIL SCALING FOR THE VSC HARDWARE

Symbol	Description	Physical Value	Scaled to Simulation
V_{vsc}	Amplifier voltage	100 V	33kV
I_{vsc}	VSC Current	7A	150 A
P_{vsc}	VSC power	2 kVA	5 MVA

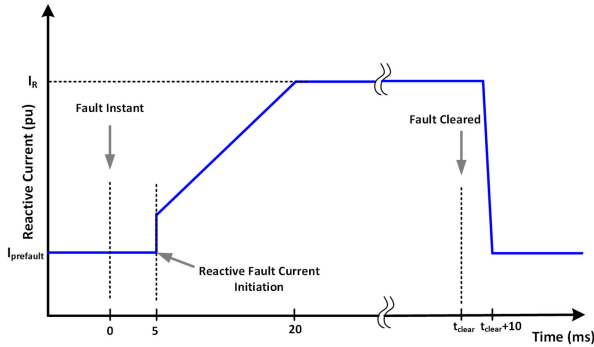


Fig. 17. Positive sequence fault current reference.

conditioned with a first-order LPF with a time constant of $250 \mu\text{s}$ to eliminate noise and ensure the PHIL simulation's stability.

The VSC control system, including the current control and the PLL's discussed in this article and their compensation strategies, are implemented on a FPGA based digital controller from national instruments (NI). The PLL's are set to track the amplifier voltage phase, which is the simulated PCC bus's scaled voltage. The sampling time for the control loop is $40 \mu\text{s}$. The controller is discretized using the trapezoidal method. The fault reactive current reference is as shown in Fig. 17. The reactive reference fault current is initiated 5 ms after the fault instant. The reference rate is limited to 1 p.u. in a cycle during the fault current initiation stage. The PLL compensation performance is then evaluated first for a symmetrical fault with a fault impedance of 0.2Ω at the load bus. The VSC performance with and without compensation for

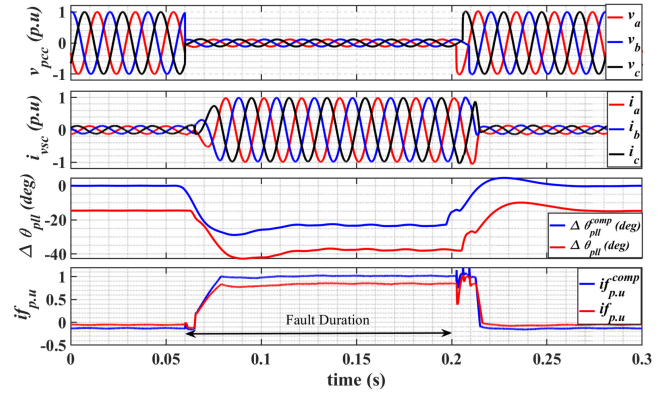


Fig. 18. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a LPF as prefilter and its compensation.

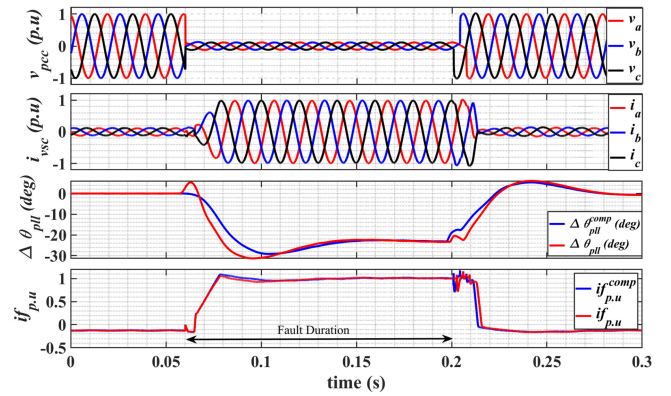


Fig. 19. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a 50 Hz BPF prefilter and compensation.

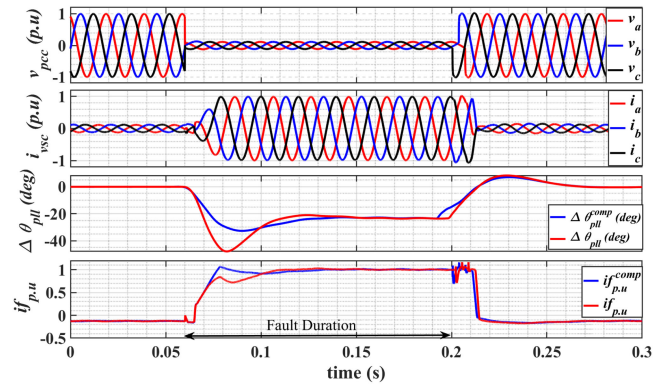


Fig. 20. Results from PHIL study of the VSC under balanced three phase fault case, for a PLL with a DSOGI prefilter and compensation.

balanced fault is shown in Figs. 18–20. All the plots captured in the NI controller and RTDS interface is exported to MATLAB and replotted for enhanced clarity. The plots for three-phase PCC voltage and the injected three-phase current is shown only for compensated case. The fault reactive current at the PCC without compensator ($i_{f.p.u.}^{comp}$) and with compensator ($i_{f.p.u.}^{comp}$) are found

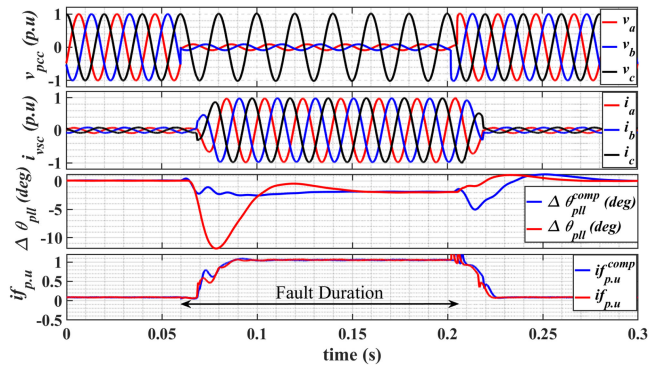


Fig. 21. Results from PHIL study of the VSC under double line to ground fault case, for a PLL with a DSOGI prefilter and compensation.

by scaling the reactive power measured at the PCC with the PCC voltage and dividing by base current (150 A) in real-time simulation. The PLL estimated phase of the terminal voltage with and without compensator $\Delta\theta_{pll}$, $\Delta\theta_{pll}^{comp}$ are captured in NI controller.

Fig. 18, shows the VSC's response for balanced fault equipped with a first-order LPF, with a time constant of 1 ms. The first-order LPF, albeit with a low time constant, introduces a phase delay of 17.4° at the fundamental frequency. This open-loop delay also results in a difference in the required reactive current injected and the measured reactive current at the PCC bus, as depicted in Fig. 18. The open-loop delay and the resulting difference in fault current are eliminated using the proposed PLL compensation. Figs. 19 and 20 depict VSC's balanced fault response with BPF and DSOGI prefilter as well as the response with proposed compensation. The reactive current injected in the prefilter compensated cases are closer to the reference reactive current because the compensation decouples the dynamics of voltage magnitude from the measured phase.

Among the PLL's considered in this article, only the DSOGI-PLL and cascaded LPF-DSOGI-PLL can reject the negative sequence voltage generated by unbalanced sag [9]. Therefore, the results for unbalanced sag cases are only demonstrated on those two PLL's against double line to ground fault at the load bus. During unbalanced fault, a balanced reactive current injection strategy is utilized in this article, the positive sequence reactive fault current reference is as shown in Fig. 17. Fig. 21 shows the VSC's output with DSOGI-PLL during double line to ground fault. It can be seen that the compensation reduces the disturbance in the estimated PLL phase (θ_{pll}). However, the difference between the estimated phases for compensated and uncompensated case is not significant in this case. Therefore, the injected reactive current during compensated and uncompensated cases are similar. Fig. 22 depicts the results of the VSC with LPF-DSOGI-PLL under double line to ground fault. The LPF in the LPF-DSOGI-PLL introduces a phase delay, which is compensated with the use of the proposed compensator. Therefore, the reactive current injected in the prefilter compensated cases are closer to the reactive reference current and better cater to the grid requirements.

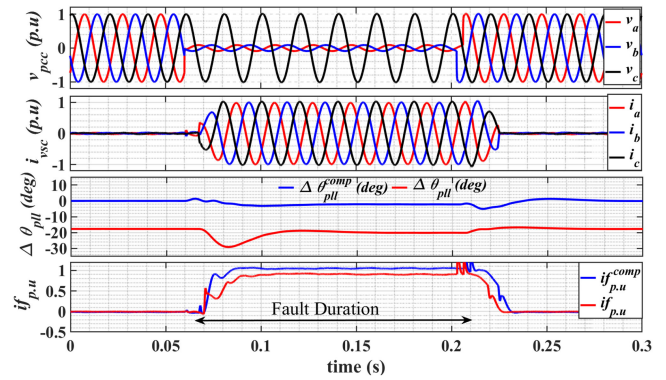


Fig. 22. Results from PHIL study of the VSC under double line to ground fault case, for a PLL with a cascaded LPF and DSOGI prefilter and compensation.

This application example of reactive fault current injection by VSC demonstrates the advantage of the proposed compensation.

VII. CONCLUSION

The fast detection of the PCC voltage phase was necessary for PE-based resources to comply with reactive current injection requirements during a fault. It was well-known that the three-phase balanced ac voltages can be represented by two instantaneous quantities, namely, the peak of the voltages and its phase angle. During symmetrical fault, there was a large disturbance in both these quantities. In this article, it was shown that during a fault in the power system, the traditionally used SISO model cannot capture the complete dynamics of the PLL with a prefiltering stage. This article proposed a nonlinear MIMO model of a general prefiltered PLL, which during a power system fault more accurately captures the transients of prefiltered PLL. The developed nonlinear model of the prefiltered PLL depicted the undesirable coupling between the instantaneous peak of the ac voltage and the estimated phase of the PLL. This article proposed a compensator to reduce this coupling, and the prefiltered PLL was made to act only on changes in the phase of PCC voltage. The proposed compensator was demonstrated with three commonly used prefiltered PLL's and on a cascaded prefilter case to show the effectiveness. The proposed control ensured an accurate current phase control and injection during faults to fulfill fault ride-through requirements.

APPENDIX

A. Test Power System Parameters

$Z_g = 0.054 + j0.54$; $Z_{line1} = 1.691 + j3.3929$; $Z_{line2} = 1.691 + j.34$; Load = 5 MW; Transformer T1 leakage reactance = 10% at 100 MVA base

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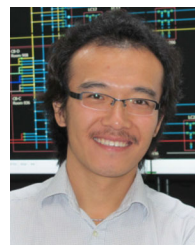
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Kanakesh Vatta KKuni (Graduate Student Member, IEEE) received the master's degree in electrical engineering from the Indian Institute of Technology Bombay, Bombay, India, in 2014. He is currently working toward the Ph.D. degree in Power system stability and application of synchronous condensers in low inertia grids with the Technical University of Denmark, Lyngby, Denmark.

From 2016 to 2018, he was Research Engineer with Berkeley Education Alliance for Research, Singapore, while from 2014 to 2016, he worked as a Research Engineer in Energy Management and Microgrid Lab with the National University of Singapore, Singapore. His research interests include power system stability, power converter control, and microgrids.



Guangya Yang (Senior Member, IEEE) received the Ph.D. degree in the field of Electrical Engineering from the University of Queensland, QLD, Australia, in 2008.

He is currently a Senior Researcher with the Technical University of Denmark, Lyngby, Denmark. He joined Technical University of Denmark as Postdoctoral Fellow, Researcher, and later Associate Professor. From 2020 to 2021, he was full-time working for Orsted as specialist on electrical design, control, and protection

of large offshore wind farms. His research interests include security, stability, and protection of power systems, with focus on offshore wind applications.

Dr. Yang is Member of IEC TC88 and TC8. He was a recipient of numerous research grants as Principal investigator with the recent H2020 Marie-Curie Innovative Training Networks project InnoCyPES (2021–2025) as a Coordinator. He is currently leading the editorial board of the IEEE Access Power and Energy Society Section, and is Editorial Board Member of IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, IEEE TRANSACTIONS ON POWER DELIVERY, and *Journal of Modern Power System and Clean Energy*.



Qiteng Hong (Member, IEEE) received the B.Eng. (Hons.) and Ph.D. degrees in electronic and electrical engineering from the University of Strathclyde, Glasgow, Scotland, in 2011 and 2015, respectively.

He is currently a Lecturer (Strathclyde Chancellors Fellow) with the University of Strathclyde. His main research interests include power system protection and control in future networks with low inertia, resulting from high penetration of renewable generation.

Dr. Hong is a Regular Member of the CIGRE Working Group B5.50, IEEE Working Group P2004, and the Technical Lead at the CIGRE U.K. Next Generation Network



Campbell Booth received the B.Eng. and Ph.D. degrees in electrical and electronic engineering from the University of Strathclyde, Glasgow, U.K., in 1991 and 1996, respectively.

He is currently a Professor and the Head of the Department for Electronic and Electrical Engineering with the University of Strathclyde. His research interests include power system protection, plant condition monitoring and intelligent asset management, applications of intelligent system techniques to power system monitoring,

protection, and control, knowledge management, and decision support systems.