# Evaluation of the OFF-State Base-Emitter Voltage Requirement of the SiC BJT With a Regenerative Proportional Base Driver Circuit and Their Application in an Inverter

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***Abstract*—A strong candidate device for use in high-efficiency and high-density power converters is the SiC bipolar junction transistor, which requires a continuous gate (base) current to maintain its ON-state. A base driver circuit with regenerative collector current feedback using a current transformer, and a negative OFF-state base-emitter voltage is presented in this article. The OFF-state base-emitter voltage required to prevent simultaneous conduction of a commercially available device when subjected to d*v*/d*t*'s is assessed. The device is then utilized in a three-phase dc-to-ac power converter where the efficacy of using the proposed base driver is evaluated. The OFF-state base-emitter voltage used is informed by the d*v*/d*t* tests. The converter is supplied from a 600-V dc rail, switches at 50 kHz and supplies a 4.1-kW load at a modulation index of 0.9. An efficiency of 97.4% was measured.**

***Index Terms*—Base driver, d*v*/d*t*, power converter, SiC bipolar junction transistor (BJT), simultaneous conduction.**

## I. Introduction

WIDE bandgap devices [1], [2], offer performance benefits when compared to their silicon counterparts, and candidate devices for use in high-efficiency power converters are SiC MOSFETs and bipolar junction transistors (BJTs). The SiC MOSFET exhibits low switching and conduction losses and has been evaluated in applications such as those in [3] and [4]. However, challenges include gate oxide reliability [5], and susceptibility to d*v*/d*t*-induced conduction ("crosstalk") [6], [7], in voltage source converters (VSCs). It is difficult avoiding crosstalk whilst not exceeding the maximum allowed OFF-state gate-source voltage of typically −10 V. Furthermore, compared to the silicon MOSFET, they tend to exhibit a low ratio of absolute maximum to threshold gate voltage. This presents the challenge of rapidly driving the gate to attain low switching losses at turn-ON, yet also ensuring that gate-source over-voltage transients exceeding the absolute maximum value are avoided [8].

Like the SiC MOSFET, the SiC BJT exhibits low switching and conduction losses, good short-circuit withstand times and absence of second breakdown [9]–[17]. In addition, the SiC BJT's base-emitter junction is formed from an inherently robust p-n diode structure, it has no oxide layer and can operate at higher temperatures than the SiC MOSFET. A feature of the SiC BJT is that it does not require a carefully controlled voltage applied to its control (base and emitter) terminals in the ON-state because it presents a forward biased p-n diode junction. It can also withstand a high reverse control voltage in the OFF-state. However, unlike MOS-gated devices, it needs a steady-state base current $i_B$ to hold it on as well as transient base currents for rapid switching. The SiC BJT can simply be supplied with the $i_B$ needed to cater for the highest collector current $i_C$ that will be encountered. However, this introduces inefficiency when supplied at lower $i_C$ values, and making $i_B$ proportional to $i_C$ is therefore desirable.

In [16], the problem of power dissipation in the driver circuit due to sourcing $i_B$ is addressed by using a low-voltage base driver supply rail to supply the steady ON-state $i_B$ in conjunction with a higher voltage rail for supplying the high transient current needed for rapid turn-ON. However, $i_B$ is still fixed for the worst-case $i_C$ with consequent losses in the driver circuit and the SiC BJT, and an additional base driver power supply rail is needed.

Proportional drive schemes for the SiC BJT are proposed in [18]–[20]. Dissipative arrangements are used in [18] and [19]. In [18], the choke current in a boost converter using a SiC BJT is sensed with a Hall-effect sensor. In response to this sensed current, $i_B$ is set at one of a number of discrete levels by a DSP, which controls a combination of switches which source currents into the base of the BJT. In [19], the choke current in a boost converter is also sensed with a Hall-effect sensor and the sensor's output signal is applied to the gate of a silicon MOSFET, which regulates the flow of $i_B$ into a SiC BJT's base. In [20], a current transformer (CT) is used in a proportional driver circuit for a SiC BJT. Apart from providing a proportional base

Manuscript received September 13, 2018; revised April 7, 2019 and July 4, 2019; accepted August 12, 2019. Date of publication September 26, 2019; date of current version April 30, 2020. This work was supported by the Engineering and Physical Sciences Research Council National Centre for Power Electronics under Grant EP/R004137/1 and Grant EP/K035096/1. *(Corresponding author: Neville McNeill.)*

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Digital Object Identifier 10.1109/TIE.2019.2938492

current, another advantage of using a CT is that it is ideally lossless as the current is not sourced through a dissipative element from a voltage supply. In practice, there are some losses due to factors such as CT core losses and the forward voltage drop of the rectifier diode normally required in series with the CT's secondary winding. The current gain of the SiC BJT is inversely related to its temperature and the current transfer ratio of the CT cannot be changed to accommodate this. This ratio, which is essentially dependent on the turns-ratio, therefore has to be set for the worst-case (highest) temperature that might be encountered. However, in many practical applications, there is little variation in the device operating temperature of the SiC BJT [18] and there is consequently little excess power dissipation incurred in the driver circuit or device by driving the BJT with an excessive $i_B$ at low temperatures. There is work on proportional drive schemes with CTs for earlier silicon BJTs in [21] and [22]. However, ensuring operation at high duty cycles is more challenging at the higher switching frequencies used with the SiC BJT.

This article proposes a regenerative proportional base driver with a negative OFF-state voltage for the SiC BJT where a CT is used to drive the BJT's base with a fraction of its collector current. The d$v$/d$t$-induced conduction characteristic of the BJT is evaluated for different conditions of rail voltage, temperature, and OFF-state base-emitter voltage. Whilst much literature is available on the SiC MOSFET's negative OFF-state gate-source requirement, and other mitigating measures [23] to address simultaneous conduction, the OFF-state requirements of the BJT have not been investigated in as much detail. Minimizing the displacement charge drawn through d$v$/d$t$-induced conduction is important as, otherwise, increased power dissipation and reduced efficiency results. Finally, the efficacy of the driver is demonstrated in an inverter. Unlike most dc–dc power converters, operation with duty cycles approaching 100% is normally desirable in an inverter. Where a CT is used, this presents the challenge of attaining high duty cycle operation by ensuring that the CT core flux is reset during short OFF-times.

This article is organized as follows. Section II describes the CT operation with regenerative collector current feedback and presents a base driver circuit. The circuitry in Section II has been presented in [24], and an extended description is given here. A comparison of the CT core flux resetting method in [24] with conventional resetting using a discrete clamping circuit is made. The maximum duty cycle limitations of the scheme in [24] are described in further detail. Section III contains an experimental evaluation of the negative OFF-state base-emitter voltage requirement of a SiC BJT. Section IV presents an evaluation of the performance of the BJT with regenerative base driver circuitry using a CT in a three-phase inverter application. A discussion is included in Section V. Section VI concludes this article.

## II. Base Driver Operation With Regenerative Current Feedback Using a CT

### A. Overview

As mentioned in Section I, the BJT needs a steady-state base current $i_B$ to hold it on as well as transient base currents for rapid switching. Its dc common-emitter current gain $h_{FE}$ is given by

$$h_{FE} = \frac{i_C}{i_B}. \tag{1}$$

The forward base-emitter voltage $V_{\mathrm{BE(on)}}$, when in conduction, of the SiC BJT is typically 3 V. This is considerably higher than that of a silicon BJT. Whilst the $h_{FE}$ of the SiC BJT of typically 80–100 at 25 °C is higher than that of the silicon power BJT, it is not sufficiently high for the base drive current and the associated power dissipation in the power device and its driver circuitry to be regarded as negligible. It is therefore desirable to supply only the $i_B$ needed to hold the device on for a given $i_C$, since setting $i_B$ for the worst-case (highest) $i_C$ incurs unwanted power losses where the current value varies sinusoidally in a fundamental period. As also mentioned in Section I, $i_B$ should ideally be supplied from a non-dissipative source for improved efficiency. Fig. 1 from [24] outlines a regenerative base driver circuit using a CT to apply a proportional base-drive current to the BJT. $N_1$ and $N_2$ are the CT's primary and secondary winding turns numbers, respectively. Dr acts as a rectifier, and D1 can be included to limit the negative-going voltage across $N_2$ when the CT's core material is resetting during TR1's OFF-time, by clamping the output of the CT to a voltage $V_{\mathrm{RESET}}$. In Fig. 1, $V_{\mathrm{RESET}}$ is realized by utilizing the reverse breakdown voltage of ZD1. Fig. 2 shows a CT equivalent circuit where $L_{m2}$ is the secondary-side magnetizing inductance and $C_{eq}$ is the associated parasitic capacitance. $v_2$ is the secondary terminal voltage across $N_2$. Fig. 3 shows the base driver circuit in [24] driving a BJT in a buck converter. The drive signal is buffered by U1/2. The emitter-follower stage formed by TR3 and TR4 provides current pulses into and out of the base of TR1 at turn-ON and

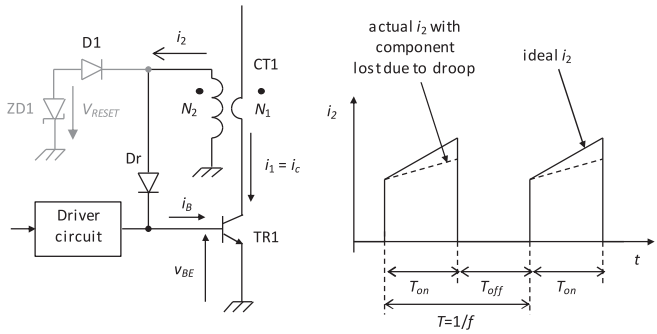


Fig. 1. Outline of base driver circuit with regenerative feedback using a CT from [24].

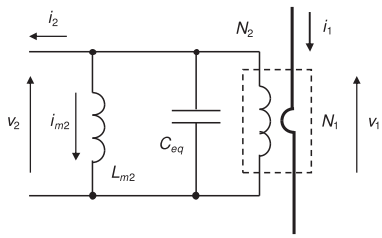


Fig. 2. CT equivalent circuit.

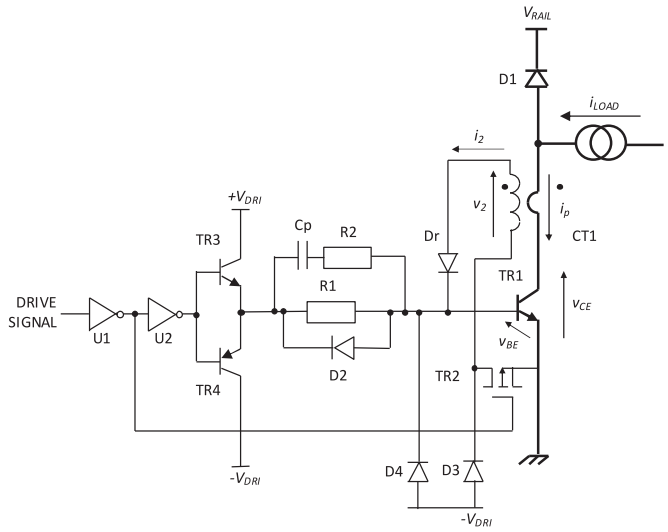


Fig. 3. Proposed driver circuit from [24].

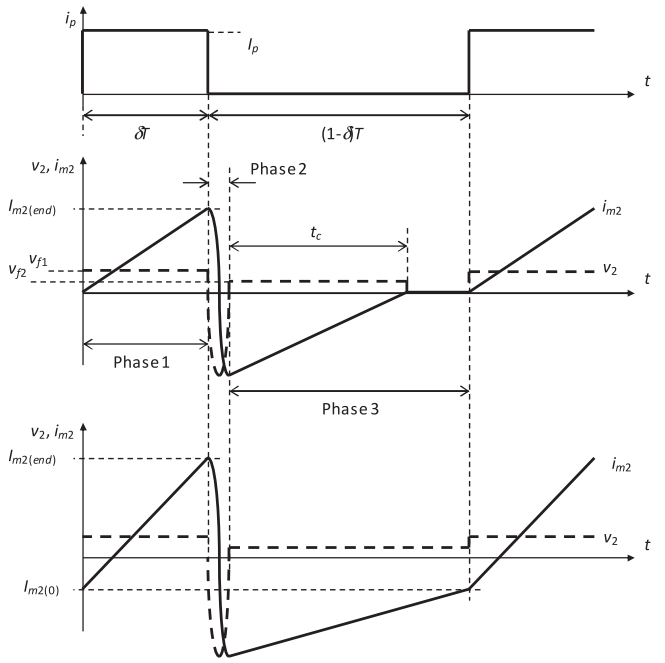


Fig. 4. CT waveforms. Top: Primary current (with ripple content neglected). Centre: Waveforms with DMCM operation. Bottom: Waveforms with CMCM operation.

turn-OFF respectively via the peaking circuit formed by Cp. R2 is included to provide damping [16], [25]. During TR1's ON-time, TR3/4 also provides a small base current into TR1 via R1 to accommodate any shortfall due to magnetizing current $i_{m2}$ drawn by $L_{m2}$.

TR2 is a P-channel MOSFET. When TR1 is OFF TR2 is also held OFF. This prevents $N_2$ from effectively forming a short circuit across $-V_{\mathrm{DRI}}$ when the base of TR1 is low with respect to 0 V. When TR1 is ON, TR2 is also ON to allow a return path for the current supplied by CT1 into TR1's base terminal.

Ideally the relationship between $i_2$ and $i_1$ is given by

$$\frac{i_2}{i_1} = \frac{N_1}{N_2} \tag{2}$$

and therefore

$$\frac{N_1}{N_2} = \frac{i_B}{i_C} \tag{3}$$

but the presence of $i_{m2}$ affects this, and the equivalent circuit shown in Fig. 2 is applied here to cater for $i_{m2}$.

Importantly, the CT shown in Fig. 3 operates without a discrete voltage clamp for resetting its core flux during the BJT's OFF-time. Instead, $i_{m2}$ is allowed to resonate in the *LC* circuit formed by $L_{m2}$ and $C_{eq}$, and this is addressed in further detail in this section.

Provided Dr can support the peak voltage $v_{2(\mathrm{pk})}$ reached, this allows the reset voltage to be accumulated more rapidly than if a discrete clamping circuit were used. In [24], a maximum duty cycle $\delta$ exceeding 90% is readily attainable at a frequency of 50 kHz. Furthermore, only a modest voltage overshoot of approximately 1% was observed across the BJT at turn-OFF due to commutating the current in the CT's leakage inductances in [24]. During the OFF-state, D2 allows the driver stage to clamp TR1's base to $-V_{\mathrm{DRI}}$ and D4 allows Cp to discharge rapidly through R2, thus allowing operation at a high $\delta$.

The circuit shown in Fig. 3 can operate in three modes. These are the discontinuous magnetizing current mode (DMCM), the continuous magnetizing current mode (CMCM), and the discontinuous secondary current mode. Fig. 4 shows a rectangular current waveform $i_p$ with a peak value $I_p$ applied to $N_1$. $i_p$'s period is $T$. The center waveforms show DMCM operation. The bottom waveforms show CMCM operation. The ramp component in $i_p$ is neglected. Dr is rated to support $v_{2(\mathrm{pk})}$. With respect to the DMCM mode in the center waveforms, $i_{m2}$ ramps up in $L_{m2}$ during $T_{\mathrm{on}}$ (Phase 1) and is lost from $i_2$. At the end of $T_{\mathrm{on}}$, $i_{m2}$ has reached $I_{m2(\mathrm{end})}$, given by

$$I_{m2(\mathrm{end})} = \frac{V_{f1}\delta T}{L_{m2}} \tag{4}$$

where $V_{f1}$ is the voltage across $L_{m2}$ during the current pulse. For the circuit shown in Fig. 3, this is given by $V_{\mathrm{BE(on)}} + V_f$, where $V_f$ is the forward voltage drop of Dr, and the voltage drops attributable to the ON-state resistance of TR2 and $N_2$'s resistance are negligible. In the DMCM, $i_{m2} = 0$ A at the beginning of the current pulse. When $I_p$ is removed there is a resonant exchange of energy between $L_{m2}$ and $C_{eq}$ during Phase 2. $v_{2(\mathrm{pk})}$ is given by

$$v_{2(\mathrm{pk})} = \frac{-\delta V_{f1}}{f_{\mathrm{sw}}\sqrt{L_{m2}C_{eq}}} \tag{5}$$

where $f_{\mathrm{sw}}$ is TR1's switching frequency. $v_{2(\mathrm{pk})}$ is fundamentally independent of the magnitude of $I_p$ as $V_{f1}$ does not vary significantly with current. The frequency $f_{\mathrm{res}}$ of the resonant action is given by

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{L_{m2}C_{eq}}} \tag{6}$$

and the resonant period $T_{\rm res}$ is the inverse of this. The damping effect of core losses is neglected in (5) and (6). When the resonant half-cycle has elapsed after a time $T_{\rm res}/2$, Phase 3 commences. $i_{m2}$ then flows through Dr, D2, and the impedance presented by the driver circuit, which causes $i_{m2}$ to decay to zero over a period $t_c$. As TR2 is OFF during this phase, D3 provides a return path for $i_{m2}$ to flow in $N_2$. Whereas in the DMCM mode, $i_{m2}$ decays to zero before the current pulse is reapplied, in the CMCM mode $i_{m2}$ has not decayed to zero at this point. Although $i_{m2}$ passes through zero in the CMCM mode, the term continuous is used here to refer to a state where $i_{m2}$ is only at zero instantaneously.

In the DMCM mode, $I_{m2(\rm end)}$ is given by (4). If $T_{\rm res}$ is taken as much smaller than $T$, then in the CMCM mode, where $I_{m2(0)}$ is the initial $i_{m2}$, $I_{m2(\rm end)}$ can be found from

$$I_{m2(\rm end)} = I_{m2(0)} + \frac{V_{f1}\delta T}{L_{m2}} \tag{7}$$

and

$$I_{m2(0)} = -I_{m2(\rm end)} + \frac{V_{f2}\,(1-\delta)\,T}{L_{m2}}. \tag{8}$$

Combining (7) and (8) yields

$$I_{m2(\rm end)} = \frac{T}{2L_{m2}}\left[V_{f2}\,(1-\delta) + V_{f1}\delta\right]. \tag{9}$$

Where $\delta$ tends to one then, provided the half-resonant period in Phase 2 is allowed to elapse fully

$$I_{m2(\rm end)} = \frac{TV_{f1}}{2L_{m2}}. \tag{10}$$

Similarly, if $V_{f2}$ is close to $V_{f1}$, then when in the CMCM, $I_{m2(\rm end)}$ is also given by (10). The total (peak-to-peak) flux density swing $\Delta B$ in the CT's core material for this scenario is given by

$$\Delta B = \frac{TV_{f1}}{N_2 A_e} \tag{11}$$

where $A_e$ is the CT core's effective area. If $V_{f2}$ is much smaller than $V_{f1}$ then

$$I_{m2(\rm end)} \cong \frac{\delta TV_{f1}}{2L_{m2}}. \tag{12}$$

The threshold duty cycle $\delta_{\rm TH}$ at which the transition between the DMCM and CMCM modes takes place is given by

$$\delta_{\rm TH} = \frac{1}{1+\frac{V_{f1}}{V_{f2}}} \tag{13}$$

and if the ratio $V_{f1}/V_{f2}$ is expressed as $k$, then

$$\delta_{\rm TH} = \frac{1}{1+k}. \tag{14}$$

In summary, with ideal resonant resetting and $V_{f2} \le V_{f1}$, $I_{m2(\rm end)}$ is always restricted to the value in (10), even for $\delta$ approaching 100%. In the CMCM mode, the direction of $i_{m2}$ when $I_p$ is applied is such that $i_2$ exceeds the value given by (2). That is, at the beginning of the current pulse, there is an initial oversupply of $i_2$ as $i_{m2}$ has reversed. Fig. 5 shows $I_{m2(\rm end)}$ against $\delta$ for different values of $k$ for the idealized circuit operation shown in Fig. 4, where losses in the CT are neglected and $T$ is taken as much greater than $T_{\rm res}/2$. Quantities shown in Fig. 5 are normalized to one, where $I_{m2(\rm end)}$ in per-unit form $I_{m2(\rm end)}(\rm pu)$ is given by

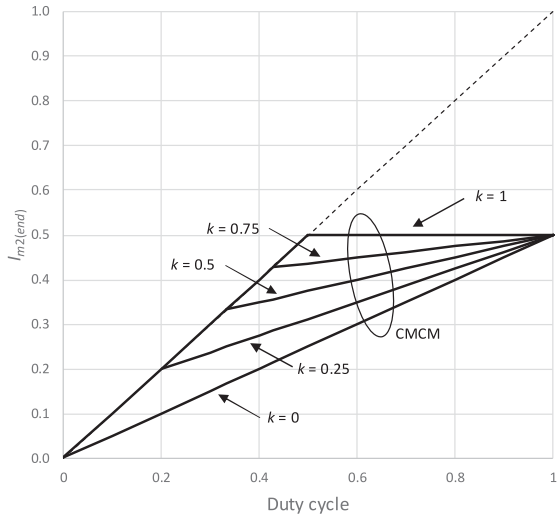


Fig. 5. Absolute droop in the form of $I_{m2(\rm end)}$ normalized to 1 and plotted against $\delta$ for $k$ between 0 and 1. In the DMCM mode, $I_{m2(\rm end)}$ is given by (4). In the CMCM mode, $I_{m2(\rm end)}$ is given by (9). $\delta_{\rm TH}$, where the transition between the DMCM and CMCM modes occurs, is given by (13).

$$I_{m2(\rm end)}\,(\rm pu) = \frac{V_{f1}T}{L_{m2}}. \tag{15}$$

The curves for $k = 1$ and $k = 0$ in the CMCM mode represent the situations in (10) and (12), respectively. Curves for intermediate values of $k$ of 0.25, 0.5, and 0.75 are also shown. If the series combination of $V_f$ and $V_{\rm BE(on)}$ is close to an ideal voltage sink, then $i_{m2}$ is independent of $i_2$. Minimizing $I_{m2(\rm end)}$ has the benefit that the current sourced through R1 to compensate for this loss in current from $i_2$ can also be minimized with a consequent reduction in losses.

### B. CT Core Resetting With Discrete Clamp Circuitry and Maximum Duty Cycle Considerations With the Proposed Circuitry

***1) Resetting With Discrete Clamp Circuitry:*** Power device duty cycles are typically limited to 50% in SMPS applications, but duty cycles close to 100% are normally essential in inverters. In Fig. 6, the effect of using a discrete circuit to apply a reset voltage $v_{\rm RESET}$ is shown.

After an ON-pulse ends, $i_{m2}$ has to be returned to 0 A or less before $I_p$ is reapplied otherwise CT core saturation will occur over a few cycles. The decay in $i_{m2}$ to 0 A during $T_{\rm off}$ takes longer ($t_c$ in Fig. 6) than that with resonant resetting. To avoid CT core saturation, the maximum duty cycle $\delta_{\rm max}$ is limited to

$$\delta_{\rm max} = \frac{1}{1+\frac{V_{f1}}{V_{\rm RESET}}}. \tag{16}$$

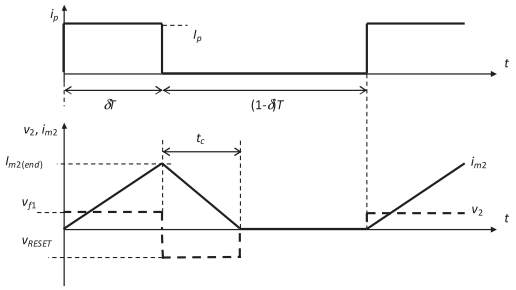


Fig. 6. CT waveforms with discrete reset clamp circuitry.

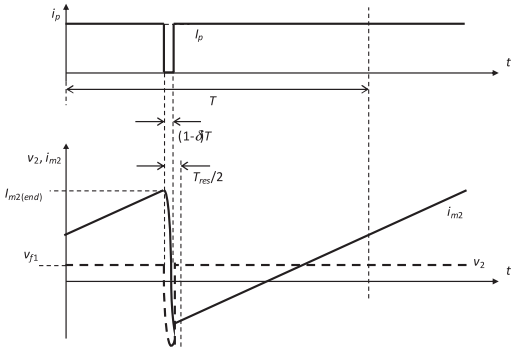


Fig. 7. Waveforms from circuit shown in Fig. 3 with $I_p$ reapplied after $i_{m\,2}$ drops below 0 A, but before the half-resonant period $T_{\rm res}/2$ elapses.

With resetting into a voltage $V_{\rm RESET}$, a lower-voltage rectifier diode than that (Dr) shown in Fig. 3 can be used with the CT. However, a particular drawback in inverter applications is the lower $\delta_{\rm max}$ attainable due to the longer minimum reset time $t_c$ needed.

***2) Duty Cycle Considerations With the Proposed Circuitry:*** With the circuit shown in Fig. 3, the behavior of the CT is only considered here for $T_{\rm off} \geq T_{\rm res}/2$. That is, $I_p$ is not reapplied until $T_{\rm res}/2$ has elapsed and $i_{m\,2}$ has been able to reverse fully. $I_p$ can, however, be reapplied between $T_{\rm res}/4$ and $T_{\rm res}/2$ (where a quarter-cycle or a half-cycle respectively of the resonant action has elapsed) without core saturation occurring as $i_{m\,2}$ is returned to 0 A or less. Waveforms for this scenario are shown in Fig. 7. However, a drawback is that, as $T_{\rm off}$ is reduced from $T_{\rm res}/2$ to $T_{\rm res}/4$, $I_{m\,2(0)}$ rises from the value in (8) to zero. Where $i_{m\,2(0)}$ is zero, it has not been reversed and the current $I_{m2({\rm end})}$ lost into $L_{m\,2}$ at the end of $T_{\rm on}$ rises from the value given by (10) to that in (4). Also, the peak voltage across Dr approximately doubles as $v_{2({\rm pk})}$ increases in magnitude. Furthermore, although there is little change in the total flux density swing, $\Delta B$ given by (11) in the CT's core, the peak flux density reached with respect to zero increases from $\Delta B/2$ to $\Delta B$. For these reasons, $\delta_{\rm max}$ is taken as $(T - T_{\rm res}/2)/T$. If $T_{\rm off}$ is less than $T_{\rm res}/4$, then CT core saturation results.

### C. Circuitry Used for Experimentation

The experimental base driver circuit used in this article is shown in Fig. 8. In [24], the circuit incorporated no galvanic isolation. However, in this article, power is supplied to the

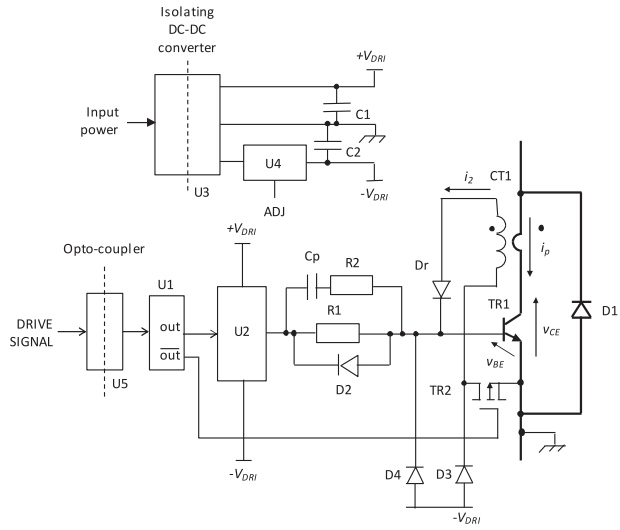


Fig. 8. Outline of BJT base driver circuit with key components shown. A SiC Schottky diode is connected in parallel with the CT's primary winding and the BJT when the BJT is used in a voltage source inverter.

circuit by means of a RECOM RB-0515D isolated-output dc–dc converter, U3, that has an isolation voltage rating of 1 kV and outputs voltages of +15 V and −15 V. The drive signal is transmitted by means of an HCPL3020 opto-coupler, U5, to provide isolation. U1 is an IX4426 driver IC with inverting and non-inverting outputs. The inverting output was used to drive TR2 and the non-inverting output is fed to an IXDN614SI driver IC, U2, which was used to replace the emitter-follower stage in [24]. The signal for the base of TR2 was derived from a 4000-series inverter in [24], but this arrangement was replaced with U1 to give a higher voltage-handling capability. The positive voltage rail, $+V_{\rm DRI}$, is nominally 15 V and is supplied directly by U3. However, the negative rail, nominally at −15 V from U3, is input to an LM337 linear voltage regulator, U4, to allow the base driver's negative OFF-state voltage $-V_{\rm DRI}$ to be varied for experimentation.

Other data are: Cp = 22 nF, R2 = 2.2 Ω, R1 = 180 Ω, D2–4 = ES1A-13-F, Dr = IDD03SG60C, and TR2 = FDT458P. C1 and C2 were 10-$\mu$F ceramic surface-mount types. The BJT does not have an intrinsic diode and the device used was not co-packaged with one, so a C4D15120D device was used in location D1 where a freewheeling function is needed. CT1 was constructed with a TN13/7.5/5 core in 3C90 material with a single primary turn and 43 secondary turns of 0.2-mm copper wire. The quoted inductance factor of the core is 1.17 $\mu$H/turn$^2$ and this gives $L_{m\,2}$ = 2.16 mH. With $V_f$ of Dr = 1 V and $V_{\rm BE(on)}$=3 V, from (10) this gives $I_{m2({\rm end})}$ = 18.5 mA at $f_{\rm sw}$=50 kHz and $\delta$ = 1, and if $k$ is taken as one. R1 was conservatively set to supply a compensating current of 67 mA.

## III. Evaluation of the OFF-State Negative Base-Emitter Voltage Requirement of the SiC BJT

When rapid voltage changes are imposed across the power electrodes of a semiconductor device, unwanted turn-ON may be induced due to current flowing into its control electrode through

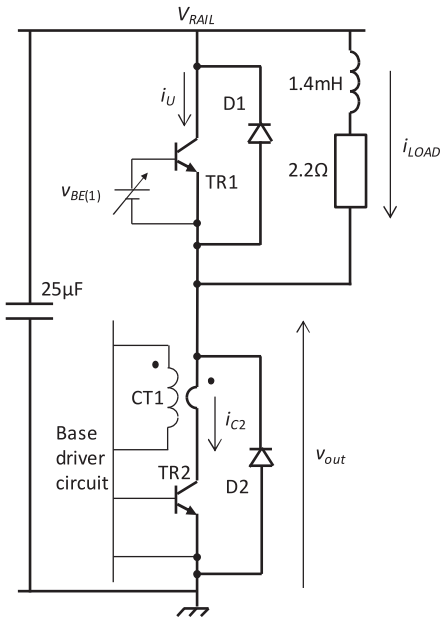


Fig. 9. Circuit used for assessing behavior of the SiC BJT when subjected to a reapplied d$v$/d$t$.

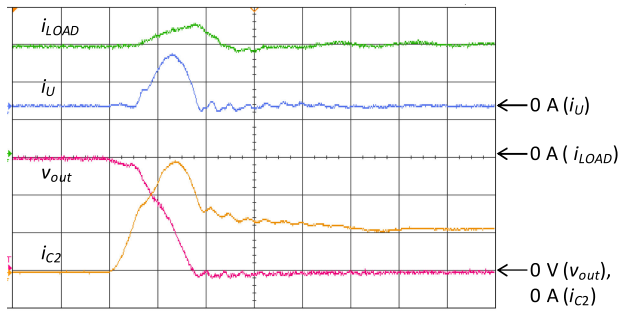


Fig. 10. Exemplifying waveforms for $v_{\mathrm{BE}(1)}=-4$ V with $V_{\mathrm{RAIL}}=600$ V and a temperature of 25 °C. Scales: $i_{\mathrm{LOAD}}=2$ A/div., $i_U=i_{C2}=5$ A/div., and $v_{\mathrm{out}}=200$ V/div. Time scale: 50 ns/div.

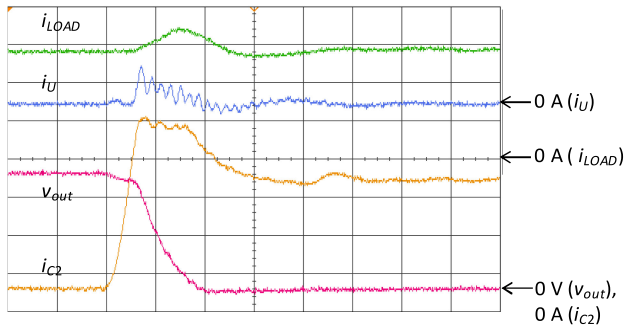


Fig. 11. Exemplifying waveforms for $v_{BE(1)}=-14$ V with $V_{\mathrm{RAIL}}=600$ V and a temperature of 25 °C. Scales: $i_{\mathrm{LOAD}}=i_U=i_{C2}=2$ A/div., and $v_{\mathrm{out}}=200$ V/div. Time scale: 50 ns/div.

its Miller capacitance. Even where the controlling voltage at the device's external terminals is held below the manufacturer's quoted dc turn-ON threshold voltage, turn-ON can nonetheless still result. This is attributable to the internal impedance lying between the terminals and the active die area, and gate or base spreading resistances within the device.

As mentioned in Section I, experimental and theoretical studies have been carried out into the behavior of various power devices when subjected to d$v$/d$t$'s across their power electrodes, for example, the IGBT [26], and the SiC MOSFET [6], [7], [27]. However, less data are available for the SiC BJT and hence the study in this article has been conducted.

Two GA06JT12-247 BJTs [28], TR1 and TR2, were configured in the test circuit shown in Fig. 9. The antiparallel diodes, D1 and D2, were C4D15120D types. TR2 was connected to the driver circuit shown in Fig. 8 and was driven on to apply a d$v$/d$t$ across TR1, the device under test (DUT). TR1 was also driven with the circuit shown in Fig. 8 set in the OFF-state. This was to test the device with a typical driver circuit in place. $v_{\mathrm{BE}(1)}$ was set at different values by configuring U4 in TR1's driver circuit as required. The CT in the driver circuit for TR1 was removed.

Double-pulse tests were then carried out and the displacement charge $Q_D$ through TR1 was measured for various conditions of temperature, rail voltage $V_{\mathrm{RAIL}}$, and TR1's OFF-state $v_{\mathrm{BE}(1)}$. An advantage of double-pulse testing compared with continuous operation is that the temperature of the heatsink on which the DUT is mounted can be readily set at different values with a resistive heater mounted onto the heatsink. The DUT's die temperature will tend to follow that of the heatsink as the steady-state power dissipation is close to zero, and there is consequently little temperature gradient between the die and the temperature recorded on the heatsink's surface. The d$v$/d$t$ applied to the DUT was not varied in these tests, but TR2 was driven to give a switching time of approximately 50 ns, corresponding to an average d$v$/d$t$ $\approx$ 20 V/ns when switching 600 V.

The current $i_U$ through TR1 was measured with a Rogowski coil sensor to give $Q_D$. The current $i_{C2}$ into TR2's collector terminal and the load current $i_{\mathrm{LOAD}}$ were measured with dc current probes. Exemplifying waveforms for $v_{\mathrm{BE}(1)}=-4$ V and $-14$ V are shown in Figs. 10 and 11, respectively. In each case $V_{\mathrm{RAIL}}=600$ V and the heatsink temperature is 25 °C. With $v_{\mathrm{BE}(1)}=-4$ V, it is seen that a transient current $i_U$ flows in TR1 during the fall-time of $v_{\mathrm{out}}$. However, this is significantly reduced with $v_{\mathrm{BE}(1)}=-14$ V. As well as for $i_U$, it is noted that $i_{C2}$ contains current components due to charging and discharging the junction capacitances of D1 and D2, respectively, and a component due to charging stray capacitances associated with the load.

The measured $Q_D$ is shown in Figs. 12 and 13. Fig. 12 shows $Q_D$ plotted against $v_{\mathrm{BE}(1)}$ at 400, 500, and 600 V for temperatures of 25, 50, 75, and 100 °C. Test results are given for $-4$ V to $-14$ V. In Fig. 13, the results at 25 and 100 °C have been superimposed. It is seen that there is little dependency on temperature, although at lower negative $v_{\mathrm{BE}(1)}$ values, a slight reduction in $Q_D$ is observed at higher temperatures. This is attributed to the fall in $h_{FE}$ with increased temperature. The maximum allowable negative base-emitter voltage of the device used is quoted at 30 V by the manufacturer [28] and applying a voltage of $-14$ V results in a safety margin of over 100%.

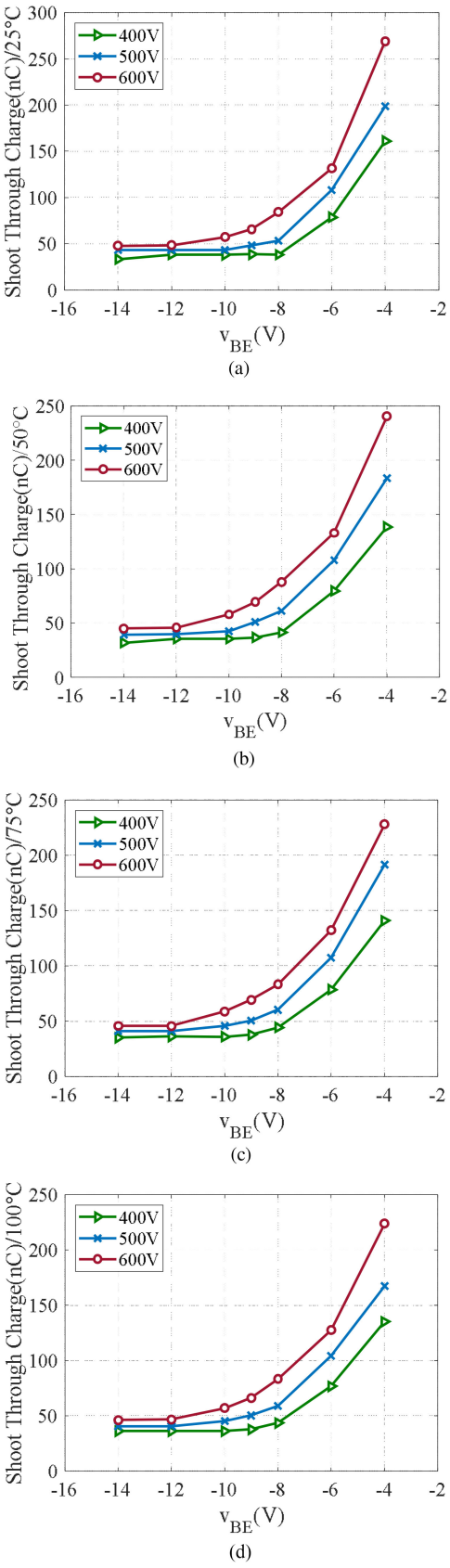


Fig. 12. Displacement charge $Q_D$ plotted against BJT base-emitter OFF-state voltage for different conditions of rail voltage and temperature. (a) Displacement charge at 25 °C. (b) Displacement charge at 50 °C. (c) Displacement charge at 75 °C. (d) Displacement charge at 100 °C.

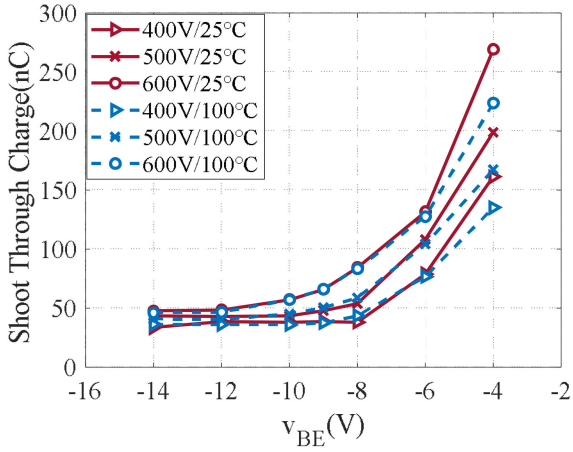


Fig. 13. Superimposed test results at temperatures of 25 and 100 °C.

As expected, the curves of $Q_D$ shown in Figs. 12 and 13 approach plateaus as the reverse OFF-state base-emitter voltage of the DUT is increased. This is attributed to the charge drawn by the inter-terminal capacitances of TR1, and this component in $Q_D$ cannot be eliminated by applying a negative OFF-state base-emitter voltage to the DUT.

The power-dissipation $W_{st}$ incurred in a phase leg at turn-ON due to supplying a displacement charge into the complementary device in a VSC bridge leg is given by

$$W_{st} = Q_D V_{\mathrm{RAIL}} f_{\mathrm{sw}}. \tag{17}$$

Taking the result at $V_{\mathrm{RAIL}} = 600$ V, $v_{\mathrm{BE}(1)} = -4$ V and a temperature of 25 °C, a displacement charge of 225 nC is measured, and this is reduced to 45 nC at $v_{\mathrm{BE}(1)} = -12$ V. At $f_{\mathrm{sw}} = 50$ kHz this represents a loss reduction of 4.5 W, and a total of 13.5 W in a three-phase converter. In practice, however, $W_{st}$ is expected to be higher than the value predicted by (17) due to the modified switching trajectory introduced by the simultaneous conduction attributable to $Q_D$. This is seen in Fig. 10 where $Q_D$ is greater than that shown in Fig. 11, and the turn-ON trajectory of $v_{\mathrm{out}}$ consequently differs.

Before proceeding with inverter operation, the switching characteristics attainable with the proposed base driver were evaluated. The exemplifying waveforms shown in Fig. 14 show the BJT's switching behavior at turn-ON and turn-OFF. Fig. 15 shows switching energy for turn-ON and turn-OFF plotted against the device current when operating at a supply voltage of 600 V [29]. Using the CT driver will reduce the turn-ON loss due to the reduction of current overshoot but slightly increase the turn-OFF loss due to the voltage overshoot.

## IV. Application of the SiC BJT With the Proposed Base Driver Circuit in an Inverter

A three-phase two-level inverter using six of the switch modules shown in Fig. 8 was constructed, Fig. 16, where TR1 and D1 were GA06JT12-247 SiC BJTs and C4D15120D SiC Schottky diodes. A two-stage $LC$ output filter was used and details are: L1 = L2 = L3 = 964.7 $\mu$H, C1 = C2 = C3 = 1.76 $\mu$F,

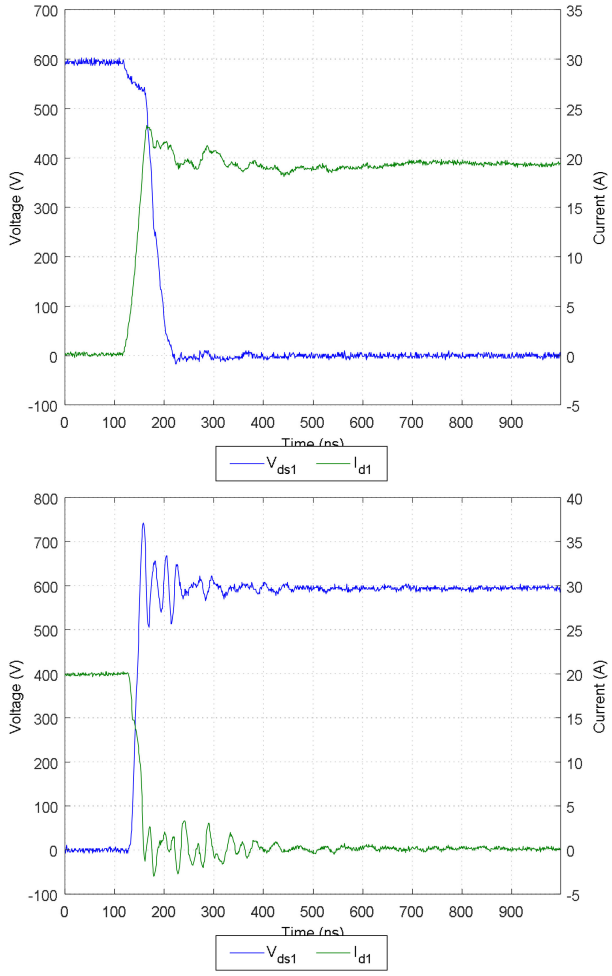


Fig. 14. Switching waveforms at turn-ON (top) and turn-OFF (bottom). $V_{\mathrm{ds1}}$ and $I_{D1}$ refer to $v_{CE}$ and $i_p$, respectively, as shown in Fig. 8.

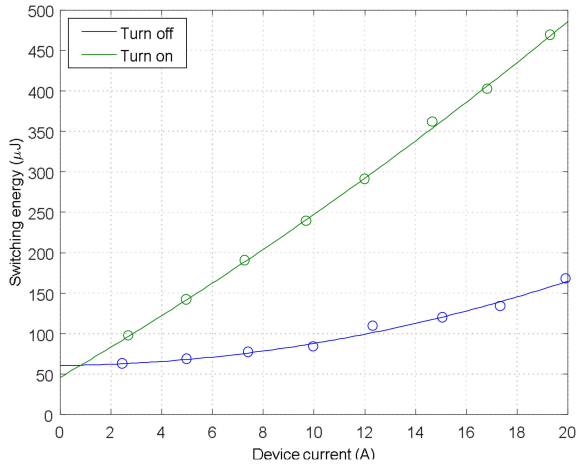


Fig. 15. Switching energy loss at turn-ON and turn-OFF plotted against device current.

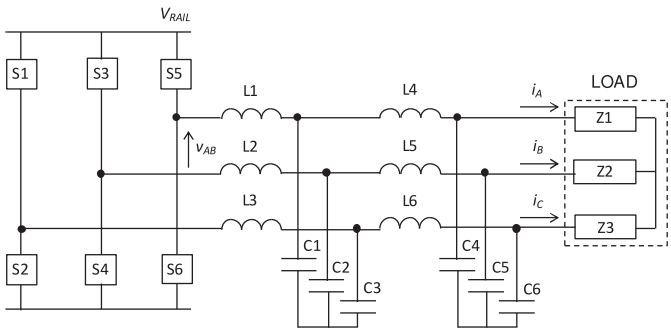


Fig. 16. Experimental inverter.

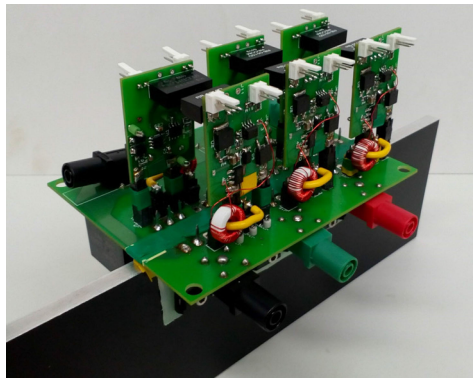

Fig. 17. Experimental inverter showing power devices mounted onto heatsink and base driver circuits.

L4 = L5 = L6 = 50 $\mu$H, and C4 = C5 = C6 = 440 nF. The load was formed with three series *LR* circuits, Z1–Z3, connected in a star arrangement with $L = 646$ $\mu$H and $R = 25$ $\Omega$. A photograph of the inverter is shown in Fig. 17.

$V_{\mathrm{RAIL}}$ was 600 V and the nominal load of 4.1 kW was driven with a modulation index $M$ of 0.9. The control algorithm used deadtime compensation and third harmonic injection. The switching frequency was 50 kHz. Using the results in Section III, an OFF-state base-emitter voltage of $-9$ V was chosen for the BJT base drivers. This was selected to give an aggregate driver rail voltage of 24 V when added to the $+V_{\mathrm{DRI}}$ of 15 V, whilst eliminating most of the $Q_D$ measured in the practical tests in Section III. The resonant frequency $f_{\mathrm{res}}$ of the CT was observed at approximately 500 kHz during experimentation. This corresponds to a period $T_{\mathrm{res}}$ of 2 $\mu$s. In order to allow the half-resonant period $T_{\mathrm{res}}/2$ during Phase 2 shown in Fig. 4 to fully elapse for the reasons given in Section II, a minimum OFF-time of 1 $\mu$s is therefore required. However, a safety margin was included and a minimum OFF-time of 2 $\mu$s was applied, hence giving a maximum $\delta$, and therefore $M$, of 90% at 50 kHz.

Fig. 18 shows waveforms for a fundamental frequency of 400 Hz. $i_A$, $i_B$, and $i_C$ are the three-phase output currents, as denoted in Fig. 16. Fig. 19 shows graphs of the measured efficiency against load, with and without the power consumption of the base driver circuitry included. As the load-dependent component of the base current is supplied by the CT, the driver circuitry drew a power that was nearly constant over the load range and was measured at between 5.30 and 5.37 W. The output phase current has an RMS value of 7.372 A, and therefore a peak value of 10.43 A. When developing the CT-based drive

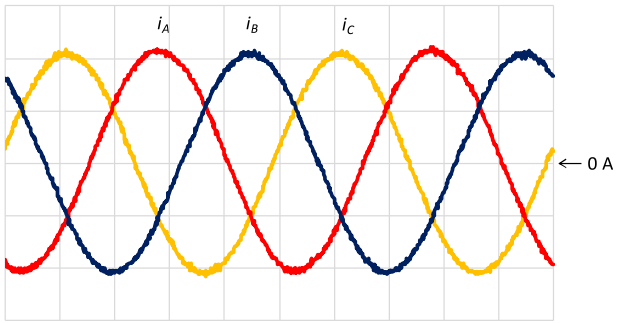


Fig. 18. Output current waveforms from circuit shown in Figs. 16 and 17. Scales: $i_A = i_B = i_C = 5$ A/div. Time scale: 500 $\mu$s/div.

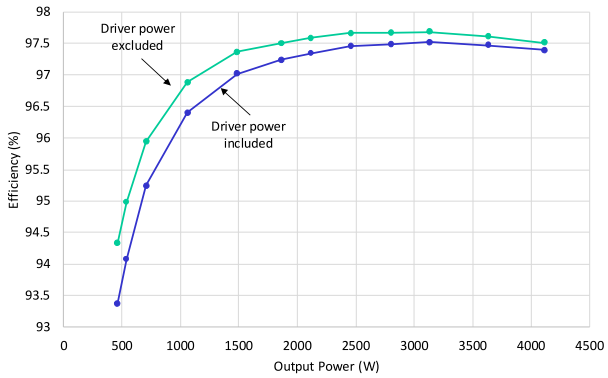


Fig. 19. Efficiency against output power.

the BJTs' $h_{FE}$ was taken as 43. An $i_B$ of 243 mA is therefore required to cover the peak current. If this is set in the normal way, 243 mA is always being supplied into the base of one of the two devices in a phase leg, apart from during deadtimes. If this current is sourced from a 15-V supply, then each phase leg needs to be supplied with 3.65 W, implying a total of 10.95 W solely to furnish the steady ON-state $i_B$ currents. It is noted that the total power drawn will exceed this due to the requirement to supply dynamic base-drive losses, and quiescent losses in the driver circuitry and dc–dc converter shown in Fig. 8.

With the CT-based drivers in place, a conservatively set current of 67 mA is being supplied through R1 shown in Fig. 8 to the base of one of the BJTs in each phase leg at any given time. This equates to 1.005 W per phase when supplied from 15 V, and 3.02 W for all three phase legs. The external power supply therefore only has to supply 28% of the original power of 10.95 W required for driving the steady-state base currents.

Efficiency was measured with two Norma 4000 units. One was used to measure the three-phase output power. The other was used to measure the power from the dc link power supply and the power drawn by the driver circuits. The measured full-load quantities were as follows, where the efficiency figure quoted takes into account the power consumption of the base driver circuitry:

1) DC link voltage $V_{\mathrm{RAIL}}$: 599.8 V.
2) DC input current: 7.044 A.
3) Input power: 4.221 kW.
4) Output phase voltage: 188.1 V.
5) Output phase current: 7.372 A.
6) Output apparent power: 4.160 kVA.
7) Output active power: 4.117 kW.
8) Efficiency: 97.4%.

As seen, the three-phase SiC inverter can operate successfully with the presented base driver and negative OFF-state voltage, and an overall full-load efficiency of 97.4% has been obtained at a 50-kHz switching frequency, with the base driver power consumption accounted for. A fan was used to provide forced cooling of the heatsink, as shown in Fig. 17. The power consumption of the fan was measured at 1.05 W and this was included in the efficiency calculation.

## V. Discussion

Whilst the high duty cycle operation needed for an inverter application is possible, the duty cycle is nonetheless limited to less than 100% due to the need for CT reset. As well as increasing the headroom voltage required by the converter, this precludes the use of dead-banding techniques such as [30]. Complementary drive signals were applied to both devices in each phase leg throughout the entire 360° base frequency cycle.

As the SiC BJT cannot effectively conduct in reverse, the power dissipation in the device and its base driver circuitry can be reduced by applying one-step commutation [31]. With this technique, BJTs in locations where the associated anti-parallel diode is conducting are not driven ON. However, knowledge of the load current direction is required. A feature of the proposed circuitry is that the CT is located directly in series with the BJT and automatically regulates the bulk of the base current in response to the collector current. Advantageously, this means that when the BJT is freewheeling, the load current flows in reverse through the antiparallel diode. Even without one-step commutation being implemented, a power saving is attained as the only losses are those associated with driving transient currents into the base, and the small component sourced via R1.

The power consumption of base driver circuits with and without a CT have been compared when driving the inverter at its rated load, and when sourcing a phase current of 7.372 A. However, this does not take into account the possibility of short-term transient operation with a higher phase current. In this case, the driver circuitry without the CT would have to be configured to source a base current higher than 243 mA. Consequently, the power consumption would be higher than the 10.95 W calculated. Conversely, the CT-based circuit automatically supplies higher base currents under such conditions without the penalty of higher power consumption being incurred during normal operation.

A minimum switch OFF-time of 2 $\mu$s was imposed to accommodate CT reset, and increased harmonic content is expected in the ac current waveform as the minimum OFF-time increases. However, as mentioned in Section IV, a minimum OFF-time of only 1 $\mu$s was observed to be necessary, and the safety margin of 100% that was applied here is conservative. Also, simple PWM was used without incorporating any of the available compensation schemes for reducing harmonic content. Using deadtime

compensation schemes will be future work to compensate the harmonic content and output voltage reduction. A further issue with applying minimum OFF-times is that a higher dc bus voltage is required for a given output ac voltage, with the corollary of higher switching losses in the BJTs. As such, there is a tradeoff between the driver stage losses and switching losses with the proposed circuitry. However, in some applications the existing bus voltage will be at a level higher than that needed to provide the maximum ac voltage required. Also, by reducing the gate driver losses and power requirement using the proposed circuit in this article, a standard gate driver power supply can be used, rather than using a special high power supply. It is noted that the CT's design has not been optimized to maximize its resonant frequency $f_{\rm res}$ for a given droop, and increasing $f_{\rm res}$ reduces the reset time, and therefore the minimum OFF-time required.

A like-for-like comparison between a 4-kW three-phase SiC MOSFET based converter and a three-phase SiC BJT based converter is given in [29]. As shown in [29], the SiC BJT and SiC MOSFET converter have very similar efficiencies, i.e., 97.3% for the BJT converter and 97.65% for the MOSFET converter at 50-kHz switching frequency. Normally, an efficiency above 97% is required for the power stage to meet the power loss and cooling requirement. Therefore, the maximum switching frequency of SiC MOSFET and BJT converters should be around 60–70 kHz to meet the efficiency requirement, also noting that adjusting the gate driver/resistance, or using soft switching may push these switching frequencies even higher.

## VI. Conclusion

Displacement currents in the SiC BJT due to d$v$/d$t$-induced conduction may be readily eliminated by applying a negative OFF-state base-emitter voltage. For the device investigated here, this voltage was experimentally assessed for switched voltages of 400, 500, and 600 V, and at device temperatures of 25, 50, 75, and 100 °C. A base-emitter voltage of $-1$ $\mu$V or lower was found to be sufficient to suppress d$v$/d$t$-induced conduction for d$v$/d$t$'s up to approximately 20 V/ns when driven from a 600-V rail. The SiC BJT used has a maximum quoted negative base-emitter voltage of 30 V. Unlike the SiC MOSFET, there was therefore little compromise required between avoiding exceeding the rated negative control electrode voltage and applying sufficient voltage to hold the device off. The efficacy of using a regenerative proportional base driver circuit with a CT in an inverter application was demonstrated. The difficulty encountered in attaining high duty cycles is addressed by configuring the CT in a driver circuit allowing resonant resetting.

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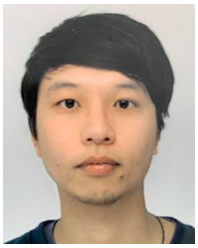

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