ON-Time Mismatch Based System Identification Technique for Buck Converters

Harald Gietler, Marc Kanzian, Christoph Unterrieder, Andreas Berger, Robert Priewasser, Mario Huemer, *Senior Member, IEEE*, and Hubert Zangl, *Member, IEEE*

***Abstract*—This article introduces a fast and low-complexity natural frequency estimation concept for power converters, enabling their adaptive control. Neither a high-resolution analog-to-digital converter nor complex arithmetic operations, such as multiplications, are required by the proposed approach. Instead, the mismatch between the ON-time of the control signal and the effective ON-time at the switching node, occurring under light load conditions, is exploited. This mismatch is caused by the parasitic drain–source capacitance and the parasitic body diode of the power MOSFETs. It is not necessary that the value of the parasitic capacitance is known nor is it required to stay constant, e.g., over temperature. Due to its simplicity, the proposed method is well-suited for practical on-chip realizations. The introduced concept is experimentally verified on the example of a buck converter with different output filter sets. A digital controller is adaptively tuned based on the estimated natural frequency, resulting in an improved dynamic performance. For the presented converter, the magnitude of the output voltage transient in response to a load change was reduced by 30%.**

***Index Terms*—Adaptive control, dc–dc power converters, digital control, parameter estimation, power MOSFET.**

I. Introduction

ALONG with the growing number of electronic devices, the demand for switched-mode power supplies (SMPSs) providing high efficiency and a well-regulated output voltage is rising. Since the SMPSs controller's performance influences the operating range, stability, and efficiency of the system, the use of sophisticated control algorithms is essential [1]–[3]. Due to component tolerances, the controller has to be designed to cover a wide range of parameter values [4]. Additionally, in many industrial applications various sets of external components, i.e., different inductor and capacitor configurations, have to be supported. Thus, the controller has to support an even wider parameter range. In order to ensure stability of the converter in all operating conditions and over all possible configurations, the controller has to be designed in a very conservative way. This degrades the possible dynamic performance. By tracking the parameter variations, the controller can be adapted, such that system performance is improved while stability is maintained [5].

In the scientific community, a large interest in online system identification (SI) concepts for estimating the parameters of a power system exists [6]–[10]. In these methods, the steady-state duty cycle is typically superimposed by a perturbation, e.g., pseudo random binary sequence (PRBS) [11]. This sequence is then used, in conjunction with the resulting output voltage perturbation, to estimate the system parameters. Parametric SI methods assume a fixed model structure and try to identify the model coefficients. The downsides of these approaches are their typically high computational complexity, the memory requirements, and the introduced uncertainties due to the assumption of a fixed model order. Although, recent research reduced the complexity of parametric SI by utilizing advanced estimation algorithms [12], [13], on-chip implementations are still very resource demanding due to the high amount of required memory and arithmetic operations. Nonparametric SI approaches in contrast, e.g., fast Fourier transform (FFT) based methods do not require a model [6]. Nevertheless, the complexity downside typically remains. To reduce the required computational cost, limit cycle oscillation (LCO) based approaches have been proposed in [14] and [15]. By introducing a relay element into the feedback loop, a LCO of the output voltage is caused. Then, from the frequency and amplitude of this oscillation, the natural frequency of the converter can be estimated. In order to cause such a LCO, the ratio between the (analog-to-digital converter) ADC resolution and the digital pulsewidth modulator (DPWM) resolution is decreased on purpose. However, in many applications the resolution of the ADC is always much higher than the resolution of the DPWM. In [15], it is suggested that pulse frequency modulation (PFM) should be used under light load conditions, since the concept proposed therein can otherwise cause instabilities under such operating conditions. But, e.g., due to fixed frequency requirements, it is not always possible to employ PFM. On the one hand, these methods are

Manuscript received December 27, 2018; revised March 20, 2019, June 11, 2019, and July 19, 2019; accepted August 25, 2019. Date of publication September 24, 2019; date of current version April 30, 2020. *(Corresponding author: Harald Gietler.)*

H. Gietler and H. Zangl are with the Institute of Smart Systems Technologies, University of Klagenfurt, 9020 Klagenfurt, Austria (e-mail: harald.gietler@aau.at; hubert.zangl@aau.at).

M. Kanzian, C. Unterrieder, A. Berger and R. Priewasser are with the Infineon Technologies Austria AG, 9500 Villach, Austria (e-mail: marc.kanzian@infineon.com; christoph.unterrieder@infineon.com; andreas.berger@infineon.com; robert.priewasser@infineon.com).

M. Huemer is with the Institute of Signal Processing,Johannes Kepler University Linz, 4040 Linz, Austria (e-mail: mario.huemer@jku.at).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2019.2939982

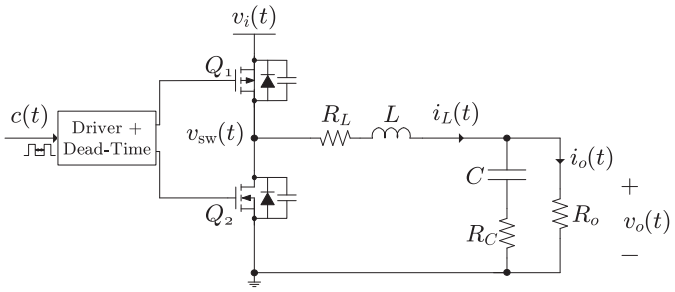


Fig. 1. Simplified schematic of a synchronous buck converter with PMOS high-side and NMOS low-side switch.

computationally less complex than other nonparametric approaches. On the other hand, they typically exhibit larger perturbation amplitudes and lower accuracy than, e.g., FFT-based methods. A well-structured comparison of recent adavances in the online SI field is given in [16].

In this article, a method for estimating the SMPSs natural frequency is proposed. The identification scheme is based on the mismatch between the ON-time of the control signal and the effective ON-time at the switching node. This discrepancy is caused by the parasitic drain–source capacitance and the parasitic body diode of the power MOSFETs. It is emphasized that the suggested approach comes with very limited resource requirements, which makes it suitable for practical on-chip realizations. In contrast to other SI methods [6]–[8], a high estimation accuracy is achieved without the need for complex arithmetic operations, e.g., multiplications. It is worth noting, that the approach achieves the best performance when running under light load conditions. Rather than relying on accurate output voltage measurements sampling of the switching node voltage by a 1-b ADC is sufficient. After the identification process, the estimated natural frequency is used to tune a digital controller to improve the system's dynamic performance.

II. Proposed Concept

In Fig. 1, the schematic of a synchronous buck converter is reported. The power stage consists of a high-side switch Q_1 and low-side switch Q_2. Here, Q_1 and Q_2 are realized as a p-type metal-oxide semiconductor (PMOS) and an n-type metal-oxide semiconductor (NMOS) transistor, respectively. The intrinsic body diodes and drain–source capacitances of the two switches are depicted as well. The output filter inductor is denoted by L and the capacitor by C. The parasitic resistances in the power path and of the capacitor are modeled by R_L and R_C, respectively. The resistance of the load is given by R_o.

Furthermore, $c(t)$, $v_i(t)$, $v_{\mathrm{sw}}(t)$, $i_L(t)$, $i_o(t)$, and $v_o(t)$ denote the control signal of the switches, the input voltage, the switching node voltage, the inductor current, the load current, and the output voltage, respectively. Note that, although a PMOS is employed as a high-side switch Q_1, the presented concept is not restricted to this configuration, but it is also applicable to converters utilizing an NMOS high-side switch.

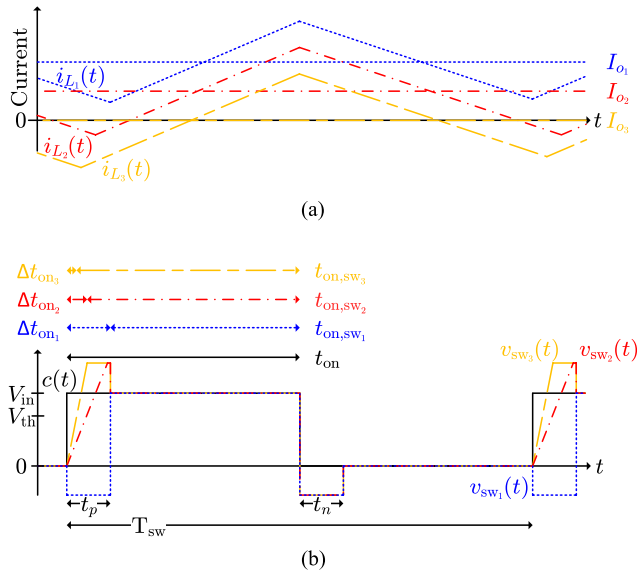


Fig. 2. ON-time mismatch caused by dead-times and conduction of the power MOSFETs' body diodes. (a) Inductor current waveforms for different load currents. (b) Steady-state ON-times t_{on} and $t_{\mathrm{on,sw}}$ of the control command $c(t)$ and the switching node voltage $v_{\mathrm{sw}}(t)$, respectively, for different load currents.

In order to achieve the desired output voltage, the power switches are controlled by the rectangular signal $c(t)$ with duty cycle $d := \frac{t_{\mathrm{on}}}{T_{\mathrm{sw}}}$, where t_{on} and T_{sw} represent the ON-time and the switching period, respectively. In order to prevent shoot-through, i.e., the simultaneous conduction of both Q_1 and Q_2, an appropriate dead-time has to be implemented.

A. Effective ON-Time Mismatch Caused by Deadtimes

The required dead-time influences the behavior of the switching node in a parasitic manner. However, this effect can be used to gather information about the SMPSs. The following sections explain how the dead-time effectively influences the switching node. In Fig. 2(a), the steady-state inductor current waveforms $i_{L_1}(t)$, $i_{L_2}(t)$, and $i_{L_3}(t)$ during a switching period for three different average load currents, denoted as I_{o_1}, I_{o_2}, and I_{o_3}, are shown. For small load currents, such as I_{o_2} and I_{o_3} in Fig. 2(a), a negative inductor current can be observed during a fraction of the switching period.

In Fig. 2(b), the control signal $c(t)$ and the switching node voltages $v_{\mathrm{sw}_1}(t)$, $v_{\mathrm{sw}_2}(t)$, and $v_{\mathrm{sw}_3}(t)$, corresponding to the inductor current waveforms of Fig. 2(a), are depicted. At the rising edge of $c(t)$, the low-side switch Q_2 is turned OFF, while the high-side switch Q_1 is still kept off for the duration of the dead-time t_p. Depending on the sign of $i_L(t)$ during t_p, two cases, namely

1) $i_L(t) >= 0$
2) $i_L(t) < 0$

have to be considered [17].

Case 1: $i_L(t) >= 0$

If $i_L(t)$ is positive during t_p, e.g., $i_{L_1}(t)$ in Fig. 2(a), the body diode of Q_2 starts to conduct, since the potential at $v_{\mathrm{sw}}(t)$ is negative, as shown by $v_{\mathrm{sw}_1}(t)$.

The delayed turn-ON of Q_1 causes a mismatch $\Delta t_{\mathrm{on}_1} := t_{\mathrm{on}} - t_{\mathrm{on,sw}_1}$, equal to t_p, between the steady-state ON-times t_{on} and $t_{\mathrm{on,sw}_1}$ of $c(t)$ and $v_{\mathrm{sw}_1}(t)$, respectively. The ON-time $t_{\mathrm{on,sw}_1}$ is defined as the time span between $v_{\mathrm{sw}_1}(t)$ exceeding a specified threshold V_{th} and falling below this threshold. Here, V_{th}, which is a design parameter in the proposed SI approach, is chosen to be $\frac{2}{3} \cdot V_i$ for illustration purposes, with V_i representing the steady-state input voltage.

Case 2: $i_L(t) < 0$

If the coil current $i_L(t)$ is negative at the beginning of the switching period, as it is true for $i_{L_2}(t)$ and $i_{L_3}(t)$ in Fig. 2(a), the body diode of Q_2 does not start to conduct. Instead, caused by the reverse direction of the current $i_L(t)$, the parasitic drain–source capacitances of Q_1 and Q_2 are charged. Consequently, the potential of the switching node $v_{\mathrm{sw}}(t)$ gradually increases as depicted by $v_{\mathrm{sw}_2}(t)$ and $v_{\mathrm{sw}_3}(t)$. If $v_{\mathrm{sw}}(t)$ exceeds the supply voltage $v_{\mathrm{i}}(t)$, the body diode of Q_1 starts to conduct. This yields a shorter turn-ON delay compared to the previous case of always positive current $i_{L_1}(t)$. Thus, the ON-time mismatch Δt_{on} is reduced, as shown in Fig. 2(b) for Δt_{on_2} and Δt_{on_3}. With more negative $i_L(t)$, the mismatch Δt_{on} also shortens, since the steepness of $v_{\mathrm{sw}}(t)$ increases due to the faster charging of the parasitic drain–source capacitances. Regarding Fig. 2(a), it is worth noting that the negative current peaks of $i_{L_2}(t)$ and $i_{L_3}(t)$ are linearly approximated. For simplicity, the quadratic behavior of $i_{L_2}(t)$ and $i_{L_3}(t)$ during the charging of Q_1's and Q_2's drain–source capacitance is neglected in this schematic view. As a consequence of the linear approximation, the valley points of the coil currents occur at different time instances.

Generally, the same switching node behavior can happen at the falling edge of $c(t)$. If $i_L(t)$ is positive, Q_1 is turned OFF and the body diode of Q_2 starts to conduct during the dead-time t_n. Instead, for negative coil current during t_n, the drain–source capacitances of Q_1 and Q_2 are charged and Q_1's body diode starts to conduct, hence $t_{\mathrm{on,sw}}$ increases.

Note that, a fixed dead-time has been presumed for the presented analysis. In practice, drivers with a dynamic dead-time control are often employed. Such control would be detrimental to the natural frequency estimation approach suggested in the next section. However, a fixed dead-time is only required during the estimation phase. As will be discussed later in more detail, the estimation can be carried out, e.g., during converter start-up, where a fixed dead-time may be configured.

B. Natural Frequency Estimation

A parameter which can be used for controller tuning is the natural frequency [1], [14]. For the presented buck converter model, this frequency can be calculated by [12]

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{R_o + R_L}{LC\,(R_o + R_C)}} \tag{1}$$

if the exact component values are known.

TABLE I
SYNCHRONOUS BUCK CONVERTER PARAMETERS

Parameter	Value	Parameter	Value
V_i	3.3 V	R_o	8.3 Ω
V_o	1.35 V	$I_{o\max}$	500 mA
L	3.3 µH	T_{sw}	1 µs
C	22 µF	f_0	18.8 kHz
R_C	10 mΩ	f_d	18.5 kHz
R_L	105 mΩ	t_p, t_n	20 ns

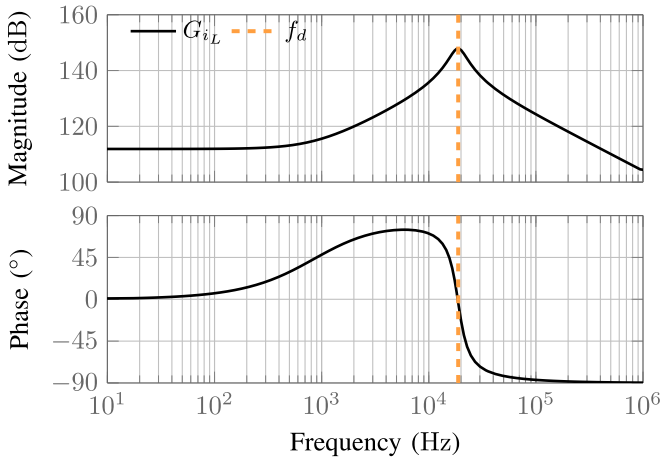


Fig. 3. Frequency response of the small-signal ON-time to inductor current TF.

In the following, a concept for obtaining an estimate of the natural frequency f_0 by exploiting the ON-time mismatch caused by the effect explained before is proposed. For this purpose, the converter is operated under light load conditions with partially negative coil current. This causes the body diode of the high-side switch Q_1 to conduct. As a stimulus to the system, the ON-time is perturbed with $\tilde{t}_{\mathrm{on}}(t)$ around its steady-state value t_{on}. Applying the state-space averaging approach [18] to the converter, yields the small-signal ON-time $\tilde{t}_{\mathrm{on}}(t)$ to inductor current $\tilde{i}_L(t)$ transfer function (TF)

$$G_{i_L}(s) = \frac{\tilde{i}_L(s)}{\tilde{t}_{\mathrm{on}}(s)} = \frac{V_i}{L}\,\frac{s + \frac{1}{C(R_o+R_C)}}{s^2 + 2\zeta\omega_0 s + \omega_0^2}\,\frac{1}{T_{\mathrm{sw}}} \tag{2}$$

with the natural angular frequency

$$\omega_0 = 2\pi f_0 \tag{3}$$

the damping factor

$$\zeta = \frac{L + C\,(R_o R_C + R_o R_L + R_C R_L)}{2LC\,(R_o + R_C)\,\omega_0} \tag{4}$$

and the Laplace variable s. From (2), it follows that the peak value of the inductor current depends on the ON-time perturbation frequency. The amplitude and phase response of $G_{i_L}(s)$, using the converter parameters from Table I, are visualized in Fig. 3.

As illustrated, the peak in magnitude occurs at the frequency f_d. To be more precise, the amplitude of the inductor current increases the most for an ON-time perturbation frequency of

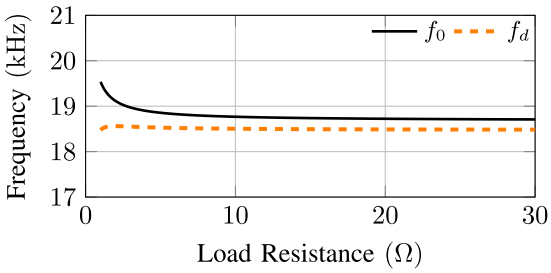


Fig. 4. Evolution of the natural frequency f_0 and the damped natural frequency f_d, when sweeping the load resistance R_o from 1 Ω to 30 Ω.

$\omega_d = 2\pi f_d$, which can be calculated from (2) to be [19]

$$\omega_d = \omega_0 \sqrt{1-\zeta^2}. \tag{5}$$

This so-called damped natural angular frequency ω_d is close to ω_0 for the unloaded converter, because the damping factor ζ decreases with decreasing load current.

The effect of the load on f_0 and f_d is analyzed and reported in Fig. 4, where R_o is swept from 1 Ω to 30 Ω. Again, the used converter parameters are as listed in Table I. The natural frequency f_0 as well as the damped natural frequency f_d are visualized. The highest difference between f_0 and f_d is approximately 1 kHz, which is negligibly small when considering controller tuning. Hence, the objective of the SI scheme proposed in this article is to obtain an estimate $\hat{f}_d$ of f_d with the approach outlined in the following paragraphs. Further note that, the natural frequency and the converter's TFs are far more sensitive with respect to variations in L and C as to different load conditions. In fact, for a pure current sink load, the small-signal control TFs are independent of the actual load current. For this reason, although the estimation procedure has to be carried out under light load conditions, the dynamic performance is also improved for higher load levels as will be shown in Section III-C.

In the following, the effect of different ON-time perturbations on the inductor current and subsequently the effect on the ON-time mismatch is explained and visualized using the commercial circuit simulator SIMetrix/SIMPLIS. For that, t_{on} is superimposed by a 9.5 kHz sinusoidal perturbation $\tilde{t}_{\mathrm{on}_1}(t)$ with a peak-to-peak amplitude of 100 ns. Fig. 5 shows the relations between the ON-time modulation $\tilde{t}_{\mathrm{on}_1}(t)$, inductor current $i_L(t)$, switching node voltage $v_{\mathrm{sw}}(t)$, and effective ON-time mismatch

$$\Delta\tilde{t}_{\mathrm{on}_1}(t) := t_p + \underbrace{t_{\mathrm{on}} + \tilde{t}_{\mathrm{on}_1}(t)}_{t_{\mathrm{on}}(t)} - t_{\mathrm{on,sw}_1}(t). \tag{6}$$

Here, $t_{\mathrm{on}}(t)$ represents the duty cycle of the control signal $c(t)$, composed of its steady-state value t_{on} and the small-signal component $\tilde{t}_{\mathrm{on}_1}(t)$ at the perturbation frequency. Furthermore, $t_{\mathrm{on,sw}_1}(t)$ denotes the ON-time as measured at the switching node $v_{\mathrm{sw}}(t)$. Note that, t_p is included in $\Delta\tilde{t}_{\mathrm{on}_1}(t)$ in order to remove the offset in the ON-time mismatch caused by the dead-time. The ON-time modulation causes negative inductor currents and subsequently, a conduction of Q_1's body diode, which leads to an ON-time mismatch $\Delta\tilde{t}_{\mathrm{on}_1}(t)$. As shown in Fig. 5(b), the highest mismatch happens at the lowest average current. Further

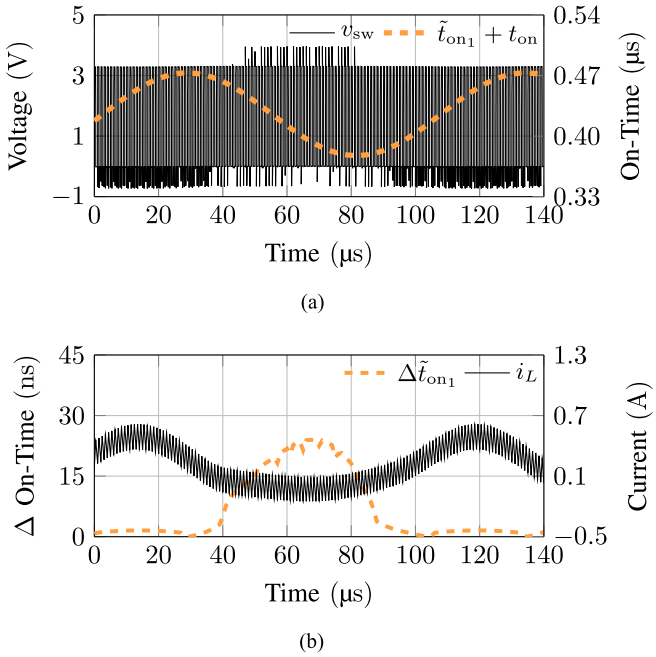


Fig. 5. (a) Switching node behavior due to a sinusoidal 9.5 KHz perturbation of the control signal. (b) Effect on the coil current and the effective ON-time mismatch.

observe the voltage spikes above the supply voltage of 3.3 V and the voltage drops below 0 V. In Section II-A, the parasitic body diodes of the power switches were identified as the sources of these phenomena. As the simplified switching waveforms in Fig. 2 show, exactly these effects are exploited by the proposed approach in order to estimate the natural frequency of the converter.

As already discussed, the average coil current depends on the frequency of the ON-time perturbation. To clarify, a second case with an ON-time modulation $\tilde{t}_{\mathrm{on}_2}(t)$ is shown in Fig. 6. Its frequency and peak-to-peak amplitude have been selected as 19 kHz and 100 ns, respectively. In this case, the perturbation frequency is close to the damped natural frequency f_d of the converter and therefore, as shown in Fig. 6(b), yields a higher peak inductor current. Thus, a larger ON-time mismatch $\Delta\tilde{t}_{\mathrm{on}_2}(t)$, compared to $\Delta\tilde{t}_{\mathrm{on}_1}(t)$, is caused. It can be observed, that the ON-time mismatch saturates quickly. To avoid this, the amplitude of the chirp signal can be lowered. Furthermore, the length of the dead-time needs to be taken into account when designing the chirp waveform in order to avoid saturation. To ensure that the presented approach works, the coil current must not saturate, because nonlinear effects are not well-covered in the approach, i.e., the prediction for high load situations might become too poor. This needs to be considered during the design phase of the converter and the natural frequency estimation approach. In contrast to that, a wide class of overcurrent protection implementations, i.e., saturation of positive currents, do not influence the approach, since the information is obtained by exploiting negative coil currents. Other overcurrent protection schemes, e.g., permanent or nonpermanent shut down, may distort the identification process, which needs to be considered.

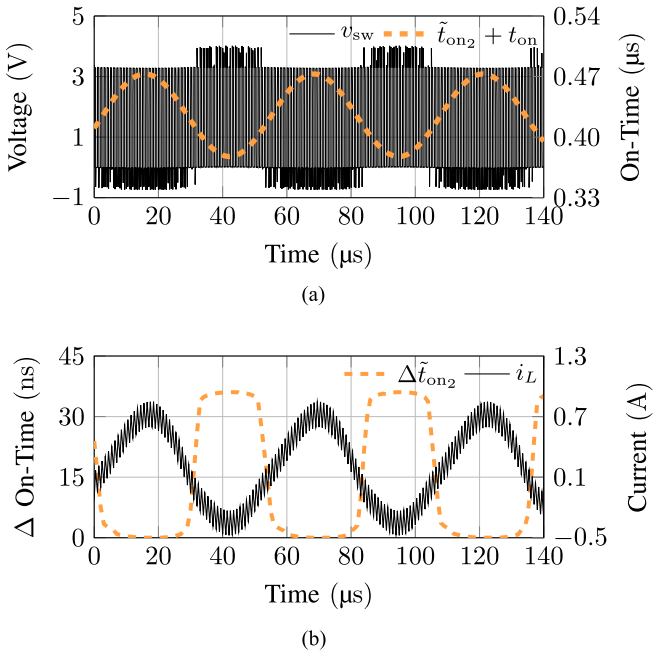


Fig. 6. (a) Switching node behavior due to a sinusoidal 19˜KHz perturbation of the control signal. (b) Effect on the coil current and the effective ON-time mismatch.

As can be concluded from Section II-A and II-B, the largest effective ON-time mismatch $\Delta\tilde{t}_{on}(t)$ is observed at f_d. Since the switching period T_{sw} is kept constant, the natural frequency of the converter can be estimated by superimposing t_{on} with a perturbation $\tilde{t}_{on}(t)$ and measuring the resulting ON-time $t_{on,sw}(t)$ of $v_{sw}(t)$. By selecting a linear chirp signal [20] $\tilde{t}_c(t)$ as the perturbation $\tilde{t}_{on}(t)$, a wide frequency range can be covered and the estimate $\hat{f}_d$ can be simply derived from the time instant at which the maximum of $\Delta\tilde{t}_{on}(t)$ occurs.

To that end, a simulation for a converter with the parameters listed in Table I has been carried out. A chirp signal with a duration of $t_d = 0.5$ ms, a start frequency of $f_s = 1$ kHz and a stop frequency of $f_e = 60$ kHz has been selected as the perturbation $\tilde{t}_c(t)$.

It is worth noting that prior knowledge about the converter needs to be available, since the frequency range of the perturbation has to cover f_d. Therefore, the possible range of f_d has to be known beforehand. The frequency of the chirp increases linearly over time, satisfying

$$f(t) = \frac{f_e - f_s}{t_d} t + f_s. \tag{7}$$

When selecting the rate of frequency change of the chirp waveform, the switching frequency of the converter needs to be taken into account. A lower switching frequency would lead to a lower chirp frequency resolution for a given perturbation time. The average frequency resolution of the chirp f_r, as a design parameter, is given by

$$f_r := \frac{T_{sw}(f_e - f_s)}{t_d}. \tag{8}$$

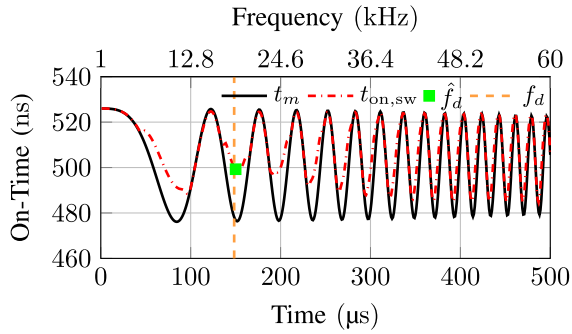


Fig. 7. ON-times $t_m(t)$ and $t_{on,sw}(t)$ of $c(t)$ and $v_{sw}(t)$, respectively, during injection of a linear chirp stimulus. The largest mismatch $\Delta\tilde{t}_{on}(t)$ is observed at the estimated damped natural frequency $\hat{f}_d$.

As (8) shows, t_d determines the achievable frequency resolution f_r. Therefore, for narrower frequency ranges $(f_e - f_s)$, i.e., for smaller variations between the possibly employed filter sets or uncertainties of passive components, t_d can be reduced without sacrificing frequency resolution. Note that, during the positive half-wave of the coil current, the frequency of the perturbation increases but negative coil currents do not occur. As a consequence, the effective resolution is decreased and moreover nonuniformly distributed. To counteract this effect and improve the accuracy, one can increase the chirp resolution. However, a second run of the identification scheme with a 180° phase shifted chirp is more effective. The second run covers the previously positive half-waves. Consequently, such an approach prolongs the system excitation time. As a result, a tradeoff between estimation accuracy and perturbation time has to be made.

Furthermore, the amplitude A_c of $\tilde{t}_c(t)$ has to be chosen such that negative coil currents during stimuli injection are guaranteed. First, the parameter set with the lowest gain at the resonant frequency, i.e., the worst case, is found via simulation. Then, with the peak and valley of the inductor current during stimuli injection given by

$$I_{L,\pm} \approx I_o \pm |G_{i_L}(j\omega_d)| A_c \tag{9}$$

the required chirp amplitude A_c that guarantees negative coil current, i.e., $I_{L,-} < 0$, for a certain steady-state output current level I_o can be calculated by substituting $|G_{i_L}(j\omega_d)|$ in (9) with the determined worst case gain. In the investigated example, the amplitude A_c of $\tilde{t}_c(t)$ has been set to 25 ns.

The chirp modulated ON-time $t_m(t) := t_{on} + \tilde{t}_c(t)$ of the control signal $c(t)$, as well as the effective ON-time $t_{on,sw}(t)$ at the switching node $v_{sw}(t)$ are reported in Fig. 7. The largest mismatch $\Delta\tilde{t}_{on}(t)$ can be observed at approximately 150 μs. With (7), the estimated damped natural frequency $\hat{f}_d = 18.7$ kHz, which is close to the true value $f_d = 18.5$ kHz, is readily calculated.

Although the basic principle of the proposed natural frequency estimation approach is described for a buck converter, it is applicable to other topologies such as multiphase buck converters. For such a topology, the ON-times of the individual phases can be perturbed in a time-multiplexed manner [21]. Then, the ON-time mismatches can be determined by the same

procedure as for a conventional buck converter. In this way, the natural frequencies of all phases are obtained. However, a more in-depth analysis of the proposed estimation approach for other converter configurations and topologies, e.g., multiphase and boost, is beyond the scope of this article.

C. Controller Tuning

Usually, power converter designers would like to offer a single controller for a list of different L–C sets. Depending on the system requirements, the user can then directly decide in the application which output filter set to use. Commonly, the user needs to adjust register settings or external wiring to select the correct controller parameters for the chosen set. The proposed identification scheme can be utilized to, e.g., automatically determine the employed L–C set and load the predefined controller coefficients without any action of the user. Apart of that, various auto-tuning approaches to use the gathered information exist [1], [22].

To show the benefits of the proposed low-complexity SI method, a controller update scheme, which focuses on simplicity, is presented. For that, the estimated damped natural frequency $\hat{f}_d$ is used to tune a digital controller with the objective of improving the dynamic performance. A proportional–integral–derivative voltage mode controller in parallel form with its discrete-time TF given as [1]

$$C(z) = K_{p,m} + \frac{K_{i,m}}{1 - z^{-1}} + K_{d,m}\left(1 - z^{-1}\right) \tag{10}$$

with $K_{p,m}$, $K_{i,m}$, and $K_{d,m}$ denoting the proportional, integral, and derivative gain, respectively, and $z := e^{sT_{\mathrm{sw}}}$, has been selected. Initially, the controller gains are designed based on the worst case converter parameters, e.g., component tolerances of the L–C filter, indicated by the subscript m, thus ensuring stability under all operating conditions and parameter variations. In this context, worst case parameters refers to the component set that yields the lowest natural frequency, i.e., a configuration with the highest value for both L and C. The damped natural frequency $f_{d,m}$ of the converter with worst case parameters is calculated by (5). After the estimate $\hat{f}_d$ is obtained by the proposed method, the controller is tuned. As a first step, a correction factor

$$\kappa := \frac{\hat{f}_d}{f_{d,m}} \tag{11}$$

is introduced. Utilizing this correction factor, it is possible to calculate tuned controller coefficients. In this article, which focuses on a low-complexity implementation, it is proposed to simply scale the initial controller coefficients by the correction factor κ, yielding the tuned coefficients

$$K_{p,t} = \kappa K_{p,m} \tag{12a}$$

$$K_{i,t} = \kappa K_{i,m} \tag{12b}$$

$$K_{d,t} = \kappa K_{d,m}. \tag{12c}$$

Here, the subscript t denotes the tuned controller coefficients. Despite its simplicity, the presented tuning method improves the dynamic performance of the controller. However, adapting the control coefficients is not in the main scope of this article. Rather, it showcases the benefits of gathering information about system parameters, which may change over time, e.g., due to aging of components. The possible improvements in terms of dynamic performance are affirmed by the experimental results presented in Section III.

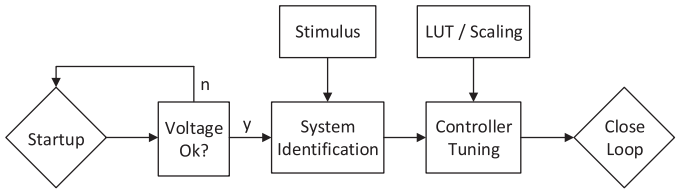


Fig. 8. Flowchart of the ON-time mismatch based SI process.

Furthermore, it is important to stress that the presented approach only estimates the natural frequency of the converter, which can then be employed for the tuning of the controller. While this parameter is especially suited as a basis for controller tuning, other system parameters such as the damping factor are not obtained. Consequently, the maximum theoretically achievable dynamic system performance may not be reached. However, in many applications scenarios the natural frequency varies over a wide range, e.g., because different L and C sets have to be supported by a single controller. In such cases, an estimate of the natural frequency alone can already be effectively used to improve the dynamic performance of the converter. In contrast to that, a more precise tuning may be achieved with methods that estimate a TF model of the converter. Nevertheless, due to their computational complexity, such approaches are often not feasible for a practical on-chip realization. Hence, the proposed solution is especially suited for applications where low power and area consumption are key figures.

The entire process is summarized in a flowchart reported in Fig. 8. In the considered application, the voltage is ramped up during start-up. After reaching a certain stable voltage level, the chirp stimulus is added to the constant open-loop duty cycle. As described previously, the behavior of the switching node during dead-times is observed and used to estimate the natural frequency of the converter. The deduced information is then used to find appropriate controller coefficients, e.g., in a lookup table or by scaling the coefficients. Finally, the control loop is closed and the converter is operated in normal mode.

D. Implementation

In Fig. 9, the schematic of the proposed digital implementation is reported. During SI, a stimuli generator is used to generate the perturbation $\tilde{t}_c[k]$ for the kth switching cycle. Since the proposed approach requires the ON-time mismatch $\Delta\tilde{t}_{\mathrm{on}}[k]$, the ON-times $t_m[k]$ and $t_{\mathrm{on,sw}}[k]$ have to be available in the digital system. As the control command $c(t)$ is generated by the system, its ON-time $t_m[k]$ is known. It is emphasized that a single ADC, e.g., a simple comparator, in combination with a digital counter is sufficient to measure the effective ON-time on the switching node. In detail, for measuring the ON-time of

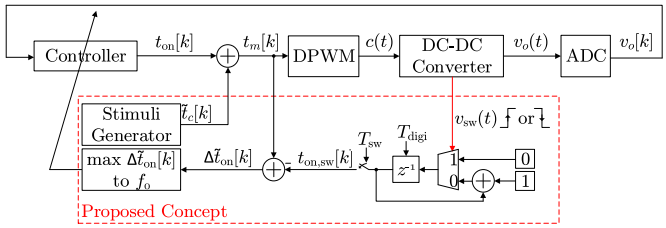


Fig. 9. Schematic of the proposed digital implementation of the natural frequency estimation approach.

$v_{sw}(t)$, a counter operating at a high rate $\frac{1}{T_{digi}}$, with $T_{digi} \ll T_{sw}$, is used. This counter is reset upon a rising edge of $v_{sw}(t)$ and stopped upon a falling edge of $v_{sw}(t)$. The comparator is used to detect the transition edges. In the prototype, the transition edges are detected according to the 3.3 V CMOS input logic level thresholds. The counter yields the ON-time $t_{on,sw}(t)$ of $v_{sw}(t)$ with a resolution of T_{digi}.

Since the resolution of $\Delta\tilde{t}_{on}[k]$ is given by T_{digi}, the proposed approach requires a high-frequency clock for the counter, which measures the ON-times. The upper bound of $\Delta\tilde{t}_{on}[k]$, which would be observed if the body diode of Q_1 fully conducts during both t_p and t_n, is given as $\Delta\tilde{t}_{on_{max}} := t_p + t_n$. From that, the number n of possible $\Delta\tilde{t}_{on}[k]$ values is determined as

$$n := \frac{\Delta\tilde{t}_{on_{max}}}{T_{digi}}. \tag{13}$$

Consequently, the clock frequency of the counter has to be chosen such that n is large enough in order to detect the perturbation frequency dependency of $\Delta\tilde{t}_{on}[k]$. In a digital controller, such a clock signal is typically available, since it is also required by, e.g., the DPWM sawtooth carrier or the digital part of the driver. In principle, it is also possible to measure the switching nodes' ON-time $t_{on,sw}(t)$ in the analog domain. The disadvantage of such an approach is the additionally required ADC, which increases the overall system complexity.

Based on the time instant at which the largest mismatch $\max|\Delta\tilde{t}_{on}[k]|$ occurs, $\hat{f}_d$ is calculated by (7). During the identification sequence, only slow changes of t_{on} are allowed. Compared to state-of-the-art SI approaches [23]–[26], the proposed SI scheme is fast and can therefore be implemented during start-up of the converter. In this article, the SI procedure is embedded in the start-up sequence of the converter right after the open-loop voltage ramp-up, where t_{on} is commonly changed slowly. Consequently, the converter start-up is artificially prolonged by the perturbation duration t_d, therefore, a fast approach is crucial. Many applications restrict the perturbation to happen in specified time-slots due to strict output-voltage specifications. The output voltage restrictions during start-up of the converter are usually more relaxed, e.g., a tight regulation is not required and it is sufficient for the output voltage to stay within specified limits. Furthermore, since the chirp signal is superimposed onto a constant duty cycle, stability issues, which may arise in LCO methods [15], are not a concern with the proposed approach. After the SI phase has finished, the controller coefficients are updated according to (11) and (12). Finally, the converter can enter its closed-loop operation mode with the tuned controller coefficients.

TABLE II
OUTPUT FILTER CONFIGURATIONS

Set	Inductor	Capacitor	Natural Frequency
1	3.3 µH	25 µF	17.5 kHz
2	4.7 µH	32 µF	13.0 kHz
3	2.2 µH	17 µF	26.0 kHz
4	3.3 µH	10 µF	27.9 kHz
5	2.2 µH	10 µF	33.9 kHz

Typically, converter parameters such as the inductance and capacitance values also vary during operation, e.g., caused by temperature changes. Hence, the dynamic performance may degrade. As for other SI methods, the stimuli injection phase has to be carried out again to detect changes in the natural frequency of the converter. One possible approach is to repeat the injection at specific time intervals. In the application scenario considered, the natural frequency estimation is carried out at converter start-up only, since variations in L and C are dominated by the wide range of possibly employed component sets and aging effects. In contrast to these causes, the impact of, e.g., inductor current, capacitor voltage, and temperature on the inductance and capacitance values is minor for the selected components.

III. EXPERIMENTAL RESULTS

A prototype comprised of a buck converter and a field programmable gate array (FPGA) has been assembled to verify the concept presented in the previous section. The parameters of the buck converter, as used in the simulation, are reported in Table I.

The experiments have been carried out for five different output filter configurations, which are listed in Table II. Note that the used coils do not saturate during the SI procedure. The natural frequency in Table II is calculated by (1), assuming an unloaded converter. The effect of the load on the natural frequency, shown in Fig. 4, is negligibly small compared to the frequency variation of the different output filter sets. The natural frequency estimation as well as the digital controller and its auto-tuning logic have been implemented on the FPGA. The clock of the FPGA has been set to $f_{digi} = 200\,\text{MHz}$, resulting in a DPWM resolution of $T_{digi} = 5\,\text{n}s$ and $n = 8$ quantization levels for $\Delta\tilde{t}_{on}[k]$. A linear chirp signal with a duration of $t_d = 0.5\,\text{ms}$ and an amplitude A_c of 5 DPWM steps has been selected as stimulus $\tilde{t}_c[k]$. Its frequency range has been chosen from $f_s = 1\,\text{kHz}$ to $f_e = 60,\text{kHz}$, which ensures that the natural frequencies of the output filter sets listed in Table II are covered. The stimulus is superimposed onto a constant and arbitrarily chosen ON-time of $t_{on} = 0.5\ \mu\text{s}$. Note that, the chosen stimuli injection time of $t_d = 0.5\,\text{ms}$ is significantly shorter than in, e.g., FFT-based methods where the identification is also carried out during open-loop operation of the converter [6].

A. Load Influence

The proposed SI approach is dependent on the load of the converter. Ideally, the converter is unloaded or lightly loaded

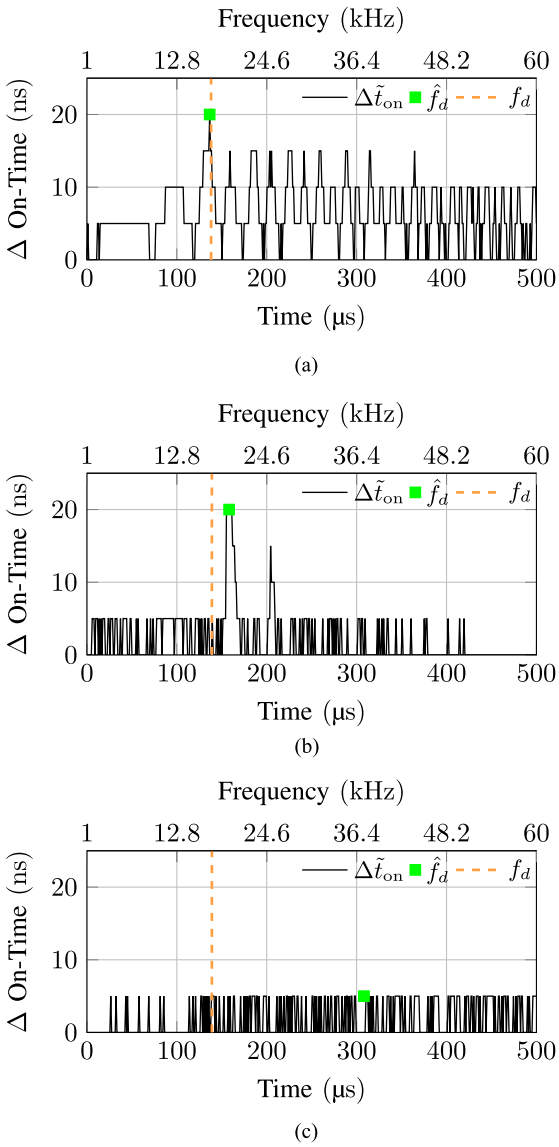


Fig. 10. Experimental performance comparison for the proposed SI approach for one output filter configuration ($L = 3.3\,\mu$H, $C = 25\,\mu$F) with different converter loads. (a) Unloaded converter; estimation error $\Delta f_d = 0.2$ kHz. (b) Load: $R_o = 8.3\,\Omega$; estimation error $\Delta f_d = 2.2$ kHz. (c) Load: $R_o = 3.7\,\Omega$; estimation error $\Delta f_d = 23.0$ kHz

when running the SI process. In this case, the coil current ripple oscillates around 0A, which guarantees negative coil currents. The higher the average load current I_o is, the more unlikely negative coil currents $i_L(t)$ are. Note that, the load current depends on the load resistance R_o and the output voltage $v_o(t)$, whereas $v_o(t)$ is considered to be fixed. The influence of the load resistance is experimentally analyzed for the first output filter configuration ($L = 3.3\,\mu$H, $C = 25\,\mu$F). First, the SI process is performed for the unloaded converter. The estimation procedure is reported in Fig. 10(a) and yields the estimation error $\Delta f_0 := |f_0 - \hat{f}_0|$. Second, the output resistance is set to 8.3 Ω. The resulting average output current is around $I_o = 200$ mA. Nonetheless, negative coil currents occur when perturbing t_{on} with frequencies close to the natural frequency. The corresponding results are reported in Fig. 10(b). Third, an 3.7 Ω output resistor is used, which leads to an average output current of about $I_o = 450$ mA. For this load level, no negative coil current occurs and therefore, the estimation error increases drastically. Consequently, the SI process has to be run during low load periods. For the targeted application, this is the case during the start-up procedure of the converter. The only additional hardware employed by the proposed approach is a comparator for measuring $t_{\mathrm{on,sw}}[k]$. In applications, where a light load condition, guaranteeing negative coil currents, cannot be assumed, an additional switch can be employed. This switch disconnects the load during stimuli injection and thus artificially creates a light load conditions.

B. Natural Frequency Estimation

In this section, the introduced SI approach is applied to different output filter configurations, which are listed in Table II. In order to guarantee for negative coil currents, the converter is operated in unloaded condition. A chirp signal with a frequency range from 1 to 60 kHz has been used in order to cover the damped natural frequency range of the possible L–C combinations, which ranges from 13 kHz up to 33.9 kHz. The frequency resolution of the perturbation is given by the system excitation time $t_d = 0.5$ ms, i.e., the duration of open-loop operation, and the covered frequency range. Using (8), this yields a chirp resolution of 128 Hz for the used parameters. The estimation process is visualized in Fig. 11 for set 2–5 and Fig. 10(a) for set 1. The estimation error varies between 0.15 and 1.26 kHz.

C. Controller Tuning

The estimate $\hat{f}_d$ is used to automatically tune the digital controller. Before tuning, the controller employs a conservative coefficient set, which ensures stability for the slowest possible L–C configuration. In this context, slow refers to the highest capacitance and inductance values, i.e., set 2 from Table II. The tuned coefficients are calculated as proposed in (12). For this experiment, the output filter configuration 4 from Table II is chosen, which is substantially faster compared to the slowest set. The converter was unloaded while performing the identification process. To visualize the improvement of the adaption process, a load jump from 0 to 400mA is performed, before and after the controller coefficient update. Note that, this represents a load jump from 0 to 80% of the maximum output current $I_{o_{\max}}$. The output voltage responses of the converter are compared in Fig. 12. Note that, the inductor current is only shown for the tuned controller. The difference in inductor current is not as pronounced as the difference in the output voltage and is therefore omitted. It is shown that the auto-tuned controller achieves a reduced undershoot, while stability is maintained. For the output filter configuration under exam, the undershoot is reduced by 36 mV, or 30%, in comparison with the initial controller settings, while stability is maintained. The controller auto-tuning presented in this article is intended to serve as an example of improving the system performance by using the obtained

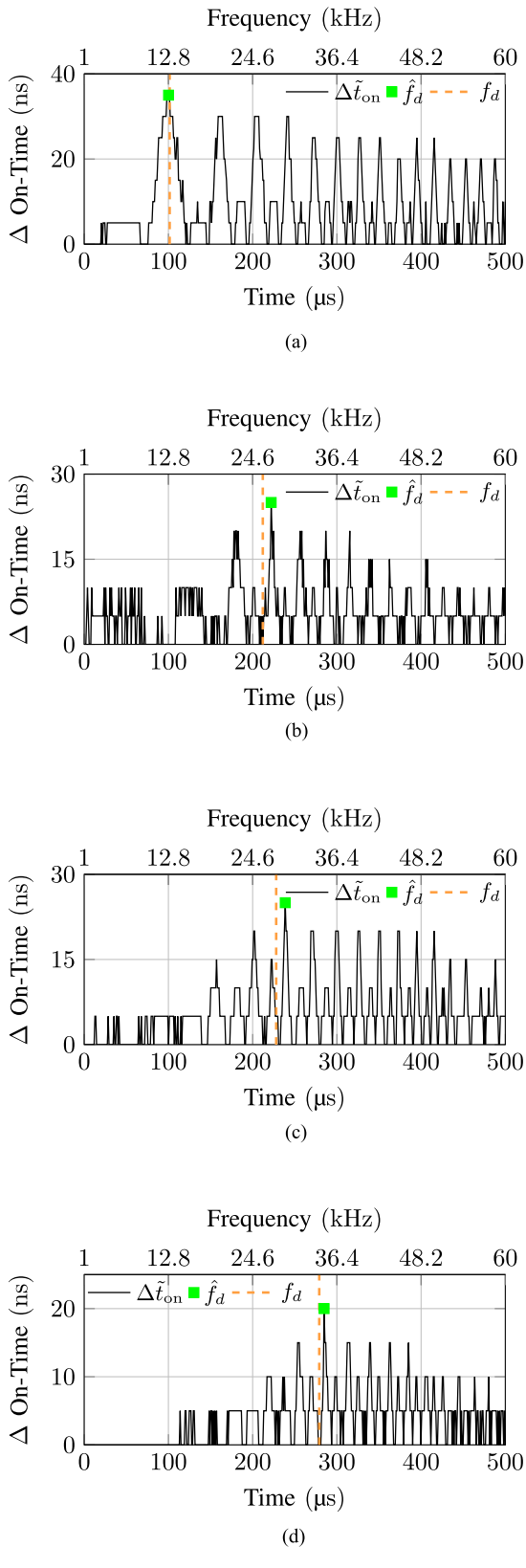


Fig. 11. Proposed SI method applied to different output filter configurations of the unloaded converter. (a) Parameters: $L = 4.7\ \mu$H, $C = 32\ \mu$F; estimation error $\Delta f_d = 0.15$ kHz. (b) Parameters: $L = 2.2\ \mu$H, $C = 17\ \mu$F; estimation error $\Delta f_d = 1.16$ kHz. (c) Parameters: $L = 3.3\ \mu$H, $C = 10\ \mu$F; estimation error $\Delta f_d = 1.26$ kHz. (d) Parameters: $L = 2.2\ \mu$H, $C = 10\ \mu$F; estimation error $\Delta f_d = 0.68$ kHz.

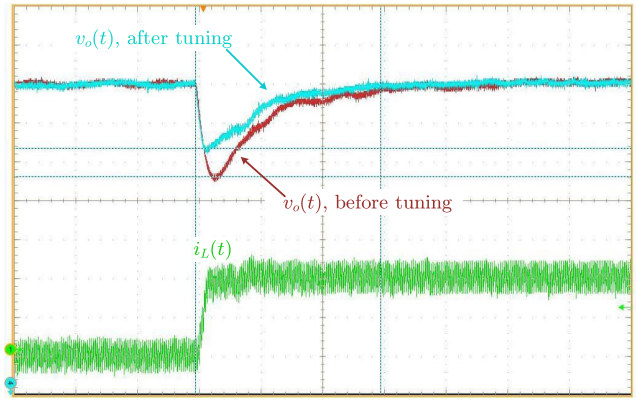


Fig. 12. Comparison of the output voltage response to a load jump from 0 to 400 mA with the $L = 3.3\,\mu$h and $C = 10\,\mu$F configuration (set 4) for the initial and tuned controller coefficients. The reported waveforms are the output voltage $v_o(t)$ (50 mV/div with 950 mV offset) and the inductor current $i_L(t)$ (200 mA/div); time basis 20 μs/div.

estimate of the damped natural frequency. Furthermore, it focuses on simplicity and applicability in low-cost segments. More sophisticated and resource expensive controller tuning schemes, which might further improve the closed-loop performance of the converter can be developed based on the estimated damped natural frequency but this is beyond the scope of this article.

IV. Conclusion

In this article, a fast, low-complexity natural frequency estimation approach for SMPSs was proposed. In contrast to state-of-the-art SI concepts, costly calculations and high-resolution ADCs are not required. Instead, the natural frequency estimation scheme exploits the behavior of the high-side MOSFET's drain–source capacitance and its body diode during dead-times with negative coil currents. Due to its simplicity, the proposed method is well suited for practical on-chip realizations. The theoretical foundations of the method were experimentally verified with a buck converter and different output filter sets. Ultimately, experimental results for a low-complexity automatic controller tuning approach based on the estimated natural frequency were shown. For the presented converter, dynamic performance was improved significantly, i.e., the magnitude of the output voltage transient was reduced by 30%.

References

[1] L. Corradini, D. Maksimović, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Piscantaway, NJ, USA: Wiley, 2015.

[2] R. Priewasser, M. Agostinelli, C. Unterrieder, S. Marsili, and M. Huemer, "Modeling, control, and implementation of dc-dc converters for variable frequency operation," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 287–301, Jan. 2014.

[3] S. Oucheriah and L. Guo, "Pwm-based adaptive sliding-mode control for boost dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3291–3294, Aug. 2013.

[4] G. Garcera, A. Abellan, and E. Figueres, "Sensitivity study of the control loops of dc-dc converters by means of robust parametric control theory," *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 581–586, Jun. 2002.

[5] B. Miao, R. Zane, and D. Maksimović, "Automated digital controller design for switching converters," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2005, pp. 2729–2735.

[6] B. Miao, R. Zane, and D. Maksimović, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1093–1099, Sep. 2005.

[7] M. Al-Greer, M. Armstrong, and D. Giaouris, "Active online system identification of switch mode dc-dc power converter based on efficient recursive DCD-IIR adaptive filter," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4425–4435, Nov. 2012.

[8] G. E. Pitel and P. T. Krein, "Real-time system identification for load monitoring and transient handling of dc-dc supplies," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun. 2008, pp. 3807–3813.

[9] W. Xiao, M. G. J. Lind, W. G. Dunford, and A. Capel, "Real-time identification of optimal operating points in photovoltaic power systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1017–1026, Jun. 2006.

[10] C. Yang, Y. Jiang, W. He, J. Na, Z. Li, and B. Xu, "Adaptive parameter estimation and control design for robot manipulators with finite-time convergence," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8112–8123, Oct. 2018.

[11] C. C. Hang and K. K. Sin, "On-line auto tuning of pid controllers based on the cross-correlation technique," *IEEE Trans. Ind. Electron.*, vol. 38, no. 6, pp. 428–437, Dec. 1991.

[12] H. Gietler, C. Unterrieder, A. Berger, R. Priewasser, and M. Lunglmayr, "Low-complexity, high frequency parametric system identification method for switched-mode power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 2004–2009.

[13] Y. V. Zakharov, G. P. White, and J. Liu, "Low-complexity RLS algorithms using dichotomous coordinate descent iterations," *IEEE Trans. Signal Process.*, vol. 56, no. 7, pp. 3150–3161, Jul. 2008.

[14] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of digitally controlled dc-dc converters based on relay feedback," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 199–207, Jan. 2007.

[15] Z. Zhao and A. Prodic, "Limit-cycle oscillations based auto-tuning system for digitally controlled dc–dc power supplies," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2211–2222, Nov. 2007.

[16] M. Al-Greer, M. Armstrong, M. Ahmeid, and D. Giaouris, "Advances on system identification techniques for dc–dc switch mode power converter applications," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6973–6990, Jul. 2019.

[17] Y. Lin and Y. Lai, "Dead-time elimination of PWM-controlled inverter/converter without separate power sources for current polarity detection circuit," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2121–2127, Jun. 2009.

[18] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. New York, NY, USA: Springer Science & Business Media, 2007.

[19] C.-T. Chen, *Analog and Digital Control System Design: Transfer-Function, State-Space, and Algebraic Methods*. Oxford, UK: Oxford University Press, Inc., 1995.

[20] X.-G. Xia, "System identification using chirp signals and time-variant filters in the joint time-frequency domain," *IEEE Trans. Signal Process.*, vol. 45, no. 8, pp. 2072–2084, Aug. 1997.

[21] R. F. Foley, R. C. Kavanagh, and M. G. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, Jun. 2012.

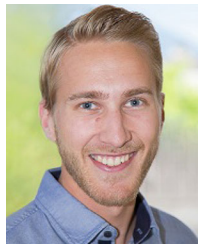
[22] R. Ortega and R. Kelly, "Pid self-tuners: Some theoretical and practical aspects," *IEEE Trans. Ind. Electron.*, vol. IE-31, no. 4, pp. 332–338, Nov. 1984.

[23] M. Ahmeid, M. Armstrong, S. Gadoue, M. Al-Greer, and P. Missailidis, "Real-time parameter estimation of dc–dc converters using a self-tuned kalman filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5666–5674, Jul. 2017.

[24] P. Jain *et al.*, "An improved robust adaptive parameter identifier for dc–dc converters using h-infinity design," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 2922–2926.

[25] T. Roinila, A. Hessamaldin, S. Arrua, and E. Santi, "Adaptive control of dc power distribution systems: Applying pseudo-random sequences and fourier techniques," in *Proc. Int. Power Electron. Conf.*, May. 2018, pp. 1719–1723.

[26] M. Kanzian, H. Gietler, C. Unterrieder, M. Agostinelli, M. Lunglmayr, and M. Huemer, "Low-complexity state-space-based system identification and controller auto-tuning method for multi-phase dc–dc converters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 2076–2087, Mar./Apr. 2019.



Harald Gietler was born in Villach, Austria. He received the B.Sc. and Dipl.-Ing. degrees in information technology from the University of Klagenfurt, Klagenfurt, Austria, in 2015 and 2017, respectively.

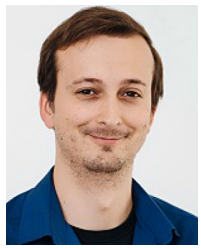
From 2015 to 2017, he was with Infineon Technologies, where he focused on system identification and digital self-tuning control for dc–dc converters. In 2017 he joined the Sensors and Actuators group at the University of Klagenfurt. His research interests include computational electromagnetics, sensor technologies, power converters, and system identification.

Marc Kanzian received the Dipl.-Ing. degree in communication engineering from the Carinthia University of Applied Sciences, Klagenfurt, Austria, in 2015, and the Dr.Tech. degree in electronics and information technology from the Johannes Kepler University Linz, Austria, in 2019.

Since 2016, he has been with Infineon Technologies Austria AG, Villach, Austria, where he is currently a Concept Engineer for power management systems.

Christoph Unterrieder was born in Graz, Austria, in 1985. He received the Dipl.-Ing. and Dr.Tech. degrees in information technology from Klagenfurt University, Klagenfurt, Austria, in 2011 and 2015, respectively.

In 2014, he joined Infineon Technologies, Villach, Austria, where he is involved in the conception and design of power and battery management circuits/systems, with a focus on automotive and consumer applications.



Andreas Berger received the doctoral degree in electronics and information technology from the Johannes Kepler University Linz, Linz, Austria, in 2019.

In 2016, he joined the company Infineon Technologies, Villach, Austria, where he is currently working with the development of mixed-signal power and battery management integrated circuits. His research interests include the optimization of wireless power transfer systems for mobile devices.

Robert Priewasser received the Dipl.-Ing. (FH) degree in direction hardware/software systems engineering from the University of Applied Sciences of Upper Austria, Wels, Austria, in 2007, and the Dr.Tech. (Ph.D.) degree in information technology from the University of Klagenfurt, Klagenfurt, Austria, in 2013.

From 2007 to 2012, he was a Research Team Member with the Embedded Systems and Signal Processing Group, Klagenfurt University, Klagenfurt. Since 2013, he has been with Infineon Technologies, Austria, where he is working as Subsystem Architect on power management circuits for deep sub-micron CMOS system-on-chips for automotive applications.

Mario Huemer (M'00–SM'07) received the Dipl.-Ing. and Dr.Tech. degrees in mechatronics from Johannes Kepler University (JKU) Linz, Austria, in 1996 and 1999, respectively.

After holding positions in industry and academia, he became an Associate Professor with the University of Erlangen-Nuremberg, Germany, from 2004 to 2007, and a Full Professor with Klagenfurt University, Klagenfurt, Austria, from 2007 to 2013. Since September 2013, he is heading the Institute of Signal Processing, JKU, Linz, Austria, as a Full Professor of Signal Processing. His research interests include statistical and adaptive signal processing, signal processing architectures, as well as mixed signal processing with applications in information and communications engineering, radio frequency transceivers for communications and radar, sensor and biomedical signal processing.

Dr. Huemer was a recipient of the dissertation awards of the German Society of Information Technology (ITG) and the Austrian Society of Information and Communications Technology (GIT), respectively, the Austrian Kardinal Innitzer award in natural sciences, and the German ITG award.

Hubert Zangl (M'06) received the Dipl.Ing. degree in telematics, the Dr.Tech. degree in electrical engineering, and the Venia Docendi in sensors and instrumentation from the Graz University of Technology (TUG), Graz, Austria, in 2001, 2005, and 2009, respectively.

From 2010 to 2013, he was an Associate Professor for Sensors and Instrumentation, Institute of Electrical Measurement and Measurement Signal Processing, TUG. Since September 2013, he has been a Professor Chairing Sensors and Actuators with the Institute of Smart System Technologies, Alpen-Adria-University Klagenfurt, Austria. His research interests include design and optimization of smart sensors and actuators, robustness and reliability of sensors and actuators, sensor signal processing, autarkic wireless sensors, energy harvesting and applications in robot sensing, and Internet of Things.