Analysis of Single-Phase-to-Ground Faults at the Valve-Side of HB-MMCs in HVDC Systems

Gen Li, Jun Liang, *Senior Member, IEEE*, Fan Ma, Carlos E. Ugalde-Loo, *Member, IEEE*, and Haifeng Liang, *Member, IEEE*

***Abstract*—Although the probability of occurrence of station internal ac grounding faults in modular multilevel converter (MMC)-based high-voltage direct-current systems is low, they may lead to severe consequences that should be considered when designing protection systems. This paper analyzes the characteristics of valve-side single-phase-to-ground (SPG) faults in three configurations of MMC systems. Fault responses for symmetrical monopole MMCs are first studied. Upper arm overvoltages and ac-side nonzero-crossing currents arising from SPG faults in asymmetrical and bipolar configurations are then investigated. DC grounding using an *LR* parallel circuit is employed to create current zero-crossings, which will enable the operation of grid-side ac circuit breakers. The theoretical analysis is verified through simulations performed in PSCAD/EMTDC, with simulation results and the theoretical analysis showing a good agreement. The studies in this paper will be valuable for the design of protection systems for station internal ac grounding faults.**

***Index Terms*—Fault tolerance, ground faults, half-bridge modular multilevel converter, high-voltage direct-current systems, station internal fault.**

I. Introduction

VOLTAGE source converters (VSCs) are becoming an attractive alternative to line commutated converters (LCCs) for high-voltage direct-current (HVdc) transmission towards large-scale renewable energy integration and the deployment of multiterminal dc (MTDC) grids [1], [2]. In particular, half-bridge modular multilevel converters (HB-MMCs) have been already implemented in commercial projects (e.g., Nemo link, Nan'ao three-terminal project, and Zhoushan five-terminal project [3]–[5]) due to their excellent steady-state performance and fault-tolerant operation [6], [7].

Fault tolerance is an important aspect in the operation of MMC-HVdc systems and thus has received a significant attention in the literature. For instance, dc fault characteristics and handling methods have been studied in [8]–[10]. In [1], [11], and [12] the modeling and control of MMCs under grid-side unbalanced ac faults have been addressed. However, MMC station internal ac faults remain an under-researched topic.

Transformers are typically installed outside the halls housing the converters. The valve-side winding bushings of these transformers protrude through the hall wall to connect to converter ac buses [13], [14]. Insulation failure and flashover of wall bushings may cause an internal single-phase-to-ground (SPG) fault between the converter and the transformer. Both LCCs and VSCs have exhibited such behavior in practical installations [15]–[18]. The wall bushings, which are in the overlapping protective zone of the converter and the transformer, require significant insulation to withstand high voltages and large currents. Upon insulation failure, valve-side SPG faults will lead to severe consequences, such as commutation failures in LCCs, dc voltage oscillations in symmetrical monopole MMCs, and nonzero-crossing fault currents in bipolar MMCs.

In [16] and [17], the characteristics of valve-side SPG faults in LCCs were analyzed and possible solutions using a phase selection strategy and zero-sequence voltage compensation were proposed. However, these cannot be applied to MMCs due to the differences between converter topologies. Internal ac bus faults in two-level VSCs were investigated in [18] and [19], but their findings are not totally applicable to MMCs either. MMC station internal ac faults were studied in [1], [20], and [21]. However, these studies do not provide a theoretical analysis of the large oscillations and overvoltage of the dc pole-to-ground voltages. In addition, the simplified lumped parameter line models used in these references do not reflect real fault characteristics.

Valve-side SPG faults also induce a special fault behavior in asymmetrical monopole HB-MMCs. An initial study was performed in [15], where solutions to the overvoltages arising in upper arm submodule (SM) capacitors were proposed. However, this type of fault also produces high dc components on the ac-side fault currents which may prevent grid-side ac circuit breakers (ACCBs) from operating due to the absence of zero-crossings. Kjærgaard *et al.* [22] and Andersson and Hytti-

Manuscript received July 25, 2017; revised January 26, 2018 and March 15, 2018; accepted April 6, 2018. Date of publication April 27, 2018; date of current version October 31, 2018. This work was supported in part by the People Programme (Marie Curie Actions) of the EU FP7 Programme (FP7/2007-2013) through the project "Multi-terminal DC grid for offshore wind" (MEDOW), under Grant 317221, and in part by the EU FP7 Programme through the project "Beyond State of the art Technologies for re-Powering AC corridors & multi-Terminal HVdc Systems" (BEST PATHS), under Grant 612748. *(Corresponding author: Carlos E. Ugalde-Loo).*

G. Li, J. Liang, and C. E. Ugalde-Loo are with the School of Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: lig9@cardiff.ac.uk; liangj1@cardiff.ac.uk; ugalde-LooC@cardiff.ac.uk).

F. Ma is with the National Key Laboratory of Science and Technology on Vessel Integrated Power System, Naval University of Engineering, Wuhan 430033, China (e-mail: mafan0803@163.com).

H. Liang is with the Department of Electrical Engineering, North China Electric Power University, Boding 071003, China (e-mail: hfliang@ncepu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2018.2829666

nen [23] propose installing an auxiliary ACCB on the grid-side to create the required current zero-crossings, but no further insight on the presence of the dc offsets is provided. Moreover, a shortcoming of this approach is that the three-phase short-circuit created by the additional ACCB will lead to severe voltage drops at the ac grid and, therefore, may aggravate the fault impact. In addition, the installation of an auxiliary ACCB will increase capital costs.

Given that an asymmetrical monopole MMC-HVdc link is the building block of bipolar systems, these will inherit its drawbacks. Although Zhou *et al*. [24] analyzes the nonzero-crossing fault currents caused by valve-side SPG faults in a bipolar system, the faulted phase reactance has been ignored and, as such, the fault current calculation accuracy is reduced. Additionally, the protection strategy is complex and the three-phase short-circuit created during the fault may burn the semiconductor devices. Moreover, the converter transformer and other equipment may be damaged by the large currents arising from closing the auxiliary arm protection switches. A hybrid MMC topology based on HB and full-bridge SMs has been proposed in [25] to address the aforementioned issues. However, the adoption of such a configuration would greatly increase capital costs due to the additional insulated-gate bipolar transistors (IGBTs), which in turn would increase power losses.

The study of HB-MMCs subject to station internal faults is currently under-researched both in the industry and academia. To bridge this gap, this paper analyzes SPG fault characteristics at the valve-side of HB-MMC-based transmission systems for three station configurations. An *LR* parallel grounding circuit is employed to address the issues arising from nonzero-crossing fault currents in asymmetrical and bipolar systems. For completeness, the analysis is supported by simulations in PSCAD/EMTDC. The theoretical analysis matches well with the simulation results and a good system performance upon the occurrence of valve-side SPG faults is ensured.

II. MMC-HVdc Station Configurations

Fig. 1 depicts possible configurations for MMC-HVdc systems. A symmetrical monopole is shown Fig. 1(a), which features two poles with opposite voltage potential. Both poles need to be fully insulated. Conversely, only one polarity is present in the asymmetrical monopole shown in Fig. 1(b). The dc current returns through the ground or a metallic return path and, thus, low-voltage insulation is required. The drawbacks of this configuration include a lack of redundancy during faults, corrosion on the metallic pipes in the ground and potential negative environmental effects [2].

An MMC-based bipolar HVdc system is shown in Fig. 1(c). It consists of two independently controlled asymmetrical monopoles. This configuration offers a higher reliability and flexibility compared to monopole systems. For instance, the loss of any converter entails a 50% loss of the total transmission capacity only. A single asymmetrical monopole link can also be installed in parallel with an existing LCC link as a hybrid LCC-MMC bipolar HVdc system, as shown in Fig. 1(d). The MMCs in this topology can minimize the risk of commutation failures on the nearby LCC link and minimize the overvoltage caused when the LCC link is blocked [22], [23].

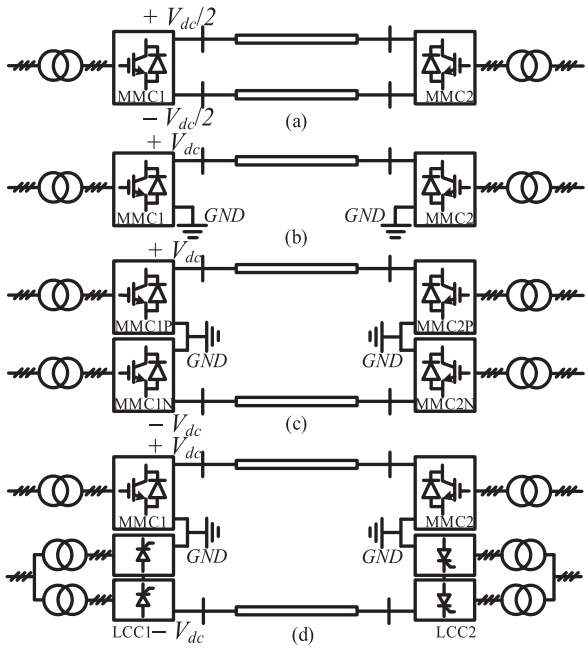

Fig. 1. MMC-based HVdc transmission systems. (a) Symmetrical monopole. (b) Asymmetrical monopole. (c) MMC bipole. (d) Hybrid LCC-MMC bipole.

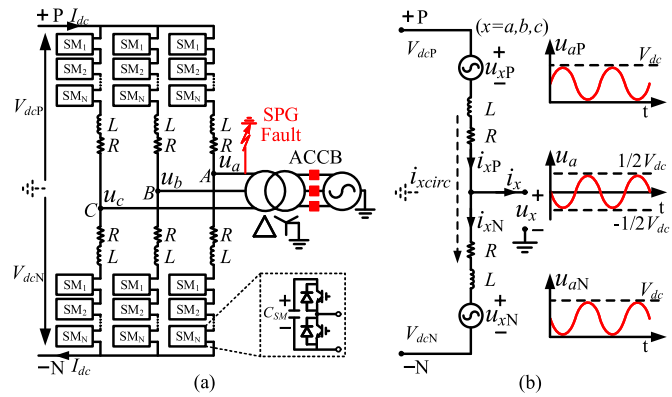

Fig. 2. Symmetrical monopole HB-MMC. (a) Converter topology. (b) Single-phase equivalent circuit.

III. Valve-Side SPG Faults in Symmetrical Monopole Systems

Fig. 2(a) shows the topology of a symmetrical monopole MMC. The windings of the transformer are connected in a delta/star (Δ/Y) configuration and the grid-side is arranged with a neutral grounding [19], [20]. Fig. 2(b) illustrates the single-phase equivalent circuit of the MMC, where u_x is the phase-to-ground voltage ($x = a, b, c$), i_x the phase current, $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ are the voltages produced by SMs in the upper and lower arms, $i_{x\mathrm{P}}$ and $i_{x\mathrm{N}}$ the arm currents, $i_{x\mathrm{circ}}$ the circulating current (which can be reduced to a very low value using damping controllers [26]), and $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ the dc pole-to-ground voltages, with

$V_{dc\mathrm{P}} = -V_{dc\mathrm{N}} = 1/2V_{dc}$, where V_{dc} is the dc pole-to-pole voltage. In normal operation, the sum of the voltages of all SM capacitors in each arm equals V_{dc}. If the circulating currents and the voltage drops on arm reactors and resistors are ignored, the dc pole voltages can be obtained as follows:

$$\begin{cases} V_{dc\mathrm{P}} = u_x + \left(u_{x\mathrm{P}} + L\frac{di_{x\mathrm{P}}}{dt} + Ri_{x\mathrm{P}}\right) \approx u_x + u_{x\mathrm{P}} \\ V_{dc\mathrm{N}} = u_x - \left(u_{x\mathrm{N}} + L\frac{di_{x\mathrm{N}}}{dt} + Ri_{x\mathrm{N}}\right) \approx u_x - u_{x\mathrm{N}} \end{cases} \tag{1}$$

where $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ can be expressed as follows:

$$\begin{cases} u_{x\mathrm{P}} = (1/2)V_{dc}[\sin(\omega t + \theta_x) + 1] \\ u_{x\mathrm{N}} = (1/2)V_{dc}[1 - \sin(\omega t + \theta_x)] \end{cases} \tag{2}$$

where θ_x is the phase angle. Voltages $u_{a\mathrm{P}}$, $u_{a\mathrm{N}}$, and u_a for phase A are illustrated in Fig. 2(b). According to (1), the following relationships can be obtained:

$$\begin{cases} u_{ab} \approx u_{b\mathrm{P}} - u_{a\mathrm{P}}, & u_{ca} \approx u_{a\mathrm{P}} - u_{c\mathrm{P}} \\ u_{ab} \approx u_{a\mathrm{N}} - u_{b\mathrm{N}}, & u_{ca} \approx u_{c\mathrm{N}} - u_{a\mathrm{N}} \end{cases}. \tag{3}$$

Due to the delta connection of the transformer, the magnitudes of the line voltages remain unchanged and the phase voltages become $u_a = 0$, $u_b = -u_{ab}$ and $u_c = u_{ca}$. If the converter is not blocked, considering (1) and (3), $V_{dc\mathrm{P}} \approx u_{a\mathrm{P}}$ and $V_{dc\mathrm{N}} \approx -u_{a\mathrm{N}}$. Therefore, the dc pole-to-ground voltages after the fault depend on the arm voltages in the faulted phase. According to (2), $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ contain large dc offsets and oscillate at the ac grid fundamental frequency. The maximum magnitudes of dc pole-to-ground voltage oscillations reach twice their rated value. However, it should be emphasized that the pole-to-pole dc voltage is not impacted by the fault. This occurs since 1) the pole-to-pole dc voltage is the sum of $u_{a\mathrm{P}}$ and $u_{a\mathrm{N}}$ and thus does not contain a sinusoidal component; and 2) the pole-to-pole dc voltage is still regulated by the dc voltage control from other MMCs. Moreover, the energy stored in the dc line will discharge through its distributed capacitors due to the oscillations of the dc pole voltages and, thus, lead to fault currents [1]. If the dc line is long and/or additional dc capacitors are employed as a dc-side filter, significant fault currents can be generated. This phenomenon will be analyzed in Section V-A.

As valve-side SPG faults are normally permanent faults [18], [20], the converter needs to be blocked immediately and the ac-side circuit breaker should be tripped. As a result, the whole system will be shut down for repairing and maintenance.

IV. Valve-Side SPG Faults in Asymmetrical Monopole Systems

Fig. 3(a) shows the topology of an asymmetric monopole HB-MMC. There is only one positive pole in the dc terminal and the other pole is grounded. If circulating currents are neglected, the valve-side phase voltages can be expressed as follows:

$$u_x = -\frac{1}{2}L\frac{di_{vx}}{dt} - \frac{1}{2}Ri_{vx} + \frac{u_{xN} - u_{xP}}{2} + \frac{1}{2}V_{dc} \quad (x = a, b, c) \tag{4}$$

where $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ are the voltages produced by SMs in the upper and lower arms. It can be seen that u_x contains a dc component $[(1/2)V_{dc}]$ which makes the valve-side voltages always positive. This is illustrated by $u_{a,b,c}$ in Fig. 3(a). As a result, the converter transformers need to be specially designed.

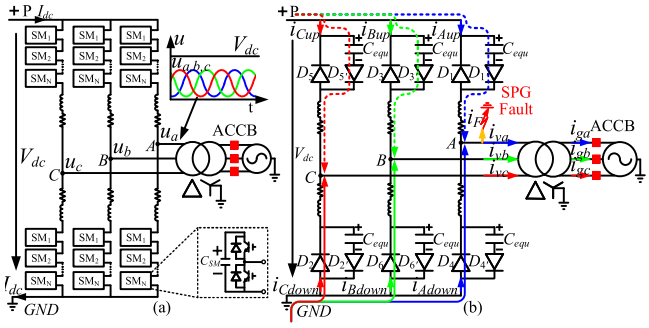

Fig. 3. Asymmetrical monopole HB-MMC. (a) Topology. (b) Equivalent circuit after blocking IGBTs.

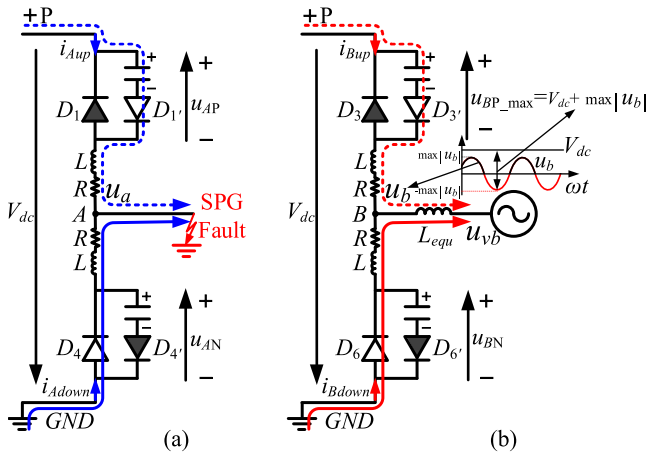

Fig. 4. Post-fault equivalent circuits. (a) Phase *A*. (b) Phase *B*.

Since a delta/star transformer connection is used, the post-fault valve-side voltages are similar to those exhibited by the symmetrical MMC configuration presented in Section III. However, significant fault currents will be created due to the converter dc grounding. To protect the system, the IGBTs should be blocked immediately once the fault is detected. The equivalent circuit of a blocked converter during a valve-side SPG fault at phase A is shown in Fig. 3(b). C_{equ} represents the equivalent capacitor of all SM capacitors in each arm.

A. Overvoltages in Upper Arm SM Capacitors

Post-fault equivalent circuits of faulted phase A and non-faulted phase B are illustrated in Fig. 4. The analysis presented for phase B also applies to phase C. L_{equ} in Fig. 4(b) is the total equivalent reactance of the transformer and the grid-side reactance referred to the valve-side. The ac source represents the transformer's post-fault voltage u_{vb}.

As shown in Fig. 4(a), an SPG fault results in a new zero-voltage potential. Due to their forward-bias characteristic, diodes D_1 and $D_{4'}$ will become reverse-biased once the converter is blocked. Because of the arm reactor, D_4 will be reverse-biased until current $i_{A\mathrm{down}}$ decays to zero. The upper arm capacitors in phase A will be charged through $D_{1'}$ as a

result of the dc-side transient overvoltages caused by the fault. $D_{1'}$ will be reverse-biased once the capacitor voltage u_{AP} is equal or higher than V_{dc}. Then, u_{AP} will remain constant.

For phase *B* [see Fig. 4(b)], D_3 and $D_{6'}$ will be reverse-biased since both the dc voltage V_{dc} and the capacitor voltage u_{BN} have a higher magnitude than u_b. However, $D_{3'}$ and D_6 will conduct during every negative half-cycle of u_b. If the arm resistance is neglected, u_b can be estimated by the following:

$$u_b \approx u_{vb} \times L/\left(L + L_{\text{equ}}\right). \tag{5}$$

The upper arm capacitors will stop being charged once their voltage reaches a maximum value

$$u_{BP\_\max} = V_{dc} + \max|u_b| \tag{6}$$

where max $|u_b|$ is the amplitude of u_b. According to (6), the voltage increase is given by the amplitude of the post-fault voltage u_b [see Fig. 4(b)]. Hence, in steady state, all upper arm capacitors will be overcharged and no more current will flow through the upper arms. However, the upper arm capacitor voltages will not reach $u_{BP\_\max}$ if the fault is isolated quickly.

It can be seen from (5) and (6) that the upper arm overvoltage in nonfaulted phases depends on system parameters. For instance, a small arm reactor or a large transformer leakage reactor could reduce it. However, arm reactors must be large enough to limit circulating and fault currents. In addition, a large circuit reactance will increase power losses and affect the system dynamic characteristics.

According to the above analysis, the capacitor overvoltage caused by an SPG fault at the power-controlling MMC will be worse than when the fault occurs at the dc voltage-controlling MMC. Blocking the MMC that regulates V_{dc} will reduce the dc voltage and, consequently, will decrease overvoltages. As this type of fault is usually permanent, the whole dc system needs to be shut down. Such MMC needs to be blocked immediately either through local fault detection or with a blocking signal from the faulted converter using communications. Alternatively, choosing a low valve-side voltage for the transformer can mitigate upper arm overvoltages, but this approach may affect the system dynamics as well. It can be concluded that a comprehensive design that considers not only system parameters but also the fault characteristics is required.

B. DC Offsets in Fault Currents

According to Fig. 3(b), an SPG fault creates closed current paths through the lower arms in nonfaulted phases and the converter dc grounding. The lower arms in nonfaulted phases will conduct large fault currents during the negative half-cycles of the valve-side voltages. Moreover, due to the inductor freewheeling effect, the diode will keep conducting when the positive half-cycles of the valve-side voltage appear. Therefore, there will be instances when the two lower arms in the nonfaulted phases conduct at the same time. The resistance in the current path affects the duration of the inductor freewheeling. As analyzed in the Appendix, the current will keep conducting in both the positive and negative voltages if the resistance is ignored. The following analysis is based on this phenomenon.

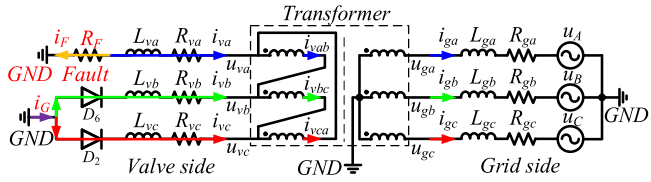

Fig. 5. System equivalent circuit during a valve-side SPG fault in phase *A*.

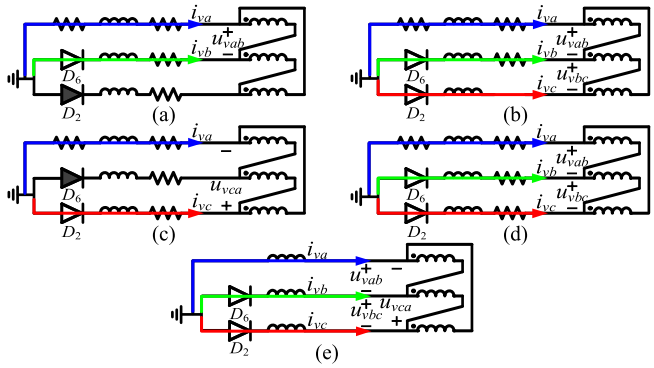

Fig. 6. Conducting modes of the lower arm diodes in the nonfaulted phases. (a) D_6 is on and D_2 is off. (b) Both D_2 and D_6 are on. (c) D_2 is on and D_6 is off. (d) Both D_2 and D_6 are on. (e) Equivalent circuit ignoring resistances.

The equivalent circuit illustrated in Fig. 5 is used to analyze the fault currents. The transformer's valve-side and grid-side voltages are respectively given by u_{vx} and u_{gx} (with $x = a, b, c$). Resistors R_{va}, R_{vb}, R_{vc} and reactors L_{va}, L_{vb}, L_{vc} represent the total equivalent resistance and reactance of the arm inductors and transformer leakage inductors. Similarly, resistors R_{ga}, R_{gb}, R_{gc} and reactors L_{ga}, L_{gb}, L_{gc} represent the total equivalent resistance and reactance of grid impedance. Currents will be positive if they flow in the directions illustrated in the figure.

Recall that there is no zero-sequence current present in the valve-side due to the transformer's delta connection. Thus, the three-phase valve-side currents satisfy the following:

$$i_{va} + i_{vb} + i_{vc} = 0. \tag{7}$$

Due to the forward-bias characteristic of diodes, i_{vb} and i_{vc} will always be positive (see Fig. 5). Thus, i_{va} will always be negative according to (7). This implies that the current in all phases contains dc components. Fig. 6(a)–(d) illustrate the diode conducting sequences in the nonfaulted phases. As an SPG fault can occur at any time, any conduction mode can be the first mode in a full conduction cycle. In this analysis, it is assumed that u_{vb} is negative and u_{vc} positive when the IGBTs are blocked. The conduction pattern of the lower arm diodes will keep repeating from Fig. 6(a)–(d). Due to the inductor freewheeling, there will be two modes when both D_2 and D_6 are conducting within a full conduction cycle. Therefore, the circuits in Fig. 6(b) and (d) are the same.

Given that fault currents flow through first-order *LR* circuits, the decay of transient dc components will be governed by a time constant $\tau = L/R$. In this case, τ is large since the reactance is

much greater than the resistance. Hence, the dc component will not decay considerably during each conducting mode. If resistance is ignored [see Fig. 6(e)], the circuit will become purely inductive. In steady state, the diodes in this circuit will always conduct. The reader is referred to the Appendix for details.

According to Fig. 6(e), the following expressions are derived:

$$\begin{cases} -L_{va}\dfrac{di_{va}}{dt} + L_{vb}\dfrac{di_{vb}}{dt} = u_{vab} \\ -L_{vb}\dfrac{di_{vb}}{dt} + L_{vc}\dfrac{di_{vc}}{dt} = u_{vbc} \\ -L_{va}\dfrac{di_{va}}{dt} + L_{vc}\dfrac{di_{vc}}{dt} = -u_{vca} \end{cases} \tag{8}$$

where u_{vab}, u_{vbc}, and u_{vca} are the line voltages, given by

$$\begin{cases} u_{vab} = \sqrt{3}U\sin(\omega t + \varphi) \\ u_{vbc} = \sqrt{3}U\sin(\omega t + \varphi + 120^\circ) \\ u_{vca} = \sqrt{3}U\sin(\omega t + \varphi - 120^\circ) \end{cases} \tag{9}$$

where ω is the system frequency, φ is the initial angle, and U is the transformer's valve-side prefault peak phase voltage. Differential equations for i_{vb} and i_{vc} can be obtained from (8) as follows:

$$\begin{cases} \dfrac{di_{vb}}{dt} = \dfrac{(L_{va}+L_{vc})u_{vab} + L_{va}u_{vca}}{L_{va}L_{vb} + L_{va}L_{vc} + L_{vb}L_{vc}} \\ \dfrac{di_{vc}}{dt} = -\dfrac{L_{va}u_{vab} + (L_{va}+L_{vb})u_{vca}}{L_{va}L_{vb} + L_{va}L_{vc} + L_{vb}L_{vc}} \end{cases}. \tag{10}$$

As shown in the Appendix, an initial condition may be chosen at any moment when the current is zero

$$\begin{cases} i_{vb}(0^+) = i_{vb}(0^-) = 0 \\ i_{vc}(0^+) = i_{vc}(0^-) = 0 \end{cases}. \tag{11}$$

According to (8)–(11), i_{vb} and i_{vc} can be derived as follows:

$$\begin{cases} i_{vb} = M_1\left[1 - \sin(\omega t + \Phi_1)\right] \\ i_{vc} = M_2\left[\sin(\omega t + \Phi_2) + 1\right] \end{cases} \tag{12}$$

where M_1, M_2, Φ_1, and Φ_2 are provided in the Appendix. Thus, current i_{va} can be expressed as follows:

$$\begin{aligned} i_{va} &= -(i_{vb} + i_{vc}) \\ &= -\left\{M_1\left[1 - \sin(\omega t + \Phi_1)\right] + M_2\left[\sin(\omega t + \Phi_2) + 1\right]\right\}. \end{aligned} \tag{13}$$

It can be seen from (12) and (13) that i_{vb} and i_{vc} are always positive and that i_{va} is always negative. Hence, all valve-side fault currents contain high dc components and do not exhibit zero-crossings. As shown in (A4) of the Appendix, the current magnitudes are mainly determined by the transformer's valve-side voltage and circuit reactors.

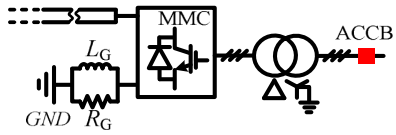

Fig. 7. Asymmetrical MMC equipped with an *LR* parallel grounding circuit.

According to Fig. 6, the currents at both sides of the transformer are related as follows:

$$\begin{cases} \dot{I}_{va} = \dot{I}_{vab} - \dot{I}_{vca} = \dfrac{\left(\dot{I}_{ga} - \dot{I}_{gc}\right)}{\sqrt{3}} \times k \\ \dot{I}_{vb} = \dot{I}_{vbc} - \dot{I}_{vab} = \dfrac{\left(\dot{I}_{gb} - \dot{I}_{ga}\right)}{\sqrt{3}} \times k \\ \dot{I}_{vc} = \dot{I}_{vca} - \dot{I}_{vbc} = \dfrac{\left(\dot{I}_{gc} - \dot{I}_{gb}\right)}{\sqrt{3}} \times k \end{cases} \tag{14}$$

where k is the transformer's turn ratio. The currents have been expressed as vectors and hence a capital notation was adopted. Since there is no zero-sequence current in the transformer's grid-side, the grid-side currents satisfy the following:

$$i_{ga} + i_{gb} + i_{gc} = 0. \tag{15}$$

From (14) and (15), the grid-side currents can be rewritten as follows:

$$\begin{cases} \dot{I}_{ga} = -\dfrac{(2\dot{I}_{vb} + \dot{I}_{vc})}{\sqrt{3}k} \\ \dot{I}_{gb} = \dfrac{(\dot{I}_{vb} - \dot{I}_{vc})}{\sqrt{3}k} \\ \dot{I}_{gc} = \dfrac{(\dot{I}_{vb} + 2\dot{I}_{vc})}{\sqrt{3}k} \end{cases}. \tag{16}$$

It can be observed from (12) and (16) that i_{ga} is always negative and i_{gc} is always positive. The dc offset of i_{gb} is given by $(M_1 - M_2)/(\sqrt{3}k)$, which has a small magnitude and hence will not lead to a nonzero-crossing.

The analysis presented in the last two sections shows that a valve-side SPG fault at an asymmetrical HB-MMC will cause upper arm overvoltages and large dc offset in currents at both sides of the converter transformer. Due to the absence of zero-crossings, ACCBs will not be capable of interrupting arcs within the parting time of the contactors in real applications [22], [23], [28].

C. Protection for Valve-Side SPG Faults

To limit upper arm overvoltages, the converter should be blocked once a fault is detected. At the same time, the voltage-regulating MMC can be blocked using local dc overcurrent protection to reduce the dc-side voltage which, in turn, will be helpful to further reduce the overvoltages.

In order to damp the dc components in fault currents, an *LR* parallel circuit is employed as the converter dc grounding. This is shown in Fig. 7. Resistor R_G will not only damp the dc components during a valve-side SPG fault, but will also limit fault current caused by dc-side faults. Inductor L_G will limit

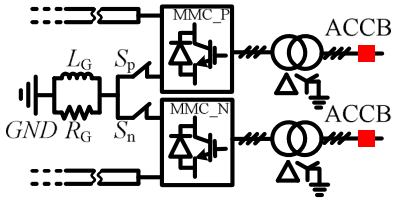

Fig. 8. Bipolar MMC system equipped with an *LR* grounding circuit.

the ac components of fault currents and drive the currents into R_G, which will in turn damp the dc components. During normal operation, R_G is bypassed by L_G. This way, normal operation is not affected and power losses are avoided.

The selection of a suitable *LR* circuit should consider system parameters such as arm reactors and resistors, transformer impedance, and resistance of switches. The value of R_G should ensure that dc components are damped enough so that zero-crossing currents arise in the grid-side. Then, L_G can be selected as low as possible. The *LR* parallel circuit could also be deployed in systems with a metallic return path.

According to the above analysis, the converter will be blocked immediately once a valve-side SPG fault occurs. Then, the grid-side ACCB will open once current zero-crossings are detected.

V. Analysis of HB-MMC-Based Bipolar Systems Subject to Valve-Side SPG Faults

Since bipolar systems consist of two symmetrical and independently controlled asymmetrical monopole links, the analysis in Section IV is applicable. An *LR* parallel grounding circuit can be also used for the systems shown in Fig. 1(c) and (d). However, such an approach has drawbacks: transient fault currents caused by both ac- and dc-side faults will produce a transient voltage on the parallel circuit, which will temporarily affect the operation of the healthy pole. The study of the dynamic behavior and possible consequences of the *LR* parallel grounding circuit under dc faults is out of the scope of this paper. The reader is referred to [29], where the analysis of dc-side grounding schemes for bipolar HVdc systems is presented.

To ensure safety isolation after the fault, disconnectors S_p and S_n are installed with the *LR* parallel grounding circuit. These are shown in Fig. 8. The disconnector associated to a fault will be tripped once the residual current in reactor L_G decays to zero after tripping the grid-side ACCB. It should be emphasized that the disconnectors are not used to interrupt the fault currents. They will be opened at zero current following the fault transients to ensure safety for fault maintenance.

VI. Simulation Results and Analysis

To verify the analysis presented in the previous sections, three different HB-MMC-based HVdc links have been built in PSCAD/EMTDC (shown in Fig. 9). Considering that the number of SMs will not affect the equivalent circuit of a converter once it is blocked, a detailed switching model with 11 levels is implemented to ensure acceptable simulation times.

Since the impact of an SPG fault at a power-control MMC is worse than an SPG fault at a dc voltage-controlling MMC, a

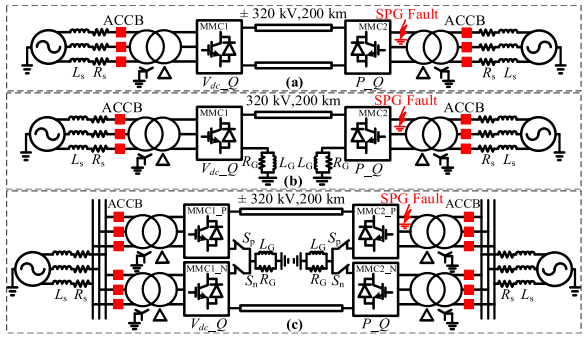

Fig. 9. Three HB-MMC based HVdc links. (a) Symmetrical monopole. (b) Asymmetrical monopole. (c) Bipolar.

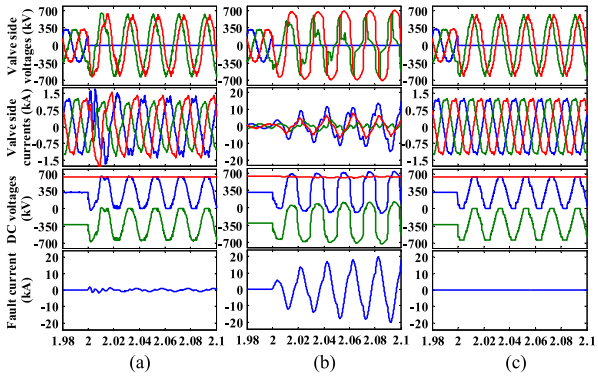

Fig. 10. Fault responses of the case shown in Fig. 13(a). (a) 20 km frequency-dependent cable model. (b) 200 km frequency-dependent cable model. (c) 200 km lumped parameter cable model ($R = 0.0192\,\Omega/km$ and $L = 0.24$ mH/ km).

valve-side SPG fault is set at $t = 2$ s in phase *A* in the power-controlling MMCs for all topologies. A fault resistance $R_F = 0.1\,\Omega$ is assumed. The ac systems are modeled as ideal voltage sources with short-circuit impedances formed by L_S and R_S. For all cases, X_S/R_S and the short-circuit ratio are assumed as 10. A frequency-dependent dc cable model is used, with parameters found in [27]. Remaining parameters are given in the Appendix.

A. Symmetrical Monopole

To illustrate the fault behavior clearly, the converter is not blocked for the system shown in Fig. 9(a). Both frequency-dependent and lumped parameter dc cable models are employed so as to investigate the impacts of dc cable models on fault responses. Two different line lengths are also assessed, with simulation results shown in Fig. 10.

By comparing the results in Fig. 10, it can be concluded that

1) the valve-side voltage of the faulted phase drops to zero, while the nonfaulted phases exhibit line voltage magnitudes;

2) the SPG fault leads to dc pole voltage oscillations whose behaviors depend on the arm voltages in the faulted phase;

3) the maximum magnitudes of the dc pole voltage oscillations reach 2 p.u. of their rated value but the pole-to-pole dc voltage is not severely affected;

4) severe fault currents arise due to the discharge from the distributed capacitors of the dc line;

5) the longer the dc line, the worse the fault consequences.

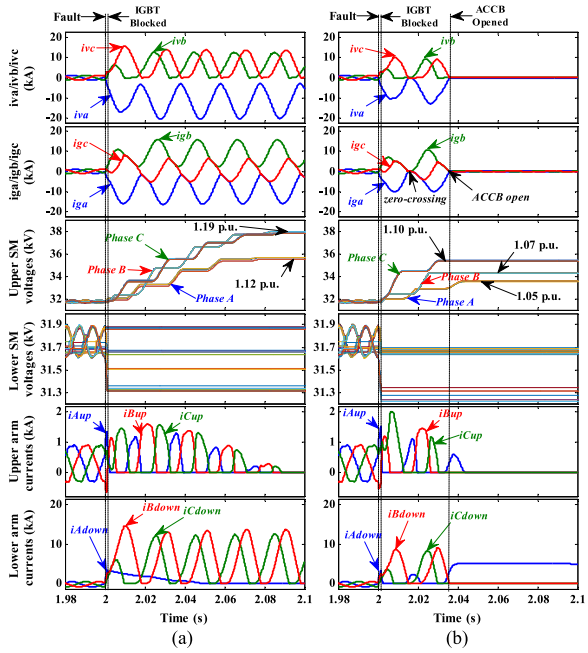

Fig. 11. Simulation results of the system shown in Fig. 9(b). The proposed protection strategy (a) is not employed and (b) is employed.

The simulation results match well with the theoretical analysis provided in Section III.

B. Asymmetrical Monopole

Consider the asymmetrical monopole configuration provided in Fig. 9(b). MMC2 is blocked once any arm current exceeds 3.125 kA, which is two times the rated dc current in this case. To investigate the most serious condition, MMC1 remains unblocked. Currents are positive if they flow in the directions shown in Fig. 3(b).

It can be seen from Fig. 11(a) that the nonfaulted phase currents i_{vb} and i_{vc} are always positive. Current i_{va} in the faulted phase is always negative and exhibits a large dc offset. The grid-side fault current i_{ga} is always negative, whereas i_{gb} is always positive. As a result, grid-side ACCBs are not able to interrupt such fault currents. The upper arm capacitors start to be charged immediately after the fault. Particularly, the upper arm SM voltages in the nonfaulted phases reach 1.19 p.u., but all lower arm SM voltages remain constant once the converter is blocked. The upper arm currents are all positive but become zero once the SM capacitors have been charged to their maximum values. The lower arm current i_{A_down} decays naturally through diode D_4 after the converter has been blocked.

Fig. 11(b) shows results if an *LR* parallel grounding circuit is applied. In this case, MMC1 is blocked once the current flowing into the converter is over 3 kA or if the dc terminal voltage is less than 85% of the rated value. It can be seen that fault currents are reduced significantly. More importantly, current zero-crossings appear and, thus, grid-side ACCBs can interrupt the fault quickly. As a result, the maximum overvoltage in the upper arm SM capacitors is reduced to 1.1 p.u. The residual current in the reactor of the *LR* parallel circuit decays naturally through diode D_4 after the grid-side ACCBs are tripped.

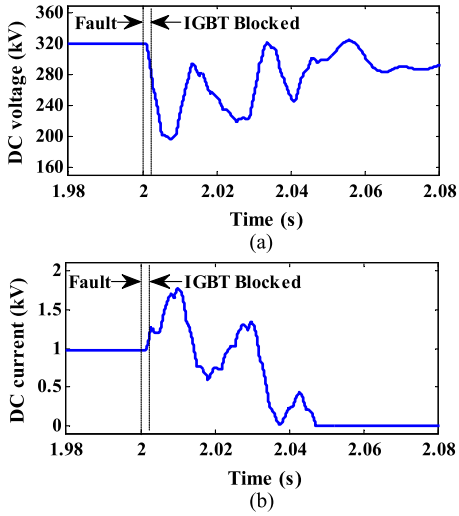

Fig. 12. DC voltage and current of MMC1.

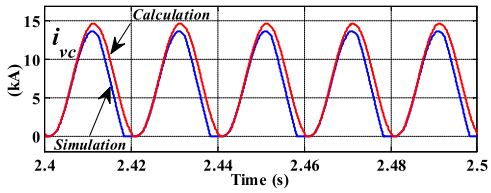

Fig. 13. Simulation and analytical calculation results for i_{vc}.

Fig. 12 illustrates the dc terminal voltage and dc current of MMC1. The converter is blocked when the voltage is lower than 85% of the rated dc voltage. The dc current decays to zero after oscillations.

Fig. 13 compares the steady-state current i_{vc} obtained from the simulation with that analytically calculated for the case when no protection is employed [as in Fig. 11(a)]. As it can be observed, no significant difference between them is present, which, in turn, verifies the theoretical analysis.

Fig. 14 illustrates the impact of the resistor R_G of the *LR* parallel grounding circuit on grid-side current i_{gb} and on the upper arm overvoltage of Phase *B*. The inductor L_G is fixed as 0.3 H. It can be seen from Fig. 14(a) that as L_G bypasses R_G during normal operation, i_{gb} has the same value when the resistance varies. This means that the *LR* parallel grounding circuit does not affect the system's normal operation. Moreover, the parallel circuit not only creates current zero-crossings, but it also reduces the magnitude of the fault current. However, R_G cannot be too large, otherwise there might be a delay of the first zero-crossing. Fig. 14(b) shows that the overvoltage of the upper arm increases when R_G increases. This occurs as the *LR* parallel grounding circuit, when considered, affects (5) as follows:

$$u_b \approx u_{vb} \times (Z_L + Z_{LR}) / (Z_L + Z_{LR} + Z_{\text{equ}}) \qquad (17)$$

where Z_L is the impedance of the arm inductor, Z_{LR} is the impedance of the *LR* parallel grounding, and Z_{equ} is the equivalent impedance of the transformer and ac grid. Voltage u_b is increased compared to the case without the *LR* parallel grounding. Therefore, according to (6), the maximum upper arm overvoltage will be increased. However, as the fault will be iso-

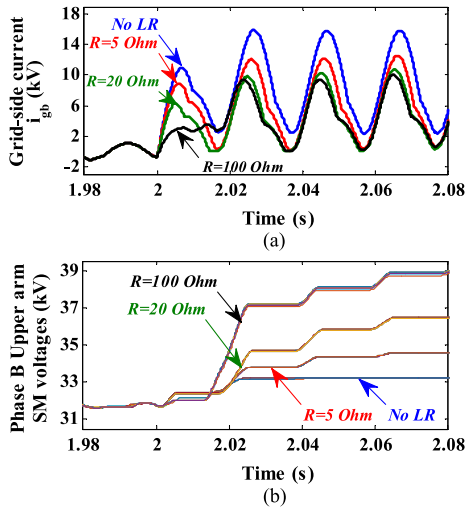

Fig. 14. Impact of resistor R_G of the *LR* parallel grounding on grid-side currents and upper arm overvoltage. (a) Grid-side current i_{gb}. (b) Phase *B* upper arm SM voltages.

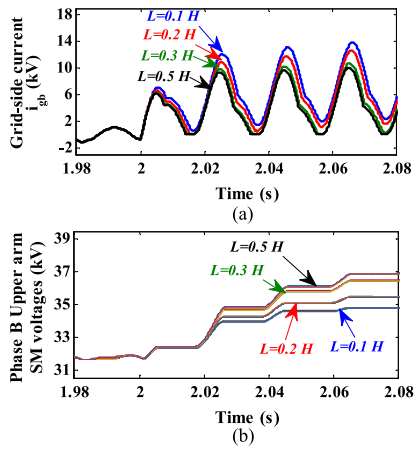

Fig. 15. Impact of inductor L_G of the *LR* parallel grounding on grid-side currents and upper arm overvoltage. (a) Grid-side current i_{gb}. (b) Phase *B* upper arm SM voltages.

lated by the grid-side ACCB before the upper arms are charged to the maximum value, the impact of the *LR* parallel circuit on the upper arm overvoltage will not be severe, as shown in Fig. 11(b).

Fig. 15 illustrates the impact of inductor L_G of the *LR* parallel grounding on grid-side current i_{gb} and on the upper arm overvoltage of Phase *B*. R_G is fixed as 20 Ω. Fig. 15(a) shows that, in this case, an inductance lower than 0.2 H cannot guarantee zero-crossings. A larger inductor may generate zero-crossings; however, as L_G and R_G are in parallel, the impedance is dominated by the resistance if L_G is larger than R_G. Thus, as shown in Fig. 14(b), the upper arm overvoltage does not increase much when the inductance increases from 0.3 to 0.5 H.

C. Bipole

The *LR* circuit and the disconnectors are applied in the bipolar system shown in Fig. 9(c). The fault behavior of the faulted pole is similar to that in Fig. 16(b) and, therefore, is not shown. Fig. 16

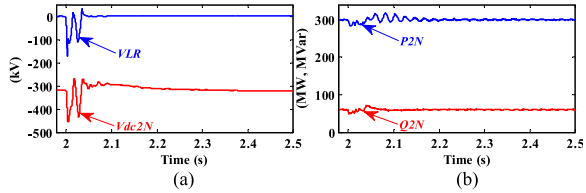

Fig. 16. Responses of the healthy pole. (a) Negative pole voltage and voltage on the *LR* circuit. (b) Output power of the healthy pole.

illustrates that the dc voltage of the healthy pole experiences oscillations. This is a result of the fault current flowing through the *LR* circuit, which produces transient voltages. The operation of the healthy pole is not impacted after the fault transients.

VII. Conclusion

Valve-side SPG faults at MMC HVdc stations result in a significantly different fault behavior compared to grid-side SPG faults. Under this type of faults, the grid-side ACCB may fail to interrupt the fault currents. In this paper, mathematical models were established and theoretical analyses were conducted to investigate the fault behavior caused by valve-side SPG faults for different MMC station configurations.

The analysis shows that a valve-side SPG fault at symmetrical monopoles will lead to large dc pole-to-ground voltage oscillations and overvoltages. In addition, the discharge of the distributed capacitors of the dc transmission line caused by the dc pole-to-ground voltage oscillations will lead to significant fault currents, especially for a long-distance transmission system. Therefore, a dc line model that does not consider distributed capacitors is not suitable to analyze the valve-side SPG faults at symmetrical monopole configurations.

The studies presented in the paper also show that valve-side SPG faults in asymmetrical monopole and bipole systems will result in overvoltages in the upper arm SM capacitors and grid-side nonzero-crossing fault currents. This phenomenon is caused by the uncontrolled freewheeling diodes in the arms connecting to the ground and by the transformer's delta/star configuration. To address these issues, the MMC controlling the dc voltage is blocked to mitigate the upper arm overvoltage and an *LR* parallel circuit is employed to overcome the problem of the nonzero-crossing currents.

The performance and parameter design of the *LR* parallel grounding circuit has been evaluated with simulations performed in PSCAD/EMTDC for both asymmetrical monopole and bipole configurations. The simulation results show that the *LR* parallel circuit performs well in overcoming the nonzero-crossing currents. Moreover, as the fault can be isolated quickly when the *LR* parallel circuit is employed, the upper arm overvoltage is not severe.

Appendix

Consider a diode in series with an inductor as shown in Fig. 17. The current characteristic for this circuit is explained below to derive the coefficients in (12). The ac voltage is assumed as sinusoidal.

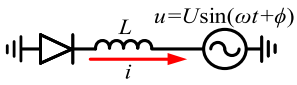

Fig. 17. Inductor in series with a diode.

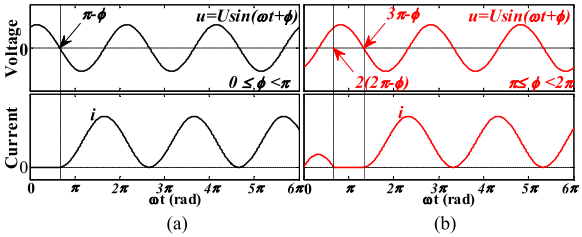

Fig. 18. Schematic diagram of the voltage and current waveforms: (a) $0 \le \phi < \pi$. (b) $\pi \le \phi < 2\pi$.

Fig. 18 illustrates the voltage and current waveforms in the circuit shown in Fig. 17 for ac voltages with different initial phase angles. The diode will conduct from the first negative period if the initial phase angle is $0 \le \phi < \pi$, as shown in Fig. 18(a). Current i is expressed as follows:

$$\begin{cases} i = 0, & 0 \le \omega t < \pi - \phi \\ i = \frac{U}{\omega L}[\cos(\omega t + \phi) + 1], & \pi - \phi \le \omega t \end{cases}. \quad \text{(A1)}$$

It can be seen from (A1) and Fig. 18(a) that the diode will conduct from the first negative period. If the initial phase angle is $\pi \le \phi < 2\pi$, the initial ac voltage will be negative and the diode will conduct immediately from a zero state. However, it will stop conducting early before the next negative period, but will start conducting once the subsequent negative period starts. At this stage, current i can be defined as follows:

$$\begin{cases} i = \frac{U}{\omega L}\cos(\omega t + \phi) - \frac{U}{\omega L}\cos\phi, & 0 \le \omega t < 2(2\pi - \phi) \\ i = 0, & 2(2\pi - \phi) \le \omega t < 3\pi - \phi \\ i = \frac{U}{\omega L}[\cos(\omega t + \phi) + 1], & 3\pi - \phi \le \omega t \end{cases}. \quad \text{(A2)}$$

It can be seen from (A1) and (A2) that the steady-state current will become nonzero-crossing regardless of its initial state. As a result, the diode will remain conducting in steady state.

According to (10), the following expressions can be obtained:

$$\begin{cases} i_{vb} = \frac{-\sqrt{3}U[(L_{va}+L_{vc})\cos(\omega t+\varphi)+L_{va}\cos(\omega t+\varphi-120^\circ)+C_1]}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \\ i_{vc} = \frac{\sqrt{3}U[L_{va}\cos(\omega t+\varphi)+(L_{va}+L_{vb})\cos(\omega t+\varphi-120^\circ)+C_2]}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \end{cases}. \quad \text{(A3)}$$

Considering the initial conditions in (11), i_{vb} and i_{vc} are given by (A4) as shown at the bottom of this page

Parameters of the system in Fig. 13(a): rated power: 1000 MW; dc voltage: ± 320 kV; ac voltage: 230 kV; ac frequency: 50 Hz; transformer ratio: 400/230 kV; transformer leakage inductance: 0.1 p.u.; number of SM in each arm: 10; SM capacitance: 25 mF; arm inductance: 0.05 H; arm resistance: 0.1 Ω; ac system resistance and reactance: 0.52641 Ω and 0.01674 H.

Parameters of the system in Fig. 13(b): rated power: 500 MW; dc voltage: 320 kV; ac voltage: 230 kV; ac frequency: 50 Hz; transformer ratio: 200/230 kV; transformer leakage inductance: 0.1 p.u.; number of SM in each arm: 10; SM capacitance: 25 mF; arm inductance: 0.025 H; arm resistance: 0.1 Ω; ac system resistance and reactance: 1.05275 Ω and 0.03351 H; *LR* parallel circuit: R_G : 20 Ω; L_G : 0.3 H.

ACKNOWLEDGMENT

The authors would like to thank Dr. Z. Song from Toshiba International (Europe) for his guidance and expertise.

REFERENCES

[1] X. Shi, Z. Wang, B. Liu, Y. Liu, L. M. Tolbert, and F. Wang, "Characteristic investigation and control of a modular multilevel converter-based HVdc system under single-line-to-ground fault conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 408–421, Jan. 2015.
[2] D. van Hertem, O. Gomis-Bellmunt, and J. Liang, "Chapter 3: HVdc technology overview," in *HVdc Grids: For Offshore and Supergrid of the Future*. Hoboken, NJ, USA: Wiley, Apr. 2016, pp. 45–76.
[3] Nemo Link. [On line]. Available: http://www.nemo-link.com/
[4] R. Hong, "Architecture of Nan'ao multi-terminal VSC-HVdc system and its multi-functional control," *CSEE J. Power Energy Syst.*, vol. 1, no. 1, pp. 9–18, Mar. 2015.
[5] G. F. Tang, Z. Y. He, H. Pang, X. M. Huang, and X. P. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE J. Power Energy Syst.*, vol. 1, no. 2, pp. 22–35, Jun. 2015.
[6] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
[7] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVdc applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.
[8] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVdc systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.
[9] W. Leterme, J. Beerten, and D. van Hertem, "Nonunit protection of HVdc grids with inductive DC cable termination," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 820–828, Apr. 2016.
[10] R. Li, L. Xu, D. Holliday, F. Page, S. J. Finney, and B. W. Williams, "Continuous operation of radial multiterminal HVdc systems under DC fault," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 351–361, Feb. 2016.
[11] Q. Tu, Z. Xu, Y. Chang, and L. Guan, "Suppressing DC voltage ripples of MMC-HVdc under unbalanced grid conditions," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1332–1338, Jul. 2012.

$$\begin{cases} i_{vb} = M_1\left[1 - \sin(\omega t + \Phi_1)\right], \quad i_{vc} = M_2\left[\sin(\omega t + \Phi_2) + 1\right], \\ \text{where} \quad \Phi_1 = \varphi + \arctan\frac{L_{va}+2L_{vc}}{\sqrt{3}L_{va}}, \quad \Phi_2 = \varphi + \arctan\frac{L_{va}-L_{vb}}{\sqrt{3}(L_{va}+L_{vb})}, \\ M_1 = \frac{\sqrt{3}U\sqrt{\left(\frac{\sqrt{3}}{2}L_{va}\right)^2+\left(\frac{1}{2}L_{va}+L_{vc}\right)^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} = \frac{\sqrt{3}U\sqrt{{L_{va}}^2+L_{va}L_{vc}+{L_{vc}}^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega}, \\ M_2 = \frac{\sqrt{3}U\sqrt{\left[\frac{\sqrt{3}}{2}(L_{la}+L_{lb})\right]^2+\left[\frac{1}{2}(L_{la}-L_{lb})\right]^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} = \frac{\sqrt{3}U\sqrt{{L_{va}}^2+L_{va}L_{vb}+{L_{vb}}^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \end{cases}. \quad \text{(A4)}$$

[12] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVdc system under unbalanced grid conditions," *IEEE Trans. Power Electron*, vol. 27, no. 12, pp. 4858–4867, Dec. 2012.
[13] M. P. Bahrman and B. K. Johnson, "The ABCs of HVdc transmission technologies," *IEEE Power Energy Mag*., vol. 5, no. 2, pp. 32–44, Mar./Apr. 2007.
[14] D. Retzmann, "High voltage direct current transmission HVdc station layout, equipment LCC & VSC and integration of renewables using HVdc," CIGRE Tutorial 2012, 2012. [Online]. Available: http://www.ptd.siemens.de/Cigre_AUS_2011_HVDC_&_GridAccess_tutorial_Re.pdf
[15] A. Nami, J. Liang, F. Dijkhuizen, and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVdc transmission systems," in *Proc. 2015 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–10.
[16] X. Li, Y. Liu, Z. Cai, and K. Han, "Research on single phase grounding fault at HVdc VSC transformer valve-side," in *Proc. 2011 4th Int. Conf. Elect. Utility Deregulation Restruct. Power Technol.*, Weihai, China, 2011, pp. 471–476.
[17] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection," *Proc. Chin. Soc. Elect. Electron. Eng.*, vol. 31, no. 22, pp. 88–95, Aug. 2011.
[18] J. Yang, J. Zheng, G. Tang, and Z. He, "Internal AC bus fault characteristics of VSC-HVdc system and protection coordination," *Proc. Chin. Soc. Elect. Electron. Eng.*, vol. 30. no. 16, pp. 6–11, Jun. 2010.
[19] L. Tang and B. T. Ooi, "Managing zero sequence in voltage source converter," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 37th IAS Annu. Meeting*, Pittsburgh, PA, USA, 2002, vol. 2, pp. 795–802.
[20] X. Chen, C. Zhao, and C. Cao, "Research on the fault characteristics of HVdc based on modular multilevel converter," in *Proc. 2011 IEEE Elect. Power Energy Conf.*, Winnipeg, MB, Canada, 2011, pp. 91–96.
[21] J. Zhang, C. Zhao, X. Huang, Y. Lu, and P. Qiu, "Simulation research on earth fault characteristics of modular multilevel converter based high voltage direct current transmission system," *Power Syst. Technol.*, vol. 38, no. 10, pp. 2658–2664.
[22] J. P. Kjærgaard *et al.*, "Bipolar operation of an HVdc VSC converter with an LCC converter," in *Proc. CIGRE Colloquium HVdc Power Electron. Syst*., San Francisco, CA, USA, 2012, pp. 1–7.
[23] G. Andersson and M. Hyttinen, "Skagerrak—the next generation," in *Proc. HVdc Power Electron. Technol.*, Lund, Sweden, 2015, pp. 1–9.
[24] Y. Zhou, Z. He, H. Pang, J. Yang, and Q. Li, "Protection of converter grounding fault on MMC based bipolar HVdc systems," *Proc. Chin. Soc. Elect. Electron. Eng.*, vol. 35, no. 16, pp. 4062–4069, Aug. 2015.
[25] G. Li, Z. Song, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in bipolar HVdc systems," in *Proc. 2017 IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 2659–2665.
[26] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
[27] M. K. Bucher and C. M. Franck, "Contribution of fault current sources in multiterminal HVdc cable networks," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1796–1803, Jul. 2013.
[28] P. Zhou, M. Dai, Y. Lou, and M. Xiu, "DC component time constant and zero offset phenomena of breaking current for 1000 kV circuit breaker," *High Voltage Eng*., vol. 35, no. 4, pp. 722–730, Apr. 2009.
[29] W. Leterme, P. Tielens, S. De Boeck, and D. van Hertem, "Overview of grounding and configuration options for meshed HVdc Grids," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2467–2475, Dec. 2014.

Gen Li received the B.Eng. degree from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree from Nanyang Technological University, Singapore, in 2013, and the Ph.D. degree from Cardiff University, Cardiff, Wales U.K., in 2018, all in electrical engineering.

From 2013 to 2016, he was a Marie Curie Early Stage Researcher funded by the European Union's MEDOW project. He has been a Visiting Researcher with China Electric Power Research Institute, Beijing, China, at Elia, Brussels, Belgium, and at Toshiba International (Europe), London, U.K. He has been a Research Associate with the School of Engineering, Cardiff University, Cardiff, U.K., since 2017. His research interests include high-voltage and medium-voltage dc technologies, power electronics, and power system stability control.

Jun Liang (M'02–SM'12) received the B.Sc. degree from the Huazhong University of Science and Technology, Wuhan, China, in 1992, and the M.S. and Ph.D. degrees from the China Electric Power Research Institute (CEPRI), Beijing, China, in 1995 and 1998, respectively, all in electrical engineering and its automation.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, London, U.K. From 2005 to 2007, he was with the University of Glamorgan as a Senior Lecturer. He is currently a Professor with the School of Engineering, Cardiff University, Cardiff, U.K. He has been appointed as an Adjunct Professor at the Changsha University of Science and Technology of China, Changsha, China, North China Electric Power University, Boding, China, and Northeast Electric Power University, Jilin, China, since 2014, 2015, and 2017, respectively. His research interests include HVdc, MVdc, FACTS, power system stability control, power electronics, and renewable power generation.

Prof. Liang is an Editorial Board Member of Chinese Society for Electrical Engineering Journal of Power and Energy Systems (CSEE JPES).

Fan Ma received the B.Sc. and M.S. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2005 and 2007, respectively, and the Ph.D. degree from the Naval University of Engineering, Wuhan, in 2013, all in electrical engineering and its automation.

He is currently an Associate Researcher with the National Key Laboratory of Science and Technology on Vessel Integrated Power System, Naval University of Engineering. His research interests include medium voltage dc technologies, power electronics, isolated power systems, and microgrids.

Carlos E. Ugalde-Loo (M'02) was born in Mexico City. He received the B.Sc. degree in electronics and communications engineering from Instituto Tecnológico y de Estudios Superiores de Monterrey, Monterrey, Mexico, in 2002, the M.Sc. degree in electrical engineering from Instituto Politécnico Nacional, Mexico City, Mexico, in 2005, and the Ph.D. degree in electronics and electrical engineering from the University of Glasgow, Scotland, U.K. in 2009.

In 2010, he joined the School of Engineering in Cardiff University, Wales, U.K., and is currently a Senior Lecturer in Electrical Power Systems. His academic expertise includes power system stability and control, grid integration and control of renewables, HVdc transmission, modeling of dynamic systems, and multivariable control.

Haifeng Liang (M'09) was born in Hebei, China. He received the B.Sc. degree from North China Electric Power University (NCEPU), Boding, China, in 1998, the M.Sc. degree from Huazhong University of Science & Technology, Wuhan, China, in 2001, and the Ph.D. degree from NCEPU, in 2009, all in power system and its automation.

From 2012 to 2013, he was a Postdoc with Tianjin University, Tianjin, China. He was a Visiting Scholar with Cardiff University, Cardiff, Wales, U.K., in 2016. Since 2001, he has been with the Department of Electrical Engineering, NCEPU. He is currently an Associate Professor. His research interests include new transmission and distribution technologies, microgrids, VSC-HVdc, and distributed generation and its grid integration technologies.