A Push–Pull Modular-Multilevel-Converter-Based Low Step-Up Ratio DC Transformer

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***Abstract*—A nonisolated dc–dc converter with chain links of submodules (SMs) is proposed in this paper. The converter can perform as a dc transformer with a low step-up ratio. To demonstrate the step-up dc–dc conversion, the converter is operated in a resonant conversion mode, achieving soft switching and inherent balancing of the SM capacitor voltages. The circuit configuration is presented and the operation principle is analyzed in this paper. Experimental results based on a downscaled prototype validate the performance of the proposed converter as a low step-up ratio dc transformer. The converter also exhibits a good linearity covering a broad range.**

***Index Terms*—DC transformer, low step ratio, medium-voltage converter, modular multilevel converter (MMC).**

I. Introduction

THE high-voltage direct current technology is rapidly developing for large-scale power transmission systems [1]–[4]. This highly involves deployments of modular multilevel converters (MMCs) [5]–[9], which are also used for industrial drive systems at the medium voltage level [10]–[12]. Although most of the existing dc systems are using the point-to-point connected MMCs, there is a growing demand on the evolution to the dc grids. A key technical challenge that has to be faced is the implementation of dc transformers used for voltage-level changes. Developing low-cost, high-efficiency dc transformers requires proper arrangement to customize. Conventional MMC technologies in the applications of dc–ac conversion cannot be used straightforwardly for dc transformation. Nevertheless, following the remarkable success in point-to-point transmission systems, MMCs for dc–dc conversion have the advantages of modularity and redundancy, which still attract great attention for the demands in dc systems.

Innovations on the MMC based dc–dc converters in medium- and high-voltage applications have made prominent achievements [13]–[21]. To accomplish low step ratio dc–dc conversion, the topologies can be classified into two different groups according to the arrangement of the stacks: front-to-front [17]–[19] and direct chain link [20]–[23]. The former architecture, which typically involves two MMCs with coupled ac sides, can be implemented with existing technologies. However, the conversion only transfers the power of one unit using two MMCs, leading to a high cost and huge losses for a low step ratio dc–dc conversion. The latter, with only one chain link required, takes less footprint and can be more efficient in principle [22]. However, the control of chain-link converters is complicated and challenging [23], [24], and the step-up conversion is severely constrained by the impedance of the passive components in the circuit. Hence, such chain-link configuration has not been seen implemented for step-up dc–dc conversion so far. Technical development on the topology and control of chain-link dc–dc converters will make contribution to bridge the gap between the state-of-the-art concept and the emerging application requirement.

In order to explore the dc transformation approach based on chain-link converters, this paper studies a low step-up ratio dc transformer topology without using isolation transformer. The converter is arranged with chain-link half-bridge submodules (SMs), being able to achieve a step-up ratio range meeting major requirements. The chain links have only one function, which provide a push–pull power to the output rectifier. The proposed converter is operated in a resonant mode for the step-up dc–dc conversion with soft switching. The converter topology described in this paper is monopolar but it can also be reconfigured for the bipolar conversion. The step-up ratio ranges mainly according to the modulation scheme. Owning to the resonant operation, the converter step-up ratio can also be regulated by the operating frequency. With appropriate modulation methods, the SM capacitor voltages of the converter can be balanced without using additional balancing control. The analysis of the step-up conversion operating in the resonant mode is verified by the relevant experimental results.

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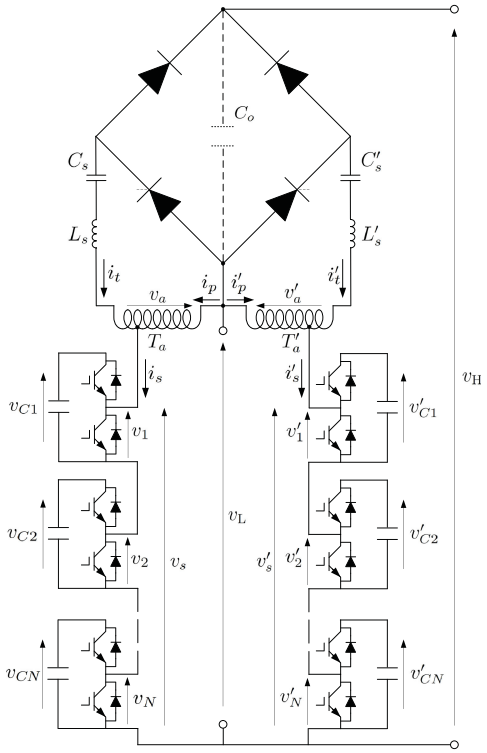

Fig. 1. Circuit topology of the monopolar low step-up ratio dc–dc converter using two chain links.

II. Low Step-Up Ratio Chain-Link DC–DC Converter

This section presents the circuit configuration of the proposed low step-up ratio chain-link dc–dc converter. The operation principle is analyzed and the general transformation feature is provided.

A. Circuit Topology of Monopolar Low Step-Up Ratio DC Transformer

The circuit topology of the low step-up ratio dc–dc converter with two chain links is shown in Fig. 1. Bipolar arrangement can be accomplished by connecting another monopolar converter configured with negative polarity. The converter is bilaterally symmetrical. It consists of two stacks each with N half-bridge submodules, autotransformers T_a and T'_a with the step ratio of γ_T, series impedance L_s and C_s (L'_s and C'_s), and an output rectifier with a virtual capacitor C_o seen on the terminal (equal to series capacitance on high-voltage side and low-voltage side). The rectifier may contain several components in series, depending on the rectifier voltage level. Deployment of thyristors can realize forward blocking, but in normal situations the operation would not differ from that of diodes. The SM capacitors on the left-hand side and right-hand side are denoted by C_j and C'_j ($j = 1, 2, \ldots, N$), respectively. The capacitor voltage and output voltage of the jth submodule are represented by v_{Cj} (or v'_{Cj}) and v_j (or v'_j), respectively. The voltage across the stack and autotransformer are represented by v_s (or v'_s) and v_a (or v'_a), respectively. The low-voltage dc and high-voltage dc are represented by $v_{\rm L}$ and $v_{\rm H}$, respectively. The final high dc voltage

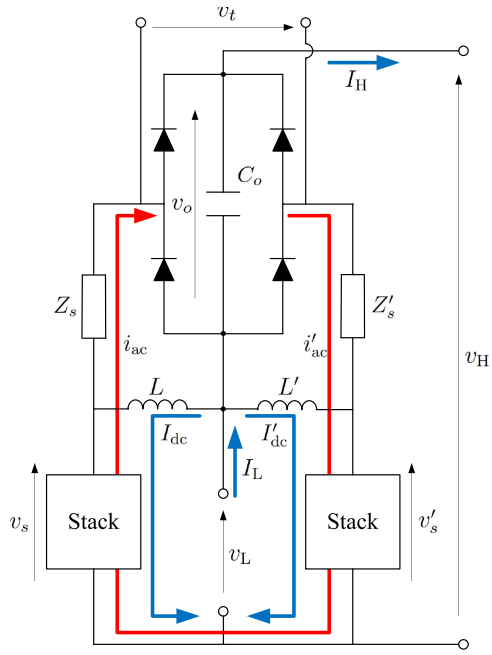

Fig. 2. Simplified circuit diagram of the proposed converter.

$v_{\rm H}$ is obtained by the dc voltage v_o rectified from the push–pull stack output plus $v_{\rm L}$. The function of the chain link is to generate an ac voltage, which enables the converter to be operated in various ways.

B. Operation Principle of the Proposed Low Step-Up Ratio Converter

To analyze the operation principle, the circuit topology in Fig. 1 is simplified to the diagram shown in Fig. 2. The converter operation presented in Fig. 2 is based on the following assumptions.

1) The parameters in the symmetric positions are the same.
2) The large inductors L and L' representing autotransformers completely block the ac current flowing through.
3) The impedances Z and Z' have infinite dc resistance but negligible ac impedance at the operating frequency.

The stacks with half-bridge SMs in the converter are operated to generate square wave voltages v_s and v'_s. The dc components of v_s and v'_s are assumed to be the same. The ac components of v_s and v'_s have a modulation index of m and a 180° phase delay to each other. Therefore, a push–pull output with the equivalent operating frequency of $f_{\rm eq}$ is generated by the stacks, which is written as follows:

$$\begin{bmatrix} v_s \\ v'_s \end{bmatrix} = \begin{bmatrix} 1 & -\mathrm{sgn}\left(\sin 2\pi f_{\rm eq} t\right) \\ 1 & +\mathrm{sgn}\left(\sin 2\pi f_{\rm eq} t\right) \end{bmatrix} \begin{bmatrix} v_{\rm L} \\ m v_{\rm L} \end{bmatrix}. \tag{1}$$

This ac voltage difference between the two stacks is further amplified by the autotransformer, yielding

$$\begin{bmatrix} v_a \\ v'_a \end{bmatrix} = -\begin{bmatrix} \gamma_T & 0 \\ 0 & \gamma_T \end{bmatrix} \begin{bmatrix} v_s \\ v'_s \end{bmatrix} + \begin{bmatrix} \gamma_T \\ \gamma_T \end{bmatrix} v_{\rm L}. \tag{2}$$

The voltage difference between v_a and v'_a is applied to the rectifier with the impedance networks in series, which is derived

as follows:

$$v_a - v_a' = 2m\gamma_T v_{\rm L} \cdot \mathrm{sgn}\left(\sin 2\pi f_{\rm eq} t\right). \tag{3}$$

For a square wave rectifier input voltage v_t with frequency matching the resonant frequency, its rectified output is approximated by

$$v_o = 2m\gamma_T v_{\rm L}. \tag{4}$$

The rectified voltage v_o in series with the low dc voltage $v_{\rm L}$ forms the high dc voltage $v_{\rm H}$. The converter step ratio is defined as $\gamma = v_{\rm H}/v_{\rm L}$.

During the step-up operation, the current flow can be observed in Fig. 2. The ac current generated from the stacks flows in a big circle. As the impedance network has negligible ac impedance at the operating frequency, when the ac current flows through the impedance network, the ac voltage across the network is small. Hence, the output voltage v_o is determined mainly by the stack ac voltage.

The step-up converter behaves as a voltage controlled converter. The current $I_{\rm H}$ is determined by $v_{\rm H}$ and the load R. If the converter is lossless, the stack currents can be written as follows:

$$\begin{cases} I_{\rm dc} = I_{\rm dc}' = (\gamma - 1) I_{\rm H}/2 \\ I_{\rm ac} = I_{\rm ac}' = I_{\rm H} \end{cases}. \tag{5}$$

Usually, the switch voltage rating requires at least 1.5 times of the cell voltage v_C. The maximum step-up ratio from the low dc voltage to the high dc voltage is

$$\gamma = 1 + 2m\gamma_T. \tag{6}$$

For an ordinary stack, there is $0 < m < 1$. The step-up ratio range is written as follows:

$$1 < \gamma < 1 + 2\gamma_T. \tag{7}$$

However, the actual step ratio is usually lower than the maximum value to leave a margin for regulation of the high dc voltage. The converter works as a low step-up ratio dc transformer. The ratio is also determined by the modulation method and the control scheme.

III. DC Transformation Operating in a Resonant Mode

This section demonstrates the modulation method of the converter in a resonant mode. The resonant mode is one of the operation modes. It can reflect the converter performance with soft switching and verify the feasibility of the step-up conversion.

A. Low Step-Up Ratio DC Transformer Operated in the Resonant Conversion Mode

The actual step ratio is dependent on the push–pull stack voltage output. Modulation and control of the stacks can determine the operation mode of the converter, achieving a flexible step-up ratio. Although many control schemes can be used, this paper demonstrates the resonant mode to explain the operation principle of the step-up conversion.

The switching of SMs determines the number of SM capacitors in series and the total voltage across the stacks. In resonant operation mode, the converter generates square wave voltages v_s and v_s'. This is obtained by changing the numbers of SM capacitors in series. To achieve a higher dc voltage $v_{\rm H}$, the amplitude of the square wave voltage should be high. Taking $N = 5$ as an example, there are five cells in the left stack and five in the right. The highest square wave voltage amplitude can be obtained by using the modulation method in Table I.

TABLE I
SM Capacitor Deployment for the Resonant Operation With $X = 5$ and $Y = 1$

State	Left stack	Right stack
1	C_1, C_2, C_3, C_4, C_5	C_1'
2	C_1	C_1', C_2', C_3', C_4', C_5'
3	C_1, C_2, C_3, C_4, C_5	C_2'
4	C_2	C_1', C_2', C_3', C_4', C_5'
5	C_1, C_2, C_3, C_4, C_5	C_3'
6	C_3	C_1', C_2', C_3', C_4', C_5'
7	C_1, C_2, C_3, C_4, C_5	C_4'
8	C_4	C_1', C_2', C_3', C_4', C_5'
9	C_1, C_2, C_3, C_4, C_5	C_5'
10	C_5	C_1', C_2', C_3', C_4', C_5'

This modulation method results in ten switching states of the converter. Each state lasts for an equal time span. In State 1, all the SM capacitors of the left stack are deployed in series to participate the resonant operation. However, only the first SM capacitor of the right stack is deployed. In the last state, only C_5 of the left stack is deployed but all the SM capacitors of the right stack are inserted. After all the states in Table I, the stacks enter the first state again and repeat this modulation table.

It can be seen that at any time the ac current flows through five capacitors in one stack but flows through one capacitor in the other stack. The number with more capacitors that the ac current flowing through is defined as X, whereas the number with fewer capacitors that the ac current flowing through is defined as Y. In the operation mode of Table I, $X = 5$ and $Y = 1$.

The voltage across the large inductor pair is $v_s - v_s'$. If all the SM capacitor voltages are the same, in each state of Table I, the voltage $v_s - v_s'$ is equal to either $4\overline{v}_C$ or $-4\overline{v}_C$. Therefore, assuming that the step ratio of autotransformers is $\gamma_T = 1$, the peak voltage of the square wave across the large inductor pair is $4\overline{v}_C$.

On the other hand, each stack voltage steps between $\overline{v}_C$ and $5\overline{v}_C$, yielding an average stack dc voltage of $3\overline{v}_C = v_{\rm L}$. As a result, the peak voltage of the square wave across the large inductor pair is $4v_{\rm L}/3$. If the square wave has a frequency matching the resonant frequency of the impedance network, the step-up ratio is $\gamma = 7/3$.

The resonant operation can also obtain a lower dc voltage $v_{\rm H}$. This can be achieved by modifying the arrangement of the SM capacitors in series deployment. Using the modulation method in Table II, the stack voltage steps between $2\overline{v}_C$ and $5\overline{v}_C$. Owning to the page limit, the detailed analysis is not presented here. At the resonant frequency, the step-up ratio is $\gamma = 13/7$.

An even lower dc voltage $v_{\rm H}$ can be obtained with the modulation method in Table III. The stack voltage steps between $3\overline{v}_C$ and $5\overline{v}_C$. The average stack dc voltage is equal to $4\overline{v}_C$. At the resonant frequency, the step-up ratio is $\gamma = 3/2$.

The smallest step-up ratio in the resonant mode is achieved by generating a low-amplitude square wave voltage push–pull

TABLE II
SM CAPACITOR DEPLOYMENT FOR RESONANT OPERATION WITH $X = 5$ AND $Y = 2$

State	Left stack	Right stack
1	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2
2	C_1, C_2	C'_1, C'_2, C'_3, C'_4, C'_5
3	C_1, C_2, C_3, C_4, C_5	C'_2, C'_3
4	C_2, C_3	C'_1, C'_2, C'_3, C'_4, C'_5
5	C_1, C_2, C_3, C_4, C_5	C'_3, C'_4
6	C_3, C_4	C'_1, C'_2, C'_3, C'_4, C'_5
7	C_1, C_2, C_3, C_4, C_5	C'_4, C'_5
8	C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
9	C_1, C_2, C_3, C_4, C_5	C'_1, C'_5
10	C_1, C_5	C'_1, C'_2, C'_3, C'_4, C'_5

TABLE III
SM CAPACITOR DEPLOYMENT FOR RESONANT OPERATION WITH $X = 5$ AND $Y = 3$

State	Left stack	Right stack
1	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2, C'_3
2	C_1, C_2, C_3	C'_1, C'_2, C'_3, C'_4, C'_5
3	C_1, C_2, C_3, C_4, C_5	C'_2, C'_3, C'_4
4	C_2, C_3, C_4	C'_1, C'_2, C'_3, C'_4, C'_5
5	C_1, C_2, C_3, C_4, C_5	C'_3, C'_4, C'_5
6	C_3, C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
7	C_1, C_2, C_3, C_4, C_5	C'_1, C'_4, C'_5
8	C_1, C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
9	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2, C'_5
10	C_1, C_2, C_5	C'_1, C'_2, C'_3, C'_4, C'_5

TABLE IV
SM CAPACITOR DEPLOYMENT FOR RESONANT OPERATION WITH $X = 5$ AND $Y = 4$

State	Left stack	Right stack
1	C_1, C_2, C_3, C_4, C_5	C'_2, C'_3, C'_4, C'_5
2	C_2, C_3, C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
3	C_1, C_2, C_3, C_4, C_5	C'_1, C'_3, C'_4, C'_5
4	C_1, C_3, C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
5	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2, C'_4, C'_5
6	C_1, C_2, C_4, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
7	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2, C'_3, C'_5
8	C_1, C_2, C_3, C_5	C'_1, C'_2, C'_3, C'_4, C'_5
9	C_1, C_2, C_3, C_4, C_5	C'_1, C'_2, C'_3, C'_4
10	C_1, C_2, C_3, C_4	C'_1, C'_2, C'_3, C'_4, C'_5

output, with the modulation method is shown in Table IV. The voltage $v_s - v'_s$ is equal to either $\overline{v}_C$ or $-\overline{v}_C$. Therefore, with the modulation method in Table IV, the peak voltage of the square wave across the large inductor pair is $\overline{v}_C$. On the other hand, the average stack dc voltage is $4.5\overline{v}_C$, which is equal to $v_{\rm L}$. As a result, the peak voltage of the square wave across the large inductor pair is $2v_{\rm L}/9$. If the square wave has a frequency matching the resonant frequency of the impedance network, the step-up ratio is $\gamma = 11/9$.

In general, the step-up ratio can be calculated based on the numbers of SM capacitors deployed in series resonant operation. In a resonant state, if one stack has X capacitors inserted in series and the other has Y capacitors inserted in series ($X > Y$), the average SM voltage is written as follows:

$$\overline{v}_C = \frac{2v_{\rm L}}{X+Y}. \tag{8}$$

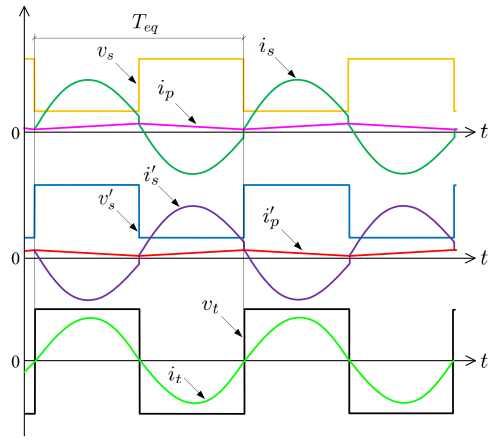

Fig. 3. Time domain key waveforms of the converter.

The rectified voltage is equal to the peak voltage of $v_a - v'_a$, yielding

$$\overline{v}_C = \frac{1}{\gamma_T}\frac{v_o}{X-Y}. \tag{9}$$

Substituting (9) into (8), the step-up ratio of the converter at the resonant frequency is

$$\gamma = 1 + 2\gamma_T \frac{X-Y}{X+Y}. \tag{10}$$

Variations on the combination of X and Y achieve a flexible step-up ratio. However, owing to the page limit, the other modulation methods in the resonant mode are not explained in detail. Regardless of the amplitude of the square wave voltage across the large inductor pair, the key voltage and current waveforms of the converter in different conduction modes are shown in Fig. 3.

Fig. 3 shows the key waveforms of the converter with the equivalent operating frequency slightly higher than the resonant frequency of the impedance network. The two sides have symmetric operations. The first-half cycle starts with $v_t = v_o$, where the stack current i_s and parallel the current i_p are overlapped. The stack current i_s resonates until the rectifier input voltage is reversed to negative. At that instant, the commutation of the rectifier current forces the stack current to overlap with the parallel current immediately. In the second half-cycle, the input voltage of the rectifier becomes negative, with i_s resonating to its negative peak. The stack current i_s finally overlaps with the parallel current i_p when the rectifier input voltage is reversed to positive. During this equivalent operating cycle, the rectifier voltage is a complete square wave. The rectifier current i_t is sinusoidal and keeps the same phase with the rectifier voltage, supplying a constant resonant power to the output. Meanwhile, the dc energy deviation and ac energy deviation of each stack keeps a zero sum, satisfying the stack power balancing condition.

B. Inherent Balancing of SM Capacitor Voltages

The inherent balancing ability is an attractive feature of the resonant conversion mode. With inherent balancing, there is no need to use additional balancing control. The balancing ability is mainly determined by the modulation method. For the

modulation method in Table I ($X = 5$, $Y = 1$), each state corresponds to an equation following the voltage law in the circuit, which can be written as follows:

$$\begin{bmatrix} \boldsymbol{A}_{5,1} & \mathbf{0}_{5\times5} & \mathbf{1}_{5\times1} \\ \mathbf{0}_{5\times5} & \boldsymbol{A}_{5,1} & \mathbf{1}_{5\times1} \\ \mathbf{1}_{1\times5} & \mathbf{0}_{1\times5} & -1 \end{bmatrix} \begin{bmatrix} \boldsymbol{v_C} \\ \boldsymbol{v'_C} \\ \frac{1}{2}v_o \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{5\times1} \\ \mathbf{1}_{5\times1} \\ 1 \end{bmatrix} v_{\text{L}} \tag{11}$$

with

$$\boldsymbol{A}_{5,1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\boldsymbol{v_C} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \end{bmatrix}, \text{ and } \boldsymbol{v'_C} = \begin{bmatrix} v'_{C1} \\ v'_{C2} \\ v'_{C3} \\ v'_{C4} \\ v'_{C5} \end{bmatrix}$$

.

It can be calculated that the equation set of (11) has a unique solution. Each SM capacitor voltage equals to $v_o/4$ and is clamped by the voltage on the output capacitor. Hence, under this operation mode, the SM capacitor voltages are well balanced.

The SM capacitor voltages in the operation mode with the modulation method in Table II ($X = 5, Y = 2$) can be described as follows:

$$\begin{bmatrix} \boldsymbol{A}_{5,2} & \mathbf{0}_{5\times5} & \mathbf{1}_{5\times1} \\ \mathbf{0}_{5\times5} & \boldsymbol{A}_{5,2} & \mathbf{1}_{5\times1} \\ \mathbf{1}_{1\times5} & \mathbf{0}_{1\times5} & -1 \end{bmatrix} \begin{bmatrix} \boldsymbol{v_C} \\ \boldsymbol{v'_C} \\ \frac{1}{2}v_o \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{5\times1} \\ \mathbf{1}_{5\times1} \\ 1 \end{bmatrix} v_{\text{L}} \tag{12}$$

with

$$\boldsymbol{A}_{5,2} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 \end{bmatrix}.$$

The equation set of (12) also has a unique solution. Each SM capacitor has a voltage equal to $v_o/3$. Under this operation mode, the SM capacitor voltages are balanced as well.

The operation mode achieved by the modulation scheme in Table III ($X = 5$, $Y = 3$) can be described by the equation set

$$\begin{bmatrix} \boldsymbol{A}_{5,3} & \mathbf{0}_{5\times5} & \mathbf{1}_{5\times1} \\ \mathbf{0}_{5\times5} & \boldsymbol{A}_{5,3} & \mathbf{1}_{5\times1} \\ \mathbf{1}_{1\times5} & \mathbf{0}_{1\times5} & -1 \end{bmatrix} \begin{bmatrix} \boldsymbol{v_C} \\ \boldsymbol{v'_C} \\ \frac{1}{2}v_o \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{5\times1} \\ \mathbf{1}_{5\times1} \\ 1 \end{bmatrix} v_{\text{L}} \tag{13}$$

with

$$\boldsymbol{A}_{5,3} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 \end{bmatrix}.$$

TABLE V
COMPARISON OF THE TWO CONVERTER SCHEMS

Converter scheme	Cell number	Voltage stress	Current stress	Power Losses
MMDC [24]	18	5.5 kV	1 kA	57 kW
Proposed	18	3.5 kV	0.8 kA	43 kW

This operation mode gives a unique solution of the SM capacitor voltages. The solution can be obtained from (13) and the SM capacitor voltages are balanced.

The operation mode with the lowest step-up ratio corresponding to the modulation method in Table IV ($X = 5$, $Y = 4$) is also studied. In this mode the capacitor voltages follow the equation set

$$\begin{bmatrix} \boldsymbol{A}_{5,4} & \mathbf{0}_{5\times5} & \mathbf{1}_{5\times1} \\ \mathbf{0}_{5\times5} & \boldsymbol{A}_{5,4} & \mathbf{1}_{5\times1} \\ \mathbf{1}_{1\times5} & \mathbf{0}_{1\times5} & -1 \end{bmatrix} \begin{bmatrix} \boldsymbol{v_C} \\ \boldsymbol{v'_C} \\ \frac{1}{2}v_o \end{bmatrix} = \begin{bmatrix} \mathbf{1}_{5\times1} \\ \mathbf{1}_{5\times1} \\ 1 \end{bmatrix} v_{\text{L}} \tag{14}$$

with

$$\boldsymbol{A}_{5,4} = \begin{bmatrix} 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \end{bmatrix}.$$

It can be calculated that the equation set of (14) has a unique solution, and the SM capacitor voltages are inherently balanced. In the equation sets of (11)–(14), each matrix on the left-hand side has full rank. Therefore, the solution should be unique and the inherent balancing of the SM capacitor voltages is guaranteed. Also, with $X = 5$, under all circumstances of an arbitrary Y, the matrices on the left-hand side of the equation set have full rank. However, a full rank matrix is not always guaranteed when X varies. Therefore, the numbers X and Y should be carefully chosen. The balancing ability will be presented and verified in the next section.

C. Comparison and Analysis on Low Step Ratio Application

The proposed converter is compared to the modular multilevel dc–dc converter (MMDC) [24] without the center tap full bridges taken into consideration for cost and losses study. Only one leg (A1 and A2) is used in the MMDC. The step-up conversion is from 25 to 30 kV with 10-MW power transmitted. The proposed converter has nine cells on both left- and right-hand sides. The Infineon insulated-gate bipolar transistor (IGBT) modules FZ1200R45HL3 and diodes DD1200S45KL3_B5 are used as half bridges and rectifiers, respectively. The modulation method of $X = 9$ and $Y = 7$ is used. On the other hand, the MMDC [24] is comprised of nine cells on the top arm and nine cells on the bottom arm. The numbers of the half bridges used in the two schemes are the same. The switching frequency is 400 Hz. A list for comparison of the two converter schemes are shown in Table V.

TABLE VI
EXPERIMENTAL PARAMETERS

Symbol	Description	Value
$V_{\rm H}$	Nominal high dc voltage	350 V
P	Nominal output power	1300 W
L, L'	Large inductor	1980 μH
L_s, L'_s	Series inductor	1320 μH
C_s, C'_s	Series capacitor	5 μF
C_o	Output capacitor	100 μF

It can be seen from Table V that the MMDC scheme has high-voltage stress in half bridges. Switch devices with series connection may be required. This is because in the modulation method of MMDC, the sum of the capacitor voltages is equal to twice the dc-side voltage. However, using the proper modulation method in the proposed scheme, the voltage stress can be much lower according to (8), namely 3.1 kV in average. The MMDC may win in control flexibility, but the proposed converter has a hybrid topology of half-bridge modules and a rectifier. In the application with step-up ratio close to unit, the cost is saved by using rectifier rather than submodules. Moreover, owning to the soft switching of the resonant operation, the proposed converter also has lower switching losses. The SM capacitors are inherently balanced. Hence, although the proposed converter can achieve ranged step ratio, it has more benefits on cost and efficiency in lower step-up ratio applications. The test results will be demonstrated in the next section.

IV. EXPERIMENTAL RESULTS

A downscaled experimental prototype with ten submodules was built to demonstrate the operation of the converter in Fig 1. Each submodule is comprised of an Infineon IGBT module FF225R12ME4 and a 550-μF capacitor. A digital signal processor TMS320F28335 from Texas Instruments was deployed to control the converter. Large inductors are placed between the low dc voltage and the stacks, representing an autotransformer with the unit step ratio. Two sets of series inductors and series capacitors were placed between the large inductors and the rectifier. A fixed resistive load was connected at the high-voltage dc side. Apart from the cell capacitor rated more than 800 V, the series capacitors and the output capacitors have a voltage rating of 700 V. All the inductors have the same current rating of 14 A. The rectifier has a voltage rating of 600 V and current rating of 30 A. The test setup is presented in Fig. 4 and the detailed circuit parameters are listed in Table VI.

A. Resonant Conversion for Low Step-Up Ratio Operation

To verify the operation principle, the converter operated in the resonant conversion mode is demonstrated. Due to the page limit, the experimental results using the modulation with $X = 5$ and $Y = 1$ and the modulation with $X = 5$ and $Y = 4$ are presented.

For converter with relatively high step-up ratio, the modulation method with $X = 5$ and $Y = 1$ is used (see Table I). In this case, the input voltage is 150 V and the operating frequency is

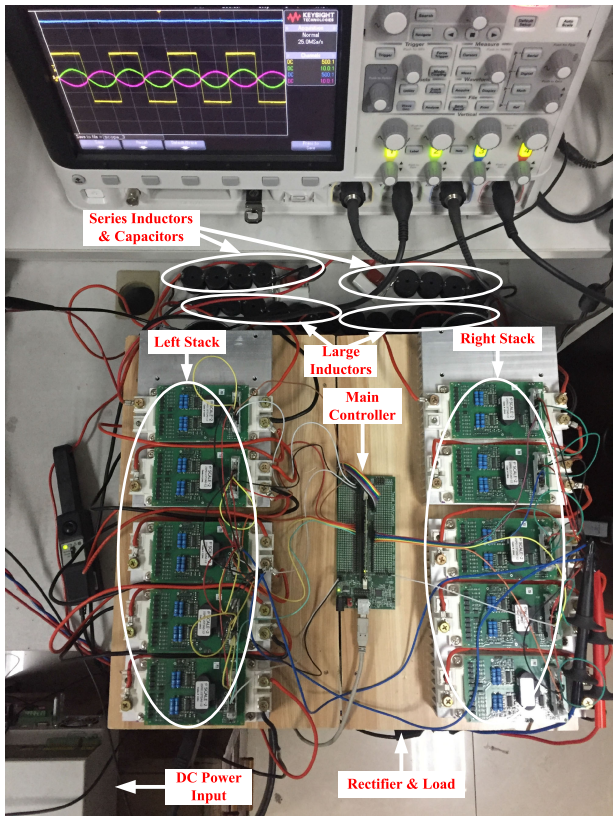

Fig. 4. Test setup of the step-up converter.

2 kHz. The converter voltage and current waveforms are shown in Fig. 5.

Fig. 5(a) shows that the converter high dc voltage is almost a constant with the average value of 350 V. The rectifier input voltage v_t is a complete square wave with the peak value of 200 V, which is also equal to the voltage on the output capacitor. The rectifier currents i_t and i'_t have same amplitude but with a phase difference of 180°. The stack voltages v_s and v'_s in Fig. 5(b) are square wave with dc offsets. They range from 50 to 250 V. As a result, the difference between v_s and v'_s is a square wave with the peak voltage of 200 V. This result is in accordance with v_t measured in Fig. 5(a). The stack currents i_s and i'_s in Fig. 5(b) consist of dc components and ac components. The dc current components with the stack dc voltages provide the dc power. This dc power is balanced with the ac power contributed by the stack ac currents and the stack ac voltages, guaranteeing a balanced power on the submodules.

The experimental waveforms of the rectifier input voltage v_t, stack current i_s, and parallel current i_p are shown in Fig. 6(a). The large inductor current i_p is a triangle wave and overlaps with i_s when v_t is reversed. The stack current i_s equals to i_t plus i_p. Moreover, the voltage of the upper switch of SM 1 $v_{\rm SW1}$ and the current of that switch $i_{\rm SW1}$ are measured and shown in Fig. 6(b). It can be seen that each upper switch achieves zero voltage switching (ZVS). The lower switch also achieves ZVS. Because the current is not approachable, the waveforms of the lower switch are not shown. The experimentally measured efficiency of the conversion is 97.7%.

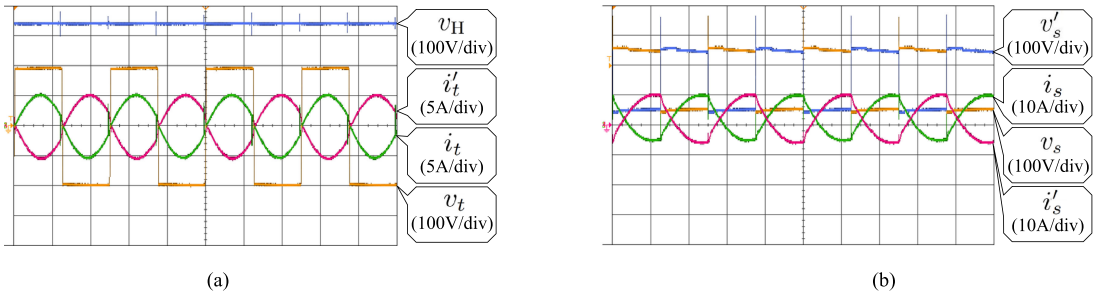

Fig. 5. Experimental voltage and current waveforms with $X = 5$ and $Y = 1$ (*X*–axis: Time, 200 μs/div). (a) High dc voltage, rectifier voltage, and currents. (b) Stack voltages and currents.

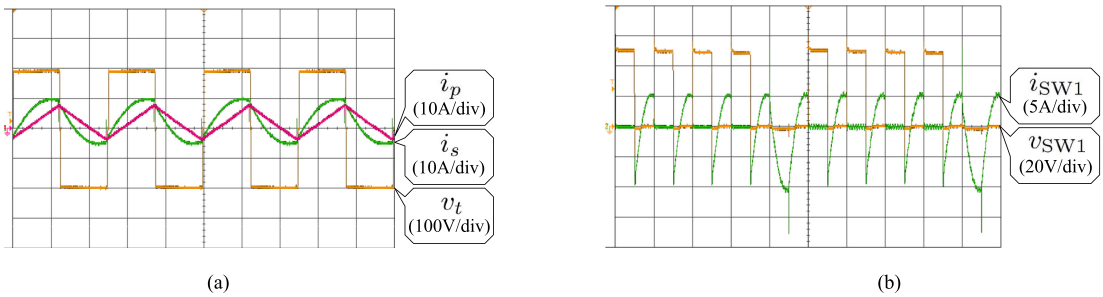

Fig. 6. Experimental voltage and current waveforms with $X = 5$ and $Y = 1$. (a) Rectifier voltage, stack current, and large inductor current (X–axis: Time, 200 μs/div). (b) Upper switch voltage and current of SM 1 (X–axis: Time, 500 μs/div).

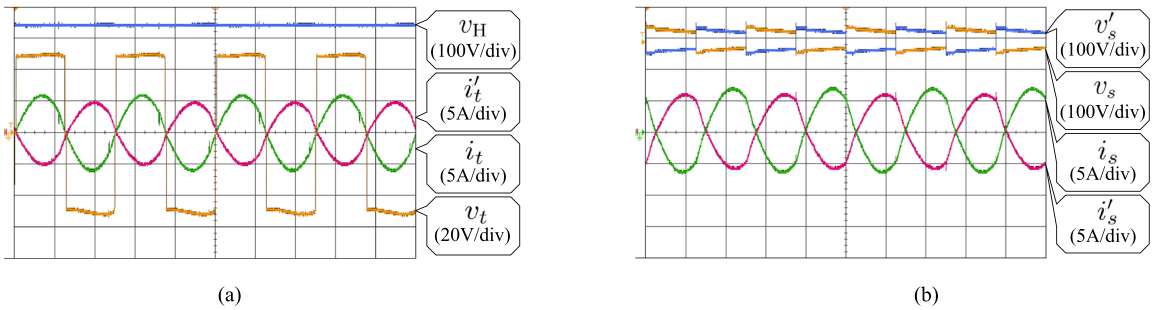

Fig. 7. Experimental voltage and current waveforms with $X = 5$ and $Y = 4$ (X–axis: Time, 200 μs/div). (a) High-dc voltage, rectifier voltage, and currents. (b) Stack voltages and currents.

With the modulation of $X = 5$ and $Y = 4$ (see Table II), the converter achieves a very low step ratio. In the test, the input low dc voltage is 300 V, and the equivalent operating frequency is 2 kHz. The key waveforms are shown in Fig. 7.

Fig. 7(a) shows that the converter high dc voltage is 350 V. The rectifier input voltage v_t is a complete square wave with the peak value of 50 V. The voltage on the output capacitor is also 50 V. The rectifier currents i_t and i'_t have a phase difference of 180°. The stack voltages v_s and v'_s in Fig. 7(b) are square wave with small ac amplitude but high dc offsets. On the other hand, the stack currents i_s and i'_s in Fig. 7(b) consist of small dc components and high ac components. This is because that the power transmitted to the rectifier is small with this modulation method. Most of the power is transmitted by the dc current via the rectifier from the input. As a result, the dc power and ac power on the stacks are relatively low.

The experimental waveforms of the rectifier input voltage v_t, stack current i_s, and parallel current i_p are shown in Fig. 8(a). The large inductor current i_p is a triangle wave. The stack current i_s equals to i_t plus i_p. Moreover, the voltage of upper switch of SM 1 v_{SW1} and the current of that switch i_{SW1} are measured and shown in Fig. 8(b). Although the equivalent operating frequency is 2 kHz, the switching frequency is only 400 Hz. All switches achieve ZVS in this operation mode. The conversion achieves a measured efficiency of 99.3% in the test.

In the experimental result of the lowest step-up ratio, the converter has the equivalent operating frequency, which is exactly five times of the switching frequency in each cell. This gives the advantage on the size reduction of passive components. If the switching frequency increases, further reduction on passive components can apply. Moreover, the converter operating in a low step-up ratio resonant mode with soft switching achieves high conversion efficiency. The modular structure also achieves the scalability of a converter with the increased voltage level. This gives feasibility of the converter in even high-voltage applications. In the application of dc grid, this converter can be used

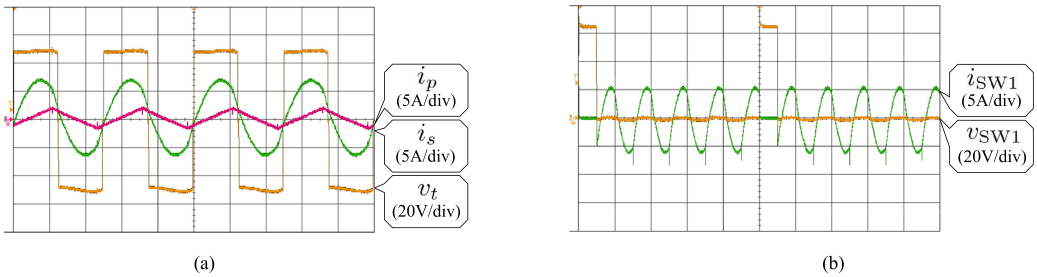

Fig. 8. Experimental voltage and current waveforms with $X = 5$ and $Y = 4$. (a) Rectifier voltage, stack current, and large inductor current (X–axis: Time, 200 μs/div). (b) Upper switch voltage and current of SM 1 (X–axis: Time, 500 μs/div).

TABLE VII
MEASURED SM CAPACITOR VOLTAGES

	$X = 5, Y = 1$		$X = 5, Y = 2$		$X = 5, Y = 3$		$X = 5, Y = 4$	
	Left	Right	Left	Right	Left	Right	Left	Right
SM 1	50.8 V	50.9 V	55.8 V	55.7 V	60.7 V	60.7 V	66.7 V	66.6 V
SM 2	50.9 V	50.8 V	55.6 V	55.8 V	60.7 V	60.8 V	66.6 V	66.7 V
SM 3	50.8 V	50.9 V	55.9 V	55.7 V	60.9 V	60.7 V	66.7 V	66.6 V
SM 4	50.9 V	50.8 V	55.5 V	55.8 V	60.6 V	60.7 V	66.7 V	66.7 V
SM 5	50.9 V	50.9 V	55.9 V	55.8 V	60.8 V	60.8 V	66.6 V	66.6 V

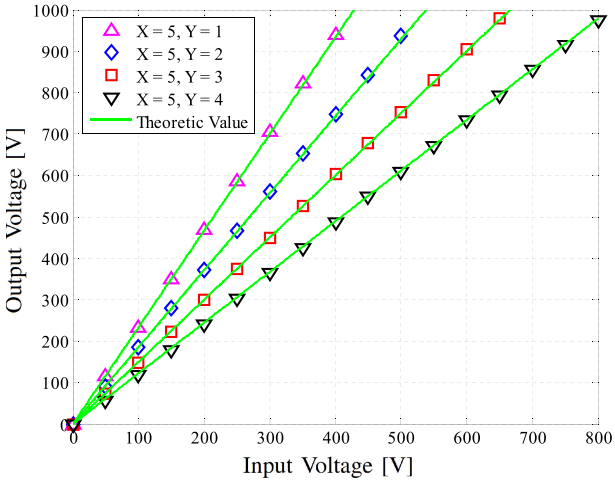

Fig. 9. Measured output voltage versus input voltage under different modulation schemes with $f_{eq} = 2$ kHz.

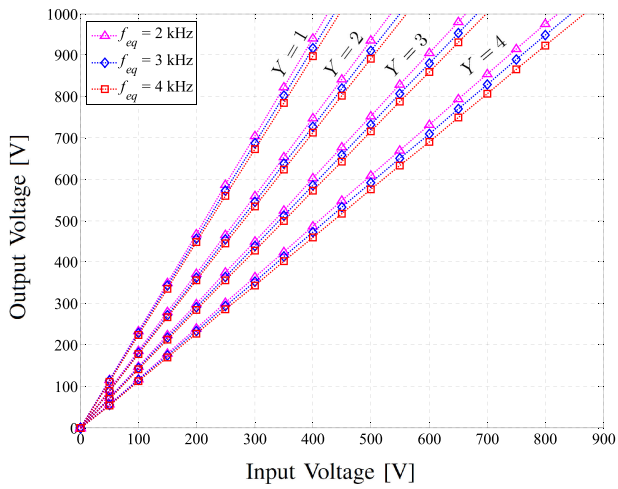

Fig. 10. Performance of dc transformation with $X = 5$.

as a dc transformer for interconnection with different voltage levels.

The SM capacitor voltages in the left stack and right stack are measured and listed in Table VII. It can be seen that under all operation modes with $X = 5$, the SM capacitor voltages are balanced completely. This result validates the conclusion in the previous analysis.

B. Step-Up DC Transformer

The step-up conversion were experimentally verified by measuring the converter output voltage versus the input voltage. The results are shown in Fig. 9, which demonstrate a good linearity under different modulation schemes. The measured results are in good accordance with the theoretic values.

The step-up ratio is also measured with different operating frequencies. If the frequency of the square wave voltage in (3) varies, the step-up ratio is slightly changed. The results are presented in Fig. 10. It can be observed that regardless of the equivalent operating frequency, the step-up conversion guarantees a good linearity. Moreover, from the resonant frequency of 2 kHz, when the operating frequency increases, the step-up ratio decreases. The deviation of the operating frequency from the resonant frequency leads to a reduced voltage gain. This feature can be used to regulate the step-up ratio, yielding an adjustable conversion range.

V. CONCLUSION

This paper presented a chain-link converter for low step-up ratio dc–dc conversion. The converter was transformerless and modular. The dc components of the stack voltages were

withstanding the low dc voltage. The ac components of the stack voltages were rectified to generate a dc voltage surplus. The converter had only one pair of push–pull chain link submodules to achieve flexible step ratio. The converter can be operated in a resonant mode, featured with the zero voltage soft switching. The converter performs efficient low step-up ratio dc–dc conversion. The step-up ratio depends on the modulation and operating frequency. Moreover, under different modulation methods, the converter behaves as a dc transformer with a good linearity and guarantees the inherent balancing ability. The analysis was finally validated by the measured results retrieved from a downscaled experimental prototype.

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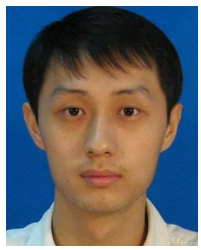

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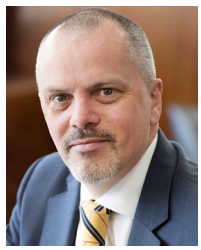

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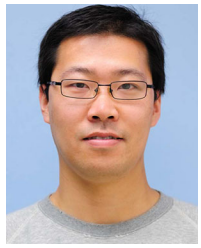

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