Submodule Temperature Regulation and Balancing in Modular Multilevel Converters

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***Abstract*—In modular multilevel converters (MMCs), temperature control of semiconductor devices in the submodules (SMs) is a key factor for the safe and reliable operation. Under normal operation, significant temperature differences can exist between SMs due to, for example, aging of semiconductor modules and module parameter mismatch. This paper presents a method for achieving SM thermal balancing by controlling the capacitor voltage of each SM in an arm, while maintaining the sum of the SM capacitor voltages at a constant value in order to regulate the dc-link voltage. The proposed temperature balancing strategy is validated using an experimental MMC setup with three SMs, where an increase in the thermal resistance to ambient of one or more SM semiconductors is created by restricting coolant flow to simulate a partial failure in the cooling system. Increases in the thermal resistance by 21% and 42%, corresponding to temperature increases of 5 and 10 °C, respectively, are managed by three SMs, using a capacitor voltage margin of 60%.**

***Index Terms*—Capacitor voltage balancing, electronics cooling, modular multilevel converter (MMC), power semiconductor devices, temperature control, thermal management of electronics.**

I. Introduction

MODULAR multilevel converters (MMCs) are a widely used voltage source converter (VSC) topology for medium voltage drives [1] and high-voltage direct current (HVdc) transmission systems [2]. For industrial applications [3], dozens or even hundreds of submodules (SMs), each supporting a few kilovolts, are employed to produce a quasi-sinusoidal voltage waveform from a dc-link. This SM-based structure distributes the stored energy across the SM capacitors instead of using a single high-voltage dc-link capacitor as in conventional two- and three-level converters.

MMCs present additional control and operational challenges when compared with two- and three-level topologies, as well as diode-clamped and multilevel flying capacitor topologies [4]. The control system of an MMC includes additional layers, e.g., to eliminate circulating currents within the converter arms [5] and a dedicated capacitor voltage balancing algorithm [6], responsible for sharing voltage equally across all operating SMs, which are inserted and bypassed in order to generate a multilevel ac voltage waveform.

For the reliable operation of any power converter, including MMCs, the temperature of the semiconductor switches in the SMs should be limited in order to avoid damage resulting from overtemperature and thermal cycling [7]. Under abnormal conditions such as overload or system cooling malfunction, one or more SMs may suffer a large temperature increase. Previous works [8], [9] have addressed system-level thermal control strategies for two- and three-level converters. Although some of these works have been extended for MMCs [10], thermal management strategies operating at the SM-level have not yet been proposed. It has also been shown that it is possible to achieve significantly different temperatures between the SMs of an arm during normal operation due to the load conditions [11], resulting in unequal current and loss distribution between the dies in the semiconductor modules.

Long-term operation of an MMC can be affected by capacitance ageing [12], parameter mismatch between SMs or partial cooling failures [13] that can lead to significant temperature differences among SMs. This poses a significant threat to the normal operation of the MMC as the power semiconductor devices have been identified as the components that fail most often in power electronic converters [14]. Their lifetime is mainly defined by the amplitude of thermal cycles and the peak junction temperature value [7]. Excessive values of either may lead to premature ageing and failure, which in turn affect maintenance strategies and the overall reliability of the converter station [15].

Temperature control in power converters may be achieved by controlling semiconductor losses, with the majority of losses in the SMs' semiconductors being conduction losses. Switching losses in MMCs are usually a small proportion of total losses as a result of a low switching frequency, which is typically a few hundred hertz [16]. Conduction losses are dependent only on the magnitude of the arm current [11] and are equal in all SMs (each SM has one power device conducting at all times).

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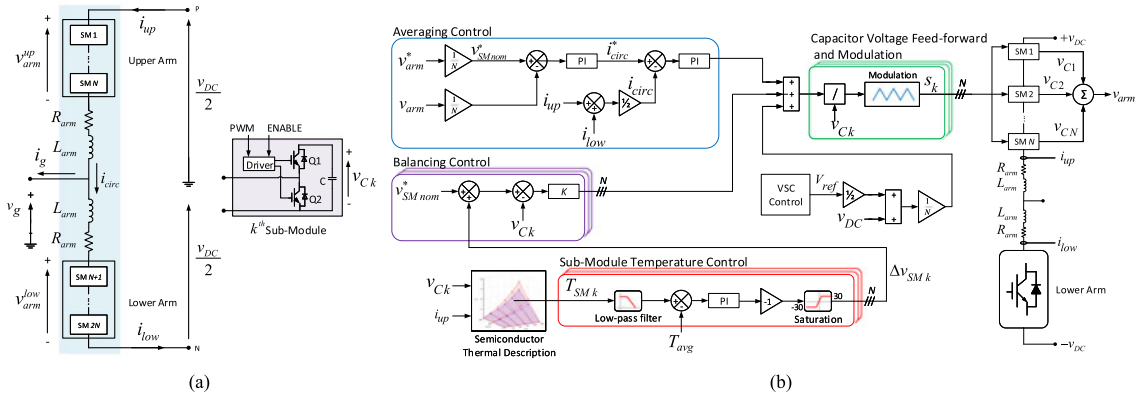

Fig. 1. MMC: (a) single-phase configuration with HB SMs and (b) proposed per-arm individual SM voltage control strategy.

SM temperature therefore can only be controlled independently by modifying switching losses through the modulation of its capacitor voltage. This poses a challenge as typical capacitor voltage algorithms are implemented per phase arm [16] in order to regulate all capacitor voltages to a shared nominal value, independent of the load conditions, i.e., they do not allow independently controlling SM capacitor voltages.

This work implements a modification of the classic MMC capacitor voltage balancing scheme [17] to allow independent regulation of $N-1$ SM voltages within an arm while maintaining the total arm voltage regulated at a reference value. An SM temperature equalization method is proposed that compensates for cooling imbalances across the SMs by modulation of the capacitor voltages (and thereby modulation of switching losses). When an SM possesses a higher temperature than the others, its voltage is decreased and the available operating voltage margin in the remaining SMs is exploited in order to compensate for this decrease, ensuring the total arm voltage, hence the dc-link voltage, remains constant. As the control algorithm relies on the individual SMs' junction temperature feedback, which is not normally accessible, the individual die temperature of the semiconductors in each SM is calculated using voltage and current measurements and semiconductor module case temperature, which are readily available. The effectiveness of the proposed individual SM temperature regulation and capacitor voltage balancing method is validated in simulation using MATLAB/Simulink and the piece-wise linear electric circuit simulation (PLECS) Toolbox [18] and experimentally verified in a scaled-down laboratory setup.

This paper is organized as follows: the control and operation of an MMC and the electrothermal dynamics of semiconductors are presented in Section II. The concept of including an estimation of junction temperature in the voltage balancing control and the proposed thermal regulation and balancing method is described in Section III. Simulation results for the voltage–temperature balancing algorithm are presented in Section IV and the results of experimental thermal regulation of an MMC arm with three SMs are discussed in Section V. Section VI discusses the limitation of the temperature calculation method used in this work and the stability of SMs' temperature regulation, and analyzes the scalability of the proposed method when applied to MMCs with a large number of SMs.

II. Control and Operation of MMCs

A. Capacitor Voltage Control

The structure of one phase of an MMC is represented in Fig. 1(a). Each phase is composed of two arms, each arm consisting of an inductor L_{arm} to limit the amplitude of the arm circulating current and fault currents [6], and a series of SMs. Frequently, an arm resistance R_{arm} is included to model inter-SM bus connection losses. Each SM can have different configurations [2]; a half-bridge (HB) configuration is considered in this paper, consisting of two insulated-gate bipolar transistors (IGBTs) with antiparallel-connected diodes and a capacitor C. i_{up}, i_{low}, i_g, and i_{circ} are the upper arm, lower arm, ac-side, and circulating currents, respectively.

A key challenge in MMCs is the balancing of SM capacitor voltages and extensive work has been done in this area [16], [19]–[22]. These methods typically compare each SM capacitor voltage to an implicit reference of $\frac{v_{\text{dc}}}{N}$, i.e., the dc-link voltage is shared equally by the operating SMs. Instead of this approach, in this work, a modified SM capacitor voltage balancing strategy, based on the one proposed in [23], is utilized. The proposed strategy enables direct SM capacitor voltage control while keeping the total arm voltage regulated to its reference value and is shown in Fig. 1(b) for the upper arm of an MMC with N SMs. The strategy is implemented in each arm and comprises two cascaded control levels:

1) Averaging control, implemented per arm and used to enforce an average capacitor voltage of $v^*_{\text{SM nom}} = \frac{v^*_{\text{arm}}}{N}$ across all SMs in an arm, thus regulating the arm voltage to its reference v^*_{arm};
2) Balancing control, implemented for each SM k and responsible for forcing each capacitor voltage $v_{C\,k}$ to follow an individual reference $v^*_{\text{SM nom}} + \Delta v_{\text{SM}\,k}$.

The ac voltage command V_{ref} is provided by the high-level VSC control of the converter and the dc voltage v_{dc} is included as a feed-forward term. The carrier waveforms of the pulse-width modulation (PWM) scheme are phase-shifted by $(360/N)^\circ$ for each SM to improve the current control and reduce harmonic content. Consequently, the arm will produce a multilevel voltage waveform with $N + 1$ levels.

TABLE I
SEMICONDUCTOR SPECIFICATIONS FOR THE IGBT MODULE FF75R12YT3

IGBT			Diode		
Parameter	Value	Unit	Parameter	Value	Unit
$V_{0\,Q}$	0.6563	V	$V_{0\,D}$	0.6263	V
$V_{1\,Q}$	0.0018	V/°C	$V_{1\,D}$	0.0030	V/°C
$R_{0\,Q}$	0.0142	Ω	$R_{0\,D}$	0.0042	Ω
$R_{1\,Q}$	0.0001	Ω/°C	$R_{1\,D}$	0.0002	Ω/°C
$E_{0\,Q}$	0.2233	J/A	$E_{0\,D}$	0.1135	J/A
$E_{1\,Q}$	0.0002	J/A^2	$E_{1\,D}$	0.0004	J/A^2

B. Semiconductor Losses and Temperature Calculation

The specifications of the semiconductor module provided by the manufacturer can be used to approximate semiconductor losses. The characteristic curves for conduction and switching loss calculations can typically be accurately approximated with a second-order polynomial curve [24] using a least-squares curve fitting method applied to the semiconductor module datasheet information. Parameters for the device modeled here are shown in Table I.

1) Conduction Losses: IGBTs and diodes are modeled as a constant voltage drop V_0 and a series resistance R_0 and losses calculated considering the average (I_{avg}) and rms (I_{rms}) values of the arm current. Including a first-order approximation for temperature (T) dependency on the curve-fitting coefficients V_Q, R_Q, V_D, and R_D, conduction losses for the IGBT (Q) and diode (D) dies are calculated as follows:

$$P_C\left(I_{\text{avg}}, I_{\text{rms}}, T\right) = \left(V_0 + V_1 T\right) I_{\text{avg}} + \left(R_0 + R_1 T\right) I_{\text{rms}}^2. \tag{1}$$

2) Switching Losses: At every switching instant, the total switching-loss energies E_{total} (turn-ON and turn-OFF losses for IGBTs and turn-off losses for diodes) are determined using the rms value of the arm current and scaled by the ratio of the SM capacitor voltage to the reference voltage $V_{\text{CE}}^{\text{ref}} = 600$ V. Switching losses for the IGBT and diode are determined by:

$$P_{sw}\left(I_{\text{rms}}, v_{\text{SM}}, f_{sw}\right) = E_{\text{Total}}\left(I_{\text{rms}}\right) \frac{v_{\text{SM}}}{v_{\text{CE}}^{\text{ref}}} f_{sw}. \tag{2}$$

The total losses P_L in the IGBT and diode dies are calculated as the sum of conduction and switching losses.

3) Temperature Calculation: The equivalent thermal network diagram shown in Fig. 2(a) is used to calculate the temperature of the dies, and the thermal resistances are given in Table II. The semiconductor modules are liquid cooled and it is assumed that the coolant temperature is known. An embedded thermistor in the semiconductor module provides a measurement T_m of the case temperature (T_{Case}) in each module and is used for the calculation of the junction temperature in the silicon dies.

The junction temperatures of the IGBT and diode parts for each SM k are calculated by:

$$\begin{aligned} T_{Q\,k} &= P_{L\,Q} R_{\text{th\,JC}\,Q} + T_{m\,k} \\ T_{D\,k} &= P_{L\,D} R_{\text{th\,JC}\,D} + T_{m\,k}. \end{aligned} \tag{3}$$

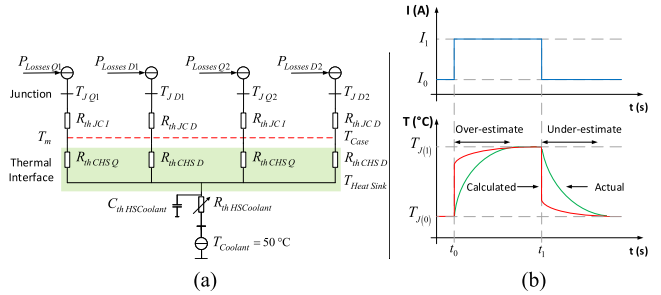

Fig. 2. Semiconductor module FF75R12YT3: (a) equivalent thermal network diagram (adapted from [25]) and (b) comparison between the dynamic behavior of junction and calculated temperatures. T_{Case} is measured by a thermistor.

TABLE II
THERMAL NETWORK PARAMETERS

Parameter	Value	Unit
Thermal Resistance Junction to Case per IGBT $R_{\text{th\,JC}\,Q}$	0.36	°C/W
Thermal Resistance Case to Heat Sink per IGBT $R_{\text{th\,CHS}\,Q}$	0.20	°C/W
Thermal Resistance Junction to Case per Diode $R_{\text{th\,JC}\,D}$	0.60	°C/W
Thermal Resistance Case to Heat Sink per Diode $R_{\text{th\,CHS}\,D}$	0.25	°C/W
Thermal Resistance Heat Sink to Coolant $R_{\text{th\,HSCoolant}}$	0.45	°C/W
Thermal Capacitance of Heat Sink ($C_{\text{th\,HSCoolant}}$)	167	J/°C

The thermal resistances allow the direct calculation of junction temperature under static conditions. The case temperature measurement captures the thermal time constant $\tau = R_{\text{th\,HSCoolant}} C_{\text{th\,HSCoolant}}$. The much smaller thermal time constant associated with the die is neglected and as a result the calculation tends to produce transient under and overtemperature values, as illustrated in Fig. 2(b).

III. PROPOSED CONTROL STRATEGY FOR SUBMODULES TEMPERATURE REGULATION

A. Description of the Temperature Control Strategy

Temperature control is exerted using the voltage difference input Δv_{SM} (Δv_{SM} is responsible for modifying each SM voltage from a starting assumption of equal voltages). The voltage differentials $\Delta v_{\text{SM}\,k}$ are set as a function of the temperature of SM k, as represented in the submodule temperature control loop in Fig. 1(b). The SM temperature is set to the maximum value of the individual die temperatures in each SM k as follows:

$$T_{\text{SM}\,k} = \max\{T_{Q1\,k}, T_{D1\,k}, T_{Q2\,k}, T_{D2\,k}\}. \tag{4}$$

The calculated SM temperature is compared with the average temperature T_{avg} of all SMs in the arm and the difference fed to a PI controller which will determine the voltage differential Δv_{SM} to be added to each individual SM voltage reference. A first-order low-pass filter is included to reduce noise in the temperature measurement. This scheme ensures that a single SM is not responsible for voltage balancing alone, i.e., there is no "master" SM used to achieve thermal regulation: all available SMs participate in the voltage–temperature balancing process equally.

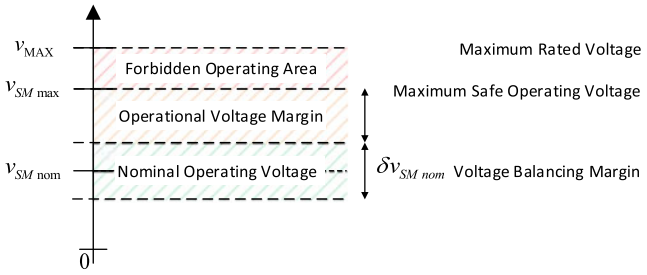

Fig. 3. Operational voltage limits in a submodule.

Considering a semiconductor module with a maximum rated voltage v_{MAX} and a nominal SM operating voltage $v_{\mathrm{SM\,nom}}$, its voltage limits and different operating areas are represented in Fig. 3. The voltage balancing margin is here defined as the span of a capacitor voltage balancing margin, where a value $\delta v_{\mathrm{SM\,nom}} \pm 10\%$ is typically considered [26] around the average capacitor voltage $v_{\mathrm{SM\,nom}}$. The operational voltage margin is effectively the exploitable voltage slack between the maximum nominal operating voltage plus half the voltage balancing margin $\delta v_{\mathrm{SM\,nom}}$, and the voltage limit $v_{\mathrm{SM\,max}}$ for the safe operation of the semiconductors. This ensures the necessary voltage margin to survive transients such as those resulting from SM bypass and fault ride-through. The forbidden operating area corresponds to the remaining possible voltage value up to the upper limit v_{MAX}, which is the maximum value between the rated capacitor voltage and the semiconductor safe operating area (SOA) maximum voltage given the nominal current.

To ensure that the capacitor voltage of each SM is properly regulated up to a maximum value of $v_{\mathrm{SM\,max}}$, saturation blocks are included in the control system of Fig. 1(b) and the PI controllers include a back-calculation antiwindup mechanism [27].

B. Analysis and Limitations of the Thermal Regulation

Considering an SM operating with a capacitor voltage $v_{\mathrm{SM}(0)}$, its initial (maximum SM) temperature is $T_{(0)}$. When an external thermal disturbance ΔT is applied to the SM and temperature regulation does not occur, the temperature will rise to $T_{(1)}$:

$$T_{(1)} = P_{L(1)} R_{\mathrm{th}} + T_{m\,0} + \Delta T. \tag{5}$$

The thermal disturbance can, for instance, be caused by an increase in the thermal resistance of the module due to ageing [28] or result from a partial cooling failure of the system [13], leading to an increase in the measured temperature value T_m.

If the proposed thermal regulation process is implemented, and assuming $v_{\mathrm{SM\,max}}$ has not been reached, i.e., there is an operational voltage margin in the SMs, each of the N available SMs will share an equal part $\frac{\Delta T}{N}$ of the total disturbance and the new SM voltage will be regulated to:

$$v_{\mathrm{SM\,1}} = v_{\mathrm{SM\,0}} + \Delta v_{\mathrm{SM}}. \tag{6}$$

And the new $T_{(2)}$ temperature will be lower:

$$T_{(2)} = T_{(0)} + \frac{\Delta T}{N} = P_{L(2)} R_{\mathrm{th}} + T_{m\,0} + \Delta T. \tag{7}$$

Substituting (1) and (2) into (7) and rearranging as a function of the voltage difference Δv_{SM} yields:

$$\Delta v_{\mathrm{SM}} = \frac{\Delta T \left(\frac{1}{N}\left(1 - R_{\mathrm{th}}\left(V_1 I_{\mathrm{avg}} + R_1 I_{\mathrm{rms}}^2\right)\right) - 1\right)}{R_{\mathrm{th}}\left(E_0 I_{\mathrm{rms}} + E_1 I_{\mathrm{rms}}^2\right) \frac{f_{sw}}{V_{\mathrm{CE}}^{\mathrm{ref}}}}. \tag{8}$$

It can be observed from (8) that the magnitude of the voltage difference Δv_{SM} is inversely proportional to the number of SMs N and directly proportional to the magnitude of the thermal disturbance ΔT. Accordingly, for a given thermal disturbance, the larger the number of SMs, the smaller the capacitor voltage variations become. However, an increase in the number of SMs to dozens or hundreds is typically accompanied by a reduction in the individual SM switching frequency f_{sw} in (8), which will lead to larger capacitor voltage variations.

The remaining SMs aiding in the thermal regulation, with an initial voltage $v_{\mathrm{SM\,0}} = v^*_{\mathrm{SM\,nom}}$, will suffer a voltage regulation to a new value $v_{\mathrm{SM}\,\chi}$ given by:

$$v_{\mathrm{SM}\,\chi} = \frac{v^*_{\mathrm{arm}} - v_{\mathrm{SM\,0}} + \Delta v_{\mathrm{SM}}}{N - 1} \tag{9}$$

which shows a reduction in the capacitor voltage variation as the number of SMs increases. It should be noted that the capacitor voltages are subjected to the limit imposed by the saturation block in the submodule temperature control loop in Fig. 1(b), and therefore will be kept below the maximum value $v_{\mathrm{SM\,max}}$ at all times. Although the amplitude of these variations is limited due to the rating of the system and SOA, it effectively develops a need for an increased rating (and therefore cost) of each SM. An economic comparison could be performed to quantify the additional cost, as well as the resulting expected increase in converter lifetime and reliability.

The proposed strategy leads to an even distribution of the thermal stress across the operating SMs at all times, without using redundant SMs typically included in MMCs [6]. The redundant SMs are therefore still available to be used for failsafe functionality, e.g., if excessive temperatures destroy a semiconductor module or if further problems such as internal SM faults occur, ensuring the MMC can operate with a high reliability [15].

The method proposed in this work relies on a phase-shifted PWM scheme to enable individual and independent SM capacitor voltage control. As the number of SMs increases to transmission voltage levels, e.g., hundreds of SMs per arm, more efficient modulation strategies such as staircase methods [6] are typically employed, which are not compatible with the capacitor voltage control strategy proposed in this work and that underpins the control strategy for SMs temperature regulation. This strategy is therefore aimed at MMCs with a low or medium number of SMs, such as medium voltage drives and the MMC CTL implementation [26], and employing PWM-based techniques.

IV. Simulation Results

A. Description of the Test System

The proposed method is validated in MATLAB/Simulink using the PLECS Toolbox [18], with the parameters of the MMC represented in Table III. The thermal network of Fig. 2 is implemented for HB semiconductor modules FF75R12YT3 from Infineon [25] using the datasheet parameters in Table II.

TABLE III
SYSTEM PARAMETERS

Parameter	Value	Unit
Number of Submodules per arm (N)	3	–
Submodule Capacitance (C_{SM})	4.7	mF
Arm Inductance (L_{arm})	3.3	mH
Nominal Submodule Voltage ($v^*_{\mathrm{SM\,nom}}$)	50	V
Submodule Operating Voltage Limit ($v_{\mathrm{SM\ \ max}}$)	80	V
Nominal (Reference) Arm Voltage (v^*_{arm})	150	V
Carrier Frequency (f_{sw})	2.5	kHz
Fundamental Frequency (f_0)	50	Hz
Nominal Coolant Temperature (T_{coolant})	50	°C

As shown in Table III, the nominal operating voltage of the SMs is $V_{\mathrm{SM\,nom}} = 50$ V, which is much smaller than the maximum rated collector–emitter voltage of the semiconductor module, $v_{\mathrm{CE\,max}} = 1200$ V, and the collector–emitter voltage to which the datasheet loss values are referenced ($v_{\mathrm{CE}} = 600$ V). This reduced ratio is due to the rating of the experimental setup and diminishes the effect of switching losses on the overall semiconductor losses. In order to compensate for this limitation, the frequency f_{sw} of the triangular carriers is set to 2.5 kHz. Although this value is significantly higher than the typical values used (hundreds of hertz), it allows the $\frac{v_{\mathrm{SM}}}{v^{\mathrm{max}}_{\mathrm{CE}}} f_{sw}$ ratio in (2) to approximate the operating electrical conditions of a commercial SM. A maximum operating voltage of $v_{\mathrm{SM\,max}} = 80$ V (60% voltage increase) is considered.

The operation of the converter without the proposed individual SM voltage control method is presented initially, followed by a case study where the SM voltages are regulated to equalize the calculated die temperatures due to thermal disturbances. These disturbances are assumed to result from partial cooling system failures, resulting in temperature increases of 5 and 10 °C, corresponding to an increase of 21% and 42%, respectively, in the thermal resistance to ambient of the semiconductor module. The setup is composed of three SMs (SM 1–3) and the disturbances are applied to SM 1 and SM 2, at 150 and 450 s, respectively.

B. Dynamic Performance

The response of the SM voltages, maximum calculated die temperatures, and measured case temperatures are shown in Fig. 4(a), when the thermal balancing algorithm is not active, i.e., individual SM voltage control does not occur.

The SMs' voltages are balanced around their nominal value $v^*_{\mathrm{SM\,nom}} = 50$ V and it can be observed that due to a large SM capacitance value (4.7 mF), the low frequency ripple in this system has a very small amplitude. For a peak arm current of 23 A, the maximum calculated die temperatures are the same in all SMs, with the lower IGBT Q2 in each module having the highest temperature (≈ 77 °C) and so determining the T_{SM} temperature to be used for the voltage regulation process.

When the increase in the thermal resistance is applied to SM 1 and SM 2 at $t = 150$ s and $t = 450$ s, respectively, their measured and calculated junction temperatures start to increase with a time constant $\tau = RC = 0.45 \times 167 \approx 75$ s, imposed by the thermal resistance and the thermal capacitance of the heat

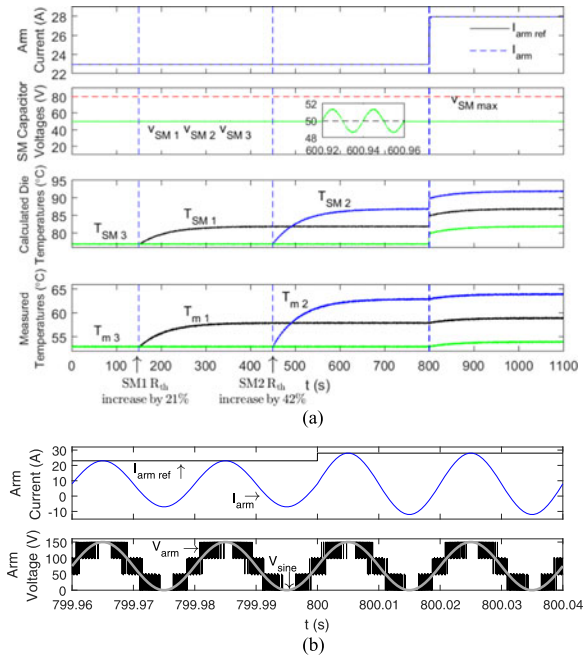

Fig. 4. Simulation of response of submodules, voltages and temperatures without thermal regulation: (a) submodules' voltages and temperatures and arm current and (b) multilevel arm voltage waveform and arm current.

sink and the coolant. When the temperatures reach a steady state, 5 and 10 °C temperature imbalances exist between SM 1 (82 °C) and SM 2 (87 °C), and SM 3 (77 °C), respectively, for both measured case temperatures and calculated die temperatures. Since the thermal balancing algorithm is not enabled, the SM capacitor voltages remain unchanged and generate a standard four-level arm voltage waveform, regulated to its nominal peak value of 150 V as represented in Fig. 4(b). The waveform has a total harmonic distortion (THD) value of 35.47%.

The response of the SM (maximum die) temperatures to the peak arm current reference step from 23 to 28 A at $t = 800$ s is also shown in Fig. 4(a). The junction temperature has an instantaneous variation due to the purely resistive thermal network model of the semiconductor module, as shown in Fig. 2(a), which does not affect the performance of the submodule temperature control loop because its bandwidth ($\tau \approx 75$ s) is much lower than the time constant of the capacitor voltage regulation. The arm voltage remains unchanged during the current reference step, as represented in Fig. 4(b).

C. Voltage Regulation With Thermal Disturbance

The results with the proposed balancing control are shown in Fig. 5(a). When the thermal resistance of SM 1 increases at $t = 150$ s and its temperature starts to increase, its capacitor voltage is decreased to 28 V ($\Delta v_{\mathrm{SM}} = 22$ V), while the difference to the nominal value is equally compensated by an increase in capacitor voltages of both SMs 2 and 3 to 61 V. This results in all the SMs calculated die temperatures being equalized at approximately 78.5 °C. These results are in agreement with the expected capacitor variation of $\Delta v_{\mathrm{SM}} = 22.07$ V obtained using (8) and $v_{\mathrm{SM}\,\chi} = 61.04$ V using (9).

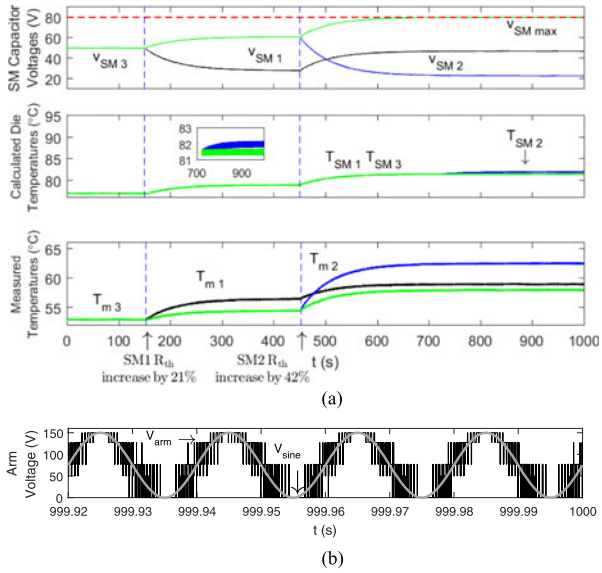

Fig. 5. Simulation of submodules' thermal regulation as a response to a thermal disturbance: (a) submodules' voltages and temperatures and (b) multilevel arm voltage waveform as a result of unbalanced SM voltages.

When the thermal resistance of SM 2 increases at $t = 450$ s, its temperature will initially increase faster as the result of a larger disturbance. Similarly to the initial disturbance applied to SM 1, SM 2 capacitor voltage is diminished as a means to regulate the maximum die temperature, while the voltage difference to the nominal value of 50 V is compensated by an increase in the voltage of SM 3 and SM 1, whose voltage was decreased previously as a result of the first disturbance. At approximately $t = 720$ s, SM 3 voltage reaches the maximum operating limit $v_{\mathrm{SM\,max}} = 80$ V and since SM 1 voltage was regulated to ensure a thermal equilibrium is reached, SM 2 voltage is further decreased in order to ensure that the arm voltage is set at 150 V. Although SM 1 and SM 3 reach a thermal equilibrium temperature of 81.5 °C, SM 2 temperature continues to increase, reaching a steady-state value of approximately 82 °C.

While the total arm voltage v_{arm} remains regulated to 150 V, as shown in Fig. 5(b), the multilevel waveform appears distorted when compared to Fig. 4(b) as a result of unbalanced SM voltages, with its THD increasing to 47.75%. Nonetheless, the use of SM capacitor voltage feed-forward, shown in Fig. 1(b), enables the fundamental component of the arm voltage (v_{sine}) to remain unchanged. The voltage waveform distortion caused by the thermal regulation process may be partially compensated by employing alternative modulation schemes such as the ones proposed in [29] and [30].

V. Experimental Results

A. Description of the Test System

The performance of the proposed method is validated using an experimental MMC arm, with parameters as in Table III. The complete laboratory setup is represented in Fig. 6(a) and is controlled by an ARM real-time processor and a Xilinx FPGA

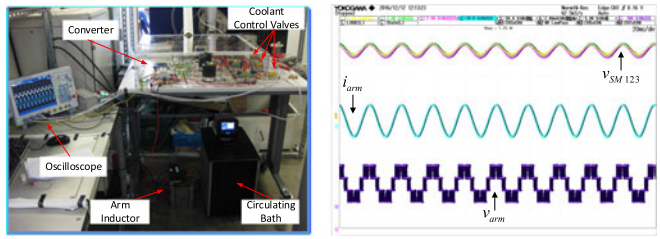

Fig. 6. Experimental MMC setup: (a) physical assembly and (b) submodule voltages (top, 2 V/div), arm current (middle, 20 V/div), and multilevel arm voltage (bottom, 100 V/div). Horizontal scale: 20 ms/div.

in a National Instruments myRIO board using LabVIEW [31]. Three HB semiconductor modules (FF75R12YT3 from Infineon [25]) are mounted on separate liquid cooled heat sinks including a thermal grease layer, where each heat sink has an individual control valve, used to regulate the coolant (water) flow from a temperature-controlled circulating bath. The coolant temperature is kept at 50 °C throughout the experiments using the temperature regulation feature of the circulating bath.

An embedded thermistor inside the semiconductor modules provides a measurement of the case temperature, used as an input for the temperature calculation expressions in (3). A first-order low-pass filter with a cutoff frequency of 5 Hz was used in order to remove some of the noise from the case temperature measurements.

The thermal imbalances are caused by controlled partial cooling failures, applied to two SMs in a two-step procedure. Characterization tests concluded that for specific valve positions, approximately one-third and two-third of the fully open position, the desired temperature increases of 5 and 10 °C, respectively, are achieved.

B. Dynamic Performance

The steady-state SM voltages (top), arm current (middle), and arm voltage (bottom) are shown in Fig. 6(b). The SM voltages are balanced around their nominal value and the multilevel arm voltage waveform exhibits four distinct and well-defined levels.

The effect of partial cooling failures of the individual temperatures of the SMs without regulation is shown in Fig. 7(a). It can be observed that without any SM capacitor voltage control action, individual SM temperatures differ significantly and the arm voltage is regulated to 150 V, as demonstrated in Fig. 7(b), even during the current reference step at $t = 800$ s. The response of the maximum die temperature in the SMs to an arm current step from 23 to 28 A is also in good agreement with simulation results of Fig. 4(b).

C. Voltage Regulation With Thermal Disturbance

When the proposed balancing control is implemented, as represented in Fig. 8(a), the cascaded 63% increase in the thermal resistance of the semiconductor modules leads to the regulation of capacitor voltages for SMs 1–3 to 47, 23, and 80 V, respectively, which are in good agreement with simulation results. Despite the distortion caused by the uneven voltage

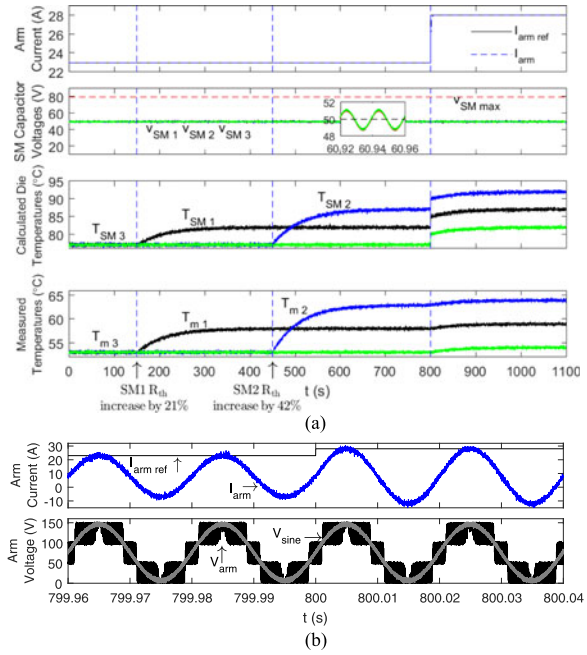

Fig. 7. Experimental response of submodules' voltages and temperatures without thermal regulation for a thermal disturbance: (a) submodule voltages and temperatures and (b) multilevel arm voltage waveform and arm current.

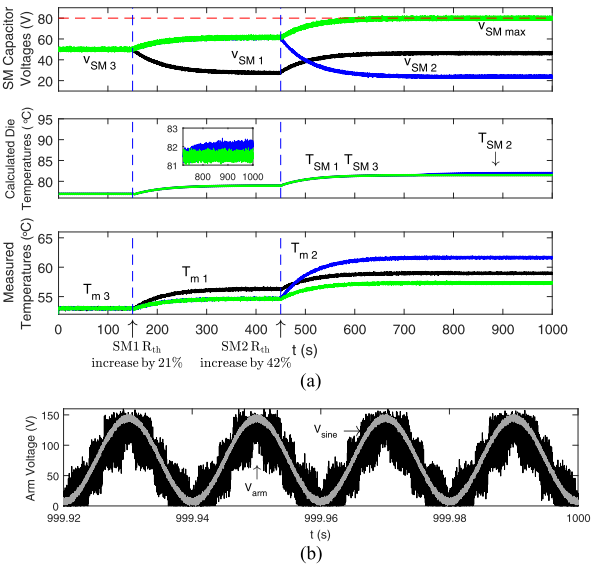

Fig. 8. Experimental submodules thermal regulation as a response to a thermal disturbance: (a) submodule voltages and temperatures and (b) multilevel arm voltage waveform as a result of unbalanced SM voltages.

steps, the fundamental frequency component of the multilevel voltage waveform in Fig. 8(b) remains unchanged compared to the scenario in Fig. 7(b) where all SM voltages are regulated to $v^*_{\text{SM nom}} = 50$ V.

Similarly to the simulation results in Fig. 5(a), the experimental results of Fig. 8(a) demonstrate the validity of the proposed algorithm in the equalization of the maximum calculated junction temperatures (middle plots), despite different measured case temperatures as a result of the thermal imbalances (bottom plots).

VI. Discussion

A. Temperature Estimation

The equalization of the estimated junction temperatures through the balancing strategy ensures similar thermal conditions for the semiconductor dies, which is expected to translate into a similar lifetime expectation for all the SMs [32], leading to an increased converter reliability [15] and more predictable lifetime behavior when compared to strategies without thermal regulation and balancing.

The use of an estimation of the temperature in the dies makes the implementation of this method straightforward. The temperature calculation in (3) relies on the accurate knowledge of the semiconductor module parameters such as turn-ON and turn-OFF energies and thermal resistances. Although these are assumed to be constant over the lifetime of the converter, their values may, in practice, change as the modules age, e.g., thermal resistances may increase due to the formation of thermal voids in the solder layer of the module. This could be overcome by online thermal resistance monitoring methods such as in [33]. Alternatively, other die temperature estimation methods that are not sensitive to the variation of the thermal resistance with time, such as the ones identified in [34], can be employed.

B. Stability of Submodule Temperature Regulation

The proposed submodule temperature control loop regulates SM capacitor voltages to prevent SM temperature from reaching dangerous values and must therefore avoid temperature overshoots. Using the principle of bandwidth separation between the cascaded loops and neglecting constant disturbances, the open-loop transfer function $G(s)$ of the system can be defined as follows:

$$G(s) = K_{PT}\left(\frac{1+sT_{IT}}{sT_{IT}}\right)\left[K_c\left(\frac{1}{1+\tau}\right)\left(\frac{1}{1+sT_{eq}}\right)\right] \tag{10}$$

where the gain K_c is defined as follows:

$$K_c = \left(\frac{R_{\text{th}\,JC}\,I\,E_{\text{Total}}\left(I_{\text{rms}}\right)f_{sw}}{3v^{\text{ref}}_{\text{CE}}}\right). \tag{11}$$

And K_{PT} and K_{IT} are the proportional and integral gains, respectively, of the PI controller in the submodule temperature control loop of Fig. 1(b), τ is the low-pass filter time constant, and $T_{eq} = 1/2f_{sw}$ corresponds to the delay of the control loop due to the PWM scheme.

The modulus optimum criterion [35] is utilized to tune the PI controller in the submodule temperature control loop. The zero of the PI controller is selected to cancel the largest time constant, while the closed loop gain should be larger than unity for as high frequencies as possible. The PI controller parameters are defined as follows:

$$\begin{cases} K_{PT} = \frac{\tau}{2T_{eq}K_c}. \\ K_{IT} = \tau \end{cases} \tag{12}$$

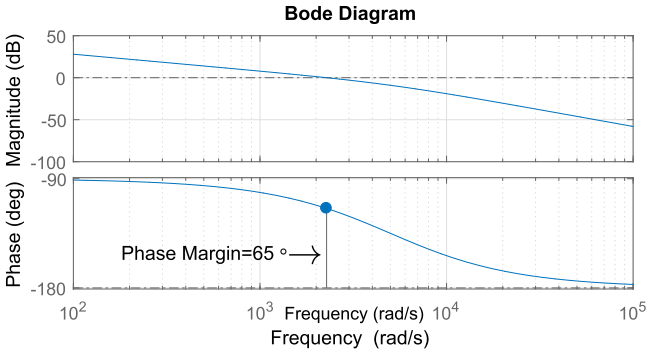

Fig. 9. Bode diagram of the submodule temperature control open-loop transfer function.

And the open-loop transfer function becomes:

$$G(s) = \frac{1}{2T_{eq}} \frac{1}{s(1+sT_{eq})}. \tag{13}$$

From which, it can be observed that the system possesses one pole at the origin and one real pole located at $\omega_n = -1/Teq = -5000$ rad/s. The system is, therefore, stable and there will be no oscillations or overshoot in the temperature.

The bode plot of the transfer function in (13) is represented in Fig. 9, where it can be observed that the system possesses a generous phase margin of 65°and an infinite gain margin. In practice, this means the system can robustly handle phase uncertainty and time delays.

C. Scalability of SM Temperature Balancing

In the simulations and experiments presented so far, since at any moment only two SMs are available to share the voltage from a "hot" SM, only small imbalances can be corrected, at the expense of quite divergent capacitor voltages. In HVdc applications, where dozens or hundreds of SMs are used, semiconductors present lower normalized conduction losses and larger switching energy loss [36] (this is typical for high voltage devices used in HVdc in the 3.3–6.5 kV range). Thus, temperature control can be achieved using smaller capacitor voltage variations from their nominal value, resulting in significantly lower multilevel voltage waveform distortion.

Considering an MMC with ten SMs per arm, the system data from [10] are used to demonstrate the scalability of the proposed method, where $v^*_{\mathrm{SM\,nom}} = 3.0$ kV. Two cascaded disturbances of 10 ° C are applied to two SMs (SM 1 and SM 2) and the results are shown in Fig. 10(a). It can be observed that the thermal disturbances lead to a final value of 3.17 kV (5.6% voltage variation) for all the SMs sharing the additional voltage, compared to a maximum variation of 30 V (60%) for SM 3 in the MMC with only three SMs; hence higher thermal unbalances can be corrected. The temperature increase in the SMs sharing the voltage burden is also smaller, ≈1 °C per thermal disturbance per SM, given its division by the higher number of available SMs.

Thermal imbalances of 10 °C lead to a voltage variation of 750 V in SM 1 and SM 2, which is in good agreement with $\Delta v_{\mathrm{SM}} = 749.35$ V obtained using (8). After the first imbalance, the unaffected SM voltages are regulated to $v_{\mathrm{SM}\,\chi} = 3083$ V,

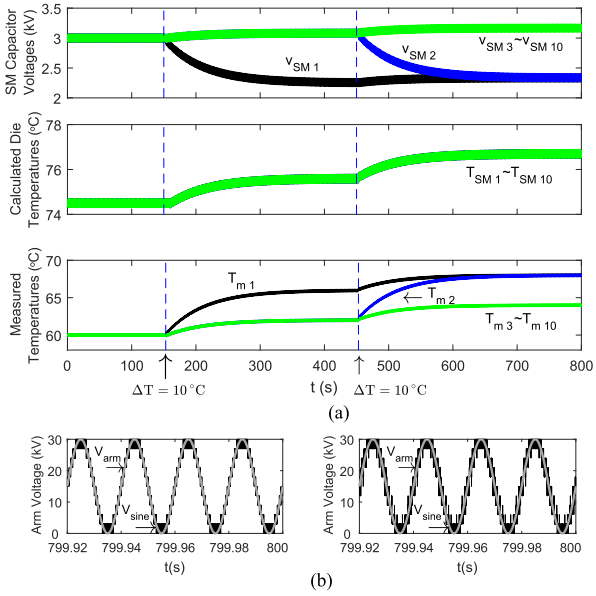

Fig. 10. Submodules' thermal regulation for a thermal disturbance: (a) submodules' voltages and temperatures and (b) multilevel arm voltage waveform—without thermal regulation (left) and as a result of unbalanced SM voltages (right).

which represents a 2.8% voltage increase from their nominal value. A similar voltage regulation occurs after the second 10 °C imbalance, resulting in final SM voltages of $v_{\mathrm{SM}\,\chi} = 3166$ V, also in good agreement with the value of 3.17 kV obtained in simulation.

It can be seen in Fig. 10(b) that there is very little distortion on the multilevel voltage waveform on the right (THD = 11.61%), compared to the waveform shown on the left (THD = 11.08%), where the proposed algorithm is not enabled and there is no SM voltage regulation. Although SM capacitor voltage feedforward allows the fundamental components of the arm voltage to remain unchanged, there is, effectively, a tradeoff between SM thermal regulation and the quality of the output voltage waveform, which becomes less significant as the number of SMs increases.

Further thermal imbalances are now considered: 5, 10, 15, and 20 °C are applied to SM 1, SM 2, SM 3, and SM 4, respectively, and the corresponding simulation results are shown in Fig. 11(a). It can be observed that the SM capacitor voltages diverge more due to the higher number of thermal imbalances and their different magnitudes. The voltages of the unaffected modules increase by 13% as a result of the decrease in the voltages of the affected modules. Furthermore, the voltage variations of the thermally imbalanced SMs and the remaining SMs are proportional to the amplitudes of the imbalances, as predicted by (8) and (9). As a result, the THD of the multilevel arm voltage waveform in the right plot of Fig. 11(b) increases from 11.08% to 16.23%; compared to the total imbalance of 20 °C considered in the right plot of Fig. 10(b), there is a 4.62% increase in THD for a 30 °C increase in the total thermal imbalance.

The limitations for the harmonic distortion introduced by power electronic converters are established on a country-by-country basis [37]. Considering the GB Grid Code [38] as an

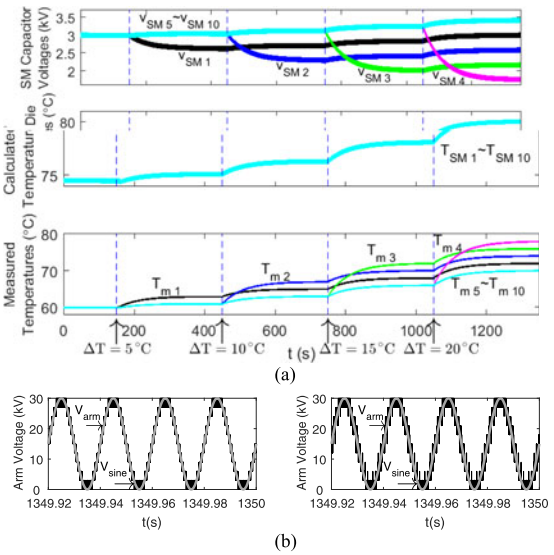

Fig. 11. Submodules' thermal regulation for four thermal disturbances: (a) submodules' voltages and temperatures and (b) multilevel arm voltage waveform—without thermal regulation (left) and as a result of unbalanced SM voltages (right).

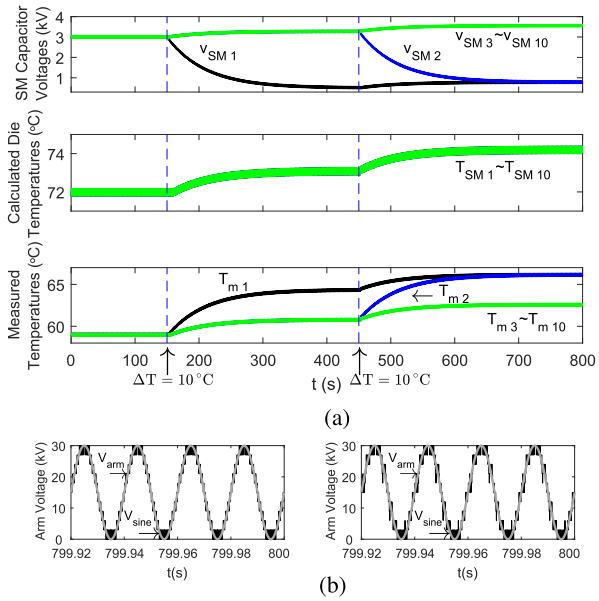

Fig. 12. Submodules' thermal regulation for a thermal disturbance at low switching frequency: (a) submodules' voltages and temperatures and (b) multilevel arm voltage waveform—without thermal regulation (left) and as a result of unbalanced SM voltages (right).

example, a THD limit of 3% for systems of up to 400 kV is specified. Given the low rating of this system (30 kV), the application of the proposed method to HVdc systems (e.g., 400 kV), where dozens or hundreds of SMs per arm are employed [17], is not expected to pose a problem due to the low THD values reported.

D. Operation at Low Switching Frequency

In HVdc systems, where dozens or hundreds of SMs per arm are employed, the switching frequency of each individual device will be very low, reducing the proportion of switching losses in the overall semiconductor losses. This is investigated through the reduction of the switching frequency of 500 Hz of the MMC with ten SMs per arm from [10], utilized for the results in Fig. 10(a), to 150 Hz. The same two cascaded disturbances of 10 °C are applied to two SMs (SM 1 and SM 2) and the results are shown in Fig. 12(a).

As predicted by (8), it can be observed that a lower switching frequency leads to an increase in the capacitor voltage variation required to correct a thermal imbalance, with the new voltage of SMs 1 and 2 being reduced to approximately 0.76 kV. The voltage in the remaining SMs reaches 3.56 kV (18.7% voltage variation), against 3.17 kV in Fig. 10(a) (5.6% voltage variation). This is accompanied in by a THD increase from 11.25% to 12.88% in Fig. 12(b). It can therefore be concluded that when applied to MMCs operating at low switching frequency, the controllability of the proposed method is reduced but not eliminated.

VII. Conclusion

This paper presented a method of SMs' semiconductor temperature balancing in MMC-based applications. Thermal balancing was achieved by controlling the capacitor voltage of each SM in an arm, while controlling the arm voltage to a reference value in order to maintain a particular dc-link voltage. The proposed control strategy required an estimation of semiconductors temperature and a simple method was used in this work, making use of a case temperature measurement provided by an embedded thermistor.

The proposed method was validated experimentally on an MMC arm with three SMs. A total imbalance of ≈ 15 °C, corresponding to a cascaded increase in an SM semiconductor module thermal resistance of 63%, was shared by only three SMs without violating their electrical operating conditions, considering an operating voltage limit of 60% above their nominal value. As a result of the proposed method, a distorted multilevel arm voltage waveform was produced from unbalanced capacitor voltages, although its fundamental frequency component remained unchanged and the distortion became negligible as the number of SMs increased.

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