A Compact Modular Multilevel DC–DC Converter for High Step-Ratio MV and HV Use

Xin Xiang , *Student Member, IEEE*, Xiaotian Zhang , *Member, IEEE*, Thomas Luth,
Michael M. C. Merlin, *Member, IEEE*, and Timothy C. Green , *Senior Member, IEEE*

Abstract—**In multi-terminal dc networks or future dc grids, there is an important role for high step-ratio dc–dc conversion to interface a high-voltage network to lower voltage infeeds or offtakes. The efficiency and controllability of dc–dc conversion will be expected to be similar to modular multilevel ac–dc converters. This paper presents a modular multilevel dc–dc converter with a high step-ratio for medium-voltage and high-voltage applications. Its topology on the high-voltage side is derived from the half-bridge single-phase inverter with stacks of sub-modules (SMs) replacing each of the switch positions. A near-square-wave current operation is proposed, which achieves near-constant instantaneous power for single-phase conversion, leading to reduced stack capacitor and filter volume and also increasing the power device utilization. A controller for energy balancing and current tracking is designed. The soft-switching operation on the low-voltage side is demonstrated. The high step-ratio is accomplished by combination of inherent half-bridge ratio, SM stack modulation, and transformer turns ratio, which also offers flexibility to satisfy wide-range conversion requirements. The theoretical analysis of this converter is verified by simulation of a full-scale 40 MW, 200 kV converter with 146 SMs and also through experimental testing of a down-scaled prototype at 4.5 kW, 1.5 kV with 18 SMs.**

Index Terms—**Compact volume, dc grids, high step-ratio, modular multilevel converter (MMC).**

NOMENCLATURE

C_h	Control headroom.
D	Duty-cycle of the near-square-wave.
E_S	Sum of the energy stored in all capacitors.
E_{Ts}, E_{Bs}	Energy stored in the top stack and bottom stack.
f_o, f_s	Operation frequency, switching frequency.
f_r	SM sorting and selection frequency.
$i_{B\,\mathrm{ac}}$	AC component of the bottom stack current.
i_{Bcp}	Current through the bottom dc-link capacitor C_B.
$i_{B\,\mathrm{dc}}$	DC component of the bottom stack current.
i_{Di}	Current through the rectifier diodes D_i ($i = 1, 2, 3, 4$).
i_H	Current on the high-voltage side.
i_L	Current on the low-voltage side.
i_{N1}	Current on the transformer primary side.
i_{N2}	Current on the transformer secondary side.
$i_{T\,\mathrm{ac}}$	AC component of the top stack current.
i_{Tcp}	Current through the top dc-link capacitor C_T.
$i_{T\,\mathrm{dc}}$	DC component of the top stack current.
i_{Ts}, i_{Bs}	Current through the top stack and bottom stack.
n_{B-}	On-state SM number in the bottom stack.
n_{SM}	SM total number.
n_T, n_B	SM number in the top stack and bottom stack.
n_{T-}	On-state SM number in the top stack.
P	Power rating.
R	Overall step-ratio.
r_S, r_T	Stack modulation ratio, transformer turns ratio.
T_o, T_s	Operation cycle, switching cycle.
v_{Bj}	Capacitor voltage of the jth SM in the bottom stack.
v_{Bl}	Voltage across the bottom arm inductor L_B.
v_{CB}	Voltage across the bottom dc-link capacitor C_B.
v_{CT}	Voltage across the top dc-link capacitor C_T.
v_{Di}	Voltage across the rectifier diodes D_i ($i = 1, 2, 3, 4$).
v_H	Voltage on the high-voltage side dc link.
v_L	Voltage on the low-voltage side dc link.
v_{N1}	Voltage on the transformer primary side.
v_{N2}	Voltage on the transformer secondary side.
v_{SM}	Average value of the SM capacitor voltages.
v_{Tj}	Capacitor voltage of the jth SM in the top stack.
v_{Tl}	Voltage across the top arm inductor L_T.
v_{Ts}, v_{Bs}	Voltage across the top stack and bottom stack.
δ_{dc}	Voltage tolerance of a dc-link capacitor.
δ_{SM}	Voltage tolerance of an SM capacitor.
$*$	Superscript for controller reference value.
$\lfloor x \rfloor$	Floor (the largest integer less than or equal to x).

I. INTRODUCTION

DC transmission is becoming the preferred option for large-scale renewable energy integration [1]. The rapid development of high-voltage direct current (HVDC) technology in the

last decade is facilitating the evolution of dc transmission from point-to-point connections to multi-terminal networks and dc grids [2]. In a multi-terminal dc network, there is a role for the high power throughput but low voltage ratio (HPLR) [3] dc–dc conversion for connecting two HVDC links of similar but not identical voltage [4], [5]. There is also a role for the low power throughput but high voltage ratio (LPHR) [3] dc–dc conversion for interfacing a high voltage (HV) network to lower voltage infeeds or offtakes, often termed "dc tap," which was first proposed in [6] and developed in [7]–[9] with different topologies and control schemes.

Although there is no full-scale practical project for dc tap up to date, it has attracted much interest in recent years for both academic research and industrial development to satisfy the demand and architecture for future dc grids [10]–[16]. It could collect power from small-scale offshore wind farms (OWF) near the cable routes by tapping into the HVDC link directly [10], [11], and the LPHR conversion can also tap out a small fraction of the link power to service demand in remote communities with inadequate ac supplies but which are crossed by the HVDC corridors [12]–[14]. A growing role for conversion between HVDC and medium voltage direct current (MVDC) grids is also anticipated [15], [16].

At low voltage (LV) level, high step-ratio dc–dc converters have been extensively investigated [17] but the use of a single device and high switching frequency make the application to higher voltage difficult. The multi-module concept has been applied to classic LV dc–dc topologies, notably the dual active bridge (DAB), for medium voltage (MV) applications [18] using parallel or series arrangements to mitigate the voltage and current stress on each device. The modular DAB topology is central to a solid-state transformer [19] and has attracted interest for MVDC networks [20]. However, the large number of module transformers and their onerous insulation requirement raise difficulties in HV and high step-ratio applications. In addition, the lack of fault tolerance capability is another drawback for the modular DAB converter [21]. The full-bridge three-level DAB or single-active-bridge (SAB) dc–dc converters were proposed and developed as a promising solution for dc collection [22], [23], facilitating the integration of wind turbines into an MVDC link, but the three-level operation would also face some serious challenges on practical design if applied directly in the HV conversion.

The difficulties and drawbacks in DAB or SAB can be avoided by using a modular multilevel converter (MMC) [24], [25] in front-to-front configuration. The front-to-front MMC brings its advantages of modularity and controllability to interfacing two different HVDC links and can block propagation of fault current from one dc link to the other [26], [27]. However, it is not a low-cost option for LPHR applications since the power devices utilization is usually lower than other competing topologies [15], [18]. The concept of the auto dc transformer based on MMC technology was proposed in [28], [29]. High power device utilization was attained leading to a reduced cost compared to the front-to-front design but the large filter required [28] and difficulty with dc fault management [29] would under-

mine this advantage. Incorporating the MMC principle with the classic dc–dc circuits in a resonant mode has been reported for HV and high step-ratio conversion [30]. However, the switches on its high-voltage side must withstand both high-voltage and high-current stress, which restricts the application scope.

The MMC principle with full-bridge or half-bridge submodules (SMs) has also been applied to the full-bridge single-phase DAB circuit for ac–ac [31] or dc–dc conversion [32] in MV and HV applications. Trapezoidal voltage or square-wave voltage modulation was used to decrease the converter volume and therefore the cost [33]. They share the advantages of the DAB converter from LV and MV applications and also inherit the good features of the MMC for HV applications. The proposal in this paper is to evolve these topologies and modulation for LPHR conversion and develop a cost-effective dc tap design for multi-terminal dc networks or dc grids. On the high-voltage side, the circuit is changed to a half-bridge single-phase inverter with stack of half-bridge SMs replacing each of the switch positions. Considering the high step-ratio conversion, the low-voltage side uses a diode/active bridge rectifier arrangement for unidirectional/bidirectional power flow, simplifying the configuration and also achieving soft-switching operation.

The overall volume of a conversion system and its associated weight is one of the most important factors in the estimation and evaluation for its overall cost [5], [32], [33], especially in the offshore cases where the platform cost is extremely expensive [34], [35]. Given that the practical volume of the valve halls is mainly governed by the isolation distances and maintenance separation between SM stacks of different phases [36], [37], the total space occupied by this two-stack half-bridge single-phase converter would be smaller for this dc tap LPHR application than the symmetrical front-to-front arrangement, which needs 12 stacks (3-phase configuration) or eight stacks (full-bridge configuration) to accomplish the dc–ac–dc conversion. Furthermore, continuous instantaneous power flow is desirable to obviate large smoothing capacitance on the dc buses and reduce the SM capacitor volume and so a near-square-wave current operation is proposed in this paper. It will be shown that this also benefits power device utilization. High step-ratio voltage conversion can be achieved by combination of inherent half-bridge ratio, stack modulation, and transformer ratio, which also provides flexibility in design and operation to meet the wide-range voltage conversion. The basic concept of this topology was first proposed in conference proceedings [38]. This paper significantly develops the concept with detailed operation principles and control scheme in Sections II and III, respectively. The specific investigation on circuit performance is provided in Section IV, and the theoretical analysis is verified by a full-scale example simulation in Section V and also through down-scaled prototype experiments in Section VI. Section VII presents the conclusion.

II. TOPOLOGY DESCRIPTION AND OPERATING PRINCIPLES

The schematic of the converter is illustrated in Fig. 1. The high-voltage side contains two stacks of half-bridge SMs, SM_T
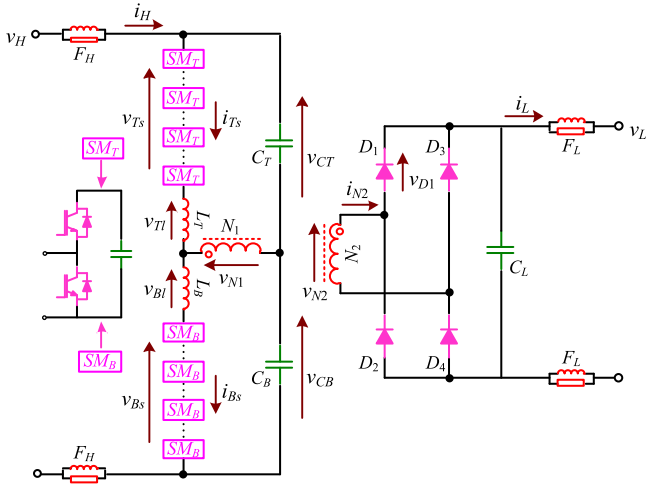
Fig. 1.   LPHR modular multilevel dc–dc converter.

Fig. 2.   Voltage and current waveforms in one operation cycle.

and SM$_B$ in the top and bottom arm, respectively, forming a single-phase MMC configuration with arm inductors L_T and L_B. There are n_{SM} SMs in total, divided equally between top and bottom stacks. The primary winding of the transformer ($r_T = N_1/N_2$) is connected between the phase midpoint and a neutral point created by two dc-link capacitors C_T and C_B. For illustration, a simple full-bridge diode rectifier (formed of series-connected diodes appropriate to the voltage rating) is chosen to connect the transformer secondary winding to a smoothing capacitor C_L on the low-voltage side. Controllable devices can be used in a rectifier for bidirectional power flow. F_H and F_L are filters on the high-voltage and low-voltage sides, formed of parallel inductors and resistors to confine ac current components to circulate within the converter.

Fig. 2 shows that there are six stages in one operation cycle. The equivalent circuits for the first three stages over $t_0 - t_3$ are shown in Fig. 3. The other half of the cycle, $t_3 - t_6$, is symmetrical to $t_0 - t_3$. The arrows in Fig. 1 define the voltage and current reference directions for the waveforms of Fig. 2 (and the rest of the paper), and the arrows in Fig. 3 display the actual current flow in each stage. n_{T-} and n_{B-} are used to describe the number of SMs in the ON-state (meaning that the upper switch is ON and the lower is OFF) for the top stack and bottom stack, respectively. It is worth noting that the total number of SMs inserted between positive terminal and negative terminal of the high-voltage dc link is not constant, and the sum of v_{Ts} and v_{Bs} varies in different operation stages. The operating principles for each stage will be analyzed in detail in the following sections.

A. Stage 1: Positive Steady State ($t_0 - t_1$)

In this stage, a small number of the SMs in the top stack (n_{T-sma}) and a large number of the SMs in the bottom stack (n_{B-lar}) are in the ON-state, generating steady voltage values of $v_{Ts}(t_0)$ and $v_{Bs}(t_0)$. Summed together they match the high-side dc-link voltage v_H but the split is such that a positive voltage is applied to the transformer winding. The stack voltages are described in (1) and (2) under the assumptions that v_{CT} and
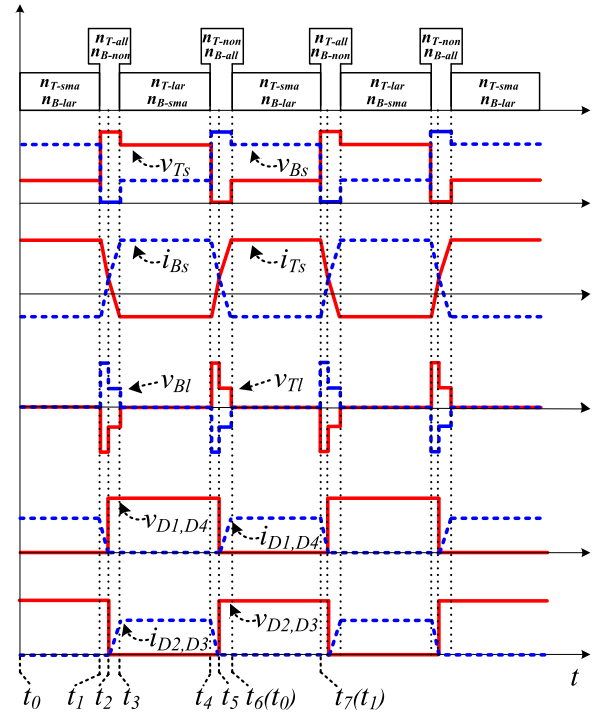
v_{CB} are balanced and all SM capacitor voltages are equal to v_{SM}. The sum of v_{Ts} and v_{Bs} equals to v_H, shown in (3), and the voltages across the top arm inductor and bottom arm inductor are both 0. This stage is considered to be the positive steady state. The stack currents through the arm inductors maintain at values of $i_{Ts}(t_0)$ and $i_{Bs}(t_0)$, expressed in (4) and (5). Diodes D_1 and D_4 are in conduction, whereas D_2 and D_3 are reverse-biased

$$v_{Ts}(t) = v_{Ts}(t_0) = \tfrac{v_H}{2} - r_T v_L = n_{T-sma} \cdot v_{SM} \quad (1)$$

$$v_{Bs}(t) = v_{Bs}(t_0) = \tfrac{v_H}{2} + r_T v_L = n_{B-lar} \cdot v_{SM} \quad (2)$$

$$v_{Ts}(t) + v_{Bs}(t) = (n_{T-sma} + n_{B-lar}) \cdot v_{SM} = v_H \quad (3)$$

$$i_{Ts}(t) = i_{Ts}(t_0) = i_H + \tfrac{i_L}{2r_T} \quad (4)$$

$$i_{Bs}(t) = i_{Bs}(t_0) = i_H - \tfrac{i_L}{2r_T}. \quad (5)$$

B. Stage 2: Force Current Reversal ($t_1 - t_2$)

A rapid current reversal is required for the near-square-wave operation and to achieve this all of the SMs in the top stack are turned ON (n_{T-all}) at t_1 and all SMs in the bottom are turned OFF (n_{B-non}) to impose the largest possible negative voltage across the arm inductor. Fig. 3 shows the commutation of the stack currents during this short stage. The stack voltage and current relationships over this period are given in (6)–(9). It needs to be noted that the controller can preset a slope limiter for the transient currents in (8) and (9), especially for the low-current operation. The inserted SM number in transient stages and transient waveform is adjustable according to the controller
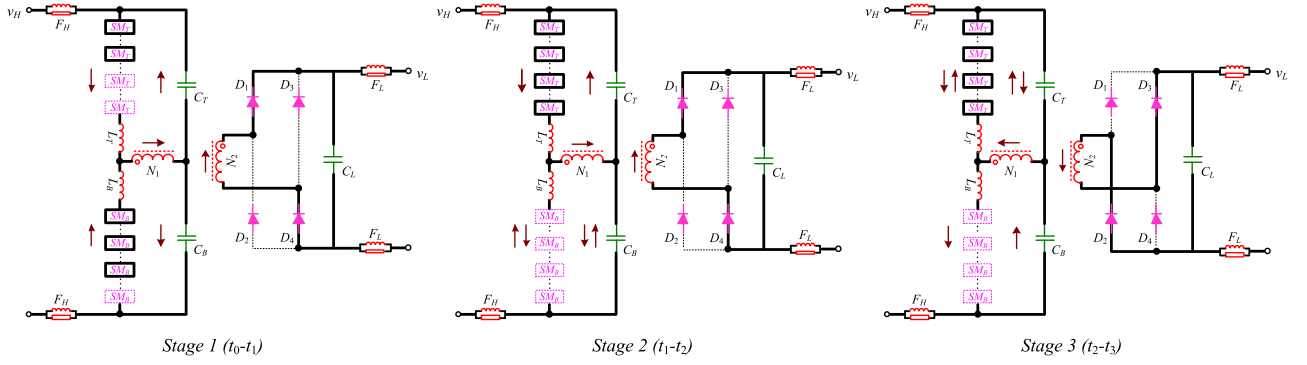
Fig. 3. Equivalent circuits and operation analysis.

capability and practical requirements.

$$v_{Ts}(t) = n_{T-\text{all}} \cdot v_{\text{SM}} = n_T \cdot v_{\text{SM}} = \frac{n_{\text{SM}}}{2} \cdot v_{\text{SM}} \qquad (6)$$

$$v_{Bs}(t) = n_{B-\text{non}} \cdot v_{\text{SM}} = 0 \qquad (7)$$

$$i_{Ts}(t) = i_{Ts}(t_1) + \frac{1}{L_T}\left[\frac{v_H}{2} - v_{Ts}(t) - r_T v_L\right](t - t_1) \quad (8)$$

$$i_{Bs}(t) = i_{Bs}(t_1) + \frac{1}{L_B}\left[\frac{v_H}{2} - v_{Bs}(t) + r_T v_L\right](t - t_1) \quad (9)$$

The control headroom C_h shown in (10) is the additional negative voltage available over and above that which will be needed to maintain the negative steady-state current. A larger value allows a faster transition of current and a waveform closer to square. Some relevant research on additional SMs insertion was also discussed in [39], [40]. The extra full-bridge SMs were designed to assist the turn-OFF operation of thyristors [39]. The redundant SMs in [40] were used to compensate the failed nonredundant SMs in other arms and improve reliability. The additional half-bridge SMs here are utilized to generate an adjustable control headroom for faster current transition, which has different roles and purposes in the operation with [39], [40]

$$C_h = \frac{n_{T-\text{all},B-\text{all}} - n_{T-\text{lar},B-\text{lar}}}{n_{T-\text{all},B-\text{all}}} = \frac{n_{\text{SM}} - (n_{T-\text{lar}} + n_{B-\text{lar}})}{n_{\text{SM}}}.$$
$$(10)$$

The sum of v_{Ts} and v_{Bs} in this stage can be expressed as (11). Compared with (3), it can be found that this value would be smaller than v_H in the normal operation unless the control headroom C_h is very large in the design

$$v_{Ts}(t) + v_{Bs}(t) = \left(n_{T-\text{lar}} + \frac{C_h}{1 - C_h} n_{T-\text{lar}}\right) \cdot v_{\text{SM}}.$$
$$(11)$$

This stage ends when i_{D1} and i_{D4} reduce to zero at t_2. Note that v_{D1} and v_{D4} enter reverse-bias after i_{D1} and i_{D4} drop to zero, and thus, the soft-switching turn-OFF operation is achieved.

C. Stage 3: Establish Negative Steady State $(t_2 - t_3)$

Having commuted the diodes, it is now necessary to establish the steady negative current. Initially, the SMs are kept the same states until t_3, at which point the stack currents reach the new steady values of $i_{Ts}(t_3)$ and $i_{Bs}(t_3)$ and the transient period is finished. As Fig. 3 illustrates, after the transformer current changed direction at t_2, the slopes of i_{Ts} and i_{Bs} became shal-

lower for $t_2 - t_3$ because D_2 and D_3 are in conduction and the low-side voltage appears in the opposite sense.

D. Stage 4: Negative Steady State $(t_3 - t_4)$

At t_3, with the new currents established, the controller turns OFF some of SMs in the top stack (the number turned ON reduces from $n_{T-\text{all}}$ to $n_{T-\text{lar}}$) and turns ON a small number in the bottom stack $(n_{B-\text{sma}})$. This is a symmetrical case to stage 1, and the description of stack voltage and current is similar to (1)–(5) but with the top and bottom stack value replacing each other.

E. Stage 5 $(t_4 - t_5)$ and Stage 6 $(t_5 - t_6)$

All of the SMs in the top stack are turned OFF (Tn_{non}) and all SMs in the bottom are turned ON (Bn_{all}) at t_4 to rapidly reduce the negative current to zero. The diodes commutate at t_5 (the end of stage 5) and the current continues its transition toward the positive steady value. The operational principles of stages 5 and 6 are the same as stages 2 and 3. The control headroom is used again to accelerate the current transition. When stack currents reach their steady-state values $i_{Ts}(t_6)$ and $i_{Bs}(t_6)$, the converter returns to stage 1 and the next cycle of operation begins.

III. ENERGY MANAGEMENT AND CONTROL SCHEME

The energy stored in each stack is expressed as (12) under the assumption that all the SM capacitances are equal to C_{SM}, and the reference value for the total energy is given in (13)

$$E_{Ts,Bs} = \sum_{j=1}^{\frac{n_{\text{SM}}}{2}} \frac{1}{2} C_{\text{SM}} v_{Tj,Bj}^2 \qquad (12)$$

$$E_S^* = \frac{1}{2} C_{\text{SM}} v_{\text{SM}}^{*2} \cdot n_{\text{SM}}. \qquad (13)$$

The objective of energy management is twofold: maintain the sum of E_{Ts} and E_{Bs} equals to E_S^*, shown in (14), and keep the difference between them to zero, given in (15)

$$E_{Ts} + E_{Bs} = E^* \qquad (14)$$

$$E_{Ts} - E_{Bs} = 0. \qquad (15)$$

The analysis in Sections II-A and II-D of the two steady-state stages revealed that the stack voltages comprise a dc offset $v_H/2$ and an ac component $\pm r_T v_L$. The stack currents also comprise
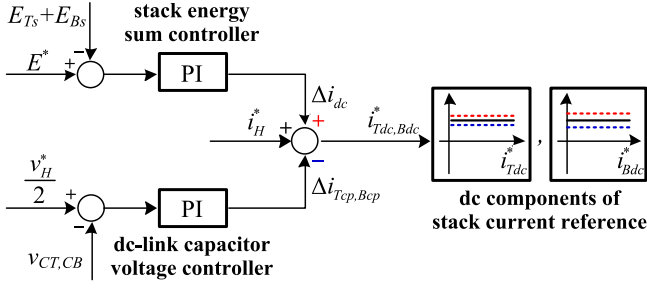
Fig. 4. Energy management of dc components.

Fig. 5. Energy management of ac components.

a dc component i_H and an ac current $\pm i_L/2r_T$. The energy exchange ΔE in one operation cycle can be approximated as (16) by neglecting the very short transient period

$$\Delta E_{Ts,Bs} = \left(\frac{v_H}{2} \mp r_T v_L\right)\left(i_H \pm \frac{i_L}{2r_T}\right)\cdot \frac{T_o}{2}$$
$$+ \left(\frac{v_H}{2} \pm r_T v_L\right)\left(i_H \mp \frac{i_L}{2r_T}\right)\cdot \frac{T_o}{2}$$
$$= \frac{(v_H i_H - v_L i_L)\cdot T_o}{2} = 0. \qquad (16)$$

It can be seen that energy deviations from the ac and dc terms are zero over an operation cycle without extra balancing control. The stack energy of this converter is naturally balanced if the original state satisfies the conditions in (14) and (15). A transient energy drift or an initially unbalanced state can be corrected by adding an extra dc component Δi_{dc} and an ac component $\pm \Delta i_{ac}/2r_T$ into the stack currents, and thereby the stack energy exchanges are adjusted according to the following equation

$$\Delta E'_{Ts,Bs} = \left(\frac{v_H}{2} \mp r_T v_L\right)\left[(i_H + \Delta i_{dc}) \pm \frac{i_L \pm \Delta i_{ac}}{2r_T}\right]\cdot \frac{T_o}{2}$$
$$+ \left(\frac{v_H}{2} \pm r_T v_L\right)\left[(i_H + \Delta i_{dc}) \mp \frac{i_L \pm \Delta i_{ac}}{2r_T}\right]\cdot \frac{T_o}{2}$$
$$= \frac{[v_H(i_H + \Delta i_{dc}) - [v_L(i_L \pm \Delta i_{ac})]\cdot T_o}{2}. \qquad (17)$$

Then, the sum and difference of the energy exchanges for the two stacks are given in (18) and (19), which reveal the adjustments for sum and difference of the stack energies are decoupled in this converter: Δi_{dc} alone sets the change in the sum and Δi_{ac} alone sets the change in the difference

$$\Delta E'_{Ts} + \Delta E'_{Bs} = v_H \Delta i_{dc} T_o \qquad (18)$$
$$\Delta E'_{Ts} - \Delta E'_{Bs} = -v_L \Delta i_{ac} T_o. \qquad (19)$$

The use of proportional-integral controllers for the energy management of the sum and difference of stack energies is illustrated in Figs. 4 and 5. Fig. 4 shows three terms combining to the dc components of stack current references i^*_{Tdc} and i^*_{Bdc}, namely: an adjustment for stack energy sum Δi_{dc}; the high-voltage side current reference i^*_H, and an adjustment for the dc-link capacitor voltage balance $\Delta i_{Tcp,Bcp}$. Fig. 5 shows three terms combining to form the ac components of stack current references i^*_{Tac} and i^*_{Bac}, namely: an adjustment for the stack
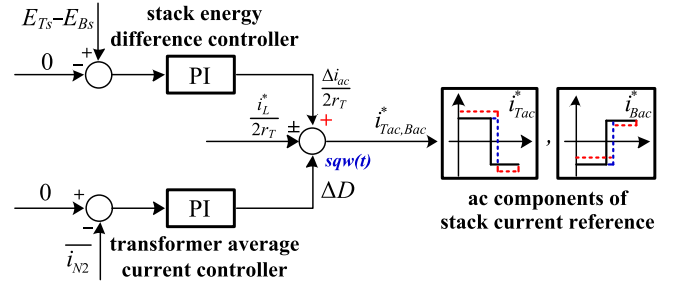
energy difference $\Delta i_{ac}/2r_T$; the low-voltage side current reference $i^*_L/2r_T$, and a duty-cycle adjustment ΔD for transformer average current neutralization. The complete stack current references for top and bottom i^*_{Ts} and i^*_{Bs}, including all the balancing terms, are summarized in (20), in which the square-wave function sqw(t) for each operation cycle T_o is defined as (21)

$$i^*_{Ts,Bs} = i^*_{Tdc,Bdc} + i^*_{Tac,Bac}$$
$$= i^*_H + \Delta i_{dc} - \Delta i_{Tcp,Bcp} \pm \frac{i^*_L \pm \Delta i_{ac}}{2r_T}\cdot \text{sqw}(t) \quad (20)$$

$$\text{sqw}(t) = \begin{cases} 1, & 0 < t \le \frac{T_o}{2} + T_o \cdot \Delta D \\ -1, & \frac{T_o}{2} + T_o \cdot \Delta D < t \le T_o. \end{cases} \qquad (21)$$

The entire control scheme is shown in Fig. 6. It comprises an outer loop to regulate v_L, which sets the principal reference for the inner current loop to which the balancing terms are added according to the energy management algorithms from Figs. 4 and 5. The detailed expression for stack current references is shown in (20). The inner loop can be used for the current source mode operation, in which the converter is controlled to interface dc grids at different voltage levels. By adding the outer loop for voltage control, this converter is operated in a voltage source mode to collect the power from OWF or feed the power to some remote area loads. The modulation scheme in Fig. 6 is a classic nearest level modulation (NLM) [24], [25] to balance all SM capacitor voltages close to v^*_{SM}. The stack sorts the SMs in the order of SM capacitor voltage and the first N_{NLM} SMs with lowest voltages are inserted into the stack when the stack current direction is charging SM capacitors, while the highest N_{NLM} SMs are switched into the stack when the current direction is discharging ($N_{NLM} = \lfloor v^*_{Ts,Bs}/v^*_{SM}\rfloor$).

IV. CIRCUIT PERFORMANCE ANALYSIS

In this section, the performance of this converter is analyzed and the operational advantages and limitations are discussed.

A. SM Capacitor Sizing

SM capacitor size typically accounts for more than half the volume of each SM in the classic MMC [41], [42] and SM capacitor size is, therefore, an important design consideration. The size is dictated by the maximum stack energy deviation and the capacitor voltage tolerance. The energy deviation for this
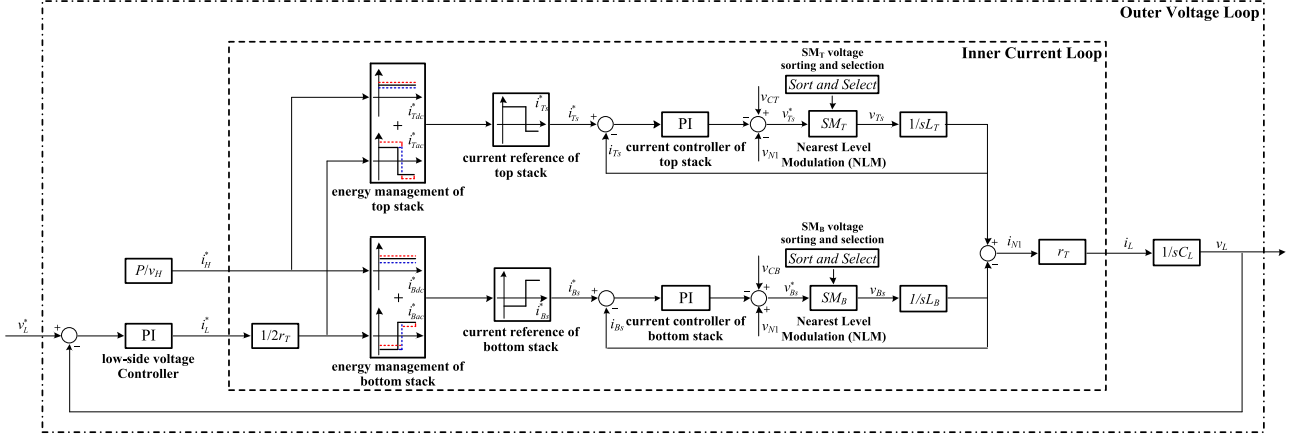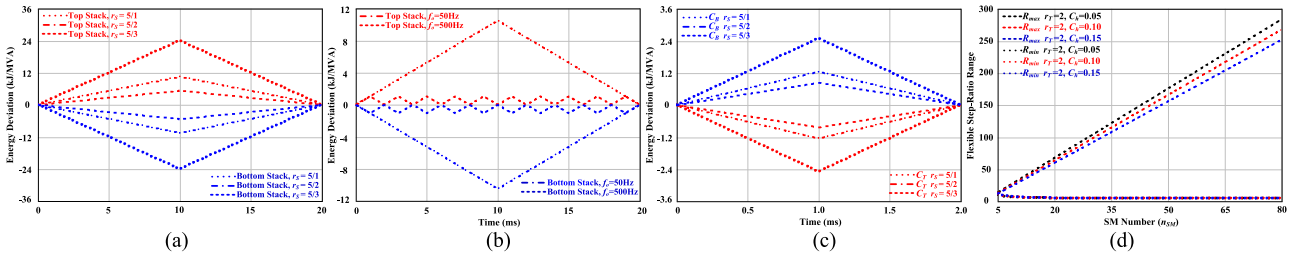
Fig. 6.   Control scheme.

Fig. 7.   Circuit performance analysis (a) Stack energy deviation with $f_o = 50$ Hz. (b) Comparison of 500 Hz operation and 50 Hz operation with $r_S = 5/2$. (c) Energy deviation for high-voltage dc-link capacitors with $f_o = 500$ Hz. (d) Flexible step-ratio range.

near-square-wave converter is given as follows:

$$
\begin{aligned}
dE_{Ts,Bs} &= \int_0^t v_{Ts,Bs}(t) \cdot i_{Ts,Bs}(t)\, dt \\
&= \int_0^t \left[\frac{v_H}{2} \mp \frac{v_H}{2r_S} \cdot \mathrm{sqw}(t) \right] \left[i_H \pm r_S i_H \cdot \mathrm{sqw}(t) \right] dt \quad (22)
\end{aligned}
$$

where $r_S = v_H/2v_{N1}$, known as the stack modulation ratio, sets the voltage conversion achieved within the stack itself.

The energy deviations for near-square-wave operation at 50 Hz with various values of r_S are shown in Fig. 7(a) and are seen to be isosceles triangles with their peaks occurring mid-cycle. Smaller r_S value gives smaller energy deviation but at the penalty of needing a larger transformer ratio to achieve the same overall voltage step-ratio, which, according to (2), requires more SMs in each stack. Because the ac stage is entirely internal to the converter, the operation frequency can be increased to 250–500 Hz [5] for a reduction in volume and weight of the SM capacitors. As Fig. 7(b) shows, the energy deviations for 500 Hz operation are, as expected, ten times smaller for 50 Hz. The maximum value is about 1 kJ/MVA with stack ratio $r_s = 5/2$, and the deviation can be further reduced to nearly 3% of that in the classic MMC when operated with the same modulation ratio [42]. This is also a smaller deviation than other modulation methods for MMC dc–dc converters operating in the same frequency range [4], [15], [32]. This 500 Hz medium frequency operation would also benefit other passive components' sizing in the converter, such as the internal transformer and arm

inductors. Their volume can be decreased to less than one-third of that for 50 Hz standard frequency operation [43], [44].

The operation frequency could be pushed higher [45], [46] for some applications but switching loss and transformer limitations need to be considered.

B. DC-Link Capacitor Sizing

The energy deviations for C_T and C_B on the high-voltage side, plotted in Fig. 7(c), are similar to those of the stacks but with the deviations in the opposite sense. Near-square-wave operation is also advantageous in achieving a small energy deviation and small capacitor stack for C_T and C_B. On the low-voltage side, the instantaneous power flow is near-constant, and the required capacitance value and physical volume of C_L can be small because it needs to only absorb the ripple arising from the imperfect square-wave current transitions.

C. Power Device Utilization

The extent to which the power devices in a modular converter utilize their current and voltage ratings is an important factor in assessing the performance of that converter. The near-square-wave current operation utilizes the current rating of SMs well compared to the sinusoidal case and uses nearly all of the SMs throughout a half-cycle. The voltage and current expressions of the top stack during the positive half-cycle of sinusoidal operation are shown in (23) and (24), under the assumption that the power factor is 1 and for the same power rating and same

voltage ratio conversion as the analysis in (1) and (4). The stack current maximum value from (24) and (4) are compared in (25)

$$v_{Ts\_\sin}(t) = \frac{v_H}{2} - r_T v_L \sin\theta \qquad (23)$$

$$i_{Ts\_\sin}(t) = i_H + \frac{i_L}{r_T}\sin\theta \qquad (24)$$

$$u = \frac{i_{Ts\_\sin\_\max}}{i_{Ts\_\mathrm{sqw}\_\max}} = \frac{i_H + \frac{i_L}{r_T}}{i_H + \frac{i_L}{2r_T}} = \frac{1+2r_S}{1+r_S} \geq 1.5\,(r_S \geq 1)\,. \quad (25)$$

The peak value of the ac current component in sinusoidal operation is twice that needed in near-square-wave operation for the same power conversion because the rms values of voltage and current that set the power are both a factor of $\sqrt{2}$ less than the peak values. As (25) shows this also, sinusoidal operation requires power devices with a current rating at least 50% higher than the near-square-wave case. This is partially offset by the need for circa 15% extra power devices to create the control headroom for the rapid reversal of a near-square-wave current.

D. Flexible Step-Ratio Range

The step-ratio of this converter is achieved by combination of inherent half-bridge ratio, stack modulation, and transformer turns ratio. This combination gives this converter flexibility in design and operation to meet a wide range of requirements.

Starting from the voltage relationships in (1) and (2), the overall step-ratio can be derived as follows:

$$R = \frac{v_H}{v_L} = 2r_S r_T = \frac{2\,(n_{T-\mathrm{lar}} + n_{T-\mathrm{sma}})}{n_{T-\mathrm{lar}} - n_{T-\mathrm{sma}}} \cdot \frac{N_1}{N_2}. \quad (26)$$

The maximum and minimum values of (26) that can be achieved for a given number of SMs and a given control headroom are presented in (27) and (28)

$$R_{\max} = 2\,(2n_{T-\mathrm{lar}} - 1) \cdot \frac{N_1}{N_2} = 2\,[(1 - C_h)\,n_{\mathrm{SM}} - 1] \cdot \frac{N_1}{N_2} \quad (27)$$

$$R_{\min} = \frac{2\,(n_{T-\mathrm{lar}} + 1)}{n_{T-\mathrm{lar}} - 1} \cdot \frac{N_1}{N_2} = \frac{2\,[(1 - C_h)\,n_{\mathrm{SM}} + 2]}{(1 - C_h)\,n_{\mathrm{SM}} - 2} \cdot \frac{N_1}{N_2}. \quad (28)$$

During the design process, the ratio between r_S and r_T can be adjusted to achieve various optimal objectives such as minimizing the physical volume, maximizing efficiency, or reducing total cost. To illustrate the flexibility during operation (i.e., once the transformer turns ratio is decided), the range of maximum and minimum R with a turns ratio of 2 is plotted in Fig. 7(d) for various choices of control headroom. Varying the combinations for $n_{T-\mathrm{sma}}$ and $n_{T-\mathrm{lar}}$ makes available $n_{\mathrm{SM}}(n_{\mathrm{SM}} - 2)/4$ choices of step-ratio, which for converters with tens or hundreds of SMs gives a large degree of operational flexibility.

The modulation scheme can be also flexible according to different conversion requirements in the practical applications.

When this converter serves as a dc tap for LPHR applications, the overall step-ratio is very high and the power throughput is expected to be less than 10% of the transmission link power [8], [13], [14]. For this application, the transformer power rating and voltage rating (less than 20 kV) will be much smaller than that

in the front-to-front configuration for interconnecting two different HVDC links (more than 400 kV) [4], [5], [27]. Although the near-square-wave operation may pose a challenge on transformers due to the partial discharge, the benefits of reduced conversion volume and higher power utilization have stimulated the innovation and rapid development in transformer design for recent years, including the optimization of core/winding material and structure [47]–[49]. A laboratory prototype of a medium-frequency and medium-voltage near-square-wave transformer is newly announced up to 5 MW demonstration [50]. Alternatively, the experience and technology of small dv/dt filter, which has been widely used in high-power medium-voltage motor drives up to 20 kV operation [51], [52], can be also utilized here in practical considerations.

In the meantime, as analyzed in Section II, the inserted SM number in transient stages and transient waveform are both adjustable according to the actual requirements. For the low step-ratio conversion, the trapezoidal voltage modulation [27] can be also implemented in the stacks as the preferred choice to fulfill the high-power and high-voltage conversion.

E. Soft-Switching Operation

Analysis of the current-reversal stages (stages 2 and 5) showed that the rectifier current can be reduced to zero before the commutation happens so that zero-current-switching (ZCS) turn-OFF operation can be achieved for all the rectifier diodes. For stages 3 and 6 where the new current is established by turning ON the alternate diodes, soft-switching operation is obtained inherently since rectifier diodes have the natural zero-voltage-switching (ZVS) capability. In the case where the rectifier is formed by active devices, both ZVS turn-ON and ZCS turn-OFF operation can still be achieved when the power flow is from the high-voltage to the low-voltage side. If the power flow is reversed, ZCS turn-OFF capability is maintained by the control scheme but ZVS turn-ON may not be possible in all situations.

V. APPLICATION EXAMPLE AND SIMULATION ANALYSIS

This section presents a set of simulations of a full-scale near-square-wave current converter in order to validate the theoretical analysis and explore an application example of making a connection between HVDC and MVDC grids.

The converter is rated at 40 MW for conversion between a 200 kV HVDC link and a 20 kV MVDC grid. The SMs in the high-voltage side have a reference voltage of 2.4 kV. Control headroom of 17% is provided, and therefore, 73 SMs are used in each stack. The ratio of power rating to SM number is still comparable to the standard MMC design [4], [25], [26]. In the low-voltage side, diodes are series connected to support v_L. The operation frequency is set at 500 Hz as a trade-off between the volume and the power losses. As an illustration, the overall step-ratio of 10:1 is composed of the inherent ratio of 2:1 of the half-bridge, a stack modulation ratio of 5:2, and a transformer turns ratio of 2:1. The simulation parameters for this example are summarized in Table I. The simulation was conducted in the MATLAB/Simulink using also the Artemis library.
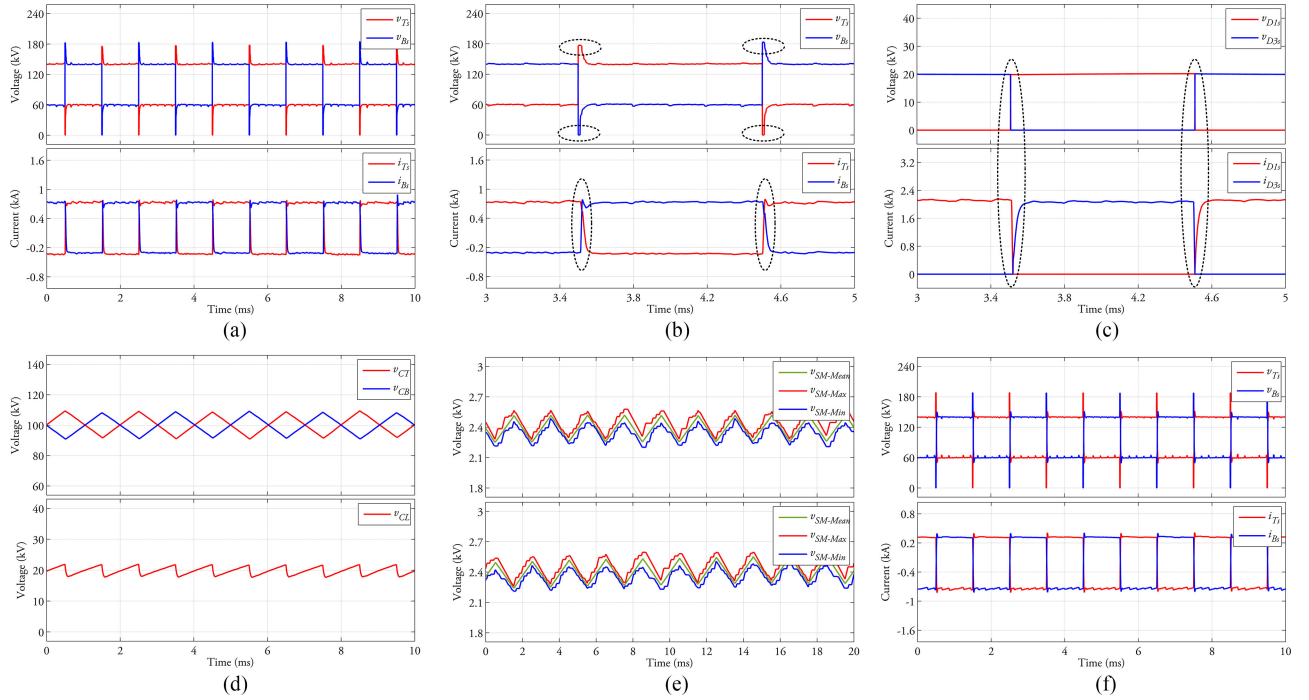
Fig. 8. Simulation results of high-voltage application example (a) Stack voltage and current. (b) Stack voltage and current in one operation cycle. (c) Rectifier voltage and current. (d) DC-link capacitors voltage deviation. (e) SM voltage deviation in top and bottom stack. (f) Power flow reversal.

TABLE I
SIMULATION PARAMETERS FOR THE APPLICATION EXAMPLE

Parameter	Value	Parameter	Value
P	40 MW	f_o	500 Hz
v_H	200 kV ($\pm$100 kV)	f_r	9.7 rot/cycle
v_L	20 kV	C_{SM}	1.0 mF
v_{SM}	2.4 kV	$C_T\ C_B$	45 μF
C_h	17%	C_L	60 μF
$n_T\ n_B$	73	E_S	21.7 kJ/MVA
r_S	5/2	$\delta_{dc}\ \delta_{SM}$	10%, 5%
r_T	2/1	$L_T\ L_B$	1.2 mH

Simulation results are shown in Fig. 8. The stack voltages and currents in Fig. 8(a) are both near-square-waves with dc offsets as expected from (1) to (5). The top stack voltage in the positive steady state (stage 1) is about 60 kV, while the bottom stack voltage is around 140 kV. The negative steady state (stage 4) is symmetrical to the positive steady state with the top stack and bottom stack values replacing each other. Fig. 8(b) shows one cycle in more detail and illustrates the use of the control headroom to commutate the stack currents and synchronize them with the stack voltages. The modulation scheme implemented in this full-scale simulation is a classic NLM with SM voltage sorting and selection algorithm, illustrated in Fig. 6. Since there is a large number of SMs in the stack, the voltage error between $v^*_{Ts,Bs}$ and $N_{NLM}v^*_{SM}$ is negligible compared to the relatively large value of $v^*_{Ts,Bs}$, and NLM is accurate enough for tracking. The ripples in Fig. 8(a) and (b) are caused by SM sorting and selection. The rectifier waveforms in Fig. 8(c) show that the near-square-wave current from the high-voltage side is rectified and appears in the low-voltage link as a near-continuous current

with brief dips toward zero. This feature significantly reduces the capacitance required for C_L compared with a single-phase sinusoidal operation. It can be observed that the diodes that are being commutated OFF have currents that drop to zero before their voltage enters reverse-bias and that those turning ON have currents that rise after their voltage reaches forward-bias. Both ZCS turn-OFF and ZVS turn-ON are achieved in this example.

The dc-link capacitor may bring about some fault current in the event of a dc-side fault. However, it is also worth noting that the fault current caused by the dc-link capacitor will not go through any power device of the converter, allowing for using slow protection means [53], [54], which is inevitable in most multi-terminal and high-voltage converters for multi-terminal dc network or dc grid applications (including the popular 3-phase or single-phase front-to-front converters [32], [33]), so the presented circuit is not inferior in this sense. On the other hand, the dc-link capacitance in this converter can be relatively small thanks to the near-square-wave current modulation and medium-frequency operation. The efficacy of the energy balancing is examined in Fig. 8(d) and (e). Fig. 8(d) shows that v_{CT} and v_{CB} are well-balanced with 45 μF C_T and C_B, and the deviation of v_{CL} is less than 10% of the nominal with 60 μF C_L. It would be possible to reduce further this capacitance if additional control headroom were provided allowing the rate-of-change of current during commutation to be increased. The mean, maximum, and minimum voltage values of the SM capacitors in each stack are shown in Fig. 8(e). It can be seen that the set of SM capacitor voltages are well-controlled and all are within 5% of the reference value of 2.4 kV. The sum of energy stored in all capacitors, including SM capacitors and dc-link capacitors, is only 21.7 kJ/MVA in the application example.

TABLE II
SIMULATION RESULTS OF POWER LOSSES

Power losses components	Value
Stack IGBT conduction	256.6 kW
Stack IGBT switching	274.3 kW
Rectifier diodes conduction	58.7 kW
Rectifier diodes switching	22.5 kW
Transformer core	108.4 kW
Transformer windings	88.2 kW
Other passives	8.5 kW
Total loss	817.2 kW

A power losses model based on IEC 61803 and IEC 62751 [55] was built in the Simulink simulation using manufacturer's data for the chosen devices, namely, the MITSUBISHI CM1000HC-66R for the SM insulated-gate bipolar transistors (IGBTs) and the MITSUBISHI press-pack diode FD3000AU-120DA in series connection for the rectifier. The model reports the conduction and switching loss of each device during the simulation period. The estimation of transformer power loss is based on the Steinmetz equation [46]–[48]. The magnetic core is assumed to be constructed from AK Steel Lite Carlite M-2 electrical steel with a lamination thickness of 0.18 mm and the peak operational flux density was set at 1.62T Litz wire using round copper was chosen for primary and secondary windings, and the number of strands in each bundle was optimized for minimal ac resistance [56].

The power losses result for this case study is presented in Table II and represents an overall efficiency of 98.0%. The IGBT switching loss was the largest term, as might be expected, given the need to create a medium-frequency ac component of 500 Hz compared to 50/60 Hz for a typical ac–dc converter. Recognizing the high step-ratio conversion and internal transformer isolation, the efficiency is reasonable for an LPHR application. The efficiency could be improved by decreasing the operation frequency, and therefore also the switching power loss, but at a volume penalty for the capacitors and transformer.

As mentioned in Section II, this converter can pass power in the reverse direction if the low-voltage side rectifier diodes are replaced by IGBTs. Results for reverse power flow results are shown in Fig. 8(f). The dc offset and ac component of stack voltage are identical to those in Fig. 8(a), but the stack currents are phase-shifted by half a cycle with respect to the voltage.

VI. ASSESSMENT OF EXPERIMENTAL RESULTS

To verify further the theoretical analysis and support the simulation results, a down-scaled laboratory prototype was built with maximum power and high-side voltage at 9 kW and 2 kV, respectively (see Fig. 9). The control scheme was implemented on an OPAL real-time controller. The OPAL controller also manages the gate signals to the converter and records sampled voltages and currents from the converter.

The parameters in experiment demonstration are listed in Table III. Noting that there are only 9 SMs in each stack, NLM is not sufficient for accurate tracking and so additional pulse
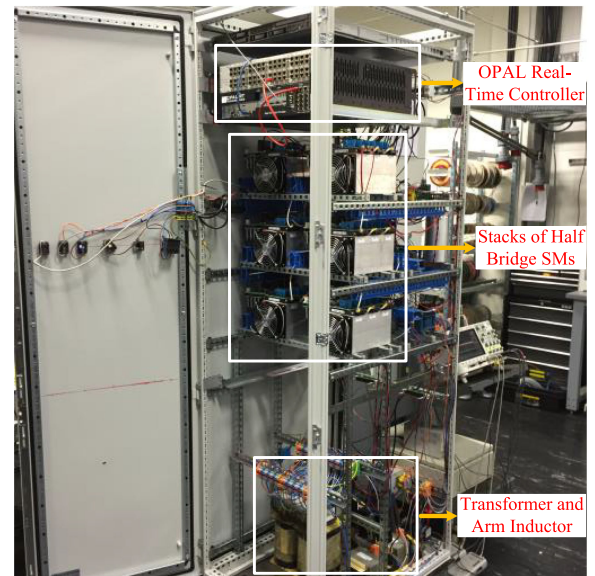
Fig. 9. Down-scaled laboratory prototype.

TABLE III
EXPERIMENT PARAMETERS OF THE LABORATORY PROTOTYPE

Parameter	Value	Parameter	Value
P	4.5 kW	$n_T\ n_B$	9
v_H	1500 V	f_o	500 Hz
v_L	150 V	r_S	5/2
v_{SM}	150 V	r_T	2/1

width modulation (PWM) is applied to one extra SM, which will be the $N_{\mathrm{NLM}} + 1$ SM in the voltage order. It provides the voltage difference between $v_{Ts,Bs}^*$ and $N_{\mathrm{NLM}} v_{\mathrm{SM}}^*$.

Experimental results are shown in Fig. 10. Fig. 10(a) shows the stack voltage and current are both, as expected, near-square-wave with dc offset of $v_H/2$ and i_H, respectively. The high-frequency voltage ripple that can be seen is the result of PWM of the $N_{\mathrm{NLM}} + 1$ SM. Fig. 10(b) demonstrates the use of control headroom to create voltage pulses across the arm inductors, which force the commutation of stack currents and reduce the transition time. These experimental results validate the theoretical analysis in Section II and simulation results in Section V.

To demonstrate the energy balancing results, the voltages and currents at both terminals are shown in Fig. 10(c) and the ranges of SM capacitor voltages are shown in Fig. 10(d). The voltages across C_T and C_B, in Fig. 10(c), are seen to be well-balanced at 750 V. It also verifies the voltage step-ratio in this test is 10:1 and the current ratio between two terminals is 1:10. The minimum and maximum SM capacitor voltages in Fig. 10(d) confirm that the balancing is within 5% of the nominal value of 150 V.

To illustrate the current source operation, the low-voltage terminal was connected to a voltage source (set variously at 150, 225, and 300 V), and the circuit is controlled by the current loop of Fig. 6. By adjusting the current references, the power
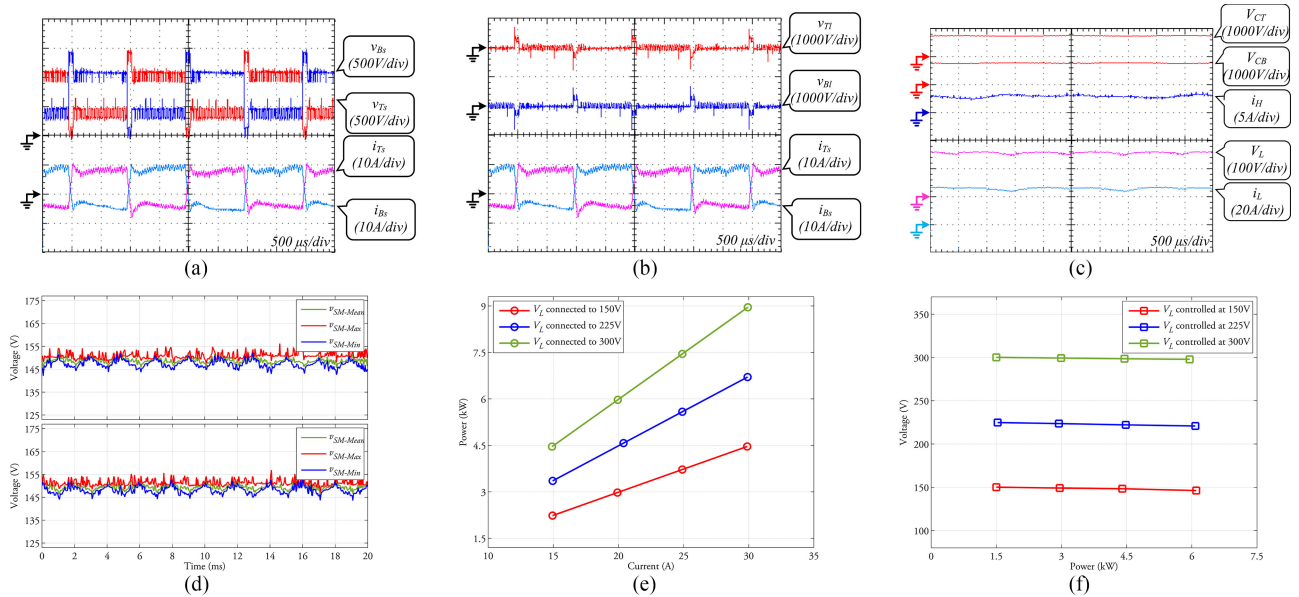
Fig. 10. Experimental results of the down-scaled prototype (a) Stack voltage and current. (b) Arm inductor voltage and current. (c) Voltage and current at both terminals. (d) SM voltage deviation in top and bottom stack. (e) Current source mode operation. (f) Voltage source mode operation.

absorbed by the low-voltage terminal was varied, as shown in Fig. 10(e). To illustrate the voltage source operation, a variable resistor was connected to the low-voltage side and the outer voltage loop of Fig. 6 was employed. Fig. 10(f) shows that V_L was well-controlled at steady values (voltage reference set variously at 150, 225, and 300 V) as the variable resistor was changed from light to heavy load.

VII. CONCLUSION

A modular multilevel dc–dc converter was presented in which a high step-ratio was achieved by a combination of inherent half-bridge ratio, SM stack modulation, and transformer turn ratio, thereby giving a degree of design and operation flexibility. The converter has good potential for operation as a dc tap or as a dc transformer for future dc grids.

The topology on the high-voltage side was the half-bridge single-phase inverter with stacks of SMs in each of the switch positions to withstand the high-side voltage stress. The high-voltage side processed all the power by only two SM stacks, so the total volume required by stack isolation can be kept low. Compactness was further advanced by using the near-square-wave current operation, which has been shown to yield a low SM capacitance size, further aided by operation in the medium-frequency range. The near-square-wave current operation meant instantaneous power flow was near constant even for a single phase such that the dc smoothing capacitors can be small compared to sinusoidal operation.

A set of control loops and an energy balancer were presented. Rapid current reversal was aided by providing control headroom in the form of additional SM over those required for the steady state. It was shown that soft switching of the diodes or switches in the low-voltage side was possible. The theoretical analysis was verified against simulations of a full-scale (40 MW, 200 kV)

example and further verified against experiments on a down-scaled (4.5 kW, 1.5 kV) prototype.

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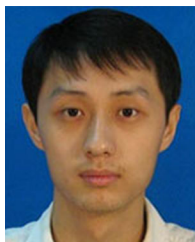
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Xin Xiang (S'17) received the B.Sc. degree in electrical engineering from Harbin Institute of Technology, China in 2011 and the M.Sc. degree in electrical engineering from Zhejiang University, China in 2014. He is currently working toward the Ph.D. degree in Imperial College London, U.K. under the supervision of Prof. Tim C. Green.

His research interests include the design and control of high-power converters for high-voltage transmission technologies and medium-voltage distribution applications.

Xiaotian Zhang (S'11–M'12) was born in Xi'an, China, in 1983. He received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2006 and 2009, respectively, and the Ph.D. degree (with Hons.) in electrical engineering and electronics from the University of Liverpool, Liverpool, U.K., in 2012.

Until 2015, he was with the Department of Electrical Engineering, Imperial College London, London, U.K. He is currently an Associate Professor with the Department of Electrical Engineering, Xi'an Jiaotong University. His research interests include control and design of high-voltage direct current converters.

Thomas Luth received the M.Eng. (first class Hons.) and Ph.D. degrees from Imperial College London, London, U.K., in 2010 and 2014, respectively, both in electrical and electronic engineering.

His work currently focuses on dc/dc converters for high-voltage direct current applications. His research interests include power electronics and transmission technologies.

Michael M. C. Merlin (M'12) received the Electrical Engineering degree from the Ecole National Superieur de l'Electronique et de ses Applications, Cergy, France, in 2008, and the M.Sc. degree in control systems and the Ph.D. degree in electrical engineering from Imperial College London, London, U.K., in 2008 and 2013, respectively.

He became a Lecturer with the University of Edinburgh, Edinburgh, U.K., in 2017. His main research interests include design, optimization, and control of power converters, more specifically of the modular types that use stacks of sub-modules (SMs) to achieve high-power efficiency and waveform quality.

Timothy C. Green (M'89–SM'02) received the B.Sc. (Eng) (first class Hons.) degree from Imperial College London, London, U.K., in 1986, and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K., in 1990, both in electrical and electronic engineering.

He is a Professor of Electrical Power Engineering with Imperial College London, and the Director of the Energy Futures Lab with a role fostering interdisciplinary energy research. He also leads the HubNet consortium of U.K. universities. In high-voltage direct current, he has contributed converter designs that reduce losses while also providing control functions assist ac system integration. In distribution systems, he has pioneered the use of soft open points and the study of stability of grid-connected inverters. His research interests include using the flexibility of power electronics to accommodate new-generation patterns and new forms of load, such as EV charging, as part of the emerging smart grid.