A Modular Multilevel DC-Link Front-to-Front DC Solid-State Transformer Based on High-Frequency Dual Active Phase Shift for HVDC Grid Integration

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***Abstract*—This paper proposes a modular multilevel dc-link dc solid-state transformer (MADCT) based on high-frequency dual active phase shift for HVDC grid integration. The proposed MADCT employs one arm of modular multilevel converter as HVDC active front-end interface and dual active bridge as high-frequency power transfer link, which brings many advantages and makes the operation of MADCT quiet different with traditional dc transformers. Compared with the traditional dc transformer schemes, the MADCT not only has good modularity and flexibility but also has good fault handling capacity. Especially, the performances of current stress, power transfer capacitor, and efficiency are improved. The topology, operation principle, voltage, current, power performances, and control and parameter design are presented and analyzed comprehensively in this paper. At last, a MADCT prototype is built and the experimental results verify the correctness and effectively of the proposed solution.**

***Index Terms*—DC transformer, dc–dc converter, dual active bridge (DAB), high-frequency conversion, high-voltage dc (HVDC), multilevel modular converter (MMC), solid-state transformer.**

I. Introduction

HIGH-VOLTAGE dc (HVDC) technology has great application prospect in the grid integration of megawatt-range wind and solar energy. With the rapidly development of HVDC systems [1]–[3], there is an urgent need to connect different HVDC systems directly. DC solid-state transformer (DCT) is a key component to achieve voltage conversion, power transfer, and electrical isolation of HVDC systems [4], [5].

Because the electromagnetic induction principle cannot be employed directly in dc system, in order to increase the voltage and power capacity of DCT, multiple topology based on dc–dc converter (abbreviated as ADCT in this paper) is the most popular research scheme for DCT to access HVDC system [6]–[9]. In particular, because dual active bridge (DAB) has the advantages of ease of realizing soft switching, bidirectional power transfer capability, and modular and symmetric structure, it is widely employed as a core cell for DCT [10], [11]. However, in HVDC system-level application, because of the concentrated dc capacitor in DCT based on DAB, there will be a large overcurrent when a fault occurs in HVDC grid [12], so an additional dc breaker should be added to cut off the connection between different HVDC systems [13]–[15]. In addition, the redundant unit cannot be added, otherwise the dc capacitor will be short-circuited, so the DCT must stop working when a submodule (SM) fails, which decreases reliability of the system, especially there are hundreds of cells in the HVDC application. Moreover, for DAB, there is a large circulating current when the terminal voltages do not match the turn ratio of the transformer, then the current impact will be high and the efficiency will be low [16], [17].

To increase the reliability of DCT based on DAB, a DCT scheme based on switched capacitor is proposed in [18], which can disconnect from the dc grid effectively as a dc breaker when a short fault occurs, and the redundancy design can be achieved when some SM fail. However, the proposed scheme can just apply to MVDC and LVDC gird, especially the fault handling of LVDC grid is also not available. Moreover, the switched capacitor is just designed to bilevel operation state, which causes the increase of current fluctuation and power loss.

In order to increase the voltage and power level of DCT based on DAB, there is a research trend to employ modular multilevel converter (MMC) as a dc–dc transformer (abbreviated as MDCT in this paper) for the interconnection of different HVDC systems [19]–[24]. However, the number of switches is increased with two times, which increases the cost and volume greatly in practice. In addition, there is just an independent transformer with high frequency, high voltage, and high power, which increase the manufacturing difficulty and limit the power capacity of DCT for HVDC application.

In view of the situation mentioned above, this paper proposes a novel modular multilevel dc-link DCT scheme (abbreviated as MADCT). The topology, operation principle, the performances of voltage, current, power, and the control and parameter design will be presented and analyzed.

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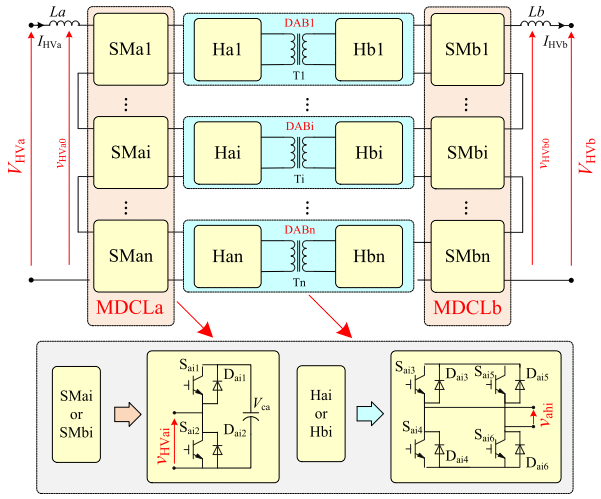

Fig. 1. Topology of the proposed MADCT for HVDC grid integration.

II. Topology of the Proposed MADCT

The topology of the proposed MADCT is shown in Fig. 1. Compared with ADCT, the MADCT employs half-bridge SM, which is basic cell in MMC, as HVDC interface, the dc side of the SM is connected with DAB, and the ac sides of n SMs are connected in series to access the HVDC bus, the structure just like one arm of MMC. However, compared with MDCT, the MADCT still employs the DAB structure as a basic cell, the system is composed of n DAB cells, both dc sides of DAB are connected to dc sides of SMs.

Then, compared with ADCT, the MADCT not only has the same modularity and flexibility but also has better fault handling capacity. Due to the employ of SM, the concentrated dc capacitor of ADCT is eliminated in MADCT and is distributed into discrete dc link of each SM, which means that the dc capacitor is not connected with the HVDC grid directly, then the MADCT can operate well when some SMs fail, the dc capacitor will not be short-circuited and there is no inrush current; in addition, the MADCT can work as a dc breaker, we just need to lock driving pulses when there is a dc fault in HVDC grid, then the connection can be disconnected. The disadvantages for MADCT are that the conversion of SMs increases the power losses of the system. However, for DAB, the power loss will be increased greatly when the terminal voltages do not match with the turn ratio of the transformer, the ADCT does not have the terminal voltage adjust ability of DAB, but the SMs provide the adjust ability for MADCT, so the MADCT just has a little lower efficiency in maximum point (matching point), the average efficiency of MADCT is still higher than that of ADCT. Compared with MDCT, the MADCT not only has the same fault handling capacity, but also has fewer switches, higher modularity, and simpler control and installation.

III. Operation Principle of the Proposed MADCT

Because the MADCT has the symmetrical structure, the operation states for the circuits in HVa and HVb sides are the same, so we mainly give the analysis in HVa side.

A. Multilevel-DC-Link (MDCL) Operation of SMs in MADCT

Similar with multilevel operation of SM in MDCT, the MDCL in MADCT also operates with multilevel principle, as shown in Fig. 2. The switches S_{i1} and S_{i2} are still switched alternately to generate two-level voltage, there is a phase-shift angle between all the two-level voltages of SMs, which are accumulated to access the HVDC bus. The difference is that the duty ratio of SM in MADCT is not 50%, which is changed according to the control requirements of terminal voltage of DAB. In addition, the aim of phase shift is not to approximate sine wave, but to increase operation frequency and decrease ripple current, so the phase-shift angle between neighboring SMs is designed with a constant value $2\pi/n$.

From Fig. 2(a), for a constant duty ratio D_a, the series voltage of all the SMs is just two level with the changing time. However, with the changing duty ratio D_a, the series voltage V_{HVa0} changes with 0, $V_{\rm ca}$, $2V_{\rm ca}, \ldots, nV_{\rm ca}$, as shown in Fig. 2(b). From the analysis above, the multilevel characteristic of a dc link for MADCT is reflected not in time domain but in duty-ratio domain.

B. High-Frequency-Link Operation of DABs in MADCT

Similar with dual-active phase-shift operation of DAB in ADCT, the DAB in MADCT also operates with dual-active phase-shift principle, as shown in Fig. 2(c). Each H-bridges generates 50% high-frequency (HF) square wave, each DAB can be equivalent to two HF square waves $v_{\rm hai}$ and $v_{\rm hbi}$ connected with an inductor. Then, the magnitude and direction of power flow can be adjusted by controlling the magnitude and direction of a phase-shift angle between two HF waves.

However, different with DAB in ADCT, the DAB in MADCT always operates in matching state because of the voltage adjustment ability of MDCL, so the high-frequency-link (HFL) current $i_{\rm Li}$ always keeps constant during $t_0 - t_1$, which is very important for the operation of MADCT in HVDC application. In fact, this quality can greatly decrease the current stress and power loss of the system.

IV. MDCL Performance of the Proposed MADCT

A. MDCL Voltage

In MADCT, the voltage adjustment function is implemented by MDCL. Assuming that the voltage of the capacitor is balanced and equal to $V_{\rm ca}$, from the analysis in Section III-A, when $i/n \le D_a < (i+1)/n$, we have

$$V_{\rm HVa0} = \begin{cases} (n-i-1)V_{\rm ca} & 0 \le t \le \left(D_a - \frac{i}{n}\right)T \\ (n-i)V_{\rm ca} & \left(D_a - \frac{i}{n}\right) \le t \le \frac{T}{n} \end{cases} \quad (1)$$

where $T = 1/f_M$ is the switching period of SM, f_M is the switching frequency, and i is a normal integer to help describing the piecewise function $0 \le i \le n-1$.

From (1), the average voltage of an inductor L_a can be derived as

$$V_{\rm La} = \frac{n}{T}\int_0^{T/n} v_{\rm La}dt = n\left[\frac{V_{\rm HVa}}{n} - V_{\rm ca}(1-D_a)\right]. \quad (2)$$

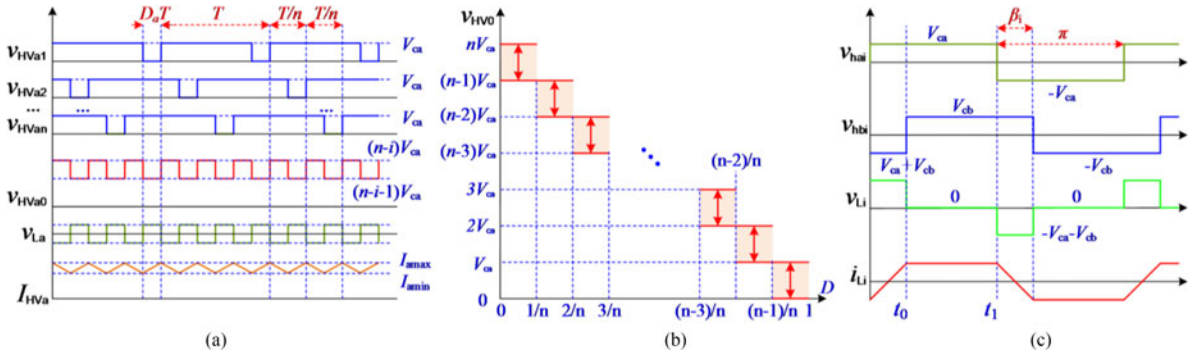

Fig. 2. Operation principle of the proposed MADCT. (a) MDCL operation. (b) Multilevel characteristics. (c) HFL operation.

In steady state, the average voltage of an inductor during one period is zero. Then, we have

$$V_{\rm ca} = \frac{V_{\rm HVa}}{n(1-D_a)} \text{ and } V_{\rm cb} = \frac{V_{\rm HVb}}{n(1-D_b)}. \tag{3}$$

From (3), the discrete voltage of a capacitor can be adjusted by controlling duty ratio D_a and D_b.

In fact, in MADCT, the voltage adjustment aim of MDCL is to ensure the DAB to operate with matching state, that is,

$$n_T = \frac{V_{\rm ca}}{V_{\rm cb}} = \frac{V_{\rm HVa}(1-D_b)}{V_{\rm HVb}(1-D_a)} \tag{4}$$

where n_T is the transformer turn ratio. To simplify analysis, we define $V_{\rm cb}$ and $V_{\rm HVb}$ are equivalent values form secondary side to primary side of the transformer, then we can use symbols $V_{\rm cb}$ and $V_{\rm HVb}$ to present $n_T V_{\rm cb}$ and $n_T V_{\rm HVb}$ in mathematical equation in this paper.

In practice, the HVDC voltage will fluctuate. Because the MDCL just can boost the voltage, in order to ensure the DAB operating in matching state during all the situations, the rated voltage of DAB is designed based on the maximum fluctuation of HVDC voltage. In this paper, the maximum fluctuation is assumed as 20% to analyze. In fact, in HVDC application, to ensure a high power quality, the allowable fluctuation range of HVDC voltage is not high, which maybe below 20%, then the rated voltage of DAB can be designed according to the practical system. Then, in order to decrease current fluctuation and voltage stress, we have

$$\frac{V_{\rm HVa}}{n(1-D_a)} = V_{\rm caN} = \frac{(1+\lambda_{\max})V_{\rm HVaN}}{n} \tag{5}$$

where $\lambda_{\max}$ is the maximum fluctuation rate of HVDC grid, and $V_{\rm HVaN}$ and $V_{\rm caN}$ are the rated voltages of HVDC grid and DAB, respectively.

The maximum value of duty ratio will be achieved when the HVDC voltage get minimum value. If considering maximum fluctuation rate 20%, the minimum value of HVDC voltage is 80% $V_{\rm HVaN}$, then from (5), we have

$$0 \le D_a \le 1/3. \tag{6}$$

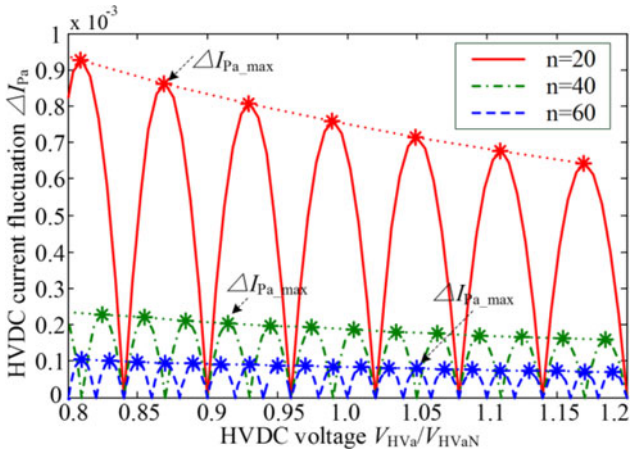

Fig. 3. HVDC current fluctuation of the proposed MADCT varied with HVDC voltage.

B. MDCL Current

From Fig. 2, with the same switching frequency, the fluctuation frequency of a dc-link voltage $V_{\rm HVa0}$ is increased with n times, then the fluctuation frequency of a dc-link current $I_{\rm HVa}$ is also increased with n times, which will has good effect to decrease the current fluctuation.

From (1), the MDCL current can be derived as

$$I_{\rm HVa} = \begin{cases} I_{a\min} + \frac{V_{\rm HVa}-(n-i-1)V_{\rm ca}}{L_a}t, & 0 \le t \le \left(D_a - \frac{i}{n}\right)T \\ I_{a\max} + \frac{V_{\rm HVa}-(n-i)V_{\rm ca}}{L_a}t, & \left(D_a - \frac{i}{n}\right)T \le t \le \frac{T}{n} \end{cases}. \tag{7}$$

The dc-link current fluctuation $\triangle I_{\rm pa}$ can be derived as

$$\begin{aligned} \Delta I_{\rm pa} &= I_{a\max} - I_{a\min} = -\frac{[V_{\rm HVa} - (n-i)V_{\rm ca}]}{L_a} \\ &\quad \times \left(\frac{i+1}{n} - D_a\right)T \\ &= \frac{V_{\rm HVa}T}{L_a}\left[\frac{(nD_a - i)(i+1-nD_a)}{n^2(1-D_a)}\right] \\ &\quad \times \frac{i}{n} \le D_a \le \frac{i+1}{n}. \end{aligned} \tag{8}$$

Fig. 3 gives curves of current fluctuation varied with the HVDC voltage. It can be seen that the current fluctuation varies

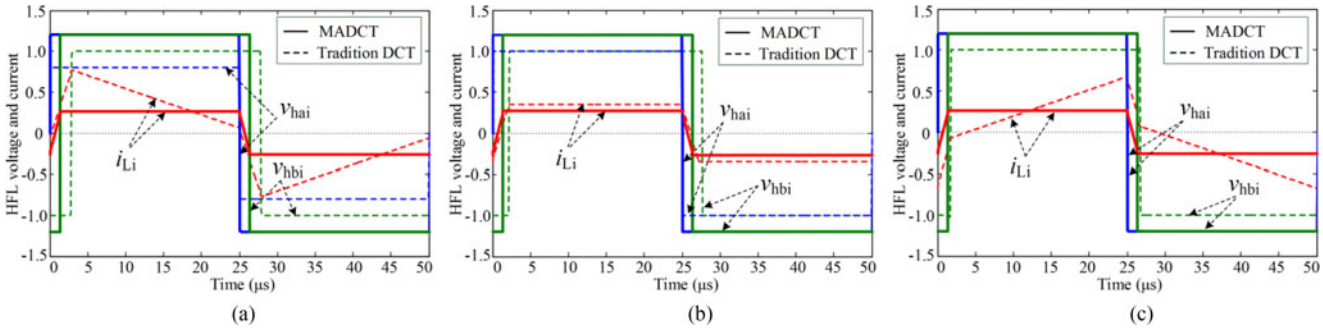

Fig. 4. HFL voltage and current peformance of the proposed MADCT. (a) $V_{\mathrm{HVa}}/V_{\mathrm{HVaN}} = 0.8$. (b) $V_{\mathrm{HVa}}/V_{\mathrm{HVaN}} = 1$. (c) $V_{\mathrm{HVa}}/V_{\mathrm{HVaN}} = 1.2$.

with different sections of a HVDC voltage. If the change is transferred to D_a, the section length is $1/n$, and the current fluctuation is zero where $D_a = i/n$. The maximum current fluctuation decreases greatly with the increase of the cell number n. In Fig. 3, the current fluctuation $\triangle I_{\mathrm{pa}}$ is normalized with $V_{\mathrm{HVa}}T/L_a$.

In fact, from (8), the maximum current fluctuation during each section can be derived as

$$\Delta I_{Pa\_\max} = \frac{V_{\mathrm{HVa}}T}{L_a}\frac{1}{2n(2n-2i-1)} \tag{9}$$

where

$$D_a = \frac{i}{n} + \frac{n-i}{n(2n-2i-1)}. \tag{10}$$

If (6) is taken into account, from (9), we have

$$\Delta I_{Pa\_\max} \le \frac{3V_{\mathrm{HVa}}T}{2n(4n-3)L_a}. \tag{11}$$

For HVDC application, the voltage is hundreds of kilovolt, the number of SMs will be hundreds, the equivalent frequency of a dc-link current is very high, the fluctuation will very low. In fact, different with high switching frequency of DAB, the switching frequency of SMs can be lower, which just needs to ensure the current fluctuation within the scope of the requirements.

V. HFL Performance of the Proposed MADCT

A. HFL Voltage and Current Performance

From the analysis in Section III, the HFL in MADCT still employs square-wave modulation, which has maximum utilization. From [16], the HFL voltage can be derived based on the Fourier series

$$\begin{cases} v_{\mathrm{hai}} = \sum\limits_{k=1,3,5,\ldots} \frac{4V_{\mathrm{HVa}}}{kn\pi(1-D_a)}\sin(kw_0t) \\ v_{\mathrm{hbi}} = \sum\limits_{k=1,3,5,\ldots} \frac{4V_{\mathrm{HVb}}}{kn\pi(1-D_b)}\sin[k(w_0t-\beta_i)] \end{cases}. \tag{12}$$

Then, the HFL current can be derived as

$$i_{\mathrm{Li}} = \sum_{k=1,3,5,\ldots} \frac{4}{k^2\pi w_0 L_i}\sqrt{A^2+B^2} \times \sin\left(kw_0t + \arctan\frac{A}{B}\right) \tag{13}$$

where

$$\begin{cases} A = \frac{V_{\mathrm{HVb}}}{n(1-D_b)}\cos(k\beta_i) - \frac{V_{\mathrm{HVa}}}{n(1-D_a)} \\ B = \frac{V_{\mathrm{HVb}}}{n(1-D_b)}\sin(k\beta_i). \end{cases} \tag{14}$$

Considering the DAB in MADCT always operates in matching stage, we have

$$i_{\mathrm{Li}} = \sum_{k=1,3,5,\ldots} \frac{4V_{\mathrm{HVa}}\sqrt{2-2\cos(k\beta_i)}}{k^2\pi w_0 n L_i(1-D_a)} \times \sin\left[kw_0t + \arctan\frac{\cos(k\beta_i)-1}{\sin(k\beta_i)}\right]. \tag{15}$$

Fig. 4 gives HFL voltage and current performance for traditional DCT and MADCT with the same transmission power. No matter how the HVDC voltage changes, the terminal voltages of DAB are constants, and the HFL current of MADCT always keep the same. Especially, the current keeps a constant value during the peak point, which decreases the current stress and switching loss of switches. In Fig. 4, the maximum fluctuation rate of HVDC grid is designed to 20%, the voltage in HVa side changes and the voltage in HVb side keeps in rated voltage. v_{hai}, v_{hbi}, and i_{Li} are normalized by V_{HVaN}/n, V_{HVbN}/n, and $V_{\mathrm{HVbN}}/(8nf_sL_i)$, respectively. The switching frequency is 20 kHz.

B. HFL Power Performance

In MADCT, the transmission power is controlled by DABs, which can be derived as

$$P_i = \sum_{k=1,3,5,\ldots} \frac{8V_{\mathrm{caN}}V_{\mathrm{cbN}}}{k^3\pi^2 w_0 L_i}\sin(k\beta_i) \tag{16}$$

where $w_0 = 2\pi f_s$ is the angular frequency, f_s is the switching frequency, L_i is the HFL inductance, β_i is the phase shift angle between v_{hai} and v_{hbi}.

Assuming the phase-shift angles and HFL inductance of all the DABs are the same, we have

$$P_{\mathrm{MADCT}} = \sum_{k=1,3,5,\ldots} \frac{8V_{\mathrm{HVa}}V_{\mathrm{HVb}}}{k^3\pi^2 w_0 L(1-D_a)(1-D_b)}\sin(k\beta) \tag{17}$$

where $L = nL_i$ is the whole HFL equivalent inductance.

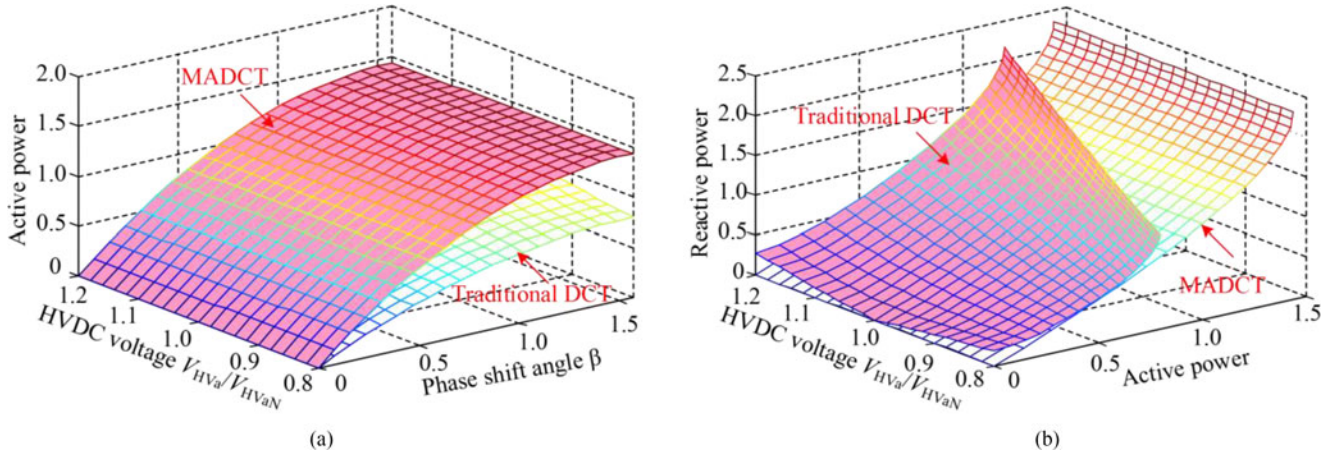

Fig. 5. HFL power performance of the proposed MADCT. (a) Active power. (b) Reactive power.

The HFL reactive power of DAB can be derived as

$$Q_i = \sqrt{S_i^2 - P_i^2} = \sqrt{(V_{\rm hai} I_{\rm Li})^2 - P_i^2} \tag{18}$$

where S_i is the apparent power, and $V_{\rm hai}$ and $I_{\rm Li}$ are RMS values of $v_{\rm hai}$ and $i_{\rm Li}$, respectively.

Similar with active power, the reactive power of MADCT is defined as the reactive power sum of all the DABs in this paper, then we have

$$Q_{\rm MADCT} = \sum_{i=1}^{n} Q_i = \sqrt{(nV_{ha} I_L)^2 - P_{\rm MADCT}^2} \tag{19}$$

where

$$\begin{cases} V_{ha} = \sqrt{\sum\limits_{k=1,3,5,\ldots} \left[\frac{2\sqrt{2}V_{\rm HVa}}{kn\pi(1-D_a)}\right]^2} \\ I_L = \sqrt{\sum\limits_{k=1,3,5,\ldots} \left[\frac{4V_{\rm HVa}\sqrt{1-\cos(k\beta)}}{k^2\pi w_0 L(1-D_a)}\right]^2} \end{cases}. \tag{20}$$

Fig. 5 gives HFL power performance of MADCT. It can be seen that the MADCT has higher active power transmission ability than the traditional DCTs because of the voltage adjust ability of MDCL. With the same active power, the reactive power of MADCT is also less than that of the traditional DCTs. In fact, a higher HFL reaction power will cause a higher RMS current, then the conduction loss will be increased. In Fig. 5, the power is normalized as

$$P_{N\_\max} = \frac{V_{\rm HVaN} V_{\rm HVbN}}{8 f_s L}. \tag{21}$$

VI. Switching Performance of the Proposed MADCT

As analyzed above, no matter how the HVDC voltage changes, the DABs in MADCT always operate in matching state, and all the cells have the same switching behaviors, as shown in Fig. 6(a). It can be seen that all the switches turn on with zero voltage switching (ZVS), all the diodes turn off with zero current switching, which has good effect on the efficiency of MADCT.

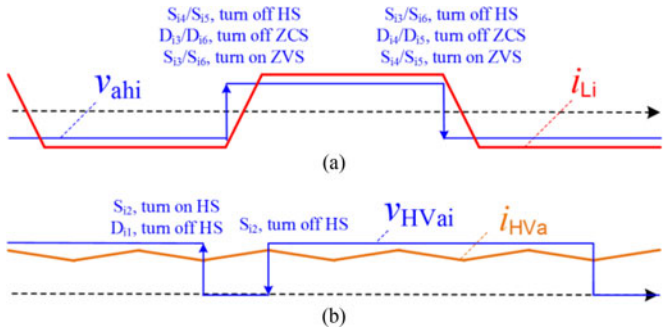

Fig. 6. Switching performance of the proposed MADCT. (a) DAB cell. (b) SM cell.

In fact, for traditional DCTs, the ZVS turn on behaviors will change to hard switching behaviors when the terminal voltage changes, which is the main defect in practice.

For MDCL, the switching behaviors of SMs are shown in Fig. 6(b). Because the dc-link currents have different directions for SMs in HV*a* and HV*b* sides, the switching behaviors of up and down switches in SMs are exchanged. However, for all the SMs, there are mainly one turn-on and one turn-off behaviors of switches, and one turn off of diode.

In addition, all the switching behaviors of SMs in HV*a* and HV*b* sides are hard switching. However, because the SMs in MADCT do not need to operate with HFL modulation, so the switching frequency can be small.

According to the analysis above, the MADCT have better soft-switching performance than traditional DCTs.

VII. Control Design of the Proposed MADCT

Fig. 7 gives a practical control design of the proposed MADCT. The discrete voltage of dc capacitors are controlled by MDCL, the power of MADCT is controlled by HFL. In MDCL control, MDCL*a* and MDCL*b* have the same control methods, which are similar to the control in [18]. However, the driving pulses of SMs should be modulated with phase shift.

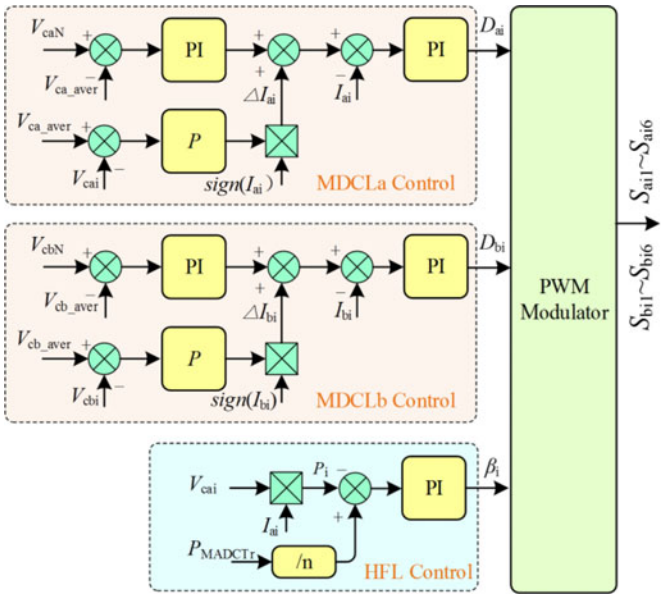

Fig. 7. Control design of the proposed MADCT.

It should be noticed that a voltage balance loop should be provided to ensure correct converter operation. Because the discrete voltage of dc capacitor is changing with the charging and discharging process, the reference value of voltage balance loop should not be a constant. The control objective can be achieved by comparing the individual voltage to the average value of all the discrete voltages. In addition, a proportion adjustment parameter is provided to control the regulating sensitivity. Because the adjustment law is different in different power flow, so the power flow direction needs to be sampled in real time to ensure that the correcting value has different polarity in different power flows, further to ensure the effective operation of the voltage balance loop [18].

In MADCT, because the voltage has been managed by MDCL, so the DAB just need to control the transmission power, where a single closed-loop control is employed. The transmission power reference is given by the superior control system, to ensure power balance, each DAB undertake the same power transfer task. The power loop samples the power of each DAB in real time and compares it with power reference; the proportional–integral controller is used to adjust the phase-shift angle β_i of HFL voltages.

It should be pointed out that all the SM in MADCT operate together to achieve control target. Therefore, there are some common commands and references values from system-level controller should be transferred to each SM (such as reference voltage, power, synchronous single, etc.). However, each SM is still controlled separately by themselves, they do not have the difference of master–slave. The same subcontroller is also applied to embed to each SM, they do not communicate and interact each other. As for phase shift between different modules, we just need to transfer different synchronous single to the SM from system-level controller according to predefined control law in Fig. 2.

In Fig. 7, $V_{ca\_aver} = (V_{ca1} + V_{ca2} + \ldots + V_{can})$ is the average value of all the discrete voltages, I_{ai} is the average value of i_{ai} during one switching period, V_{caN} is the rated reference value of the discrete voltage, and $P_{\mathrm{MADCT}r}$ is the power reference value.

VIII. Parameter Design of the Proposed MADCT

A. Rated Voltage and Current of Switches and Series Number

In practice, the HVDC rated voltage V_{HVaN} and V_{HVbN} are decided directly according to the actual demand. From the analysis in Section IV, in order to decrease current fluctuation and voltage stress, the rated operation voltage of DAB can be designed based on the maximum HVDC operation voltage in practice. Then, the rated voltage of switches in MADCT is

$$V_{\mathrm{SWaN}} = V_{\mathrm{caN}} = \frac{(1+\lambda_{\max})V_{\mathrm{HVaN}}}{n} \tag{22}$$

where V_{SWaN} is the rated operation voltage of switches in HVa sides, respectively.

Then, the rated voltage of switches and the number n of series cell can be designed according to the employed switches. For MADCT, because all the cells are connected in series and the DAB always operates in matching state, in general design, the rated current of all the switches can be designed according to the HVDC current, that is,

$$I_{\mathrm{SWaN}} = I_{HVa\_\max} = \frac{P_{MADCTN}}{(1-\lambda_{\max})V_{\mathrm{HVaN}}}. \tag{23}$$

So in an actual system, the rated voltage and current of switches and series number can be designed by the specific applications easily.

B. MDCL Inductance and Switching Frequency

The dc inductance of MADCT is designed based on the maximum fluctuate current. From the analysis in Section IV, we have

$$f_M L_a \geq \frac{3V_{\mathrm{HVaN}}^2}{2n(4n-3)\varepsilon P_{MADCTN}} \tag{24}$$

where ε is the allowable current fluctuation rate in HVDC side.

In HVDC application, to ensure a high power quality, the allowable current fluctuation rate should be below 5%. From (23), the MDCL inductance and switching frequency can be designed according to the number of SMs and current fluctuation rate. Usually, the number of SMs will be hundreds in HVDC application, the equivalent frequency of a dc-link current is very high, the fluctuation will very low, the MDCL inductance and switching frequency can be designed with small values.

C. HFL Inductance, Switching Frequency, and Transformer Ratio

The design of HFL inductance, switching frequency, and transformer ratio are similar to the design of traditional ADCT. In order to ensure reliable operation, the design of HFL inductance and switching frequency must satisfy that the transmission

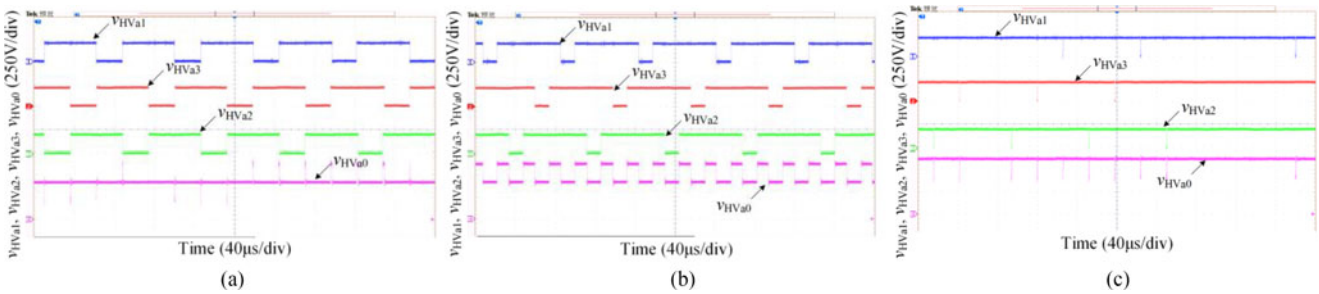

Fig. 8. Experimental waveforms of MDCL with different voltage fluctuation for MADCT. (a) Minimum HVDC voltage. (b) Rated HVDC voltage. (c) Maximum HVDC voltage.

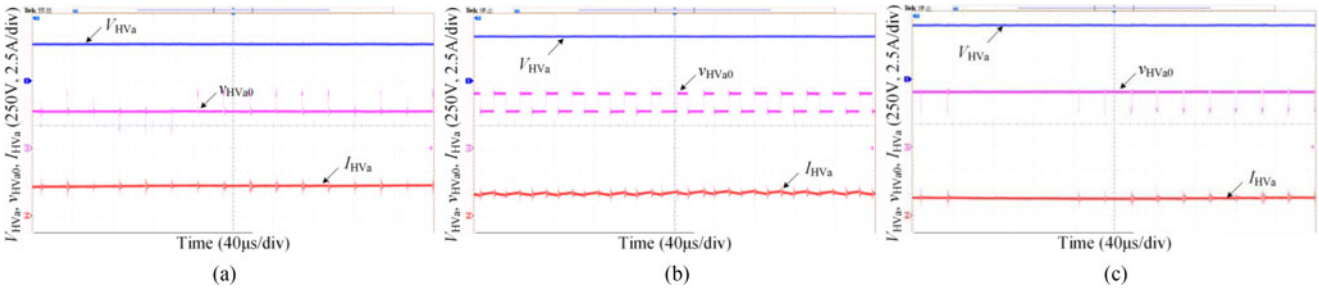

Fig. 9. Experimental waveforms of HVDC voltage and current with different voltage fluctuation for MADCT. (a) Minimum HVDC voltage. (b) Rated HVDC voltage. (c) Maximum HVDC voltage.

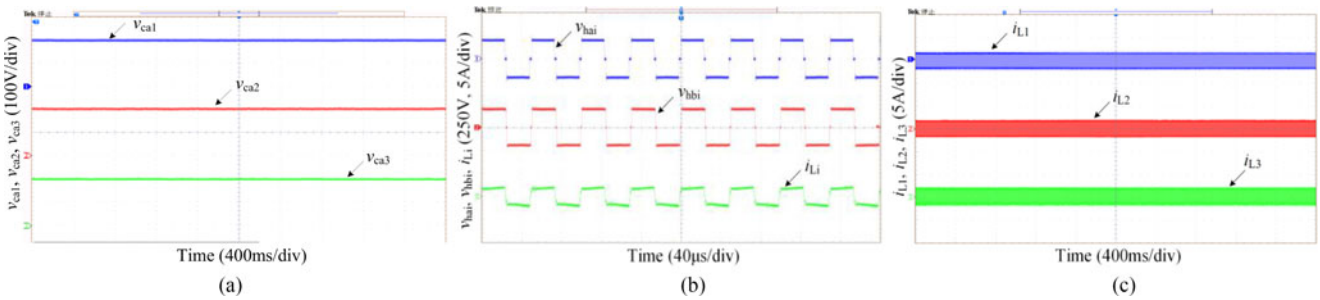

Fig. 10. Experimental waveforms of dc capacitors and HFL for MADCT. (a) Capacitor voltage. (b) HFL voltage and current of one module. (c) HFL currents of all the modules.

power can achieve the rated power of load, so the minimum value of the theoretical maximum power should be larger than the rated power of load. For switching frequency f_s, it is designed according to the power loss and power density. In general design, we can limit it according to the power switches.

In order to decrease circulating current and increase efficiency, the transformer turn ratio n_T should match the voltage conversion ratio of DAB, that is, $n_T = V_{\mathrm{caN}}/V_{\mathrm{cbN}}$. To simplify expressions, we define V_{cb} and V_{HVb} are equivalent voltages in HVa side, thus n_T can be seen as *1* in this paper.

IX. Experimental Analysis

In order to verify the theoretical analysis, a MADCT prototype platform with three cells is built. The rated HVDC voltages $V_{\mathrm{HVaN}} = V_{\mathrm{HVbN}} = 500$ V, the maximum voltage fluctuation rate of HVDC grid is assumed 20%, that is, the HVDC voltage may change from 400 to 600 V, then the rated terminal voltages of DABs $V_{\mathrm{caN}} = V_{\mathrm{cbN}} = 200$ V, the transformer ratio $n_T = 1$, the switching frequency $f_s = 20$ kHz, the HFL inductance is 80 μH.

Fig. 8 shows the experimental waveforms of MDCL with different voltage fluctuation. It can be seen that there is a $2\pi/3$ phase-shift angle exists between adjacent SMs and the MDCL voltage is changed with the change of the HVDC voltage. In Fig. 8(a), the HVDC voltage is 400 V, the MDCL voltage v_{HVa0} is a constant value at 400 V because the duty ratio is 1/3. In Fig. 8(b), the HVDC voltage is 500 V, the MDCL voltage v_{HVa0} changes between 400 and 600 V, because the duty ratio is 1/6. The fluctuation frequency of the dc-link voltage v_{HVa0} is increased thrice. In Fig. 8(c), the HVDC voltage is 600 V, the MDCL voltage v_{HVa0} is a constant value at 600 V because the duty ratio is 0.

Fig. 9 shows the experimental waveforms of HVDC voltage and current with different voltage fluctuation. It can be seen

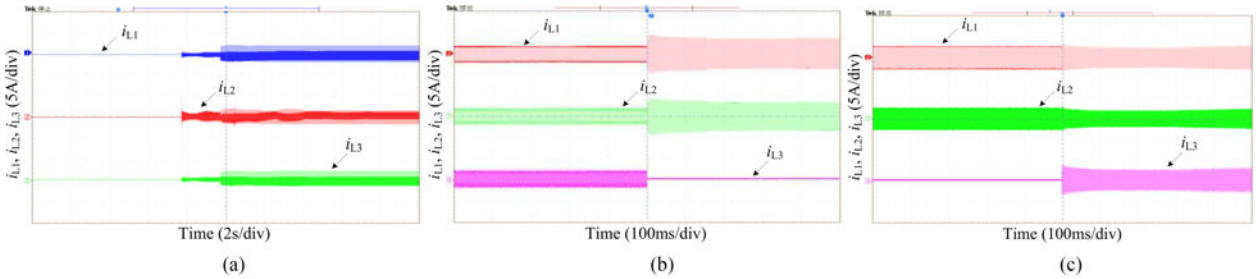

Fig. 11. Transient experimental waveforms for MADCT. (a) Startup process. (b) One module fault process. (c) Fault recovery process.

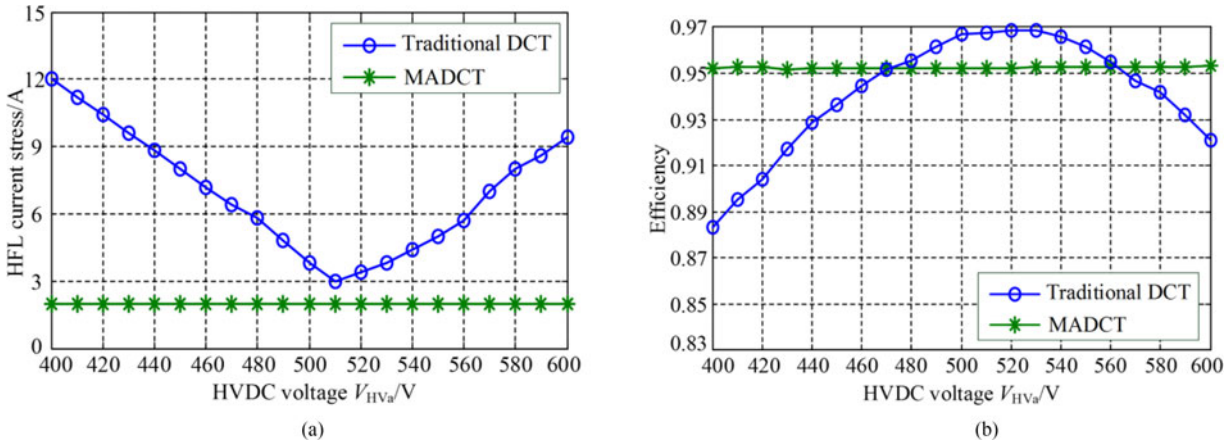

Fig. 12. Experimental results of HFL current stress and efficiency varied with HVDC voltage. (a) HFL current stress. (b) Efficiency.

that the HVDC current changes with the change of the HVDC voltage; however, the current always keep small because the fluctuation frequency of the dc-link current is increased thrice.

Fig. 10 gives the experimental waveforms of dc capacitors and HFL. No matter how the HVDC voltage changes, the dc voltage of capacitors always stay at 200 V, which reflects good voltage-balance effect. In this case, the terminal voltages of the DAB always remain the same; thus, the HFL waveforms are the same for the three preceding situations. Each H-bridge of the DAB generates HF square wave. The HFL current keeps a constant value during the peak point. The current is negative when S_{i3}/S_{i6} turns ON, and the current is positive when S_{i4}/S_{i5} turns ON. All the turn-on behaviors are ZVS. The HFL currents of all the DABs are the same. This observation reflects good power sharing effect.

Fig. 11 shows the transient experimental waveforms for MADCT. It can be seen that the MADCT can startup with small current impact. When one SM fails, the MADCT can switch it out and the system still keeps working. After the fault SM recovers to right, the MADCT can switch it into operation online. The MADCT has good fault handling ability and reliability.

Fig. 12 shows the experimental results of the HFL current stress and efficiency, which vary with HVDC voltage. The HFL current stress of the MADCT remains the same when the HVDC voltage changes because the terminal voltage of DAB is always in matching state. However, this HFL current stress changes for the traditional DCT when the HVDC voltage fluctuates; thus, the current stress of the MADCT is always lower than that in traditional DCTs. Because the conversion of SMs is added to MADCT, so the maximum efficiency of the MADCT is lower than that of the traditional DCT. However, because the power loss will be increased greatly for traditional DCT when the terminal voltages do not match with the turn ratio of the transformer, so the average efficiency of the former is higher than the latter.

X. Conclusion

A novel MADCT scheme was proposed in this paper for HVDC grid integration. The topology, operation principle, performances of voltage, current, power, and control and parameter design method of the proposed MADCT are presented and analyzed. According to the theoretical and experimental results, unlike the traditional DCTs, the MADCT has good modularity and flexibility. The MADCT also has good fault handling capacity. Given the adjust ability of SMs, the MADCT has a high-power transfer capacitor, and the terminal voltages of the DABs always operate in matching state. In particular, the MDCL can be designed to multilevel operation, thereby greatly improving the performances of current stress and efficiency. The MADCT is an effective and practical solution of DCT for HVDC grid integration.

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