Derivation of Voltage Source Multilevel Converter Topologies

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***Abstract*—Multilevel converters have gained popularity in both medium voltage and low voltage applications. To find out the connections between various multilevel voltage-source converter topologies and to reveal how to obtain new topologies, this paper has presented four methods to derive multilevel converter topologies. Many existing topologies as well as new topologies can be derived with the methods presented in this paper. The fundamental characteristics of the multilevel converters which determine their usability such as dc-link neutral point voltage balancing and flying capacitor voltage control are also investigated in this paper with a mathematical model and an example. It is expected that more new topologies will be invented based on the work in this paper for emerging applications.**

***Index Terms*—Flying capacitor, modulation, multilevel converters, neutral point voltage, topologies.**

I. Introduction

MULTILEVEL converters have superior characteristics over the standard two-level converter such as reduced output harmonics, lower dv/dt, and switching loss. They are widely used in high or medium voltage (>3 kV) power conversion systems due to their capability to handle higher voltage and higher power [1]. They are also considered for low-voltage (e.g., 380 V) applications for reducing the output harmonics and filters and improving the system efficiency by reducing the switching losses [2], [3] for a high-density design. Many multilevel converter topologies have been reported in the literature since 1970s [4], [5] yet there are still new topologies coming out, finding applications in emerging areas [6]–[10].

The most popular conventional multilevel topologies which found wide industrial applications include diode neutral point clamped (NPC) converter [11], flying capacitor (FC) converter [12], and cascaded H-bridge (CHB) converter [4], [13]. Meanwhile, active-neutral-point-clamped (ANPC) three [14], five, and seven-level converters [15], three-level T-type converters [3], [16], and multilevel modular converters (MMC) [17]–[19] are gaining more and more research interests recently in emerging application areas such as HVdc, more electric aircraft, and renewable power generation systems. The invention of new converter topologies is highly valued in the power electronics research besides the invention of new power semiconductor devices, e.g., new wide-bandgap material (SiC, GaN) based devices [20]. There are some discussions regarding the value of researching converter topologies given the fact that only several topologies have been widely used among hundreds of available topologies [21]. It is the author's view that it is still very valuable to investigate and invent new topologies. Although some topologies may not find wide application today, it may gain popularity when new application emerges. For example, the three-level T-type converter has been proposed for almost 40 years now [16]. It is only recently that it draws great attention due to its advantage for low-voltage applications with low output harmonics, simpler structure, and the potential for a high-density system, e.g., in solar power generation systems [3], [22].

There are always research questions such as where the new topologies come from, whether there are fundamental common building blocks in multilevel converters, whether there is a generic multilevel converter from which all or most multilevel converters can be derived or there is a common way to form various multilevel converters. This paper therefore attempts to answer the above questions based on the work in [23]–[27]. It has been found out though it is not possible to derive all the topologies from a single unified topology, there are several generic topologies and building blocks that can be used to derive many topologies. This is important because this makes the invention of the new topologies not a random thing, but more predictable and derivable. As will be seen in this paper, new topologies such as MMC and ANPC can be derived following a set of principles from the generic topology with the presented approach. Furthermore, several new topologies have been derived in this paper based on the proposed principle. The topology derivation process also helps to identify device voltage rating requirement. The critical issues in voltage-source multilevel converters which determine their usability such as dc-link neutral-point voltage balancing capability and FC voltage control capability have also been discussed together with the modulation strategies. This paper does not intend to provide an exhaustive approach for the derivation of all the voltage source multilevel converters. Rather, it provides a basis where further study can be made to improve or expand the approaches, e.g., other unified topologies, etc.

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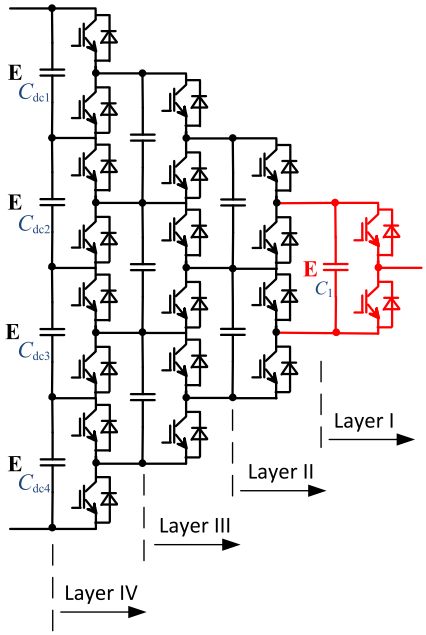

Fig. 1. Generalized topology I.

This paper presents four methods to derive multilevel converters, in the hope that these can inspire researchers to identify more useful topologies, which may find application in emerging areas.

II. Four Converter Topology Derivation Methods

A. Generalized Topology and Derivation Method I

The first generalized topology given here was proposed by Peng [24], in 2001, where two-level converter cells (P2) are connected in a way as shown in Fig. 1 for a phase leg structure. The number of phase output voltage levels depend on the number of layers in the structure. If the number of layers is N, there will be $N + 1$ voltage levels. For example, in Fig. 1, four voltage layers are shown and there are five output voltage levels, i.e., 0, E, 2E, 3E, and 4E. The generalized topology itself can be used directly with dc-link capacitor voltage balancing capability and FC voltage control capability. In this paper, capacitors at the dc-link such as $C_{\rm dc1}$, $C_{\rm dc2}$, $C_{\rm dc3}$, and $C_{\rm dc4}$ shown in Fig. 1 are referred as dc-link capacitors. The capacitors inside the structure such as C_1 are referred as FCs.

Many voltage source multilevel converters can be derived from the generalized structure in Fig. 1. Taking a four-level converter as an example, Fig. 2(a) shows the four-level FC converter [12] that can be seen as a part of the generalized structure in Fig. 1 with the first three layers (I, II, III). Similarly, the symmetric diode clamped four-level converter shown in Fig. 2(b) [28] can be derived from the generalized structure as well. Note that, in multilevel converters, a key aspect to consider when assessing the topologies is the ability to balance the voltage of dc-link capacitors and FCs. For example, the voltage of the FCs in Fig. 2(a) can be well controlled regardless of the load power factor and the modulation index. The topology shown in

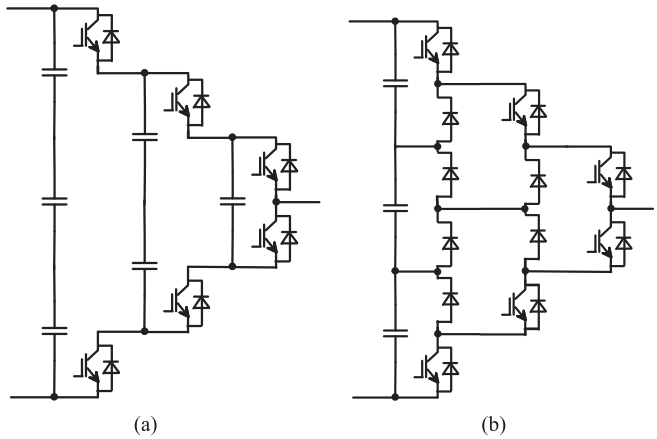

Fig. 2. Two four-level converters derived from the generalized multilevel topology in Fig. 1. (a) FC four-level converter. (b) Symmetric diode-clamped four-level converter.

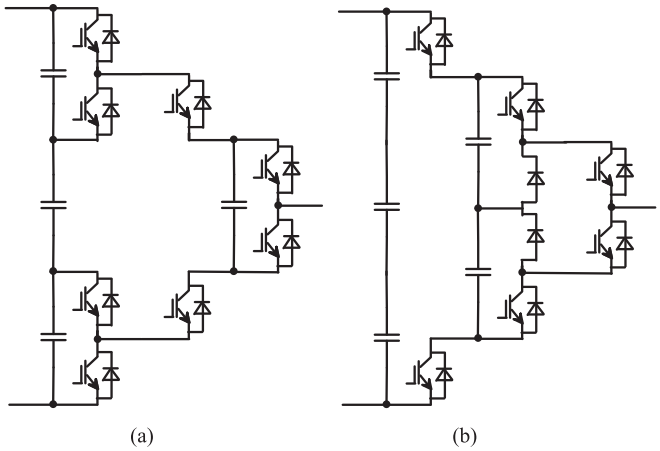

Fig. 3. Two hybrid four-level converters derived from the generalized topology in Fig. 1. (a) Hybrid four-level converter topology in [30]. (b) Nested four-level converter topology [31].

Fig. 2(b), however, cannot maintain the balance of the dc-link capacitor voltages at high modulation indices and high power factors [29]. The method to analyze the converter dc-link capacitor voltage and FC voltage control capability will be given in Section III of this paper.

Fig. 3(a) shows an alternative hybrid four-level converter topology [30] that can be derived from the generalized structure in Fig. 1 as well. This topology uses less number of FCs compared with the FC topology in Fig. 2(a) and has the ability to control the voltages of dc-link neutral points and FCs. Fig. 3(b) shows another four-level converter topology [31] with the ability to balance the neutral point voltage and FC voltage, which can also be seen as part of the generalized topology in Fig. 1. This topology requires more FCs than the structure in Fig. 3(a) but fewer insulated-gate bipolar transistors (IGBTs).

Note that the structures in Figs. 2 and 3 can be further simplified to reduce the number of devices (capacitors, IGBTs), but the circuit may lose the ability to balance the dc-link neutral point voltages or FC voltages. For example, the topology

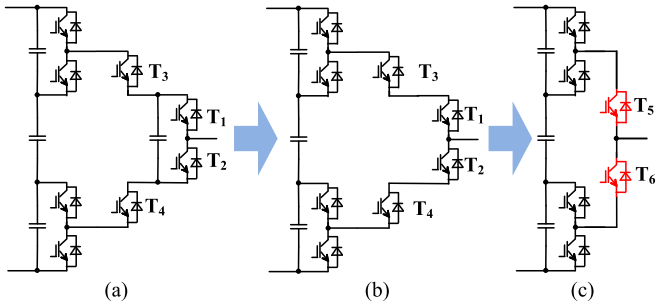

Fig. 4. Simplified four-level converter topology.

in Fig. 3(a) can be further simplified following the process illustrated in Fig. 4. Fig. 4(a) is the same as Fig. 3(a). If the FC of Fig. 3(a) is removed, then the topology becomes Fig. 4(b). Further, given two power devices (T1 and T3 or T2 and T4) are in series, they may be replaced with a single device as T5 and T6 in Fig. 4(c), but T5 and T6 need to be able to withstand twice of the voltage of the rest of devices, i.e., $2/3$ of the dc-link voltage. Fig. 4(c) shows the four-level topology with minimum number of devices (six IGBTs). However, the dc-link neutral point voltages of this structure cannot be balanced with a single inverter or rectifier. The balance of dc-link neutral point voltages can only be achieved with a back-to-back structure [32], [33]. Another advantage to obtain the topology through the derivation process is that it is easy to understand in some topologies why certain devices need to block higher voltages, e.g., T5 and T6 in Fig. 4(c) need to block twice the voltage of other devices because they replaced two devices in series.

Though reference [24] has proposed the generalized structure in Fig. 1, the principle to simplify the generalized structure and derive new topologies has not been given in the reference. This paper summarizes the derivation principles based on the work in [25] as follows.

1) Outermost two devices in each layer must be kept and cannot be removed.
2) There must be at least one bidirectional current path for each voltage level between the dc link and phase output.
3) Elements (power devices, capacitors) within the generalized topology must be removed symmetrically from the upper and lower half of each layer.
4) Switching states and current paths need to be analyzed for any new topology derived to check whether the new topology has the ability to balance the dc-link neutral points' voltages andFC voltages.
5) From the application point view, the FCs in higher layers should be considered to be removed first to reduce the capacitor requirement for an improved power density and reliability.

With the above principles, other converter topologies may be derived. For example, the topology in Fig. 5 [34] can be derived from the generalized topology following the principles and can be seen as an alternative configuration of the popular MMC for HVdc applications [17], [18].

Fig. 6 shows another topology derived from the generalized topology by applying the derivation principles, which is

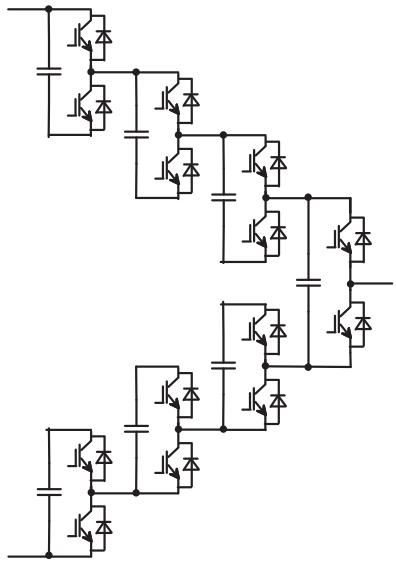

Fig. 5. Alternative MMC configuration [34].

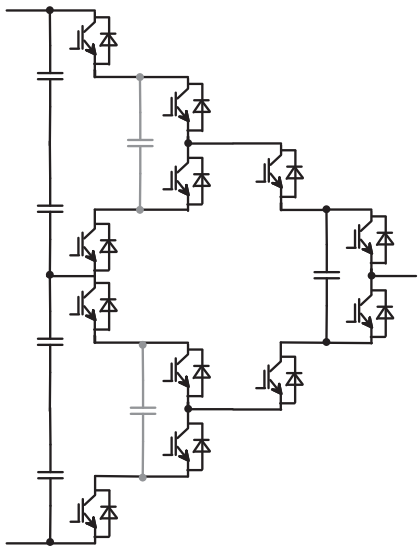

Fig. 6. Five-level ANPC topology.

an emerging and promising configuration for medium voltage drive applications, called five-level ANPC converter [15]. This topology has the dc-link neutral points' voltage and FC voltage control ability and has advantages over the standard five-level diode NPC converter and the FC converter. It does not require clamping diodes as in the diode NPC converter and can overcome the dc-link neutral points' voltage unbalance issue of the five-level diode NPC converter. It also does not need as many FCs as in the FC converter. In Fig. 6, the two capacitors in gray can be kept in the topology to avoid series connection of power devices or they can be removed to enable by using a double voltage rating device to replace the two series-connected power devices and reduce the total number of power devices. Again, through the topology derivation process, it is trivial to identify the voltage rating requirement for power devices at various locations.

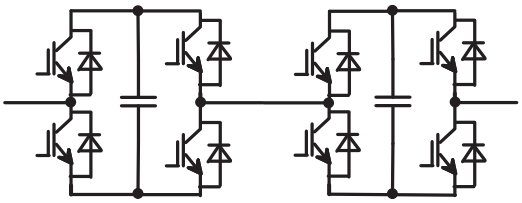

Fig. 7. CHB converter seen as a part of the generalized topology.

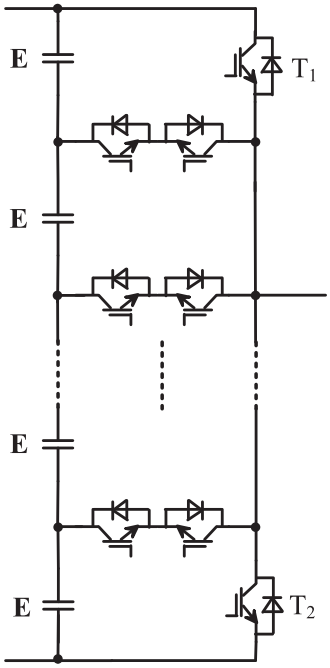

Fig. 8. Generalized topology II.

Fig. 7 shows a five-level CHB converter that may be seen as a part of the generalized topology in Fig. 1. However, in this cascaded structure, the principle No. 1 in the derivation rules does not apply.

There are many other new topologies which may be derived following the derivation principles to fit into various applications based on their characteristics at different number of levels, e.g., five-level, six-level, seven-level, etc. In Fig. 1, the two-level cell is used as the basic building block for the generalized structure. In addition, the three-level FC cell can also be used as the building block as discussed in [24].

B. Generalized Topology and Derivation Method II

The second generalized structure is shown in Fig. 8 [26], where the total dc-link voltage is divided into a number of levels, which are connected to the phase output through bidirectional paths, e.g., by back-to-back connected IGBTs. The structure is very simple and an additional voltage level can be created by adding another bidirectional path. The two main switches T1 and T2 need to remain in the structure for any topology derived and they need to block the whole dc-link voltage. This restricts the application of this kind of converters in medium/high voltage applications due to the constraint of the device voltage rating

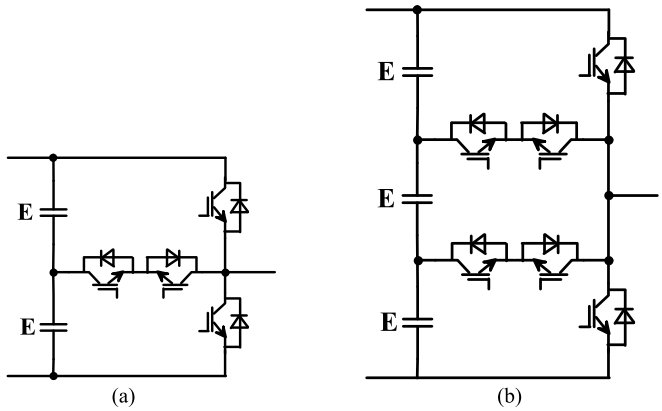

Fig. 9. Two topologies derived from the generalized topology II. (a) Three-level T-type converter. (b) Four-level π-type converter.

unless the series connection of devices is applied. Nevertheless, this topology can gain popularity in low voltage applications, for low output harmonics and lower switching loss due to the fact that the switching voltage is only a portion of the dc-link voltage. This topology requires minimum number of devices to generate a given number of voltage levels. Fig. 9(a) shows a three-level T-type converter topology which can be derived from the generalized topology in Fig. 8. The T-type converter [3], [35] has found applications as an alternative to the three-level diode-NPC converter without the need of clamping diodes. Another example is the four-level π-type converter [36] that can also be derived from the generalized topology. Note that the dc-link neutral point voltages may not be balanced under high modulation indices and high power factors if a single rectifier or inverter is used for the topology in Fig. 9(b), which can be solved with a back-to-back configuration.

C. Topology Derivation Through Parallel or Series Connection of Basic Cells (Method III)

The third method to form multilevel converters is to connect the basic cells in parallel or in series and then simplify the structure by removing certain components. The basic cells (building blocks) can be a two-level converter cell, three-level FC cell, three-level NPC cell, three-level T-type cell, or more complicated cells such as four-level or five-level cells. Note that when selecting the cells, the cell itself should have the ability to balance its own neutral point or flying capacitor voltage. Otherwise, the converter constructed from the cells will lose the neutral point or FC voltage control capability. For example, the four-level diode NPC converter shown in Fig. 2(b) is not a good cell choice given its dc-link capacitor voltages cannot be balanced under high modulation indices and high power factors.

Fig. 10 shows an example, where three FC cells are combined together to form a five-level converter. First, in Fig. 10(a), two three-level FC cells are stacked together and then the output of these two FC converters is connected to a third three-level FC converter. In the next step shown in Fig. 10(b), the two FCs in the left two cells are removed and then the two series-connected FCs (2E) in the right cell are removed. As seen in Fig. 10(b),

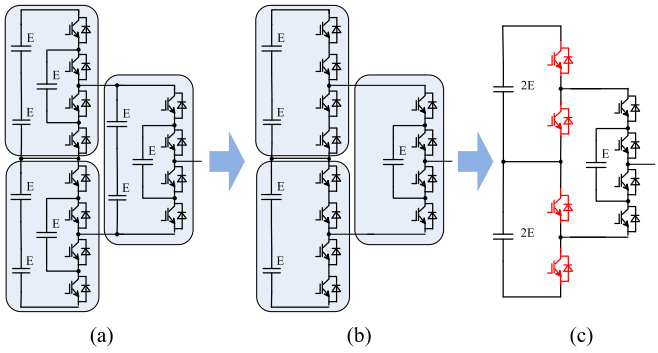

Fig. 10. Derivation of the five-level ANPC converter through combination of basic cells.

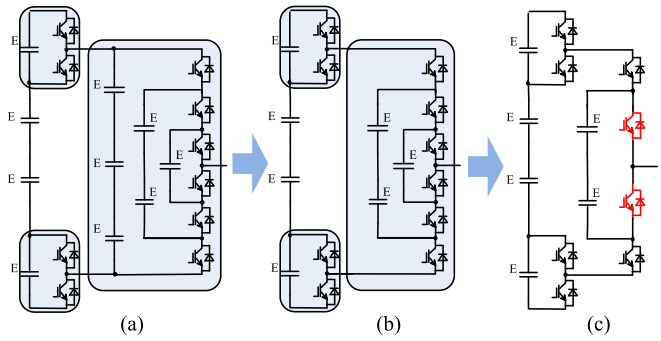

Fig. 11. Alternative five-level converter formed through the combination of basic cells.

there are two power devices in series which can be replaced by a single device with double voltage rating. Then, the circuit can be simplified to the structure in Fig. 10(c), which is the popular five-level ANPC converter. As discussed earlier, this topology can also be derived from the generalized topology I as shown in Fig. 6.

Fig. 11 shows another topology by combing two two-level converter cells with a four-level FC cell. The initial topology is shown in Fig. 11(a), which is then simplified to Fig. 11(b) by removing the 3E FCs in the four-level FC cell. The topology in Fig. 11(b) is able to balance both the dc-link neutral points and the FC voltages by selecting among the redundant switching states and there is no need to connect any power devices in series. The topology in Fig. 11(b) can be further simplified to Fig. 11(c) by removing one more FC (E). The inner two series connected devices may be replaced by a single device with double voltage rating.

Fig. 12(a) shows a new four-level topology by combing two two-level converter cells and a three-level T-type converter. The two devices in the two two-level cells can be further removed to simply the topology as shown in Fig. 12(b). This topology only requires six power devices and two FCs.

Fig. 13 shows the derivation of a seven-level converter by combining three four-level FC cells. Fig. 13(a) shows the complete three four-level FC converters. In Fig. 13(b), the FCs in the left two-cells are removed. Then, if the three series-connected capacitors (3E) in the right cell are removed, the topology can

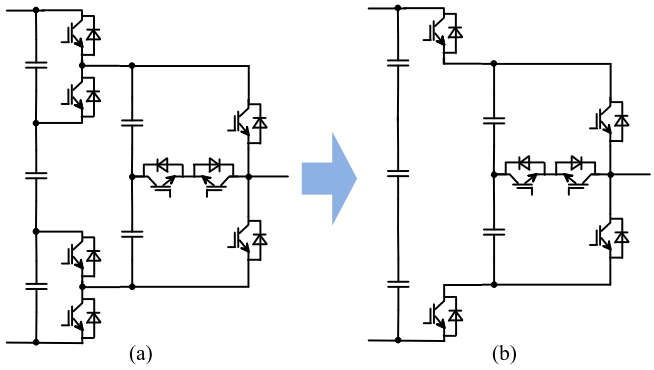

Fig. 12. New topology by the combination of two-level cells and a T-type converter.

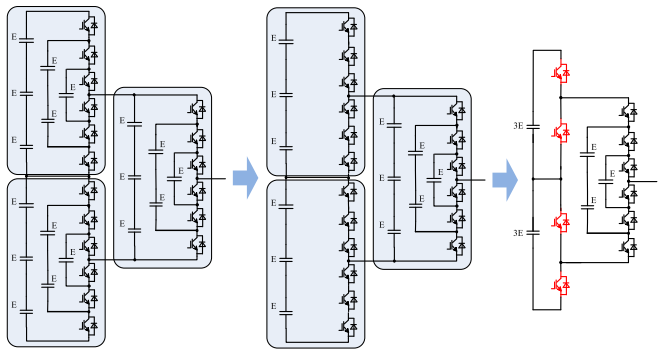

Fig. 13. Combination of three four-level FC cells to derive a seven-level converter.

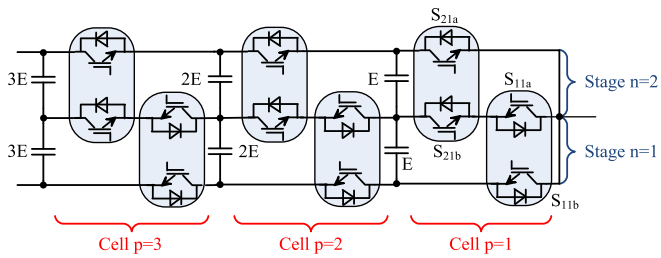

Fig. 14. Generalized structure (SMC).

be simplified to the one shown in Fig. 13(c). Note that the three series-connected devices in the left cells may be replaced with a single device of triple voltage rating (3E). The topology is the same as the ANPC seven-level topology proposed in [15] and has the neutral point voltage and FC voltage control capability.

D. Generalized Topology and Derivation Method IV

Another generalized structure is shown in Fig. 14, which is called stacked multicell converter (SMC) [27], [37]. The topology is formed by a series and parallel connection of the basic cell (e.g., S21a and S21b) as illustrated. Multiple stages and/or multiple cells can be stacked together. In each cell, the two devices (e.g., S21a and S21b) switch complementarily. Also, note that the outer devices (e.g., S21a and S11b) need to block twice the voltage of the inner ones (e.g., S21b and S11a).

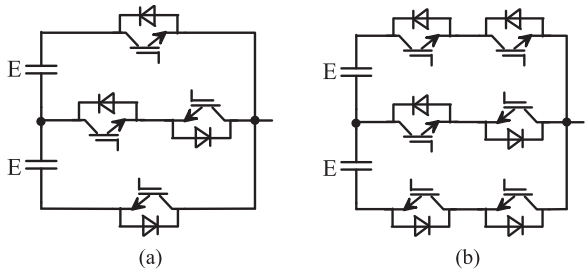

Fig. 15. T-type converter derived with two stages and one cell.

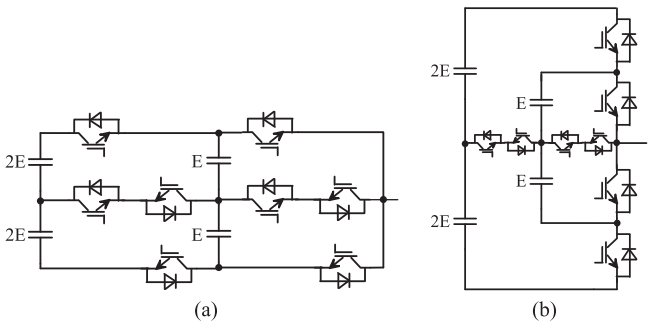

Fig. 16. Five-level topology derived with the generalized topology in Fig. 14.

From this generalized topology, several topologies can be derived. For example, with two stages and one cell, the T-type converter can be derived in Fig. 15(a). Given that the outer two-devices need to block twice of the voltage that the inner devices need to block, they can be replaced by two series-connected devices as shown in Fig. 15(b).

With two stages and two cells, a five-level topology can be derived as shown in Fig. 16(a) with only eight power devices and two-FCs [38]. The topology in Fig. 16(a) can also be seen as two three-level T-type converters cascaded together horizontally. Fig. 16(b) shows an alternative drawing of the topology in Fig. 16(a).

The SMC cell can also be combined with other topology cells. For example, Fig. 17(a) shows a two-stage one cell SMC (T-type) converter followed by a three-level FC cell, forming a new five-level converter. Similarly, Fig. 17(b) shows a two-stage one cell (T-type) converter followed by a three-level diode NPC converter forming a five-level converter.

It can also be noted that the generalized structure in Fig. 8 can also be seen as a one-cell multistage SMC. The multilevel FC converter can be seen as a one stage multicell SMC.

E. Other Topology Derivation Methods

From the above four methods, many of the voltage source multilevel converter topologies can be derived, though there are other methods that may lead to new topologies. For example, with the five-level ANPC topology in Fig. 10(c), by analyzing the current flow paths, the two devices T1 and T2 may be grouped together to form a new current flow path as shown in Fig. 18(b) [39]. T1 and T2 as well as T3 and T4 create a bidirectional current flow path. They can also be replaced with

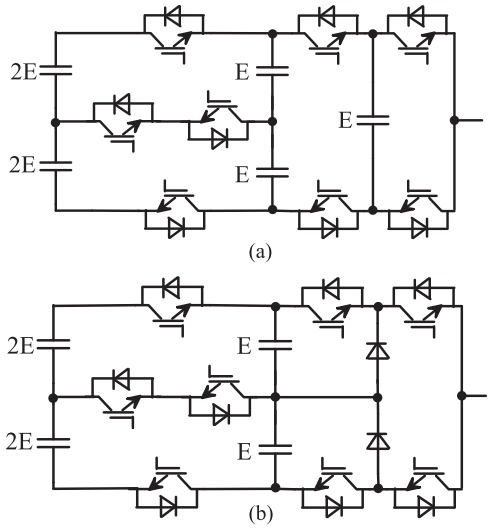

Fig. 17. Two five-level topologies.

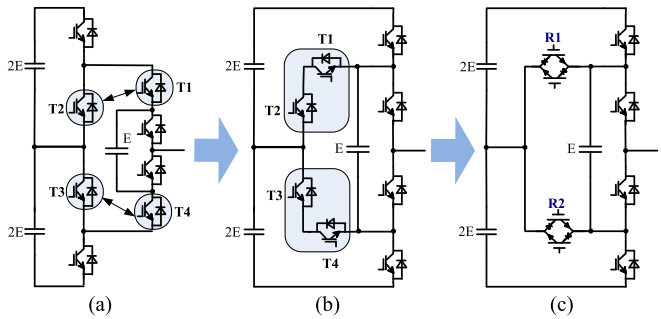

Fig. 18. Alternative five-level converter.

reverse-blocking IGBTs as shown in Fig. 18(c) to simplify the structure and reduce the conduction losses.

III. Neutral Point Voltage Balancing Ability and FC Voltage Control Ability

Though many new topologies may be derived to fit for various purposes, two fundamental properties must be maintained when simplifying the topology, i.e., the ability to balance the dc-link neutral points' voltages and to control the FC voltages. This governs whether the topology may be further simplified, e.g., removing some further power devices, diodes, FCs, etc. Though modulation and control techniques may help to attenuate the neutral point voltage ripple or FC voltage ripple, the following fundamental power balance rules must be met. Otherwise, no matter how advanced the modulation and control methods are the neutral point voltage or FC voltage may lose the balance.

A. DC-Link Neutral Point Voltage Balance

The key thing to check for the neutral point voltage balance is whether the current flowing into the neutral point(s) (charge) equals to the current flowing out of the neutral point (s) (discharge) within one fundamental cycle (e.g., 50 Hz) [40]. Taking the five-level ANPC topology shown in Fig. 10(c) as an

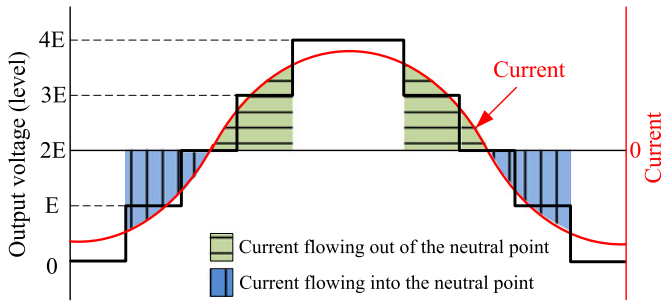

Fig. 19. Method to analyze the dc-link neutral point voltage balancing ability.

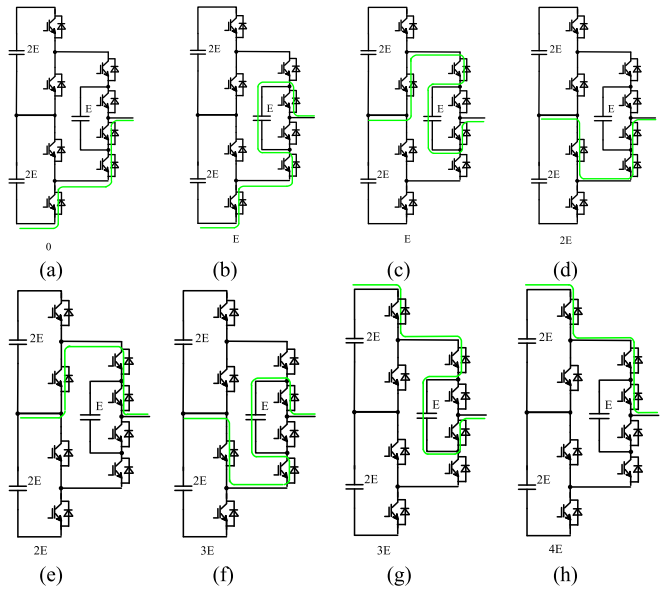

Fig. 20. Output voltage level and current flow paths for the five-level ANPC.

example, there are five output voltage levels: 0, E, 2E, 3E, and 4E as shown in Fig. 19. Though the actual converter output voltage will be in the form of modulated pulses, here staircase waveforms are used to simplify the analysis. The load current is assumed to be sinusoidal and in phase with the voltage, i.e., the unity power factor. Note that the unity power factor is the worst-case scenario and only this case needs to be checked. If the neutral point charge balance can be achieved for the unity power factor, it can also be achieved for other power factors.

Fig. 20 shows the output voltage level and the corresponding current flow paths for the five-level ANPC. There is only one dc-link neutral point and only when the current flows through the neutral point can affect the neutral point voltage balance.

As seen for the voltage level of E [see Fig. 20(c)] and voltage level of 3E [see Fig. 20 (f)], the current may flow through the neutral point. For the voltage level of 2E [see Fig. 20(d) and (e)], the current may also flow through the neutral point. In case of the voltage level of E [see Fig. 20(c)], the neutral point is connected to the phase output. As illustrated in Fig. 19, the load current is negative (flowing into the neutral point) during E. In contrast, during 3E [see Fig. 20(f)], the current is positive and the current flows out of the neutral. As seen, the current flowing into the neutral (charge) during E and out of the neutral (discharge) during 3E is balanced. Similarly, as seen in Fig. 19, during the voltage level of 2E [see Fig. 20(d) or (e)], the current charge and discharge are also balanced. This indicates that the dc-link neutral point voltage is fundamentally stable due to the charge balance over one fundamental output cycle. Note that for the level of E and 3E, there are also alternative switching states, where the load current does not need to flow through the neutral point.

Hence, whether the topology's neutral point voltage can be balanced is analyzed by using the charge balance shown in Fig. 19. This method can also be used to analyze topologies with two or more neutral points such as the topology shown in Figs. 4(a) and 9(b), etc. In addition, advanced pulse width modulation (PWM) methods can be applied to further attenuate the voltage ripple [41]–[45]. Note that, for a three-phase converter, the dc-link neutral point voltage will be regulated by the three phases together. For some topologies, for example, Figs. 4(c) and (b), by using the analyzing method in Fig. 19, it can be found that the neutral point voltage cannot be balanced under the unity power factor. This indicates that the converter cannot work independently as an inverter or rectifier. However, a back-to-back structure with both the rectifier and inverter may still be able to balance the neutral points' voltages [36], [40], [42]. The neutral point voltage balancing capability also relates to the modulation index. Generally, at lower modulation indices, the neutral point voltage is easier to balance and is difficult at high modulation indices. More comprehensive analysis of the neutral point voltage controllable zone with regards to modulation index and power factor is given in [29] and [41].

B. FC Voltage Balance

In most cases, the FC in the converter should serve as a high-frequency (switching frequency) capacitor rather than a fundamental frequency (low frequency) capacitor. Ideally, within one switching cycle, the switching states can be selected flexibly to either charge or discharge the FC for a given current direction. Again, by using the topology shown in Fig. 20 as an example, at the voltage level of E, for a given current direction, e.g., flowing into the converter, the switching states can be chosen between Fig. 20(b) and (c), where Fig. 20(b) will charge the FC and Fig. 20(c) will discharge the FC. This will make sure that the FC voltage can be well controlled. The other similar scenario is that one switching state will either charge or discharge the capacitor and the other state can bypass the capacitor (neither charge nor discharge). As long as the capacitor charge can balance over one fundamental cycle, the capacitor voltage can be maintained. However, the capacitor in this case serves as a low-frequency capacitor and a larger capacitor value is required such as in topology shown in Figs. 5 and 11.

The topology derivation process discussed above can be summarized as in the flowchart shown in Fig. 21.

C. DC-Link Neutral Point and FC Voltage Control Strategy

As seen, selecting from redundant switching states in Fig. 20 can help with both dc-link neutral points' voltage balance and the FC voltage control. The FC voltage control is normally

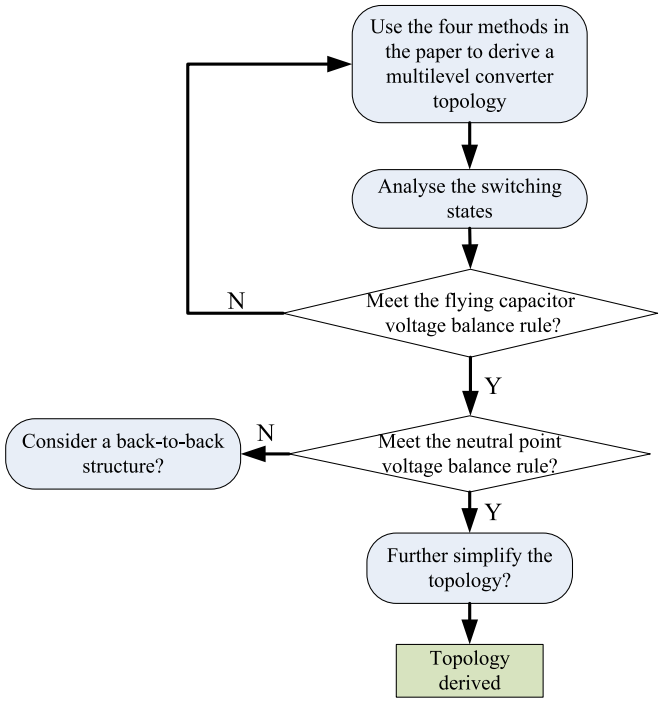

Fig. 21. Topology derivation flowchart.

given a higher priority because it can only be controlled by each phase, while the dc-link neutral points' voltage is shared by and can be controlled by the three phases, thus, given a lower priority. The optimal switching state is first selected to control the FC voltage. Once the FC voltage error is within a certain range, then the switching states are selected to control the neutral point voltage. For example, the switching states can be selected between Fig. 20(b) and (c) to let the load current flow through or not flow through the neutral point; thus, affecting the neutral point voltage balance. Controlling the neutral point voltage and FC voltage through selecting the redundant switching states within each phase is called *"single-phase method"* in this paper.

Apart from using the redundant switching states within each phase to control the FC voltage and dc-link neutral point's voltage, for three-phase converters, the other option is to select from the redundant space vectors in a multilevel space vector modulation (SVM) [29], [42] or equivalently select the optimal zero-sequence component to add on top of the fundamental components (three-phase sinusoidal) [45] in a carrier-based modulation. The SVMs with optimal redundant vector selection and carrier-based method with optimal zero-sequence component selection are equivalent and are called "*three-phase method*" in this paper.

Ideally, the two methods, the "single-phase method" and the "three-phase method' should be used together to select both the optimal space vector (or zero-sequence) of the three phases and the optimal switching states within each phase. However, if for each space vector (zero-sequence), the switching states within each phase are also evaluated, the computation effort will increase significantly. By investigating various topologies and their control [39], [46], it has been found that if there are redundant switching states within each phase, where the "single-phase method" can be applied, it is sufficient to regulate the dc-link neutral point voltage and FC voltage by the "single-phase method." Therefore, the "three-phase method" can adopt a simple form such as a third-order harmonic injection in a carrier-based modulation (or symmetrical modulation in SVM) to extend the modulation index without considering the neutral point voltage and FC voltage control.

If, however, there are no redundant switching states within each phase where the single-phase method cannot be applied, such as in diode-clamped topologies in Fig. 2(b) or the four-level π-type converter in Fig. 9(b), the "three-phase method" must be used. This is normally the case in topologies, where there are no FCs and the dc-link neutral point voltage control is the sole control objective. How to select the optimal redundant space vector or optimal zero-sequence component and how to define the optimal dc-link capacitor energy have been investigated in [29], [36], and [42].

For example, the control objective regarding dc-link capacitor voltage balancing for a four-level converter can be defined as [36], [42]

$$\min V = \sum_{j=1}^{3} \Delta v_{\mathrm{C}j} i_{\mathrm{C}j} = \sum_{j=1}^{3} \left(v_{\mathrm{C}j} - \frac{V_{\mathrm{dc}}}{3} \right) \cdot i_{\mathrm{C}j} \qquad (1)$$

where $i_{\mathrm{C}j}$ is the current flowing through the dc-link capacitor C_j; $\Delta v_{\mathrm{C}j}$ is the voltage deviation of capacitor C_j from $1/3$ of the dc-link voltage. $v_{\mathrm{C}j}$ is the capacitor voltage. V_{dc} is the total dc-link voltage. The optimal redundant vector or zero-sequence component should be selected to minimize the objective function in (1).

The control flowchart for the dc-link neutral points' voltage balancing and FC voltage control with the "single-phase method" or the "three-phase method" is shown in Fig. 22.

A number of topologies derived in this paper with the proposed control and modulation methods as well as simulation or experimental results can be found in [30], [36], [39], and [46].

IV. Mathematical Models of Multilevel Converters

It is important to establish mathematical models to represent the behavior of multilevel converters and to develop the corresponding modulation and control strategy [23]. Although it is challenging to develop a single generalized model for all the multilevel converters, this paper presents a relatively generalized model as shown in Fig. 23.

In Fig. 23, V_{dc} and i_{dc} are dc-link voltage and current, respectively. V_{c1} and $V_{\mathrm{c2}}, \ldots, V_{\mathrm{cn}}$ are dc-link capacitor voltages, respectively. i_{c1}, $i_{\mathrm{c2}}, \ldots, i_{\mathrm{cn}}$ are the current flowing through each dc-link capacitor. $i_0, i_1, \ldots, i_{\mathrm{n}}$ are the dc-link branch current and will flow to the load (output) if the output is connected to the corresponding position $(1, 2, \ldots, n)$. V_a and i_a are the phase output voltage and current. $V_{\mathrm{cf1}}, \ldots, V_{\mathrm{cfm}}$ represent the voltages of the FCs. The number of FCs involved in the current flowing path depends on the switching states and the converter structure. Note that the polarity of the FCs' voltages $(V_{\mathrm{cf1}}, \ldots, V_{\mathrm{cfm}})$ can be positive or negative depending on the way it is connected, which will affect the output voltage level and the charging and discharging states of the FC. The phase output is connected

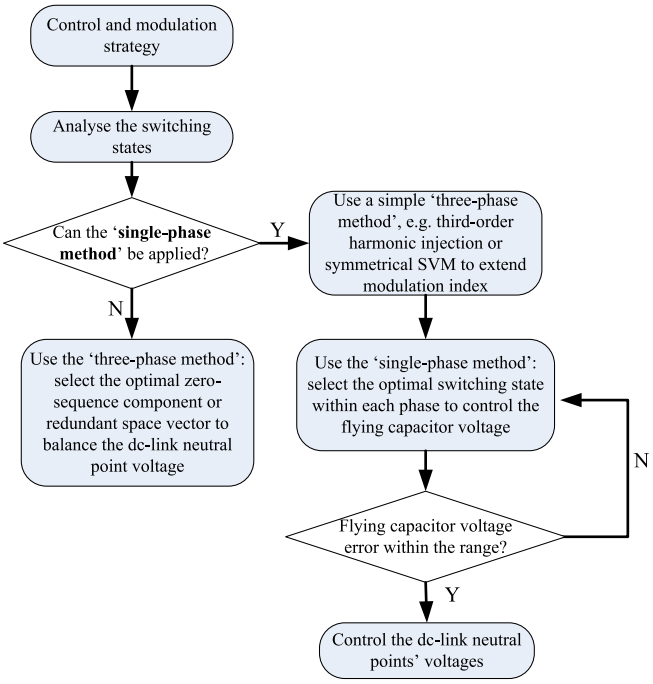

Fig. 22. Flowchart of the dc-link neutral points' voltage balancing and FC voltage control.

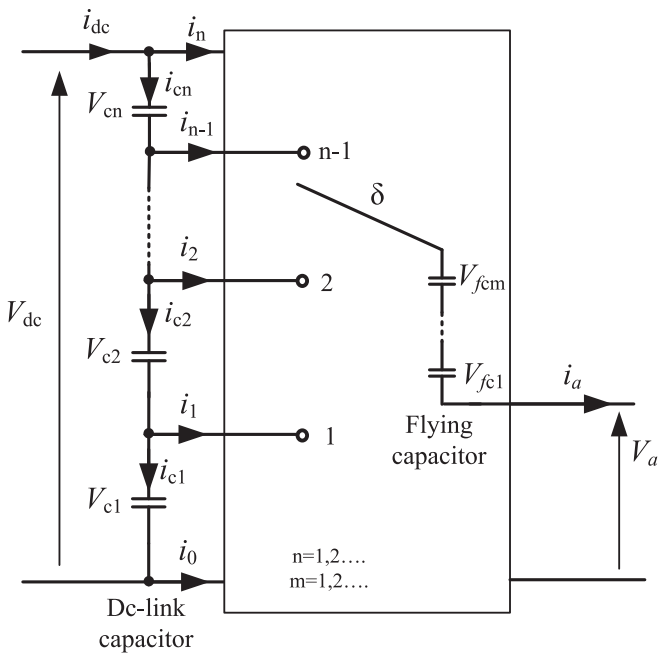

Fig. 23. Model for multilevel converters.

to the dc-link neutral points, which is represented by a single-pole-multiple-throw (SPMT) switch. The position of the switch is defined by the following switching function δ, where

$$\delta = 0, 1, 2, \ldots, n. \tag{2}$$

When $\delta = 0$, the SPMT is connected to the negative dc-bus. When $\delta = 1$, the SPMT is connected to position 1 in Fig. 23. Then, the phase output voltage of the multilevel converter (V_a) can be given as

$$V_a = \sum_{k=0}^{\delta} V_{ck} + \sum_{m=0} (\pm) V_{fcm}. \tag{3}$$

Equation (3) means that the output voltage equals to the sum of the selected dc-link capacitor voltages (depending on the position of the tap) plus the sum of the FC voltages. Note that, as mentioned, the FCs' voltages can be positive or negative. The voltage of each FC can be equal to that of each dc-link capacitor or it can be multiples or fraction of that. Regarding the control of the dc-link capacitor voltages and FC voltages, it is important to find out the relationship between the phase output current $i_{\rm a}$ and the dc-link capacitor voltage or the FC voltage, which is derived below. Assuming that the parameters of the dc-link capacitors are the same, i.e., same capacitance value and the total dc-link voltage is a constant, then the current flowing through each dc-link capacitor $i_{\rm cn}$ can link to the branch current i_n by (4), where N is the total number of dc-link capacitors

$$\begin{cases} i_{c1} = -\frac{N-1}{N} i_1 - \frac{N-2}{N} i_2 - \frac{N-3}{N} i_3 .... - \frac{N-(n-1)}{N} i_{n-1} \\ i_{c2} = \frac{1}{N} i_1 - \frac{N-2}{N} i_2 - \frac{N-3}{N} i_3 .... - \frac{N-(n-1)}{N} i_{n-1} \\ i_{c3} = \frac{1}{N} i_1 + \frac{2}{N} i_2 - \frac{N-3}{N} i_3 .... - \frac{N-(n-1)}{N} i_{n-1} \end{cases}. \tag{4}$$

Equation (4) only gives the relationship between the first three dc-link capacitors' currents ($i_{\rm c1}$, $i_{\rm c2}$, and $i_{\rm c3}$) in Fig. 23 and the branch currents. Other dc-link capacitor currents can be derived accordingly like (4). Practically, within one switching cycle, the SPMT will either just stay at one branch position or jump between two adjacent branches. The time duration at each branch depends on the duty cycle. Therefore, the average current at each branch can be linked to the phase output current as

$$i_n = \frac{1}{T_s} \int_0^{T_n} i_a dt \tag{5}$$

where $T_{\rm s}$ is the switching cycle and T_n is the time duration when the SPMT stays at position n. The capacitor voltage and current relationship can be expressed as (6) for the dc-link capacitor

$$i_{\rm cn} = C \frac{dV_{\rm cn}}{dt}. \tag{6}$$

From (4) to (6), the relationship between the output current and dc-link capacitor voltage can be found. The control needs to identify a suitable position and duration for the SPMT in order to maintain the balance of the dc-link capacitors while keeping the output voltage at the required level.

Similarly, the FC voltage and current relationship can be expressed as

$$i_a = C \frac{dV_{\rm fcm}}{dt}. \tag{7}$$

The optimal switching state should be selected to regulate the FC voltage to be at the reference value. The dc-link capacitor voltage and FC voltage control based on the mathematical model can be found in [36] and [46].

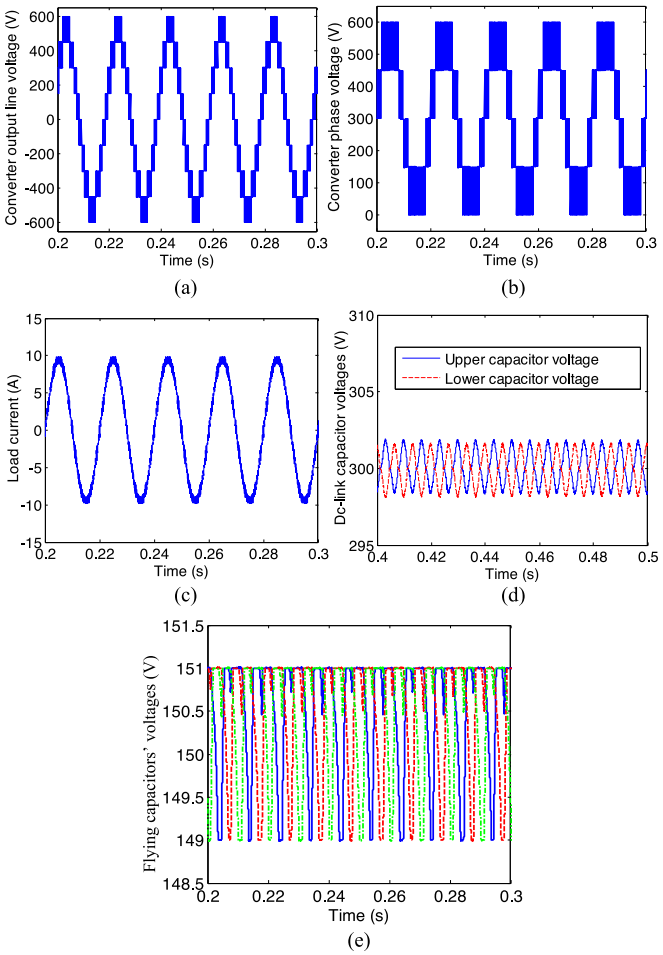

Fig. 24. Simulation results of the five-level converter. (a) Converter output line voltage. (b) Converter output phase voltage. (c) Converter output current. (d) DC-link upper and lower capacitors' voltages. (e) FCs' voltages of the three phases.

V. Simulation Results

In this section, the five-level topology shown in Fig. 18 is simulated in MATLAB/Simulink to validate the proper function of the topology and the ability to regulate the dc-link neutral point and FC voltages. The dc-link voltage is set at 600 V and the switching frequency is 10 kHz. A sinusoidal PWM is used and the modulation index is 0.9. The "single-phase method" is used to regulate the dc-link neutral point and FC voltages. The converter (inverter) supplies power to a three-phase *R-L* (30 Ω and 1 mH) load. The dc-link upper and lower capacitors' value is 1 mF each.

Fig. 24(a) shows the converter output line voltage, which has nine levels. Fig. 24(b) shows the converter phase voltage referring to the negative dc-link, which has five levels as expected. Fig. 24(c) shows the sinusoidal load current. Fig. 24(d) shows the upper and lower dc-link capacitor voltages, which are well regulated around the reference voltage of 300 V (half of the total dc-link voltage). A voltage ripple (150 Hz) is observed across the upper and lower capacitor and the frequency is three times of the fundamental output frequency (50 Hz). Fig. 24(e) shows the FC voltages of the three phases, which are well regulated

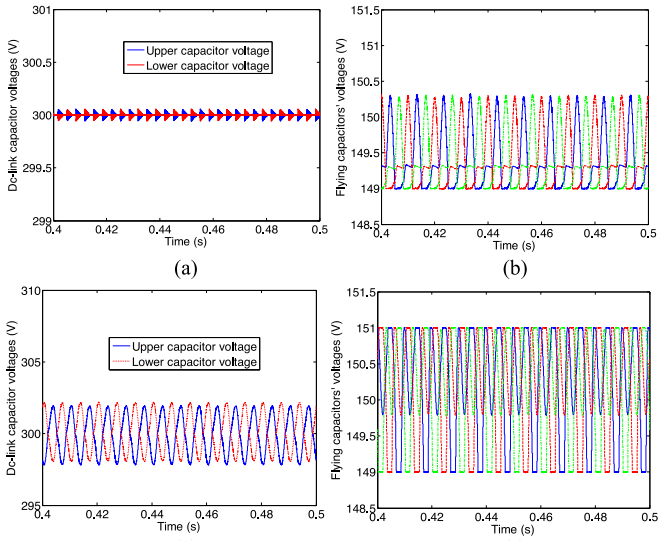

Fig. 25. DC-link capacitor voltages and FC voltages. (a) DC-link upper and lower capacitors' voltages at modulation index = 0.5 and power factor = 0.95. (b) FCs' voltages of the three phases at modulation index = 0.5 and power factor = 0.95. (c) DC-link upper and lower capacitors' voltages at modulation index = 0.95 and power factor = 0.6. (d) FCs' voltages of the three phases at modulation index = 0.95 and power factor = 0.6.

at around 150 V. The predefined FC voltage error tolerance is set as 1 V (149–151 V). These simulation results validate the converter topology and the control strategy.

The results in Fig. 24 are in the condition of high modulation index (0.95) and high power factor (0.95). In order to validate the neutral point voltage and FC voltage control capability under various modulation indices and power factors, a set of simulations has been run with the results shown in Fig. 25. Fig. 25(a) and (b) shows the simulation results under low modulation index (0.5) and high power factor (0.95). Fig. 25(c) and (d) shows the simulation results under high modulation index (0.95) and low power factor (0.6). As can be seen, the neutral point voltage and FC voltage can be well regulated.

VI. Conclusion

This paper has summarized four methods to derive multilevel converters. As seen, there are connections between the three generalized topologies. Some topologies can also be derived from more than one method. It is hoped that this paper can inspire other topology derivation methods as well as new multilevel converter topologies.

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