# Recent Advances in Multilevel Inverters and Their Applications—Part I

MULTILEVEL inverters have experienced, in terms of research and applications, a continuous and increasing growth during the last two decades. The effort of the researchers and industry has led to a rapid development of different multilevel inverter topologies, modulation techniques, and control strategies. In addition, other interesting research topics such as the fault tolerant operation, efficiency improvement, optimized control strategies, and new applications are also important. This "Special Section on Recent Advances in Multilevel Inverters and Their Applications—Part I" of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Issue presents to the power electronics community the most recent advances with topics such as the following:

1) new multilevel inverter topologies;
2) new modulation and control strategies for multilevel inverters;
3) industrial applications of multilevel inverters;
4) multilevel inverters for renewable energy applications;
5) common-mode voltage reduction methods in multilevel inverters;
6) fault-tolerant design of multilevel inverters.

It is our pleasure to present this Special Section. Due to the high number of good papers submitted, this Special Section will be divided into at least two parts.

In [1], a new module for cascaded multilevel inverter is proposed. This module is named as the Envelope Type (E-Type) module and can generate 13 levels with reduced components. In [2], a new general multilevel inverter topology based on cascaded connection of submultilevel units with reduced switching components, dc voltage sources, and blocked voltage by switches is proposed. The proposed topology is optimized to generate any level with a minimum number of components and peak voltage on switches. The presented topology can be used in high-voltage applications as it employs the switches with low voltage rating. Moreover, other topologies of multilevel inverters are presented in [3]–[7]. A new single-phase $\pi$-type five-level inverter using three-terminal switch-network is proposed in [3]. The proposed topology is considered as a variant of T-type three-level structure or dual-buck inverter with coupled inductors. This new inverter is suitable for multilevel power inversion with low dc-bus voltage. The merit of the proposed topology is to apply only four active power switches to achieve five-level operation. Other benefits include double frequency operation of output inductors and equal division of the current that flows through power switches and filter inductor. Hence, it leads to high efficiency and low harmonics. These characteristics allow improvement of losses distribution and volume reduction of output filter inductor.

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The large number of semiconductors typically implemented in multilevel inverters generates large stray inductances in their commutation loops. As a consequence, high voltage overshoots appear in the semiconductors during commutation which may limit the operation of the inverter. Reference [4] analyzes these overvoltages in the five-level active neutral-point-clamped inverter. A new single dc source cascaded seven-level inverter integrating switched capacitor techniques is developed in [5]. Compared with the traditional cascaded multilevel inverter, the proposed topology replaces all the separate dc voltage sources with capacitors, leaving only one H-bridge cell with a real dc voltage source and only adds two charging switches. In [6], a new topology of six-level inverters for medium-voltage high-power applications is proposed, which consists of inner flying-capacitor inverter units and outer two-level inverter units. In [7], a new structure for symmetric cascade multilevel inverters is presented. This structure requires the least power electronic components, gate driver circuits, a power diode, and a dc voltage source.

The main challenge of using modular multilevel inverters in variable-speed drives is the large voltage ripple of submodule capacitors at low speed with constant torque. In [8], an improved circulating current injection method is proposed, which does not completely eliminate the capacitor voltage ripple, but maintains it bounded within reasonable values. As a result, the magnitude of the injected circulating current is reduced, leading to converter efficiency improvement and reduction of semiconductor current ratings.

In this first part of the Special Section, there are also some control methods for multilevel inverters for different objectives. In [9], a harmonic elimination technique is proposed based on a three-level dodecagonal space vector structure for open-end winding induction machine drives with a single dc supply. Thus, the advantages of dodecagonal space vector switching and multilevel inverters are achieved in this work using a single dc supply. A hybrid switching technique by using selective harmonic mitigation (SHM) and selective harmonic elimination (SHE) based on pulse amplitude modulation concept is presented in [10]. This technique has been applied on a four-leg neutral-point-clamped inverter to eliminate and mitigate more harmonic orders than recently proposed hybrid SHM-SHE-PWM method while generating switching pulses at the same frequency.

Several PWM strategies have been presented for three-phase multilevel inverters. Typically, these PWM methods can be either space-vector or carrier-based implementations, where the carrier-based implementation usually presents a lower computation complexity. In [11], a new approach for the carrier-based implementation of different existing PWM methods is proposed for three- and four-level dc–ac inverters, which can be easily extended to any number of levels. The main features of the

proposed approach are its reduced computation complexity and computation time.

The modular multilevel converter (MMC) is attractive for medium- or high-power applications because of the advantages of its high modularity, availability, and high power quality. The fault-tolerant operation is one of the important issues for the MMC. In this first part of the Special Section, some work has also been done in fault-tolerant approaches. In [12], a fault-tolerant approach for the MMC under submodule faults is proposed. To increase the fault tolerance for cascaded H-bridge multilevel inverters based on level-shifted PWM (LS-PWM), in [13], a modified LS-PWM method is proposed for the inverters operating under faulty conditions.

Finally, some new works based on model based predictive control has been done for multilevel inverters [14], [15]. In [14], a multilevel power conditioner and its model predictive control for railway traction system are presented. In [15], a finite control set model predictive control (FCS-MPC) for a grid-tied packed U cells multilevel inverter is presented. The system under study consists of a single-phase three-cells packed U cell inverter connected to the grid through a filtering inductor. The aim of the proposed FCS-MPC technique is to achieve, under various operating conditions, grid-tie current injection with unity power factor and low total harmonic distortion while balancing the capacitor voltage.

We hope that this Special Section will increase the interest of the scientific community in this field and will motivate the generation of new ideas for future research applications.

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