Improving the Stability of Cascaded DC/DC Converter Systems via Shaping the Input Impedance of the Load Converter With a Parallel or Series Virtual Impedance

Xin Zhang, *Member, IEEE*, Xinbo Ruan, *Senior Member, IEEE*, and Qing-Chang Zhong, *Senior Member, IEEE*

***Abstract*—Interactions between individually designed power subsystems in a cascaded system may cause instability. This paper proposes an approach, which connects a virtual impedance in parallel or series with the input impedance of the load converter so that the magnitude or phase of the load converter's input impedance is modified in a small range of frequency, to solve the instability problem of a cascaded system. The requirements on the parallel virtual impedance (PVI) and series virtual impedance (SVI) are derived, and the control strategies to implement the PVI and SVI are proposed. The comparison and general design procedure of the PVI and SVI control strategies are also discussed. Finally, considering the worst stability problem that often occurs at the system whose source converter is an LC filter, two cascaded systems consisting of a source converter with an LC input filter and a load converter, which is either a buck converter or a boost converter, are fabricated and tested to validate the effectiveness of the proposed control methods.**

***Index Terms*—Cascaded system, dynamic performance, input impedance regulator (IIR), instability problem, load converter, parallel virtual impedance (PVI), series virtual impedance (SVI).**

I. Introduction

DC distributed power systems (DPSs) have been widely used in space stations, aircraft, ships, hybrid vehicles, communication systems, and renewable energy systems in the last few decades, due to the flexible system configurations, high efficiency, and high-power delivery capability [1]–[6]. In a dc DPS, there are various forms for connecting the subsystems; among which, cascaded configuration is the typical one [7]. Fig. 1 shows a typical cascaded system, which is composed of a source converter and a load converter. Although both the source and load converters can work well individually, the whole system may become unstable because of their interactions, as reported in [8]–[12]. The stability of the cascade system can be guaranteed if the Middlebrook criterion is satisfied [13]–[17], i.e., Z_{o_S}/Z_{in_L} satisfies the Nyquist criterion, where Z_{o_S} is the source converter's output impedance, and Z_{in_L} is the load converter's input impedance.

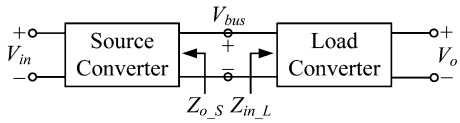

Fig. 1. Cascaded system.

In order to meet the Middlebrook criterion, various solutions have been proposed, and they can be classified into two types: passive [18] and active [19]–[23] methods. For passive methods, the passive components, such as resistors, capacitors, and inductors, are employed. In [18], the RC and RL dampers were introduced to reduce the output impedance resonant peak of the source converter, so that Z_o is less than Z_{in} in the entire frequency range, and thus, the system stability is guaranteed. However, the passive components might lead to significant power loss. As a result, the active methods, which are based on advanced control of the source converter [19]–[21] and/or the load converter [22], or adding a power buffer between the source and load converters [23], are proposed.

Compared to the stability solutions by changing the source converter's output impedance, the methods of regulating the load converter's input impedance are rarely reported. This is because the load converter's input impedance is preferred to be regulated to a negative resistor when achieving a good dynamic performance [24], but this negative resistor characteristic is bad news for the stability of a cascaded system [13]. Accordingly, it is a big challenge to regulate the load

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X. Zhang was with the Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China. He is now with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield S1 3JD, U.K. (e-mail: xin.zhang@sheffield.ac.uk).

X. Ruan is with the Aero-Power Sci-Tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: ruanxb@nuaa.edu.cn).

Q.-C. Zhong is with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA, and also with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield S1 3JD, U.K. (e-mail: zhongqc@ieee.org).

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converter's input impedance, when ensuring the stability of the cascaded system and good dynamic performance of the load converter, simultaneously. In [25], one solution of this contradictory issue is presented by developing the regulation signal maps of the source converter into the regulation loop of the load converter. However, this method may be unachievable in some applications. For instance, if the source converter is a simple LC filter, there will be no regulation signals of the source converter, and as a result, the load converter's input impedance cannot be regulated to stabilize the cascaded system. Moreover, if the source converter is an LC filter, its output impedance is higher than that of other source converter types and the system's stability problem is more likely to appear [26]. Therefore, it is highly desirable to find more general stability solutions to regulate the input impedance of load converter.

This paper proposes a set of virtual-impedance-based control strategies to introduce a virtual impedance to be connected in parallel or series with the load converter's input impedance and thus regulate the load converter's input impedance. The proposed control strategies take into account both the stability of the cascaded system and the dynamic performance of the load converter, and they can be applied to any kind of cascaded systems. The remaining parts of this paper are organized as follows: In Section II, the instability reason of the cascaded system is reviewed and the stability-preferred input impedance of the load converter is discussed. Then, the parallel-virtual-impedance (PVI) control strategy and series-virtual-impedance (SVI) control strategy are presented in Sections III and IV, respectively. After that, two design examples are given in Section V. Section VI shows the experimental results, which verify the effectiveness of the proposed methods. Section VII compares the two control strategies and concludes their general design procedure. Finally, Section VIII summarizes this paper.

II. Instability Reason of Cascaded System and Stability-Preferred Input Impedance of Load Converter

A. Review of Subsystems' Impedance Characteristics and Instability Cause of the Cascaded System

For cascaded systems, the impedance characteristics of subsystems and the cause of instability have been studied extensively in the last three decades [27]–[33]. Some general conclusions are summarized as follows.

a) Impedance characteristic of Z_{o_S}: Z_{o_S} is the source converter's output impedance independent of its load. The characteristic of Z_{o_S} is depicted with dotted lines, as shown in Fig. 2. Here, if the source converter is a switching-mode power supply, f_{c_S} is the cutoff frequency of its voltage loop; if the source converter is an LC input filter, f_{c_S} is the filter's resonant frequency. It is obvious that Z_{o_S} is similar to the output impedance of an LC filter. If $f < f_{c\_S}$, Z_{o_S} presents the characteristic of an inductor, and if $f > f_{c\_S}$, Z_{o_S} presents the characteristic of source converter's output filter capacitor. Note that the source converter's open-loop output impedance is higher than its closed-loop output impedance, and if the source converter is an LC filter, its output impedance is higher than the output impedance of other source converter types [27].

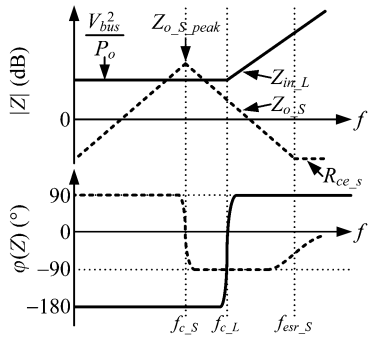


Fig. 2. Impedance characteristics of Z_{o_S} and Z_{in_L}.

b) Impedance characteristic of Z_{in_L}: Z_{in_L} is the input impedance of the load converter operating in continuous current mode (CCM). The characteristic of Z_{in_L} is depicted with solid lines, as shown In Fig. 2, where f_{c_L} is the cutoff frequency of the load converter's voltage loop. If $f < f_{c\_L}$, Z_{in_L} behaves as a negative resistor with the value of $-V_{\text{bus}}^2/P_o$ [28], where V_{bus} is the intermediate bus voltage, and P_o is the load converter's output power, and if $f > f_{c\_L}$, Z_{in_L} behaves as an inductor. Note that, when $f < f_{c\_L}$, the magnitude of Z_{in_L} is inversely proportional to P_o [29]–[31].

c) Cause of instability: For a cascaded system, if Z_{o_S} is intersected with Z_{in_L}, and if f_{c_S} is less than f_{c_L}, as shown in Fig. 2, the cascaded system is unstable [31]. The $-180°$ phase resulted by the load converter's negative resistor characteristic is the main factor that causes the instability of the cascaded system [32], [33].

d) Worst case of instability problem: According to the characteristic of Z_{o_S}, when the source converter is an LC filter, its output impedance is higher than that of other types of source converters [26]. According to the characteristic of Z_{in_L}, when the load converter operates at full load, it has lowest input impedance. Hence, the worst case of instability problem of a cascaded system occurs at full load and with the source converter being an LC filter.

B. Stability-Preferred Input Impedance of Load Converter

As described earlier, for the purpose of ensuring system stability, the negative resistor characteristic of the load converter's input impedance Z_{in_L} should be removed. However, this will sacrifice the load converter's dynamic performance. Therefore, in order to make the cascaded system stable while keeping a good dynamic performance of the load converter, it is better to only regulate the characteristics of Z_{in_L} in the vicinity of the intersection frequencies of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$. Fig. 3 gives two ways of regulating Z_{in_L} as follows:

1) Make a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$ by increasing the magnitude of Z_{in_L} within $[f_1, f_2]$ [see Fig. 3(a)].

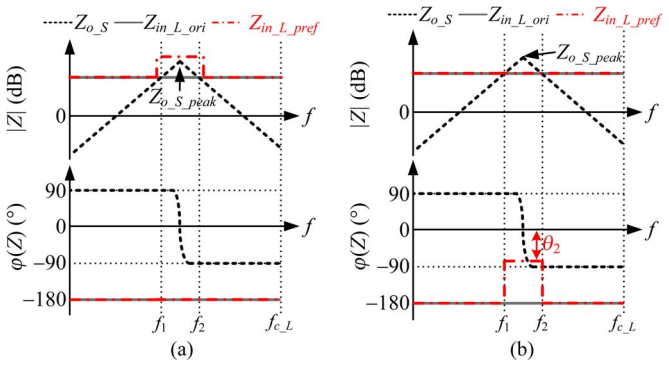


Fig. 3. Stability-preferred input impedance of the load converter. (a) Total separation of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$. (b) Ensure $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$ within $[f_1, f_2]$.

2) Ensure that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$ within $[f_1, f_2]$ by compensating the phase of Z_{in_L} [see Fig. 3(b)]. Here, f_1 and f_2 are the intersection frequencies of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$.

According to Fig. 3(a), the preferred Z_{in_L} can be described as

$$Z_{\text{in}\_L\_\text{pref}}(s) = \begin{cases} |Z_{\text{in}\_L1}| \cdot e^{j\theta_1} & f \in [f_1, f_2] \\ Z_{\text{in}\_L\_\text{ori}}(s) & f \notin [f_1, f_2] \end{cases} \quad (1)$$

where $Z_{\text{in}\_L1\_\text{ori}}$ is the original input impedance of the load converter, and $|Z_{\text{in}\_L1}|$ and θ_1 are the magnitude and phase of the preferred input impedance of the load converter within $[f_1, f_2]$, respectively. In order to make a total separation between $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$, $|Z_{\text{in}\_L1}|$ should satisfy

$$|Z_{\text{in}\_L1}| > |Z_{o\_S\_\text{peak}}| \quad (2)$$

where $Z_{o\_S\_\text{peak}}$ is the peak value of Z_{o_S}. Since $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$ are totally separated, θ_1 can be any values. In order to minimize the effect on the load converter, θ_1 is recommended to be the phase of the load converter's original input impedance, i.e., $\theta_1 = -180°$ [see Fig. 3(a)].

According to Fig. 3(b), the preferred Z_{in_L} can be expressed as

$$Z_{\text{in}\_L\_\text{pref}}(s) = \begin{cases} |Z_{\text{in}\_L2}| \cdot e^{j\theta_2} & f \in [f_1, f_2] \\ Z_{\text{in}\_L\_\text{ori}}(s) & f \notin [f_1, f_2] \end{cases} \quad (3)$$

where $|Z_{\text{in}\_L2}|$ and θ_2 are the magnitude and phase of the preferred input impedance of the load converter within $[f_1, f_2]$, respectively. In order to ensure that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$ at the intersection frequencies of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$, θ_2 should satisfy

$$\theta_2 \in (-90°, 90°). \quad (4)$$

Since $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$ at f_1 and f_2, $|Z_{\text{in}\_L2}|$ can be any values. In order to minimize the resulting effect on the load converter, $|Z_{\text{in}\_L2}|$ is designed to be equal to $|Z_{\text{in}\_L\_\text{ori}}|$ [see Fig. 3(b)].

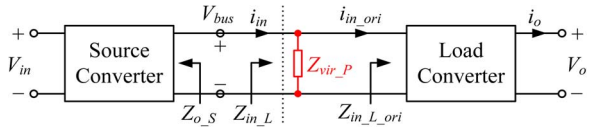


Fig. 4. Cascaded system with PVI.

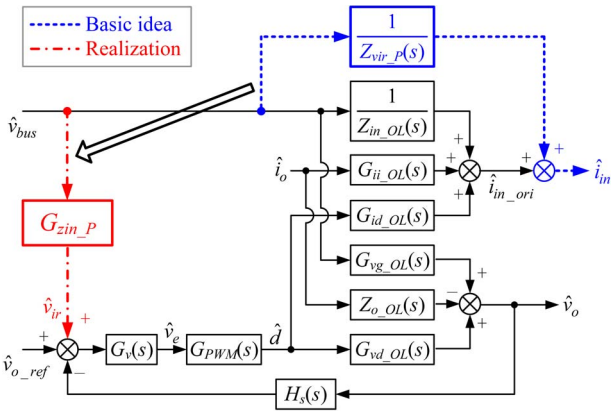


Fig. 5. PVI control strategy.

III. PVI Control Strategy for Regulating the Input Impedance of Load Converter

A. Concept of PVI

As shown in Fig. 4, the PVI $Z_{\text{vir}\_P}(s)$ is introduced to be in parallel with the input port of the load converter. Hence, the load converter's input impedance is changed to

$$Z_{\text{in}\_L}(s) = Z_{\text{in}\_L\_\text{ori}}(s) // Z_{\text{vir}\_P}(s) = \frac{Z_{\text{in}\_L\_\text{ori}}(s) Z_{\text{vir}\_P}(s)}{Z_{\text{in}\_L\_\text{ori}}(s) + Z_{\text{vir}\_P}(s)} \quad (5)$$

where $Z_{\text{in}\_L\_\text{ori}}(s)$ is the original input impedance of the load converter, and if $f < f_{c\_L}$, $Z_{\text{in}\_L\_\text{ori}}(s)$ is given by

$$Z_{\text{in}\_L\_\text{ori}}(s) = -V_{\text{bus}}^2 / P_o. \quad (6)$$

By regulating $Z_{\text{vir}\_P}(s)$, the load converter's input impedance can be modified to the preferred one shown in Fig. 3. Substituting (1) into (5), the required $Z_{\text{vir}\_P}(s)$ for achieving a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$ can be obtained as

$$Z_{\text{vir}\_P}(s) = \begin{cases} \frac{-V_{\text{bus}}^2 |Z_{\text{in}\_L1}|}{(V_{\text{bus}}^2 - |Z_{\text{in}\_L1}| P_o)} & f \in [f_1, f_2] \\ +\infty & f \notin [f_1, f_2]. \end{cases} \quad (7)$$

Likewise, substituting (3) into (5), the required $Z_{\text{vir}\_P}(s)$, for ensuring that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$ at f_1 and f_2, can be obtained as

$$Z_{\text{vir}\_P}(s) = \begin{cases} \frac{(V_{\text{bus}}^2 e^{j\theta_2})}{[P_o(1+e^{j\theta_2})]} & f \in [f_1, f_2] \\ +\infty & f \notin [f_1, f_2]. \end{cases} \quad (8)$$

B. PVI Control Strategy

Fig. 5 shows the small-signal control block of the original load converter. Its variables and transfer functions are described in Table I. The transfer function $1/Z_{\text{vir}\_P}(s)$, which is shown

TABLE I
VARIABLES AND TRANSFER FUNCTIONS IN LOAD CONVERTER

$\hat{v}_{bus}$	Disturbance of the bus voltage	$\hat{i}_{in\_ori}$	Disturbance of the input current
$\hat{v}_o$	Disturbance of the output voltage	$\hat{i}_o$	Disturbance of the output current
$\hat{d}$	Disturbance of the duty cycle	$\hat{v}_{o\_ref}$	Disturbance of the output voltage reference
$G_{PWM}(s)$	Transfer function of the modulator	$H_s(s)$	Sampling coefficient of the output voltage
$G_v(s)$	Transfer function of the voltage regulator	$Z_{in\_OL}(s)$	Open-loop input impedance
$Z_{o\_OL}(s)$	Open-loop output impedance	$G_{id\_OL}(s)$	Control to input current transfer function
$G_{vd\_OL}(s)$	Control to output voltage transfer function	$G_{ii\_OL}(s)$	Open-loop load to input current transfer function
$G_{vg\_OL}(s)$	Open-loop input to output voltage transfer function		

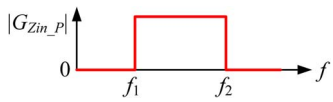


Fig. 6. Characteristic of $|G_{\mathrm{Zin\_}P}(s)|$.

with dashed lines, is introduced to the control block between the input voltage and the input current to realize the PVI, and $\hat{i}_{\mathrm{in}}$ is the disturbance of the load converter's input current with $Z_{\mathrm{vir\_}P}(s)$. This is the basic idea of PVI. Moving the output of $1/Z_{\mathrm{vir\_}P}(s)$ to the output voltage reference, and adjusting the transfer function to $G_{\mathrm{Zin\_}P}(s)$, as shown with the dot-dashed lines, we have the equivalent transformation. This is the proposed PVI control strategy, and $G_{\mathrm{Zin\_}P}(s)$ is named as the *input impedance regulator* (IIR), which can be expressed as

$$G_{\mathrm{Zin\_}P}(s)=\frac{1}{Z_{\mathrm{vir\_}P}(s)}\cdot\frac{1+T_v(s)}{G_v(s)G_{\mathrm{PWM}}(s)G_{id\_\mathrm{OL}}(s)} \tag{9}$$

where $T_v(s)=H_s(s)G_v(s)G_{\mathrm{PWM}}(s)G_{vd\_\mathrm{OL}}(s)$ is the loop gain of the voltage closed loop of load converter.

C. Realization of $G_{\mathrm{Zin\_}P}(s)$

Substituting (7) and (8) into (9), respectively, $G_{\mathrm{Zin\_}P}(s)$ can be further described as

$$G_{\mathrm{Zin\_}P}(s)=\begin{cases}\frac{|Z_{\mathrm{in\_}L1}|P_o-V_{\mathrm{bus}}^2}{|Z_{\mathrm{in\_}L1}|V_{\mathrm{bus}}^2}\\ \times\frac{1+T_v(s)}{G_v(s)G_{\mathrm{PWM}}(s)G_{id\_\mathrm{OL}}(s)} & f\in[f_1,f_2]\\ 0 & f\notin[f_1,f_2]\end{cases} \tag{10}$$

$$G_{\mathrm{Zin\_}P}(s)=\begin{cases}\frac{P_o}{V_{\mathrm{bus}}^2}(1+e^{-j\theta_2})\\ \times\frac{1+T_v(s)}{G_v(s)G_{\mathrm{PWM}}(s)G_{id\_\mathrm{OL}}(s)} & f\in[f_1,f_2]\\ 0 & f\notin[f_1,f_2].\end{cases} \tag{11}$$

As seen from (10) and (11), $G_{\mathrm{Zin\_}P}(s)$ is a frequency-based piecewise function, which is shown in Fig. 6, where $|G_{\mathrm{Zin\_}P}(s)|$ is a nonzero value within $[f_1,f_2]$ and zero outside

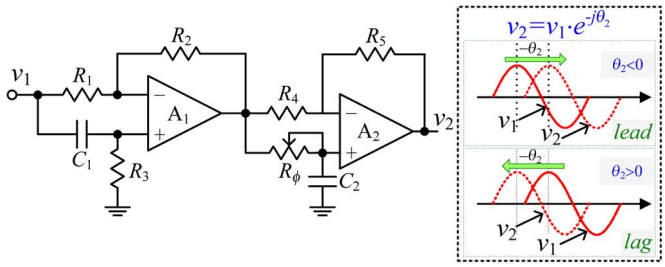


Fig. 7. Analog phase-shifted circuit.

$[f_1,f_2]$. Hence, a bandpass filter $G_{\mathrm{BPF}}(s)$ can be utilized to realize $G_{\mathrm{Zin\_}P}(s)$, i.e.,

$$G_{\mathrm{Zin\_}P}(s)=\frac{|Z_{\mathrm{in\_}L1}|P_o-V_{\mathrm{bus}}^2}{V_{\mathrm{bus}}^2|Z_{\mathrm{in\_}L1}|}\times\frac{1+T_v(s)}{G_v(s)G_{\mathrm{PWM}}(s)G_{id\_\mathrm{OL}}(s)}G_{\mathrm{BPF}}(s) \tag{12}$$

$$G_{\mathrm{Zin\_}P}(s)=\frac{P_o}{V_{\mathrm{bus}}^2}(1+e^{-j\theta_2})\times\frac{1+T_v(s)}{G_v(s)G_{\mathrm{PWM}}(s)G_{id\_\mathrm{OL}}(s)}G_{\mathrm{BPF}}(s). \tag{13}$$

In this paper, $G_{\mathrm{BPF}}(s)$ adopts a typical second-order bandpass filter, which is composed of a second-order high-pass filter and a second-order low-pass filter, given as

$$G_{\mathrm{BPF}}(s)=\frac{s^2}{s^2+\left(\frac{\omega_1}{Q_H}\right)s+\omega_1^2}\cdot\frac{\omega_2^2}{s^2+\left(\frac{\omega_2}{Q_L}\right)s+\omega_2^2} \tag{14}$$

where $\omega_1=2\pi f_1$ and $\omega_2=2\pi f_2$ are the characteristic angular frequencies of high-pass filter and low-pass filter, respectively; Q_H and Q_L are the quality factors of the high-pass filter and low-pass filter, respectively.

In (13), the shifted phase θ_2 can be implemented by digital control chips, such as a digital signal processor (DSP), a field-programmable gate array (FPGA), and a microcontroller unit (MCU), and can also be realized by an analog phase-shifted circuit [34], as shown in Fig. 7, where we let $R_1=R_2=R_3=R_4=R_5$; thus, θ_2 is given by

$$\theta_2=-2\arctan\frac{1-(2\pi f_{c\_S})^2R_1C_1C_2R_\phi}{2\pi f_{c\_S}(C_2R_\phi+R_2C_1)} \tag{15}$$

where f_{c_S} is defined in Fig. 2. Since the vicinity of the intersection frequencies of source converter's output impedance and load converter's input impedance is usually very small, f_1 and f_2 are very close to f_{c_S}. As a result, we can get the following relationship:

$$v_2(f)=v_1(f)\cdot e^{-j\theta_2}\ f\in[f_1,f_2]. \tag{16}$$

IV. SVI CONTROL STRATEGY FOR REGULATING THE INPUT IMPEDANCE OF LOAD CONVERTER

A. Concept of SVI

Fig. 8 shows the introduced SVI $Z_{\mathrm{vir\_}S}(s)$ at the input port of the load converter. As a result, the load converter's input impedance becomes

$$Z_{\mathrm{in\_}L}(s)=Z_{\mathrm{in\_}L\_\mathrm{ori}}(s)+Z_{\mathrm{vir\_}S}(s) \tag{17}$$

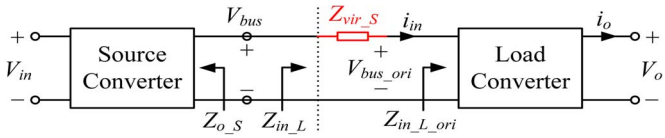


Fig. 8. Cascaded system with SVI.

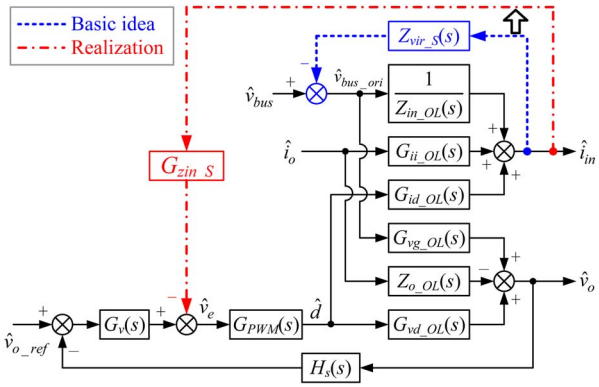


Fig. 9. SVI control strategy.

where $Z_{\text{in\_}L\_\text{ori}}(s)$ at the frequencies below f_{c_L} is expressed as

$$Z_{\text{in\_}L\_\text{ori}}(s) = -V_{\text{bus\_ori}}^2/P_o. \tag{18}$$

Similar to the PVI control strategy, the load converter's input impedance can be modified to the required one shown in Fig. 3 by regulating $Z_{\text{vir\_}S}(s)$. By substituting (1) into (17), the required $Z_{\text{vir\_}S}(s)$ for realizing a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in\_}L}|$ [see Fig. 3(a)] can be derived as

$$Z_{\text{vir\_}S}(s) = \begin{cases} \left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) - |Z_{\text{in\_}L1}| & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2]. \end{cases} \tag{19}$$

Likewise, by putting (3) into (17), the required $Z_{\text{vir\_}S}(s)$, for ensuring that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in\_}L})| < 180^\circ$ at f_1 and f_2 [see Fig. 3(b)] can be derived as

$$Z_{\text{vir\_}S}(s) = \begin{cases} \left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) \cdot (1 + e^{j\theta_2}) & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2]. \end{cases} \tag{20}$$

B. SVI Control Strategy

Fig. 9 shows the small-signal control block of the original load converter. Its variables and transfer functions are the same as those in Fig. 5. The transfer function $Z_{\text{vir\_}S}(s)$ is introduced to the control block between the input current and the input voltage (dash line) to realize the SVI, and $\hat{v}_{\text{bus\_ori}}$ is the disturbance of the load converter's input voltage with $Z_{\text{vir\_}S}(s)$. This is the basic idea of the SVI control strategy. By moving the feedback node of i_{in} to the output of $G_v(s)$ and adjusting the transfer function to $G_{\text{Zin\_}S}(s)$, as shown with the dot-dashed lines, the equivalent control block diagram is obtained. Here, $G_{\text{Zin\_}S}(s)$ is named as the IIR of the SVI control strategy, which can be expressed as

$$G_{\text{Zin\_}S}(s) = -\frac{Z_{\text{vir}}(s)}{G_{id\_\text{OL}}(s)G_{\text{PWM}}(s)Z_{\text{in\_}L\_\text{ori}}(s)} \frac{1 + T_v(s)}{T_v(s)}. \tag{21}$$

C. Realization of $G_{\text{Zin\_}S}(s)$

By substituting (19) into (21), the required $G_{\text{Zin\_}S}(s)$ for achieving a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in\_}L}|$ is expressed as

$$G_{\text{Zin\_}S}(s) = \begin{cases} \frac{-\left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) + |Z_{\text{in\_}L1}|}{G_{id\_\text{OL}}(s)G_{\text{PWM}}(s)Z_{\text{in\_}L\_\text{ori}}(s)} \frac{1+T_v(s)}{T_v(s)} & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2]. \end{cases} \tag{22}$$

Likewise, by putting (20) to (21), the required $G_{\text{Zin\_}S}(s)$, for ensuring that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in\_}L})| < 180^\circ$ at f_1 and f_2, is derived as

$$G_{\text{Zin\_}S}(s) = \begin{cases} \frac{-\left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) \cdot (e^{j\theta_2} + 1)}{G_{id\_\text{OL}}(s)G_{\text{PWM}}(s)Z_{\text{in\_}L\_\text{ori}}(s)} \frac{1+T_v(s)}{T_v(s)} & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2]. \end{cases} \tag{23}$$

Similar to $G_{\text{Zin\_}P}(s)$, $G_{\text{Zin\_}S}(s)$ is also a frequency-based piecewise function, and the bandpass filter $G_{\text{BPF}}(s)$ can be used to realize $G_{\text{Zin\_}S}(s)$. For achieving a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in\_}L}|$, the required $G_{\text{Zin\_}S}(s)$ can be expressed as

$$G_{\text{Zin\_}S}(s) = \frac{-\left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) + |Z_{\text{in\_}L1}|}{G_{id\_\text{OL}}(s)G_{\text{PWM}}(s)Z_{\text{in\_}L\_\text{ori}}(s)} \times \frac{1 + T_v(s)}{T_v(s)} G_{\text{BPF}}(s). \tag{24}$$

In addition, for ensuring that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in\_}L})| < 180^\circ$ at f_1 and f_2, the required $G_{\text{Zin\_}S}(s)$ can be derived as

$$G_{\text{Zin\_}S}(s) = \frac{-\left(\frac{V_{\text{bus\_ori}}^2}{P_o}\right) \cdot (e^{j\theta_2} + 1)}{G_{id\_\text{OL}}(s)G_{\text{PWM}}(s)Z_{\text{in\_}L\_\text{ori}}(s)} \times \frac{1 + T_v(s)}{T_v(s)} G_{\text{BPF}}(s). \tag{25}$$

As well known, the traditional compensation method regulates the output voltage or current of the load converter and ensures a good dynamic performance. Thus, the load converter behaves as a constant-power load, and its input impedance is regulated to a negative resistor. For the proposed PVI and SVI control strategies, they modify the magnitude or phase of load converter's input impedance only in a small range of frequency to stabilize the cascaded system, and the output voltage or current of the load converter is still well regulated. It should be pointed out that, since the proposed method is achieved by the control, it is only effective below the cutoff frequency of the load converter. However, according to Fig. 2, it is very interesting to find that, if the source converter's output impedance is intersected with the load converter's input impedance outside the cutoff frequency of the load converter, the cascaded system is still stable. Therefore, the proposed method is an effective approach for improving the stability of the cascaded system.

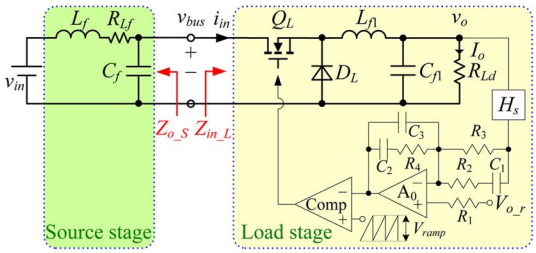


Fig. 10. Cascaded system of example I.

TABLE II
PARAMETERS OF THE CASCADED SYSTEM IN EXAMPLE I

Parameter	L_f	C_f	L_{f1}	C_{f1}	R_{Ld}
Value	700 μH	68 μF	33 μH	2400 μF	1.44Ω
Parameter	R_1	R_2	R_3	R_4	C_1
Value	650Ω	3.3Ω	650Ω	10kΩ	470 nF
Parameter	C_2	C_3	H_s	V_{ramp}	V_{o_r}
Value	30 nF	159 pF	0.1	2.34V	1.2V

V. Design Examples

As illustrated in Section II, the worst instability phenomenon is most likely to occur when the source converter is an LC filter. In addition, buck and boost converters are two typical dc/dc converters, and analog and digital control are two classical implementation methods. Hence, a 100-W cascaded system, which consists of an LC filter and a 48 V−12 V analog-control-based buck converter, and a 200-W cascaded system, which includes an LC filter and a 24 V–48 V digital-control-based boost converter, are discussed in this section.

A. Example I: Cascaded System Consisting of an Input LC Filter and an Analog-Control-Based Buck Converter

A 100-W cascaded system with an input LC filter (source stage) and a 48 V−12 V analog-control-based buck converter (load stage) is designed, which is shown in Fig. 10. The buck converter is operated at 100 kHz. A type-III network is used for the compensator, and the cutoff frequency and phase margin are set to 20 kHz and 45°, respectively. The corresponding system parameters are summarized in Table II.

The output impedance $Z_{o\_S}(s)$ of the input LC filter is given in (26a), where $R_{\rm Lf}$ is the parasitic resistor of L_f, and the measured value is 0.1 Ω. According to the small-signal circuit model of the buck converter [35], $Z_{{\rm in}\_L}(s)$ can be expressed as (26b), where P_o and D are the output power and the duty cycle of the buck converter, respectively. That is,

$$Z_{o\_S}(s)=\frac{sL_f+R_{\rm Lf}}{s^2L_fC_f+sR_{\rm Lf}C_f+1} \tag{26a}$$

$$Z_{{\rm in}\_L}(s)=\left(\frac{-T_v(s)}{1+T_v(s)}\frac{P_o}{V_{\rm bus}^2}+\frac{1}{1+T_v(s)}\times\frac{sC_{f1}D^2+\frac{D^2}{R_{\rm Ld}}}{s^2L_{f1}C_{f1}+s\frac{L_{f1}}{R_{\rm Ld}}+1}\right)^{-1}. \tag{26b}$$

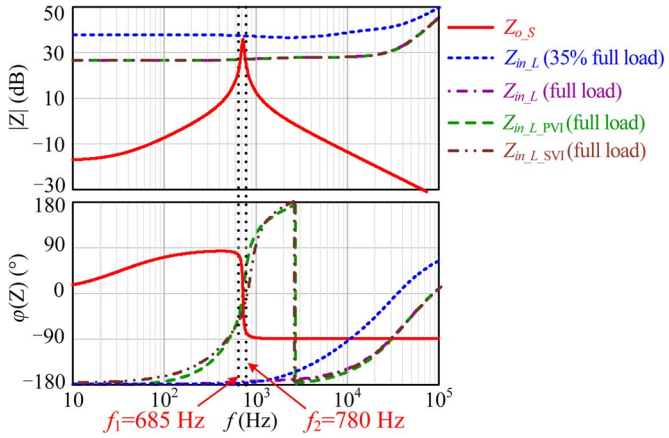


Fig. 11. Bode plot of Z_{o_S} and $Z_{{\rm in}\_L}$ in the cascaded system of example I.

According to (26), the Bode plots of Z_{o_S} and $Z_{{\rm in}\_L}$ at different loads are plotted in Fig. 11. Obviously, when the load is lower than 35% of the full load, Z_{o_S} is less than $Z_{{\rm in}\_L}$; hence, the cascaded system is stable. When the load is higher than 35% of the full load, $|Z_{o\_S}|$ and $|Z_{{\rm in}\_L}|$ are intersected at about 685 Hz and 780 Hz. Since the difference between $\varphi(Z_{o\_S})$ and $\varphi(Z_{{\rm in}\_L})$ is larger than 180° at about 685 Hz, the cascaded system is unstable, and the oscillation will occur at about 685 Hz [36].

As discussed in Section II, changing the magnitude or phase of load converter's input impedance can stabilize the system. For a fair comparison, here, changing the phase of the load converter's input impedance is taken as the example in both PVI and SVI control strategies.

1) Design of PVI Control Strategy: In order to solve the instability problem conveniently, $Z_{{\rm in}\_L}$ is designed to a positive resistor within $[f_1, f_2]$ to ensure that $|\varphi(Z_{o\_S})-\varphi(Z_{{\rm in}\_L})|<180°$. Hence, we let $\theta_2=0$, which will simplify the control circuit.

According to the small-signal circuit model of the buck converter [35], $G_v(s)$, $G_{\rm PWM}(s)$, $G_{vd\_{\rm OL}}(s)$, and $G_{id\_{\rm OL}}(s)$ can be derived as (27), shown at the bottom of the next page.

Since $|T_v(s)|=|G_v(s)G_{\rm PWM}(s)G_{vd\_{\rm OL}}(s)H_s(s)|\gg 1$ within $[f_1, f_2]$, $|T_v(s)|+1\approx T_v(s)|$. Substituting $\theta_2=0$ and (27) into (13), we have

$$G_{{\rm Zin}\_P}(s)=G_{{\rm Zin}\_P1}\cdot P_o\cdot G_{\rm BPF}(s) \tag{28}$$

where

$$G_{{\rm Zin}\_P1}(s)\approx\frac{2H_s(s)R_{\rm Ld}}{V_{\rm bus}V_o\left[s^2L_{f1}C_{f1}+s(R_{\rm Ld}C_{f1}+L_{f1}/R_{\rm Ld})+2\right]}. \tag{29}$$

In $G_{\rm BPF}(s)$, $f_1=685$ Hz and $f_2=780$ Hz, and both Q_H and Q_L are selected to 0.707 for better amplitude–frequency characteristics of $G_{\rm BPF}(s)$.

The Bode plot of the modified input impedance $Z_{{\rm in}\_L\_{\rm PVI}}$ is shown with dashed line in Fig. 11. As shown, $|\varphi(Z_{o\_S})-\varphi(Z_{{\rm in}\_L\_{\rm PVI}})|<180°$ at f_1 and f_2. Therefore, the cascaded system will be stable, and the design of $G_{{\rm Zin}\_P}(s)$ is appropriate.

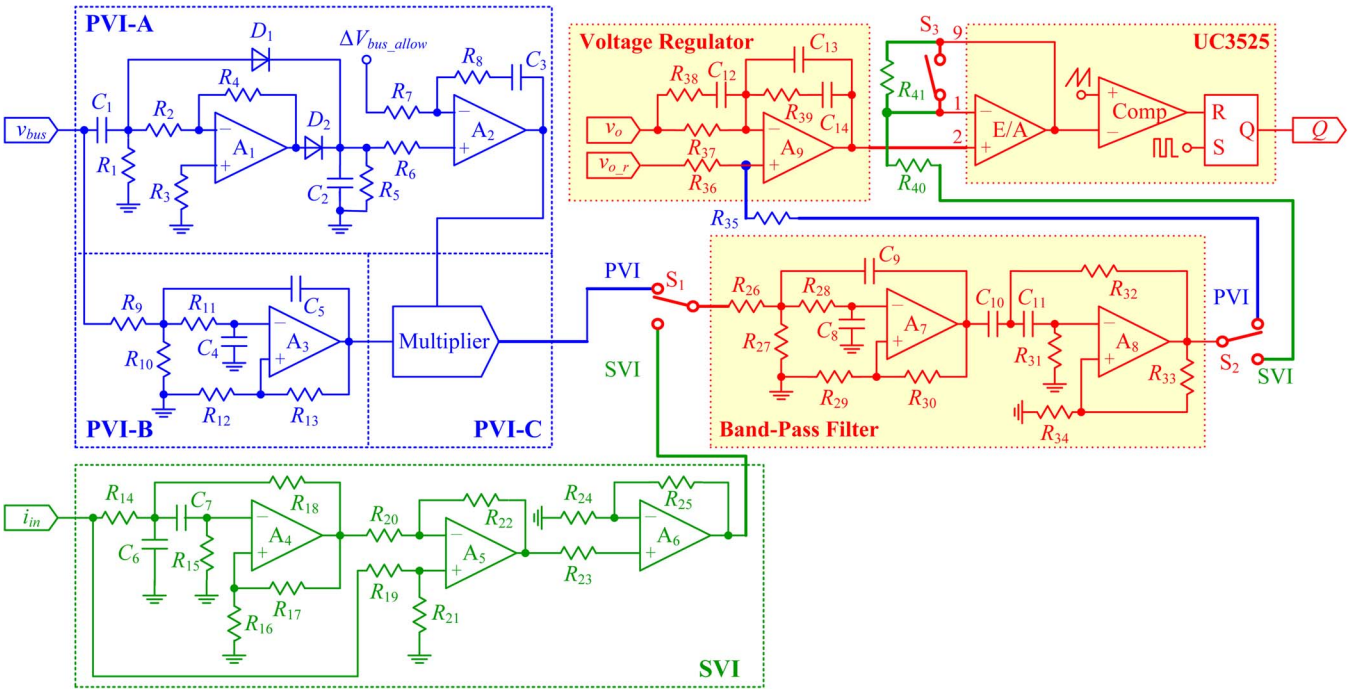


Fig. 12. PVI/SVI control circuit of the load converter.

Fig. 12 shows the circuit implementation of PVI control and SVI control of the load converter. When the single-pole–double-throw switches S_1 and S_2 are connected to the PVI terminals, and the single-pole–single-throw switch S_3 is closed, the circuit is for the PVI control. When S_1 and S_2 are connected to the SVI terminals, and S_3 is opened, the circuit is for the SVI control.

In subcircuit PVI-A, $v_{\rm bus}$ first goes through a high-pass filter comprising C_1 and R_1 to extract $\Delta v_{\rm bus}$, and then, it is sent to the rectifier circuit and a peak value detection circuit, producing the magnitude of $\Delta v_{\rm bus}$. This magnitude is compared with the preset allowable voltage ripple $\Delta V_{\rm bus\_allow}$, and the error is amplified by amplifier A_2. The output of A_2 is adaptively varied by P_o: a large P_o brings a larger $\Delta v_{\rm bus}$, and on the contrary, a smaller P_o gives a smaller $\Delta v_{\rm bus}$. Meanwhile, $v_{\rm bus}$ is sent to subcircuit PVI-B, which is composed of R_9-R_{13}, C_4, C_5, and amplifier A_3, to realize the function of $G_{{\rm Zin}\_P1}(s)$ in (29). Subcircuit PVI-C multiplies the outputs of subcircuits PVI-A and PVI-B, and sends it to the second-order bandpass filter to obtain the output of $G_{{\rm Zin}\_P}(s)$ in (28).

A voltage closed loop is incorporated for regulating the output voltage of the load converter. Specifically, the sum of the output voltage's original reference and the bandpass filter's output is used as the final reference of the load converter's output voltage. The type-III network composed of $R_{36}-R_{39}$, $C_{12}-C_{14}$, and the amplifier A_9 is used as the regulator.

Finally, UC3525 is employed as the pulsewidth modulation (PWM) and drive circuit of the load converter.

Here, since the analog chip AD534 [37] is available in our laboratory, it is utilized to realize the function of multiplier. Compared to the relatively high-cost AD534, some low-cost analog multiplier circuits can be used to implement the same function, as recommended in [38], as well. This would further reduce the cost of the system.

2) Design of the SVI Control Strategy: Similar with the PVI control strategy, $\varphi(Z_{{\rm in}\_L})$ is also chosen as zero within

$$G_v(s)=\frac{s^2(R_2+R_3)R_4C_1C_2+s(R_2C_1+R_3C_1+R_4C_2)+1}{s^3R_2R_3R_4C_1C_2C_3+s^2R_3\left[R_4C_2C_3+R_2C_1(C_2+C_3)\right]+s(C_2+C_3)R_3} \tag{27a}$$

$$G_{\rm PWM}(s)=\frac{1}{V_{\rm ramp}} \tag{27b}$$

$$G_{vd\_{\rm OL}}(s)=\frac{V_{\rm bus}}{\left[s^2L_{f1}C_{f1}+s\left(\frac{L_{f1}}{R_{\rm Ld}}\right)+1\right]} \tag{27c}$$

$$G_{id\_{\rm OL}}(s)=\frac{DV_{\rm bus}}{R_{\rm Ld}}\left[1+\frac{1+sR_{\rm Ld}C_{f1}}{s^2L_{f1}C_{f1}+sL_{f1}/R_{\rm Ld}+1}\right] \tag{27d}$$

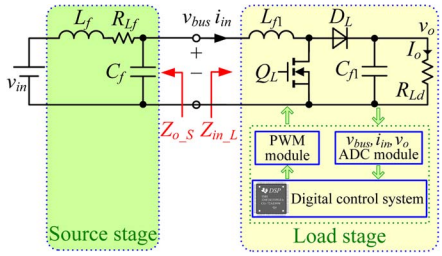


Fig. 13. Cascaded system of example II.

$[f_1, f_2]$ to ensure that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$. Hence, we let $\theta_2 = 0$. Similarly, $G_{\text{Zin}\_S}(s)$ can be derived as

$$G_{\text{Zin}\_S}(s) = G_{\text{Zin}\_S1} G_{\text{BPF}}(s) \tag{30}$$

where

$$G_{\text{Zin}\_S1} \approx \left(1 - \frac{1 + sR_{\text{Ld}}C_{f1}}{s^2 L_{f1}C_{f1} + s(L_{f1}/R_{\text{Ld}} + R_{\text{Ld}}C_{f1}) + 2}\right) \times \frac{2V_{\text{ramp}}R_{\text{Ld}}}{DV_{\text{bus}}}. \tag{31}$$

In addition, for $G_{\text{BPF}}(s)$, $f_1 = 685$ Hz and $f_2 = 780$ Hz, and $Q_H = Q_L = 0.707$.

The Bode plot of the improved input impedance $Z_{\text{in}\_L\_\text{SVI}}$ is also shown with double-dashed line in Fig. 11. As shown, $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L\_\text{SVI}})| < 180°$ at f_1 and f_2. Therefore, the improved cascaded system is stable, and the design of $G_{\text{Zin}\_S}(s)$ is effective.

Fig. 12 describes the detailed SVI control circuit of the load converter, where S_1 and S_2 are connected to the SVI terminals, and S_3 is opened. The subcircuit SVI employs R_{14}–R_{25}, C_6, C_7, and amplifiers A_4–A_6 to realize the function of $G_{\text{Zin}\_S1}(s)$ in (31). The output of the subcircuit SVI is sent to the second-order bandpass filter to obtain the output of $G_{\text{Zin}\_S}(s)$ in (30), which is subtracted from the output of the voltage regulator through the operational amplifier inside UC3525, forming the modulation signal. UC3525 is again used as the PWM and produces the drive signal of the power switch of the load converter.

B. Example II: Cascaded System Consisting of an Input LC Filter and a Digital-Control-Based Boost Converter

Fig. 13 shows a 200-W cascaded system consisting of an input LC filter (source stage) and a 24 V–48 V digital-control-based boost converter (load stage) operated at 100 kHz. Since the boost converter is a nonminimum phase system, a proportional–integral controller is employed as the compensator, and the cutoff frequency and phase margin are set to 2.5 kHz and 32°, respectively. The corresponding system parameters are summarized in Table III.

The output impedance $Z_{o\_S}(s)$ of the input LC filter has been given in (26a). According to the small-signal circuit model of the boost converter [35], $Z_{\text{in}\_L}(s)$ can be expressed as

$$Z_{\text{in}\_L}(s) = \left(\frac{-T_v(s)}{1 + T_v(s)} \frac{P_o}{V_{\text{bus}}^2} + \frac{1}{1 + T_v(s)} \cdot \frac{sC_{f1}R_{\text{Ld}} + 1}{s^2 L_{f1}C_{f1} + R_{\text{Ld}} + sL_{f1} + R_{\text{Ld}}(1-D)^2}\right)^{-1} \tag{32}$$

TABLE III
PARAMETERS OF THE CASCADED SYSTEM IN EXAMPLE II

Parameter	L_f	C_f	L_{f1}	C_{f1}
Value	250 μH	330 μF	720 μH	450 μF
Parameter	R_{Ld}	k_p	k_i	
Value	11.52 Ω	15	450	

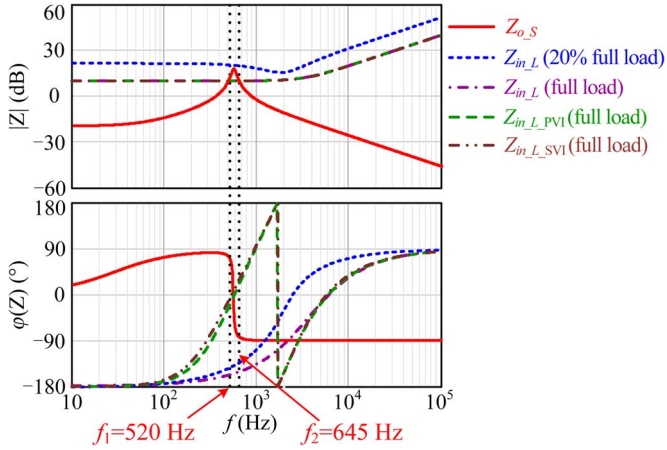


Fig. 14. Bode plot of Z_{o_S} and Z_{in_L} in the cascaded system of example II.

where D and P_o are the duty cycle and output power of the boost converter, respectively.

According to (26a) and (32), Fig. 14 plots the Bode plots of Z_{o_S} and Z_{in_L} at different loads. As shown, when the load is lower than 20% of the full load, there will be a total separation of $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$; the cascaded system is stable. Otherwise, there are intersections between $|Z_{o\_S}|$ and $|Z_{\text{in}\_L}|$, and the two intersection frequencies are about 520 Hz and 645 Hz. Considering that the difference between $\varphi(Z_{o\_S})$ and $\varphi(Z_{\text{in}\_L})$ is larger than 180° at about 520 Hz, the cascaded system is unstable, and the oscillation will appear at about 520 Hz [36].

Similar to example I, both the PVI and SVI control strategies change the phase of the load converter's input impedance in example II.

1) Design of PVI Control Strategy: In order to solve the instability problem conveniently, Z_{in_L} is designed to a positive resistor within $[f_1, f_2]$ to ensure that $|\varphi(Z_{o\_S}) - \varphi(Z_{\text{in}\_L})| < 180°$, i.e., θ_2 is set to 0.

According to the small-signal circuit model of the boost converter [35], $G_v(s)$, $G_{\text{PWM}}(s)$, $G_{vd\_\text{OL}}(s)$, and $G_{id\_\text{OL}}(s)$ can be expressed as

$$G_v(s) = k_p + \frac{k_i}{s} \tag{33a}$$

$$G_{\text{PWM}}(s) = \frac{1}{V_{\text{ramp}}} \tag{33b}$$

$$G_{vd\_\text{OL}}(s) = \frac{V_{\text{bus}}\left[R_{\text{Ld}} - \frac{sL_{f1}}{(1-D)^2}\right]}{s^2 L_{f1}C_{f1}R_{\text{Ld}} + sL_{f1} + R_{\text{Ld}}(1-D)^2} \tag{33c}$$

$$G_{id\_\text{OL}}(s) = \frac{V_o(sC_{f1}R_{\text{Ld}} + 2)}{s^2 L_{f1}C_{f1}R_{\text{Ld}} + sL_{f1} + R_{\text{Ld}}(1-D)^2}. \tag{33d}$$

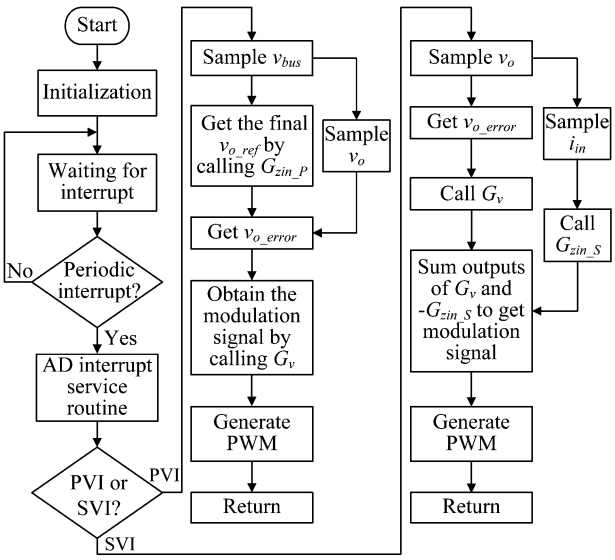


Fig. 15. Software flowchart of the PVI and SVI control algorithm.

Since $|T_v(s)|=|G_v(s)G_{\rm PWM}(s)G_{vd\_OL}(s)H_s(s)|\gg 1$ during $[f_1, f_2]$, $|T_v(s)|+1\approx|T_v(s)|$. Substituting $\theta_2=0$ and (33) into (13), $G_{{\rm Zin}\_P}(s)$ can be derived as

$$G_{{\rm Zin}\_P}(s)\approx G_{{\rm Zin}\_P1}(s)G_{\rm BPF}(s) \tag{34}$$

where

$$G_{{\rm Zin}\_P1}(s)=\frac{2H_s(s)P_o}{V_{\rm bus}V_o}\frac{R_{\rm Ld}-sL_{f1}/(1-D)^2}{sC_{f1}R_{\rm Ld}+2}. \tag{35}$$

In addition, for $G_{\rm BPF}(s)$, $f_1=520$ Hz and $f_2=645$ Hz, and $Q_H=Q_L=0.707$.

The Bode plot of the improved input impedance $Z_{{\rm in}\_L\_{\rm PVI}}$ is shown with dashed line in Fig. 14. As shown, $|\varphi(Z_{o\_S})-\varphi(Z_{{\rm in}\_L\_{\rm PVI}})|<180^\circ$ at f_1 and f_2. Therefore, the improved cascaded system is stable, and the design of $G_{{\rm Zin}\_P}(s)$ is appropriate.

The PVI control system was implemented by a DSP TMS320F28335. Fig. 15 shows the flowchart of its mechanism. As shown, the input voltage $v_{\rm bus}$ and the output voltage v_o of the load converter are sampled to provide the necessary information for the PVI control and to calculate the final reference of output voltage. With the calculated reference of v_o, the output voltage of the load converter is regulated by the compensator $G_v(s)$.

2) Design Example of the SVI Control Strategy: In this example, similar to the PVI control strategy, $\varphi(Z_{{\rm in}\_L})$ is also chosen as zero within $[f_1, f_2]$ to ensure that $|\varphi(Z_{o\_S})-\varphi(Z_{{\rm in}\_L})|<180^\circ$; hence, θ_2 is set to 0, and $G_{{\rm Zin}\_S}(s)$ can be derived and simplified as

$$G_{{\rm Zin}\_S}(s)\approx G_{{\rm Zin}\_S1}(s)G_{\rm BPF}(s) \tag{36}$$

where

$$G_{{\rm Zin}\_S1}(s)=\frac{2V_{\rm ramp}\left[s^2L_{f1}C_{f1}R_{\rm Ld}+sL_{f1}+R_{\rm Ld}(1-D)^2\right]}{V_o(sC_{f1}R_{\rm Ld}+2)}. \tag{37}$$

For $G_{\rm BPF}(s)$, here, $f_1=520$ Hz and $f_2=645$ Hz, and $Q_H=Q_L=0.707$.

The Bode plot of the improved input impedance $Z_{{\rm in}\_L\_{\rm SVI}}$ is also shown with double-dashed line in Fig. 14. As shown, $|\varphi(Z_{o\_S})-\varphi(Z_{{\rm in}\_L\_{\rm SVI}})|<180^\circ$ at f_1 and f_2. Therefore, the improved cascaded system is stable, and the design of $G_{{\rm Zin}\_S}(s)$ is effective.

Similar to the PVI control method, the SVI control system was also implemented by a DSP TMS320F28335. The flowchart of its mechanism is also given in Fig. 15.

As shown in Fig. 15, the input current $i_{\rm in}$ and the output voltage v_o of the load converter are sampled to provide the necessary information for the SVI control and to output voltage regulation. The algorithm obtained the modulation signal by subtracting the output of $G_{{\rm Zin}\_S}(s)$ from the output of $G_v(s)$. Then, it generated the PWM signal by PWM module.

C. Comparison of Analog and Digital Implementations of the Proposed Control Strategies

As discussed earlier, both the PVI and SVI control strategies can be realized by analog circuits or digital algorithm. Generally speaking, the analog chips are often cheaper than digital chips, and hence, the analog implementation is more affordable than digital realization. In addition, since the analog control system does not suffer the delay problem existing in the digital control system, the proposed method is expected to have a better performance with analog control. Furthermore, the execution time of the program cannot be ignored for the dc/dc converter in practice, i.e., the digital control limits the allowed maximum switching frequency of the dc/dc converter. For instance, in example II, the total call and execution time of the PVI control program is 4.5 μs; thus, the load converter's maximum switching frequency is limited to 222 kHz. Therefore, from the perspective of cost, performance, and constraints, the analog implementation is better than digital implementation.

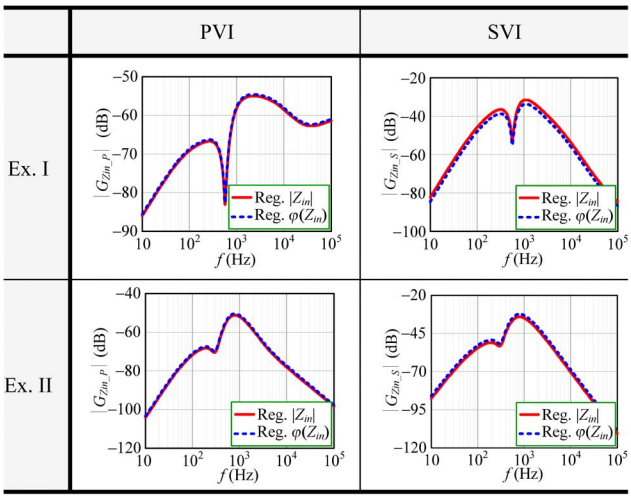
However, considering that the expressions of $G_{{\rm Zin}\_P}(s)$ and $G_{{\rm Zin}\_S}(s)$ are slightly complex, the proposed strategies are easier to be realized by digital algorithm rather than analog circuits.

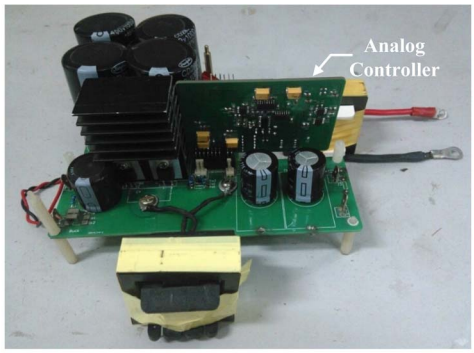
As mentioned in Section II, regulating either the magnitude or the phase of the load converter's input impedance can stabilize the system. However, according to Sections III and IV, the design of PVI and SVI control strategies via regulating the magnitude of the load converter's input impedance is similar to that via regulating the phase of the load converter's input impedance. In addition, as shown in Table IV, this section also gives the Bode plots of $G_{\rm Zin}(s)$ with changing the magnitude and phase methods in examples I and II. It shows that, although the two methods have different physical concepts, their actual impact on the load converter is indeed very similar. Therefore, considering the aforementioned reasons and space limit, the detailed design procedure and demonstration of the regulating magnitude method is not presented here.

VI. Experimental Verification

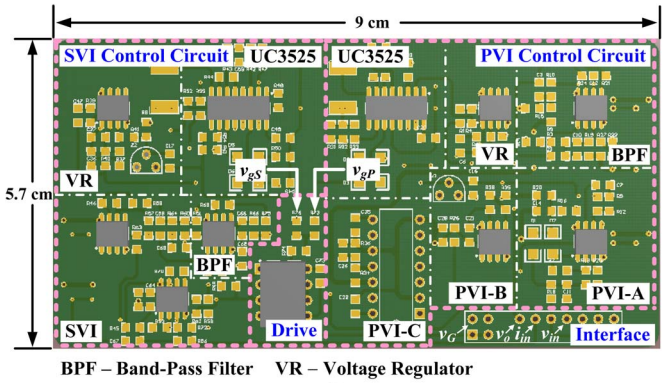
According to the design examples, two prototypes have been fabricated and tested in the laboratory to verify the validity of the proposed control strategies.

TABLE IV
COMPARISON OF $G_{\mathrm{Zin}}(S)$ WITH CHANGING THE MAGNITUDE AND PHASE METHODS IN EXAMPLES I AND II





(a)

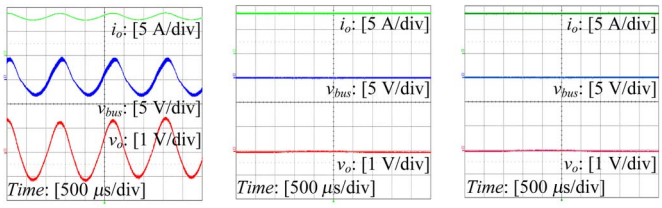


(b)

Fig. 16. Photograph of the prototype. (a) Prototype. (b) PCB of the analog controller.

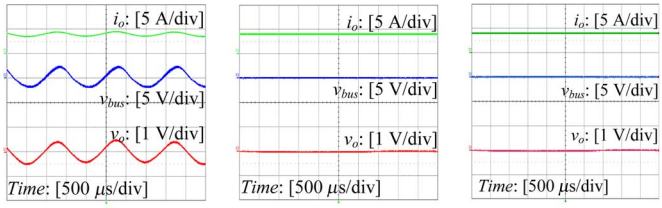
A. Prototype I: Cascaded System Consists of an Input LC Filter and an Analog-Controlled Buck Converter

Prototype I is a 100-W cascaded system consisting of an input LC filter and a 48 V−24 V analog-controlled buck converter. Fig. 16(a) shows its photograph. Note that both PVI and SVI control circuits are laid out in one printed circuit board (PCB), as shown in Fig. 16(b), where the detailed information of the corresponding subcircuits in Fig. 12 is also marked.



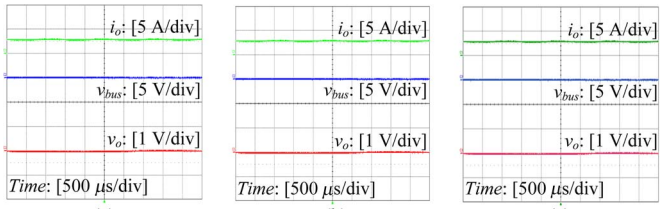
(a) (b) (c)

Fig. 17. Experimental waveforms at full load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.



(a) (b) (c)

Fig. 18. Experimental waveforms at half load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.



(a) (b) (c)

Fig. 19. Experimental waveforms at 35% full load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.

The experimental results of the cascaded system without proposed control strategies, with PVI control strategy, and with SVI control strategy, at different loads, are given in Figs. 17–19, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation. As shown in Figs. 17(a) and 18(a), the cascaded system is unstable at full load and half load when the proposed control strategies are absent, and the oscillating frequencies of the bus voltage and output voltage are both about 685 Hz, which is coincided with the conclusion in Fig. 11. It is worth noting that, although the cascaded system is unstable, the system can only operate with an underdamped resonance instead of divergent resonance. This can be explained as follows. If the system is unstable, the converter's inductor current starts to diverge. When it reduces to zero, the converter will operate in discontinuous current mode (DCM). Fortunately, in DCM, the converter's order is reduced, and the whole system could readily return to stable operation. As a result, the current ceases to diverge and converges again. Finally, the system will find an equilibrium state and behave as underdamped resonance. As shown in Figs. 17(b) and (c) and 18(b) and (c), when the PVI or SVI control strategy is incorporated, the

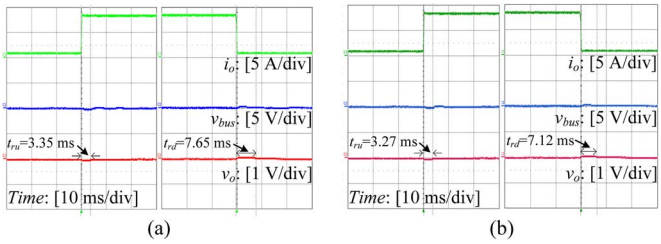


Fig. 20. Dynamic waveforms of the system when the load steps between full load and 10% full load. (a) PVI control strategy. (b) SVI control strategy.

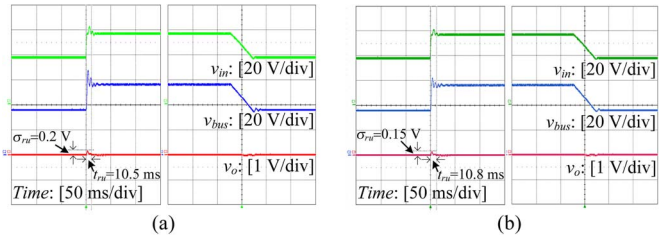


Fig. 21. Dynamic waveforms of the system when the input voltage steps between 80% and 120% rated voltage. (a) PVI control strategy. (b) SVI control strategy.

cascaded system becomes stable at full load and half load, and no oscillation occurs in $v_{\rm bus}$ and v_o. Fig. 19(a) shows the experimental waveforms of i_o, $v_{\rm bus}$, and v_o at 35% full load without the proposed control strategy. It shows that the cascaded system is stable, which is consistent with Fig. 11. In addition, as shown in Fig. 19(b) and (c), the cascaded system is also stable when the PVI or SVI control strategy is utilized.

Fig. 20 shows the dynamic performance of the cascaded system, when its load steps between 10% and 100% full load at the rated input voltage (48 V). It can be found that the dynamic performances of the cascaded system with PVI control strategy and with SVI control strategy are both good. It is worth explaining that, since the proposed control strategies are aimed to the load converter, the dynamic performance of the source converter is not affected.

Fig. 21 shows the dynamic performance of the cascaded system, when its input voltage steps between 80% and 120% rated voltage at full load. It shows that the dynamic performances of the cascaded system with PVI control strategy and with SVI control strategy are both good. Note that the dc power supply "Chroma 62012P-80-60" is utilized to program the input voltage of the cascaded system, and it is a unidirectional dc power supply. Therefore, it takes a short time to step $v_{\rm in}$ up from 80% to 120% rated voltage but spends a relatively long time to step $v_{\rm in}$ down from 120% to 80% rated voltage, which is found in Fig. 21. This phenomenon is common for all the unidirectional dc power supplies.

In summary, the experimental results given in Figs. 17–21 show that both PVI control strategy and SVI control strategy are valid solutions to instability of prototype I. In addition, the proposed methods not only stabilize the system but also keep a good dynamic performance.

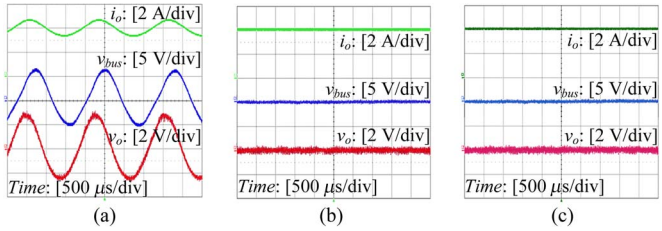


Fig. 22. Experimental waveforms at full load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.

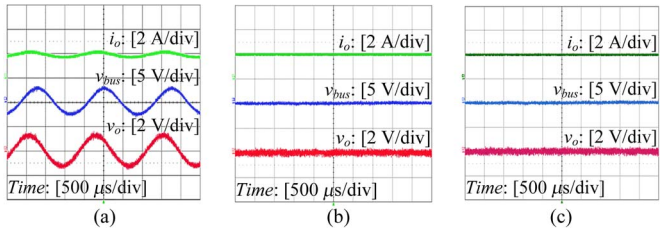


Fig. 23. Experimental waveforms at half load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.

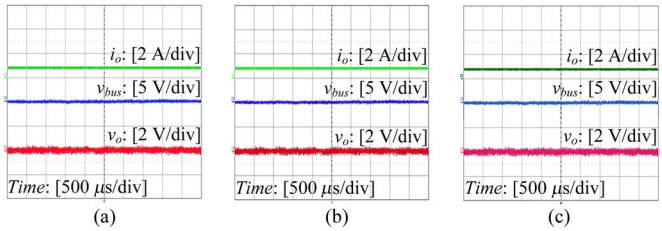


Fig. 24. Experimental waveforms at 20% full load. (a) Without the proposed control strategies. (b) With PVI control strategy. (c) With SVI control strategy.

B. Prototype II: Cascaded System Consists of an Input LC Filter and a Digital-Controlled Boost Converter

Here, a 200-W cascaded system with an input LC filter and a 24 V−48 V digital-control-based boost converter is built. The topology, parameters, and control algorithm have already been discussed in Section V-B.

The experimental results of the cascaded system without the proposed control strategies, with PVI control strategy, and with SVI control strategy, at different loads, are given in Figs. 22–24, where the waveforms of $v_{\rm bus}$ and v_o are their ac components to clearly show the oscillation. In Figs. 22(a) and 23(a), the cascaded system is unstable at full load and half load when the proposed control strategies are absent, and the oscillating frequencies of the bus voltage and output voltage are both about 520 Hz, which is consistent with the conclusion in Fig. 14. The reason why the unstable system is operating with an underdamped resonance instead of divergent resonance is already explained in Section VI-A, which is not repeated here. As shown in Figs. 22(b) and (c) and 23(b) and (c), when the PVI or SVI control strategy is introduced, the cascaded system becomes stable at full load and half load, and no oscillation

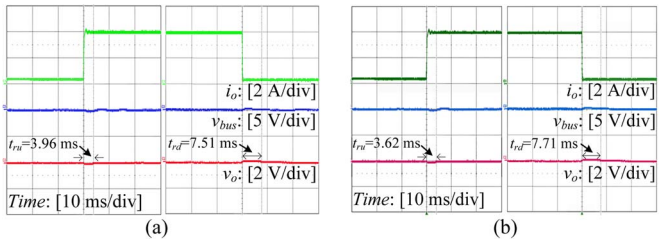


Fig. 25. Dynamic waveforms of the system, when its load steps between 10% and 100% full load. (a) With PVI control strategy. (b) With SVI control strategy.

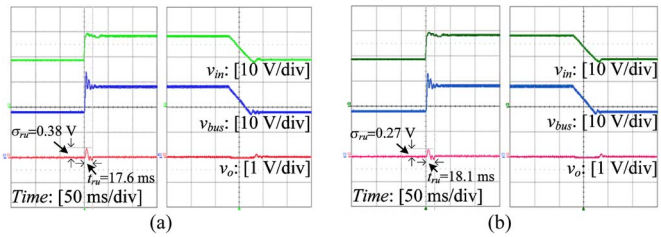


Fig. 26. Dynamic waveforms of the system, when its input voltage steps between 80% and 120% rated voltage. (a) With PVI control strategy. (b) With SVI control strategy.

occurs in $v_{\rm bus}$ and v_o. Fig. 24(a) shows the experimental waveforms of i_o, $v_{\rm bus}$, and v_o at 20% full load without the proposed control strategy. It shows that the cascaded system is stable, which is consistent with Fig. 14. In addition, as shown in Fig. 24(b) and (c), the cascaded system is also stable when the PVI or SVI control strategy is utilized.

Fig. 25 shows the dynamic waveforms of the cascaded system, when its load steps between 10% and 100% full load at the rated input voltage (24 V). As shown, the dynamic performances of the cascaded system with PVI control strategy and with SVI control strategy are both good.

Fig. 26 shows the dynamic performance of the cascaded system when the input voltage steps between 80% and 120% rated voltage at full load. It shows that the dynamic performances of the cascaded system with PVI control strategy and with SVI control strategy are both good. Similar to Fig. 21, it takes a short time to step $v_{\rm in}$ up but spends a relatively long time to step $v_{\rm in}$ down.

In summary, the experimental results given in Figs. 22–26 show that both PVI control strategy and SVI control strategy are valid solutions to instability of prototype II. In addition, the proposed methods keep a good dynamic performance.

According to the aforementioned two examples, it proves that the proposed control strategies are effective and feasible in practice.

VII. Comparison and Design Procedure of the Proposed Control Strategy

Goals of both the PVI and SVI control strategies are realizing the stability-preferred input impedance in Fig 3. Hence, in essence, they have the same stabilize ability for the cascaded system. In addition, considering the PVI and SVI control strategies changing load converter's input impedance in the same frequency range, their influences on the load converter's dynamic performance are almost the same. The experimental results proved the aforementioned points as well. The only difference between the two strategies is that the PVI control strategy requires an additional input voltage sensor of the load converter, while the SVI control strategy requires an additional input current sensor. Table V compares the features of the PVI and SVI methods, including stabilize ability, dynamic performance, cost, and price.

TABLE V
Comparison of PVI and SVI Control Strategies

Control Strategy	Stabilize ability	Dynamic performance	Cost	Price
PVI	Same*	Same*	Low†	Need an additional input voltage sensor
SVI	Same*	Same*	Low†	Need an additional input current sensor

* Please see the experimental results in section VI; † Can use analog control circuit.

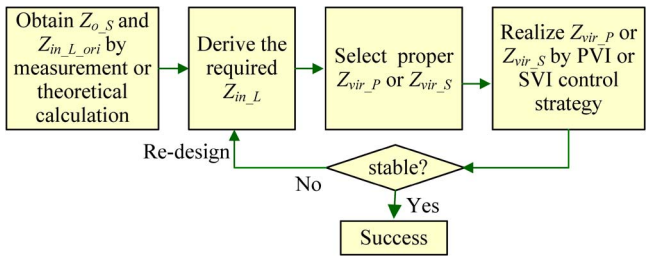


Fig. 27. General design steps of PVI and SVI control strategies.

Moreover, in order to popularize the proposed strategies, a general design procedure of PVI and SVI control strategies is presented in Fig. 27.

VIII. Conclusion

In order to solve the instability problem of the cascaded system, a set of virtual-impedance-based control strategies, i.e., PVI and SVI control strategies, has been proposed in this paper. Our study shows that the proposed strategies modify the input impedance of the load converter only in a small range of frequencies. Therefore, it not only stabilizes the whole system but also ensures a good dynamic performance of the load converter. Furthermore, the proposed methods can be realized by analog control circuit or digital control algorithm without the help of the source converter; thus, our approaches are feasible in practice. Finally, a general design procedure is introduced to popularize the proposed strategies, and two example systems are fabricated to validate the correctness of our methods.

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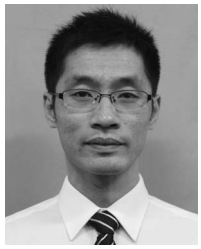

Xin Zhang (M'15) received the B.S. and Ph.D. degrees in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2007 and 2014, respectively. He is currently working toward the Ph.D. degree in automatic control and systems engineering at The University of Sheffield, Sheffield, U.K.

He is also currently a Research Associate with The University of Sheffield. His main research interests include soft-switching dc/dc converters, modeling of dc/dc converters, and reliability and stability of distributed power systems.

Xinbo Ruan (M'97–SM'02) received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the College of Automation Engineering, NUAA, where he became a Professor in 2002. From 2008 to 2011, he was also with the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China. He is the author or coauthor of seven books and more than 180 technical papers published in journals and conference proceedings. His main research interests include soft-switching power electronics converters, power electronics system integration, and renewable energy generation systems.

Prof. Ruan served as Vice President of the China Power Supply Society from 2005 to 2013. He has been an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS since 2011 and 2013, respectively.

Qing-Chang Zhong (M'04–SM'04) received the Ph.D. degree in control theory and engineering from Shanghai Jiao Tong University, Shanghai, China, in 2000 and the Ph.D. degree in control and power engineering from Imperial College London, London, U.K., in 2004.

He is the Max McGraw Endowed Chair Professor in Energy and Power Engineering with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA, and the Research Professor in Control of Power Systems with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield, U.K. He (co)authored three research monographs, including *Control of Power Inverters in Renewable Energy and Smart Grid Integration* (Wiley-IEEE Press, 2013). His research focuses on power electronics and advanced control theory, together with their applications in various sectors.

Dr. Zhong is a Distinguished Lecturer of both the IEEE Control Systems Society and the IEEE Power Electronics Society. He serves as an Associate Editor for the IEEE TRANSACTIONS ON AUTOMATIC CONTROL, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY, IEEE ACCESS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and *European Journal of Control*.