# Optimized Operation of Current-Fed Dual Active Bridge DC–DC Converter for PV Applications

Yuxiang Shi, *Student Member, IEEE*, Rui Li, *Member, IEEE*,
Yaosuo Xue, *Senior Member, IEEE*, and Hui Li, *Senior Member, IEEE*

***Abstract*—The current-fed dual active bridge (CF-DAB) dc–dc converter gains growing applications in photovoltaic (PV) and energy storage systems due to its advantages, e.g., a wide input voltage range, a high step-up ratio, a low input current ripple, and a multiport interface capability. In addition, the direct input current controllability and extra control freedom of the CF-DAB converter make it possible to buffer the double-line-frequency energy in grid-interactive PV systems without using electrolytic capacitors in the dc link. Therefore, a PV system achieves high reliability and highly efficient maximum power point tracking. This paper studies the optimized operation of a CF-DAB converter for a PV application in order to improve the system efficiency. The operating principle and soft-switching conditions over the wide operating range are thoroughly analyzed with phase-shift control and duty-cycle control, and an optimized operating mode is proposed to achieve the minimum root-mean-square transformer current. The proposed operating mode can extend the soft-switching region and reduce the power loss, particularly under a heavy load and a high input voltage. Moreover, the efficiency can be further improved with a higher dc-link voltage. A 5-kW hardware prototype was built in the laboratory, and experimental results are provided for verification. This paper provides a design guideline for the CF-DAB converter applied to PV systems, as well as other applications with a wide input voltage variation.**

***Index Terms*—Current-fed dual active bridge (CF-DAB), optimized operation, photovoltaic (PV), root-mean-square (RMS) current, soft switching.**

## I. Introduction

DUAL active bridge (DAB) dc–dc converters have been popular for various applications over the past two decades due to the advantages of high-frequency galvanic isolation, soft-switching characteristic, and bidirectional power flow [1]–[10]. Moreover, it can be easily extended to multiterminal topologies to integrate dc sources, energy storage devices, or loads [11]–[13]. However, to achieve high efficiency, a wide zero-voltage switching (ZVS) range and low circulating energy are both desired for the converter, which are in conflict with each other. Therefore, many efforts have been devoted to improve the performance of DAB converters [14]–[23].

For a traditional DAB converter with phase-shift modulation [1], the ZVS range is limited by the voltage conversion ratio and load conditions [14]. Reference [15] introduced duty-cycle modulation in one side of a DAB converter to extend the ZVS range and reduce the transformer RMS current. Dual phase shift (DPS) control methods were proposed to reduce the reactive current using additional phase-shift control inside H bridges [16]–[18]. Optimal phase-shift pairs with extended DPS control were further proposed to minimize nonactive power loss [19]. In [2] and [20], advanced modulation methods such as trapezoidal modulation (TZM) and triangular modulation (TRM) have been presented, where the transformer current is modulated in triangular or trapezoidal waveforms to reduce the conduction and the switching loss. A hybrid modulation strategy combining different existing modulation schemes in [21] and [22], and hybrid modulations with a variable switching frequency in [23] were reported, which further improve the efficiency over a wide operating range. With these modulation methods, the performance and efficiency of a DAB converter can be greatly improved. However, all these methods are specific for a voltage-fed DAB (VF-DAB) converter and are not applicable for current-fed DAB (CF-DAB) converters due to the more complicated operating principle and ZVS conditions of the latter [24], [25].

CF-DAB converters gain growing recognition in photovoltaic (PV) and energy storage applications [26]–[30]. Compared with a VF-DAB converter, a CF-DAB converter has unique advantages, e.g., a wide input voltage range, a high step-up ratio, a low input current ripple, and a multiport interface, which make the topology suitable for PV applications [29]. With direct input current controllability and extra control freedom, a CF-DAB converter allows using a small dc-link capacitor instead of a large electrolytic capacitor, without affecting the input PV side, in grid-interactive PV systems, where double-line-frequency energy oscillation exists [29], [30]. Therefore, a PV system can achieve high reliability and highly efficient maximum power point tracking.

Manuscript received October 29, 2014; revised February 10, 2015; accepted April 2, 2015. Date of publication May 12, 2015; date of current version October 7, 2015.

Y. Shi and H. Li are with the Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL 32310 USA (e-mail: shi@caps.fsu.edu; hli@caps.fsu.edu).

R. Li is with the Department of Electrical and Computer Engineering, Center for Advanced Power Systems, College of Engineering, Florida State University, Tallahassee, FL 32310 USA, and also with the Department of Electrical Engineering, Information and Electrical Engineering, School of Electronics, Shanghai Jiao Tong University, Shanghai 200240 China (e-mail: rli@caps.fsu.edu).

Y. Xue is with Siemens Corporate Technology, Princeton, NJ 08540 USA (e-mail: yaosuo.xue@siemens.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2015.2432093

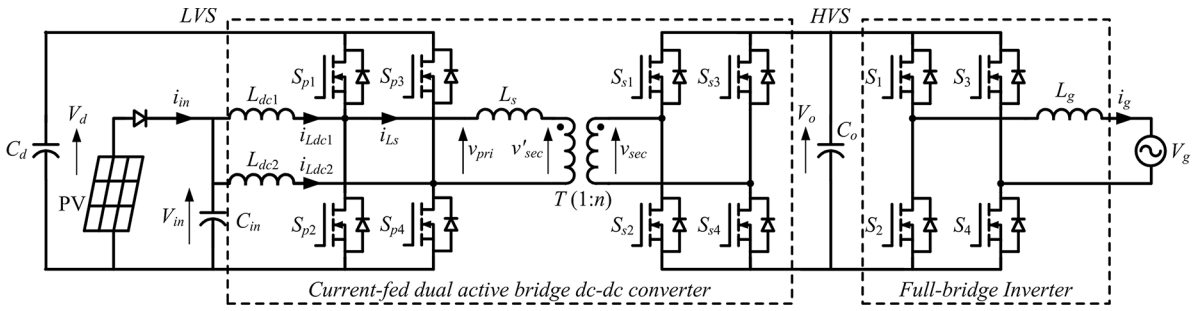



Fig. 1. CF-DAB dc–dc converter for a PV application.

There are few studies on optimizing the operation of a CF-DAB converter with soft-switching conditions, whereas some methods have been reported to optimize the operation of current-fed-type isolated dc–dc converters. A phase shift with duty-cycle modulation was proposed for a current–voltage-fed bidirectional dc–dc converter in [31]. A voltage balancing strategy adjusting the duty cycle that minimizes the transformer peak current is implemented to reduce the circulating energy. Nonetheless, the circulating energy is still relatively large. In [32], an RMS-current-optimized operation mode was proposed for a current-fed dual half-bridge (CF-DHB) dc–dc converter in energy storage applications. However, a CF-DHB converter is not suitable for high-power applications, and a CF-DAB converter is quite different from a CF-DHB converter due to extra operating modes and a different ZVS operating range.

This paper proposes an optimized operating mode for a CF-DAB converter in a PV application, which minimizes the transformer RMS current and extends the soft-switching operating range. The analysis and experimental results show that this operating mode extends the ZVS range and gives less power loss, particularly under a heavy load and a high input voltage. In addition, the efficiency and the performance can be further improved if a higher dc-link voltage can be applied. The rest of this paper is organized as follows. In Section II, the operating principle of a CF-DAB converter with duty-cycle control plus phase-shift control is presented over the whole operating range, as well as the analysis of soft-switching conditions. The proposed optimized operating mode is described in detail and compared with the minimum-peak-current mode, i.e., the "$d = 1$" mode, in Section III. The influence of the dc-link voltage on the converter performance is also addressed. A 5-kW hardware prototype was built in the laboratory, and experimental results are provided for verification in Section IV. Finally, conclusions are drawn in Section V.

## II. Operation Principle Analysis of CF-DAB PV Converter

Fig. 1 shows a simplified converter module of the CF-DAB dc–dc-converter-based grid-connected cascaded multilevel PV system in [30]. The front-end CF-DAB dc–dc converter provides galvanic isolation and boosts the PV voltage to a suitable level so that both the dc–dc converter and the inverter can operate efficiently. Since the potential of efficiency improvement is limited for a traditional H-bridge inverter, the total efficiency of the PV converter largely depends on the optimized operation of the dc–dc stage. The analysis of the CF-DAB converter covering all the operating range has not been reported before. Although the operating principle of the "3+1"-port bidirectional isolated dc–dc converter had been analyzed in [28], the topology is different. Two operation modes of the CF-DAB converter had been introduced in [29]; nonetheless, other operation modes and the soft-switching condition analysis have not been included. Therefore, the operating principle and the soft-switching condition are thoroughly analyzed in this section in order to derive the optimized operation in Section III. Considering a wide input voltage operating range of PV applications, 50%–100% variation of the PV voltage is taken into account in this paper.

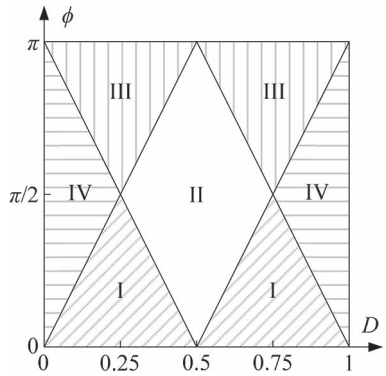



Fig. 2. Operating areas of the CF-DAB converter.

### A. Operation Principle of CF-DAB DC–DC Converter

The operating range of the CF-DAB converter with a positive power flow is illustrated in Fig. 2, where duty cycle $D$ varies from [0, 1], and phase-shift angle $\phi$ varies from [0, $\pi$]. There are seven subareas that can be combined into four operating modes symmetrically, and each one has two conditions, i.e., $D < 0.5$ and $D > 0.5$. The key waveforms of the CF-DAB dc–dc converter in each mode are depicted in Fig. 3. For a negative power flow, the operating principle can be derived symmetrically. Although the transformer voltage and the current patterns are similar to those of a VF-DAB converter, the operating principle for the CF-DAB converter is different due to the additional dc inductor current flow through the low-voltage side (LVS) bridges, resulting in different ZVS conditions.

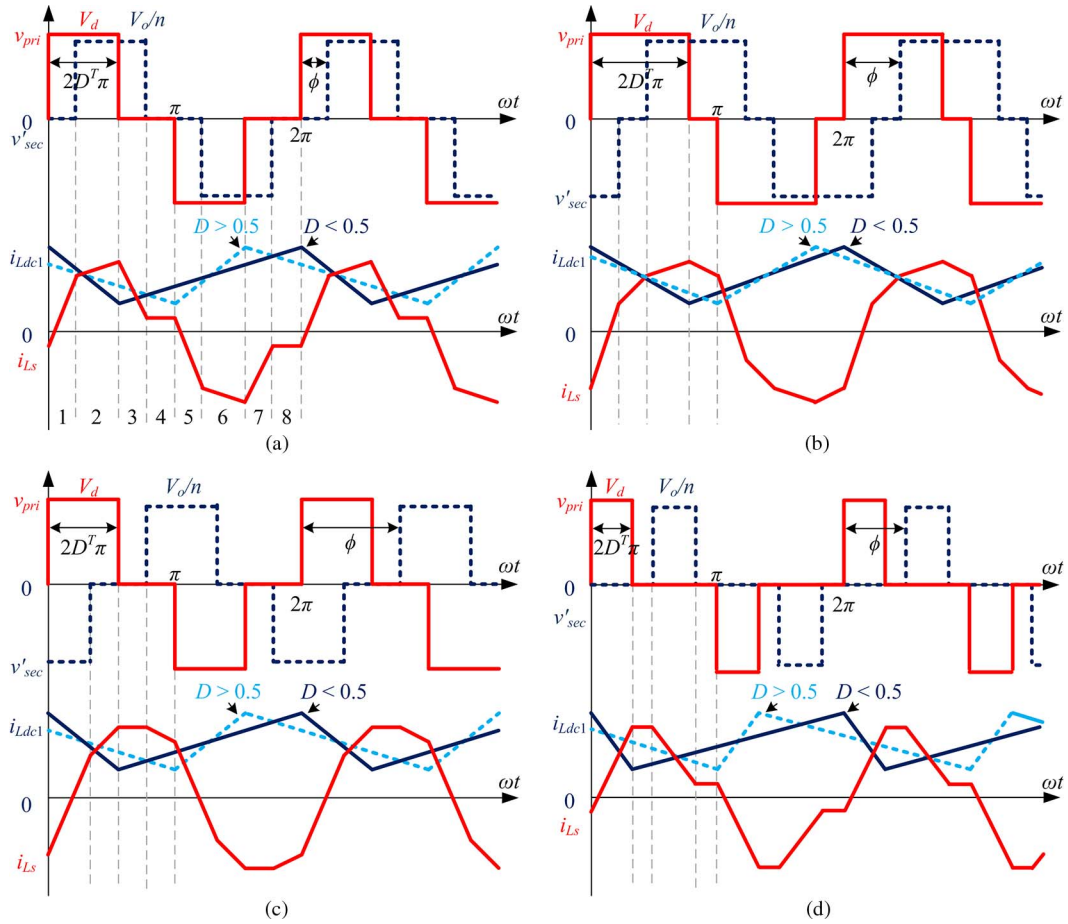



Fig. 3. Key waveforms of the CF-DAB converter. (a) Mode I: $0 < \phi < \min\{2D^T\pi, \pi - 2D^T\pi\}$. (b) Mode II: $0.25 \le D^T \le 0.5, 2D^T\pi \le \phi \le \pi - 2D^T\pi$. (c) Mode III: $\max\{2D^T\pi, \pi - 2D^T\pi\} < \phi < \pi$. (d) Mode IV: $0 < D^T < 0.25, 2D^T\pi \le \phi \le \pi - 2D^T\pi$. $D^T = \min\{D, 1-D\}$.

The key waveforms of operating mode I are shown in Fig. 3(a), where $0 < \phi < \min\{2D^T\pi, \pi - 2D^T\pi\}$, and $D^T$ is the minimum value of $D$ and $1-D$. $v_{\rm pri}$ and $v'_{\rm sec}$ are the transformer primary-side voltage and the primary referred secondary-side voltage, respectively. $i_{Ldc1}$ is the dc inductor current, and $i_{Ls}$ is the transformer primary current. It can be observed that the transformer current is periodic and symmetrical over a switching cycle; hence, the waveforms in a half switching cycle are used for analysis. The instantaneous current $i_{Ls}(\omega t)$ over a half switching cycle is represented as

$$i_{Ls}(\omega t) = \begin{cases} \frac{V_d}{\omega L_s}\left(\omega t - (1-d)D^T\pi\right), & 0 < \omega t \le \phi \\ \frac{V_d}{\omega L_s}\left(d\phi + (1-d)(\omega t - D^T\pi)\right), & \phi < \omega t \le 2D^T\pi \\ \frac{V_d}{\omega L_s}\left(d(\phi - \omega t) + (1+d)D^T\pi\right), & 2D^T\pi < \omega t \le 2D^T\pi + \phi \\ \frac{V_d}{\omega L_s}(1-d)D^T\pi, & 2D^T\pi + \phi < \omega t \le \pi \end{cases} \tag{1}$$

where $\omega$ is the angular switching frequency, $L_s$ is the leakage inductance, and $d$ is the primary referred voltage ratio of the high-voltage side (HVS) dc link to the LVS dc link, i.e., $d = V_o/nV_d$, with $V_o$ and $V_d$ being the HVS and LVS dc-link voltages, respectively, and $n$ being the transformer turns ratio.

Therefore, the transformer primary RMS current and peak current can be derived in the following:

$$I_{\rm rms1} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{Ls}(\omega t)^2 d\omega t} = \frac{V_d}{\omega L_s}\sqrt{\left(1 - \frac{4}{3}D^T\right)\left[(1-d)D^T\pi\right]^2 + \frac{d(6D^T\pi - \phi)\phi^2}{3\pi}} \tag{2}$$

$$I_{\rm pk1} = \begin{cases} i_{Ls}(2D^T\pi) = \frac{V_d}{\omega L_s}\left[d\phi + (1-d)D^T\pi\right], & d \le 1 \\ i_{Ls}(\phi) = \frac{V_d}{\omega L_s}\left[\phi - (1-d)D^T\pi\right], & d > 1. \end{cases} \tag{3}$$

The power flow equation is calculated by integrating the instant power over a half switching cycle as follows:

$$P_1 = \frac{1}{\pi}\int_0^{\pi} v_{\rm pri}(\omega t) i_{Ls}(\omega t) d\omega t = \frac{V_d^2}{\omega L_s} d\phi \left(2D^T - \frac{\phi}{2\pi}\right) \tag{4}$$

where $v_{\rm pri}(\omega t)$ is the primary-side voltage of the transformer, and $i_{Ls}(\omega t)$ is the primary-side transformer current. Similarly, the transformer RMS and peak currents, and the power flow

TABLE I
POWER AND TRANSFORMER CURRENT OF THE CF-DAB DC–DC CONVERTER

| Mode | Throughout Power | Transformer rms current | Transformer peak current |
|---|---|---|---|
| I | $\frac{V_d^2}{\omega L_s} d\phi\left(2D^T-\frac{\phi}{2\pi}\right)$ | $\frac{V_d}{\omega L_s}\sqrt{\left(1-\frac{4}{3}D^T\right)\left[(1-d)D^T\pi\right]^2+\frac{d\left(6D^T\pi-\phi\right)\phi^2}{3\pi}}$ | $\begin{cases}\frac{V_d}{\omega L_s}\left[d\phi+(1-d)D^T\pi\right], & d\le 1\\ \frac{V_d}{\omega L_s}\left[\phi-(1-d)D^T\pi\right], & d>1\end{cases}$ |
| II | $\frac{V_d^2}{\omega L_s} d\left[\phi\left(1-\frac{\phi}{\pi}\right)-\frac{\pi}{2}\left(1-2D^T\right)^2\right]$ | $\frac{V_d}{\omega L_s}\sqrt{\left(1-\frac{4}{3}D^T\right)\left[(1-d)D^T\pi\right]^2+\frac{d\left\{\left(6D^T\pi-\phi\right)\phi^2-\left[\phi-\left(1-2D^T\right)\pi\right]^3\right\}}{3\pi}}$ | |
| III | $\frac{V_d^2}{\omega L_s} d(\pi-\phi)\left[\frac{\phi}{2\pi}-\left(1-2D^T\right)\right]$ | $\frac{V_d}{\omega L_s}\sqrt{\left(1-\frac{4}{3}D^T\right)\left[(1-d)D^T\pi\right]^2+\frac{d\left\{\left(3\phi-2D^T\pi\right)\left(2D^T\pi\right)^2-\left[\phi-\left(1-2D^T\right)\pi\right]^3\right\}}{3\pi}}$ | $\frac{V_d}{\omega L_s}(1+d)D^T\pi$ |
| IV | $\frac{2V_d^2}{\omega L_s} d\pi\left(D^T\right)^2$ | $\frac{V_d}{\omega L_s}\sqrt{\left(1-\frac{4}{3}D^T\right)\left[(1-d)D^T\pi\right]^2+\frac{d\left(3\phi-2D^T\pi\right)\left(2D^T\pi\right)^2}{3\pi}}$ | |

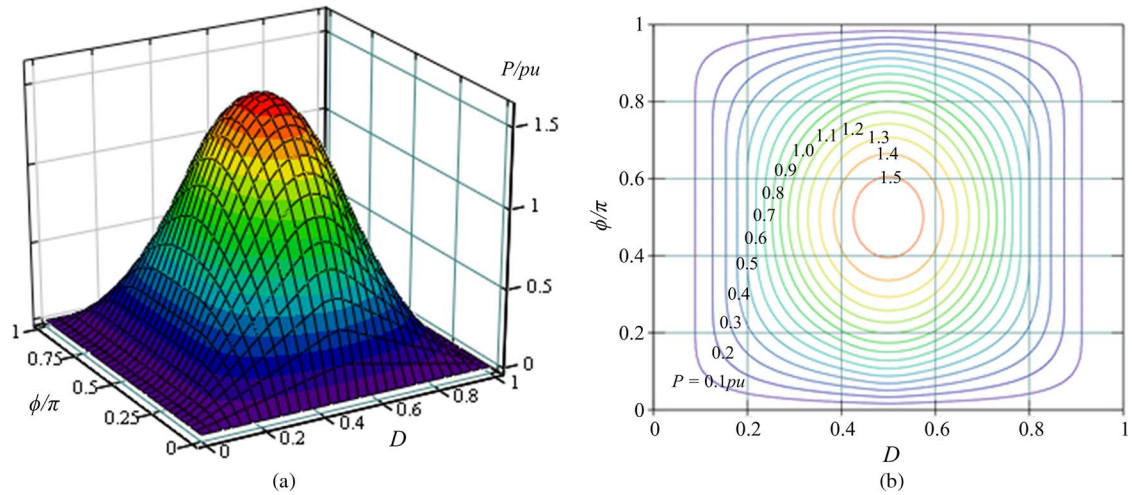



Fig. 4. Power flow when $V_d = 1$ and $d = 1$. (a) Surface plot. (b) Contour plot.

equations for other operating modes can be derived, which are summarized in Table I.

As the converter mainly operates in modes I and II, the minimized transformer peak current in (3) for a fixed dc-link voltage is achieved when the voltages on the LVS and the HVS are matched, i.e., $d = 1$. However, $d = 1$ will not minimize the RMS current in (2). Since the ZVS technique is applied to the CF-DAB converter, the switching loss is greatly reduced, whereas the conduction loss becomes dominating in the device loss. Therefore, the RMS current is more critical than the peak current from the perspective of reducing power loss. To achieve a low power loss, the operating mode with a minimized RMS current is highly desired and will be discussed in Section III. From the power equations derived in Table I, the relationship of the power flow with $(D, \phi)$ is depicted in Fig. 4, with $V_d = 1$ p.u. and $d = 1$. The power flow plots when $V_d \neq 1$ p.u. and $d \neq 1$ have the same shape but different values. By analyzing the contour plot in Fig. 4(b), the maximal deliverable power is at the central point in area II in Fig. 2, where $(D, \phi) = (0.5, 0.5\pi)$, and it can be written as

$$P_{\max} = \frac{d\pi V_d^2}{4\omega L_s} = \frac{\pi V_o^2}{4dn^2\omega L_s}. \tag{5}$$

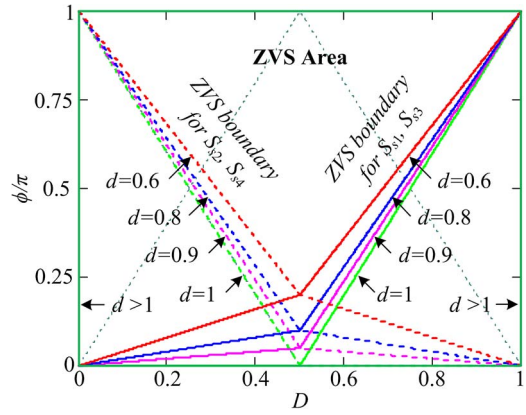



Fig. 5. ZVS boundaries of the secondary switches under different $d$.

## B. Soft-Switching Condition Analysis

It can be seen in Fig. 3 that the ZVS condition for the secondary-side switches can be expressed as

$$\begin{cases} -i_{Ls(\phi)}0, & \text{for } S_{s1}\ S_{s3},\ D<0.5\\ -i_{Ls(\phi+\pi+2D^T\pi)}<0, & \text{for } S_{s1}\ S_{s3},\ D>0.5\\ i_{Ls(\phi+2D^T\pi)}<0, & \text{for } S_{s2}\ S_{s4},\ D<0.5\\ i_{Ls(\phi+\pi)}<0, & \text{for } S_{s2}\ S_{s4},\ D>0.5. \end{cases} \tag{6}$$

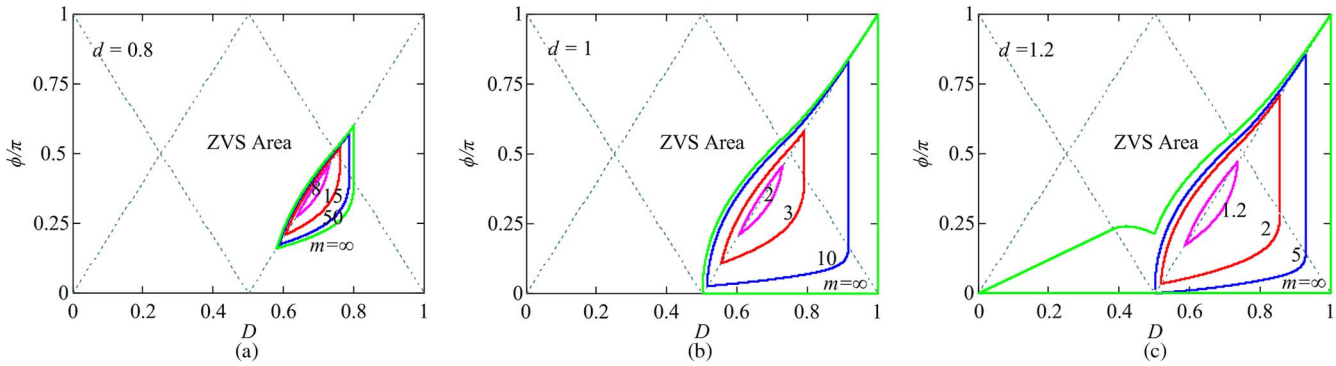



Fig. 6. ZVS boundaries of $S_{p2}$ and $S_{p4}$ under different $m$. (a) $d = 0.8$. (b) $d = 1$. (c) $d = 1.2$.

By substituting the instant current, the ZVS boundary for the secondary switches can be obtained, as shown in Fig. 5. The ZVS boundaries of the upper and lower switches are symmetrical with $D = 0.5$, and the ZVS area is extended with a larger $d$. When $d > 1$, the ZVS can be always achieved for the secondary switches.

As to the primary side, the current flow through the switches is not only affected by the transformer current but also by the dc inductor current. As shown in Fig. 3, the dc inductor current waveforms for $D > 0.5$ and $D < 0.5$ are different, and the soft switching conditions are different. The ZVS condition on the primary switches can be written as

$$\begin{cases} i_{Ls(0)} - i_{Ldc1(0)} < 0, & \text{for } S_{p1}\ S_{p3},\ D < 0.5 \\ i_{Ls(\pi+2D^T\pi)} - i_{Ldc1(\pi+2D^T\pi)} < 0, & \text{for } S_{p1}\ S_{p3},\ D > 0.5 \\ i_{Ldc1(2D^T\pi)} - i_{Ls(2D^T\pi)} < 0, & \text{for } S_{p2}\ S_{p4},\ D < 0.5 \\ i_{Ldc1(\pi)} - i_{Ls(\pi)} < 0, & \text{for } S_{p2}\ S_{p4},\ D > 0.5. \end{cases} \tag{7}$$

For $S_{p1}$ and $S_{p3}$, the ZVS can be easily satisfied, and they are always soft switched if $S_{p2}$ and $S_{p4}$ are soft switched. However, the ZVS condition for the lower switches depends on many factors and becomes more difficult to maintain. For the specific operating mode II with $D > 0.5$, (7) can be further expressed as

$$\begin{cases} \frac{P_2}{2V_{\text{in}}} + \frac{V_{\text{in}}(1-D)\pi}{m\omega L_s} + \frac{V_d[d\phi+(1-d)(1-D)\pi]}{\omega L_s} > 0, & \text{for } S_{p1},\ S_{p3} \\ \frac{P_2}{2V_{\text{in}}} - \frac{V_{\text{in}}(1-D)\pi}{m\omega L_s} - \frac{V_d[d(\phi-\pi)+(1+d)(1-D)\pi]}{\omega L_s} < 0, & \text{for } S_{p2},\ S_{p4} \end{cases} \tag{8}$$

where $V_{\text{in}}$ is the input voltage, and $m = L_{\text{dc1}}/L_s$.

Similarly, the ZVS condition for $S_{p2}$ and $S_{p4}$ in other areas can be also derived. As it is difficult to get a closed-form solution, Fig. 6 plots the ZVS boundaries for $S_{p2}$ and $S_{p4}$ under different $m$, where soft switching is achieved for the outside. It is clear that the ZVS range will be extended with a smaller $d$. When $d < 1$, soft switching can be always maintained in the left-half region, where $D < 0.5$. However, $d < 1$ will result in hard switching in the secondary switches. The soft-switching region will also increase when $m$ decreases, i.e., with a small dc inductor. Nevertheless, the small dc inductor will result in a large inductor current ripple. Fortunately, the total input current ripple will not increase much due to the cancelation effect of the interleaved input structure.

## III. Optimized Operating Mode With Minimized RMS Current

As there are multiple operating points $(D, \phi)$ delivering the same output power but with a different power loss, an optimized operating point can be selected to achieve high efficiency. Since hard switching is one of the main reasons causing a high power loss in high-frequency converters, the ZVS condition is essential to reduce the power loss. Another important aspect is the transformer peak and RMS currents that are related to nonconducting and conducting losses, respectively, and they are considered here to represent the power loss of the transformer and the switches.

Fig. 7 depicts the peak and RMS currents of the transformer primary side at different operating points for a certain condition $(V_{\text{in}}, V_o, P)$. It can be seen that $(D, \phi)$ for the minimum $I_{\text{pk}}$ and $I_{\text{rms}}$ varies with the operating condition $(V_{\text{in}}, V_o, P)$, and they are inconsistent with each other. In the $d = 1$ mode, the minimized peak current operation can be easily obtained in most operating conditions. However, the RMS current is usually more critical for loss reduction and is desired to be minimized, particularly when the ZVS is employed.

Fig. 8 shows the operating loci of the minimum-RMS-current mode and the $d = 1$ mode for varied output power under different $(V_{\text{in}}, V_o)$. The corresponding ZVS operating ranges for the primary and secondary switches are also presented in this figure. There are several observations. First, for a fixed $V_o$, the ZVS operating ranges for $S_{p2}$ and $S_{p4}$ are decreased with a higher input voltage, whereas they increase the ZVS area for the secondary switches. With a higher $V_o$, the optimized operating points $(D, \phi)$ are pushed toward the origin, and this enhances the ZVS condition for the primary switches. Second, for the $d = 1$ mode, the ZVS condition for the secondary switches is always satisfied. However, if $D \neq 0.5$, either the upper switches or the lower switches will be at the boundary condition depending on $(V_{\text{in}}, P)$. In addition, $S_{p2}$ and $S_{p4}$ will lose the ZVS condition at a high input voltage under the $d = 1$ mode. Third, the minimum-RMS-current mode will not bring the converter to enter hard switching from the ZVS; on the contrary, it enhances the ZVS condition and allows $S_{p2}$ and $S_{p4}$ to be soft switched at a high input voltage and high power. Finally, when $V_o \geq V_{\text{in}}$, the converter will operate under $D \leq 0.5$, and the ZVS conditions of all switches for both modes are satisfied, except for the boundary conditions of $S_{s2}$ and $S_{s4}$ with the $d = 1$ mode.

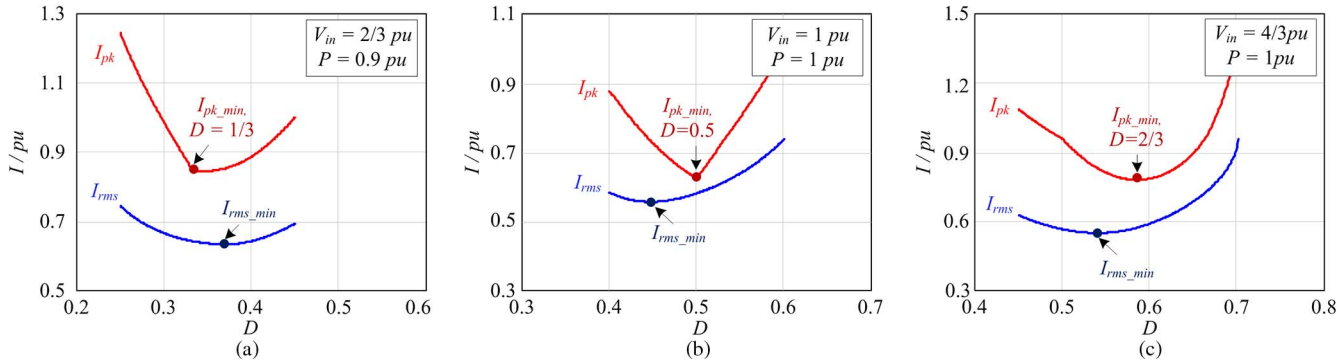



Fig. 7. Transformer primary peak current and RMS current under different conditions when $V_o = 1$ p.u. (a) $V_{\text{in}} = 2/3$ p.u. (b) $V_{\text{in}} = 1$ p.u. (c) $V_{\text{in}} = 4/3$ p.u.

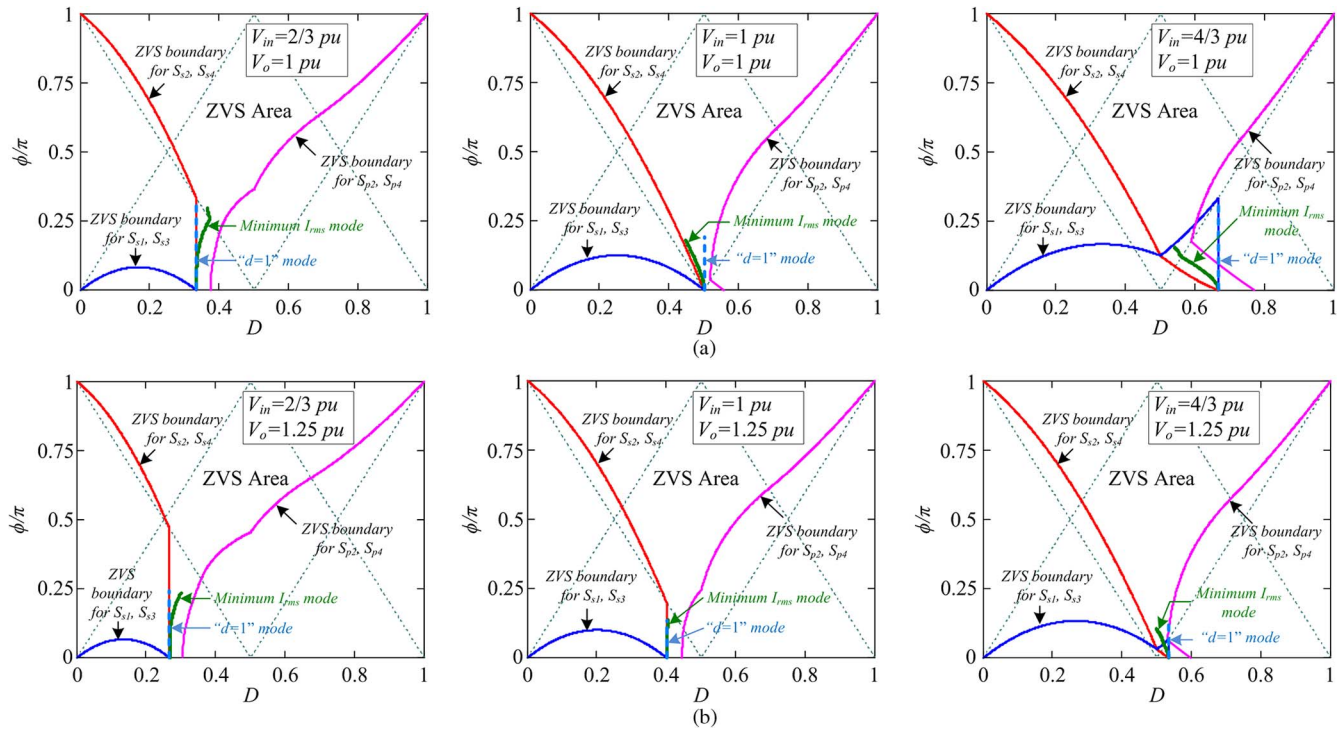



Fig. 8. Operating loci and ZVS conditions under different $V_{\text{in}}$ with $P = 0 \sim 1$ p.u. (a) $V_o = 1$ p.u. (b) $V_o = 1.25$ p.u.

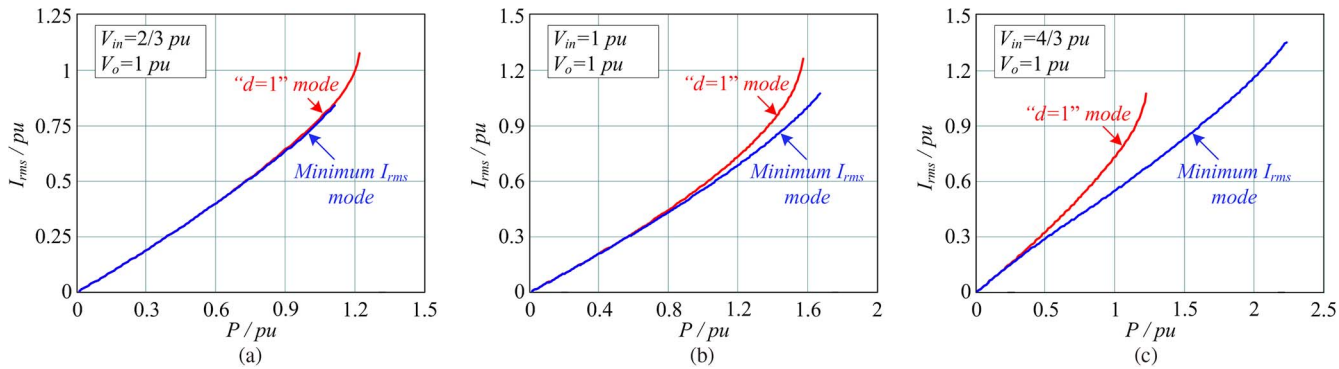



Fig. 9. RMS current comparison of the "$d = 1$" mode and the minimum-RMS-current mode when $V_o = 1$ p.u. (a) $V_{\text{in}} = 2/3$ p.u. (b) $V_{\text{in}} = 1$ p.u. (c) $V_{\text{in}} = 4/3$ p.u.

Fig. 9 compares the RMS current of the two different operating modes. For a low power flow, the two loci generate a similar RMS current. However, the RMS current in the $d = 1$ mode increases faster when the output power increases, particularly with high $V_{\text{in}}$, resulting in lower efficiency at a high output power.

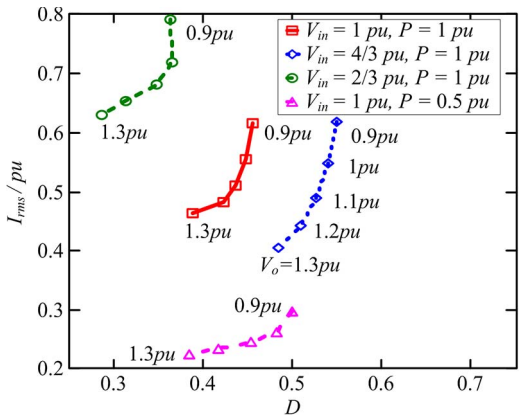



Fig. 10. Minimized RMS current versus $V_o$ under different $(V_{\text{in}}, P)$.

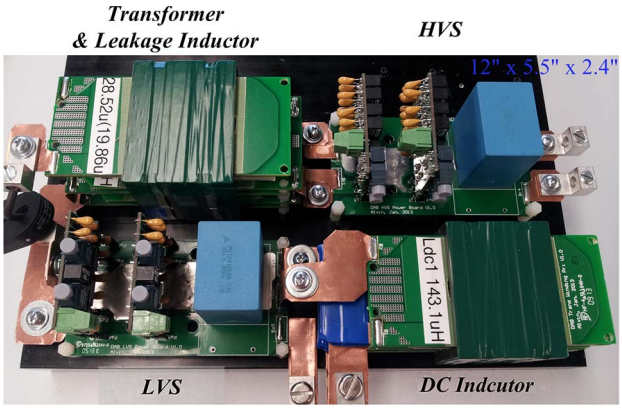



Fig. 11. Prototype of the 5-kW CF-DAB converter module.

Fig. 10 illustrates the minimized RMS current loci with respect to $V_o$ under different conditions of $(V_{\text{in}}, P)$. It is clearly showed that the RMS current is significantly reduced with a higher output voltage. As a result, to reduce the RMS current, a high HVS dc-link voltage should be selected. However, the dc-link voltage is subjected to applications.

As presented earlier, the minimum-RMS-current mode will not only benefit the CF-DAB converter with a lower conducting loss but also enhance the ZVS condition of the converter. Nevertheless, the optimized operating points vary from application to application, which makes it more complicated. The $d = 1$ mode is very simple compared with the minimum-RMS-current mode, and the soft-switching condition is guaranteed with $D = 0.5$. To achieve high efficiency over a wide input voltage range with the $d = 1$ mode, $V_o$ could be coordinated with $V_{\text{in}}$ in a certain range to let $D = 0.5$, if allowed.

## IV. Experimental Results

A 5-kW prototype of the CF-DAB converter was built in the laboratory, as shown in Fig. 11. The converter is intended to be implemented as a dc–dc converter module in the 12-kV 3-MW grid-connected cascaded multilevel PV system proposed in [30]. Hence, the HVS dc-link voltage is set relatively high at 600–750 V. The circuit parameters are listed in Table II. The leakage inductance was designed based on the assumption that

TABLE II
Circuit Parameters of the Converter

| Items | Descriptions | Specifications |
|---|---|---|
| $P_N$ | Rated power | 5 kW |
| $V_{in}$ | Input voltage | 100-200 V |
| $V_o$ | HVS dc-link voltage | 600-750 V |
| $n$ | Transformer turns ratio | 2 |
| $L_s$ | Leakage inductor | 28.5 μH |
| $L_{dc1}$, $L_{dc2}$ | DC inductor | 143.1μH |
| $C_{in}$ | Input capacitor | 10 μF |
| $C_d$ | LVS dc-link capacitor | 30 μF |
| $C_o$ | HVS dc-link capacitor | 80 μF |
| $f_{sw}$ | Switching frequency | 50.4 kHz |

the base power for the per-unit system defined in the Appendix is equal to the converter's rated power. As a result, the phase-shift angle at the rated power is around $0.2\pi$ [see Fig. 4(b)], which ensures both small circulating energy and high control accuracy. The dc inductance was selected to be five times the leakage inductance, considering the ZVS operating range and the inductor's current ripple. To reduce the switching loss, an FCN76N60NF SupreMOS and a CMF20120D SiC MOS field-effect transistor were used as the primary and secondary switches, respectively. Experimental results with a high input voltage $(V_{\text{in}} = 4/3$ p.u.) are given to verify the theoretical analysis.

Fig. 12 shows the experimental waveforms when the converter operated under different modes when $V_{\text{in}} = 200$ V $(4/3$ p.u.), $V_o = 600$ V (1 p.u.), and input power $P = 4$ kW (0.8 p.u.). As can be seen, the $d = 1$ mode in Fig. 12(a) has the minimum peak current, whereas its RMS current is much larger than that of the minimum-RMS-current mode $(d = 0.875)$ in Fig. 12(b). Moreover, the lower switches in the primary side, i.e., $S_{p2}$ and $S_{p4}$, suffers from hard switching in the $d = 1$ mode, whereas soft switching is realized in the minimum-RMS-current mode. This is consistent with the analysis in Section II that the minimum-RMS-current mode can extend the soft-switching range at a high input voltage. It should be noted that, different from the analysis in Section III, the ZVS is not fully achieved for $S_{p2}$ in Fig. 12(b). This is because the analysis is based on an ideal model, without considering the parasitic capacitance and the power loss in the circuit. In a real case, to achieve the ZVS, the energy in the circuit must be sufficient to charge or discharge the output capacitance of the switches $(C_{\text{oss}})$ during the dead time. In Fig. 12(c), the ZVS of $S_{p2}$ is achieved when $V_d$ is further increased to 355 V, i.e., $d = 0.845$. Due to the ZVS turn on, the converter achieves the highest efficiency despite the increased peak and RMS currents over the minimum-RMS-current mode. Fig. 13 gives the operating waveforms when the converter operated at different power under the $d = 1$ mode at $V_{\text{in}} = 200$ V (4/3 p.u.) and $V_o = 750$ V (1.25 p.u.). With the higher dc-link voltage $V_o$, both the peak and RMS currents are much lower compared with the current at $V_o = 600$ V. As shown in Fig. 13(a), where $P = 4$ kW, the converter achieves the ZVS for $S_{p2}$ under the $d = 1$ mode. These benefits greatly reduce the power loss of the converter and boost the system efficiency. However, when $P = 1$ kW in Fig. 13(b), $S_{p2}$ loses the ZVS condition due to insufficient

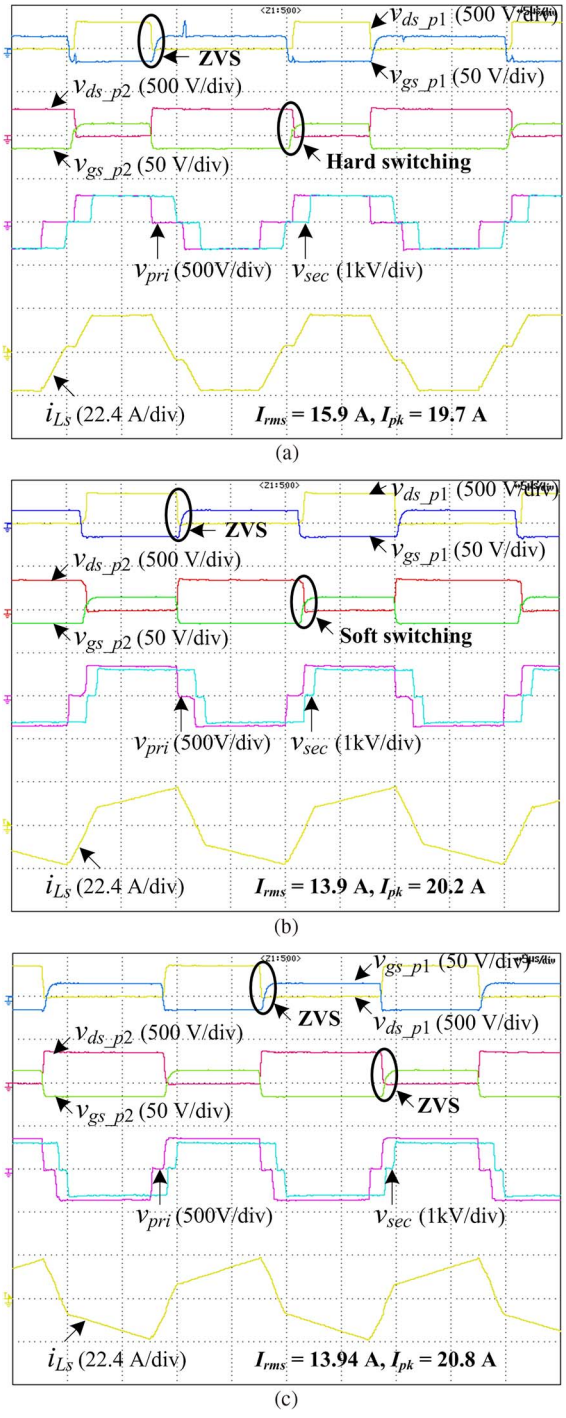



Fig. 12. Experimental waveforms at $V_{\text{in}} = 200$ V, $V_o = 600$ V, and $P = 4$ kW. (a) $d = 1$ mode at $V_d = 307$ V. (b) Minimum-RMS-current mode at $V_d = 343$ V. (c) Best efficiency operating at $V_d = 355$ V (time base: 5 $\mu$s/div).

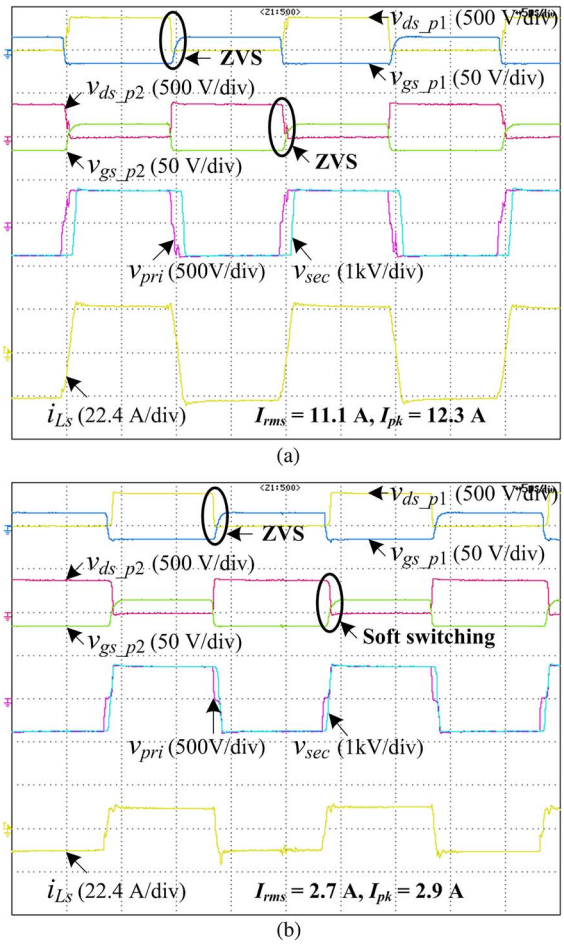



Fig. 13. Experimental waveforms under the $d = 1$ mode at $V_{\text{in}} = 200$ V, $V_d = 376$ V, and $V_o = 750$ V. (a) $P = 4$ kW. (b) $P = 1$ kW (time base: 5 $\mu$s/div).

energy to charge or discharge the $C_{\text{oss}}$ of the switches during the dead time.

The measured peak and RMS current curves under different operating modes and the HVS dc-link voltage when $V_{\text{in}} = 200$ V (4/3 p.u.) are depicted in Fig. 14(a) and (b), and the corresponding efficiency curves are shown in Fig. 14(c). The minimum-RMS-current mode presents a lower RMS current but a higher peak current than the $d = 1$ mode, resulting in higher efficiency over a wide input power range, particularly at high power. Moreover, the RMS current curve of the best efficiency operation is very close to that in the minimum-RMS-current mode, whereas the peak current is even larger, benefiting the converter with the ZVS operation. As seen from the two efficiency curves under the $d = 1$ mode in Fig. 14, the higher dc-link voltage can achieve much higher efficiency at high power because of the reduced current and the extended ZVS condition, although it results in lower efficiency at low power due to partial hard switching. Therefore, to achieve high efficiency over a full-load range, a variable dc-link voltage corresponding to the input voltage and power could be applied.

## V. Conclusion

In this paper, a CF-DAB converter for a PV application has been proposed. A thorough study for CF-DAB converters over a whole operating range employing duty-cycle control plus phase-shift control is presented. To achieve high efficiency over a wide input voltage range, an optimized operating mode generating a low power loss is developed with selected $(D, \phi)$. The operating loci with the minimum RMS current of the transformer for different operating conditions are derived, as well as

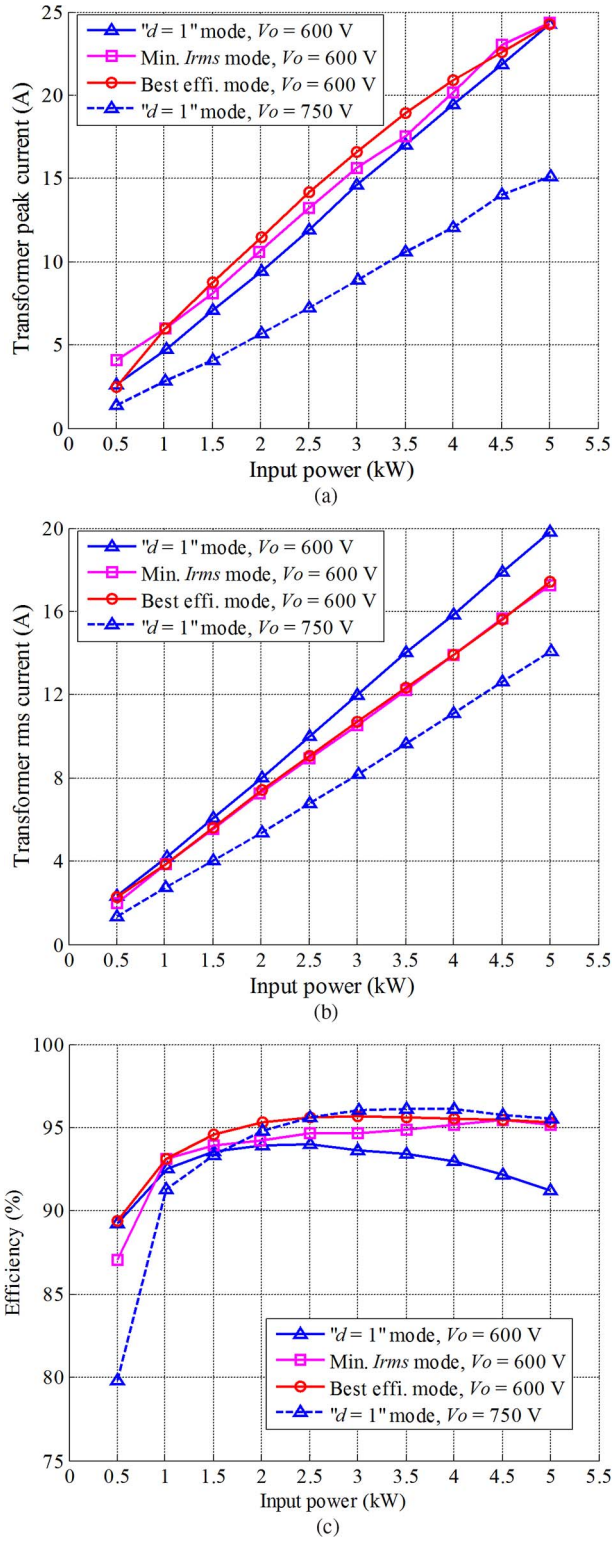



Fig. 14. Experimental curves when $V_{\text{in}} = 200$ V with different $V_o$ and operating modes. (a) Peak current. (b) RMS current. (c) Efficiency.

soft-switching conditions. The analysis and experimental results verify that this operating mode can extend the ZVS range and achieve a lower conducting loss compared with the $d=1$ mode, particularly for a high input voltage, and the efficiency can be further improved by choosing a higher variable dc-link voltage corresponding to the input voltage. Since CF-DAB converters can be extended to multiterminal applications, this paper has provided a foundation to study the optimized operation for those topologies.

## Appendix

The per-unit system in this paper is defined as follows ($V_{\text{in\_base}}$ is the medium value of the input voltage, and $P_N$ is the converter's power rating):

$$V_{d\_\text{base}} = 2V_{\text{in\_base}} \qquad V_{o\_\text{base}} = 2nV_{\text{in\_base}}$$
$$I_{\text{base}} = 2V_{\text{in\_base}}/\omega L_s \qquad P_{\text{base}} = V_{\text{in\_base}} I_{\text{base}} = P_N.$$

## References

[1] R. W. De Donker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power density dc/dc converter for high power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[2] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.

[3] F. Krismer and J. W. Kolar, "Efficiency-optimized high current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[4] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-power bidirectional DC–DC converter for aerospace applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4366–4379, Nov. 2012.

[5] L. Xue *et al.*, "Dual active bridge based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 1920–1925.

[6] B. Zhao, Q. Song, W. Liu, and W. Sun, "A synthetic discrete design methodology of high-frequency isolated bidirectional DC/DC converter for grid-connected battery energy storage system using advanced components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5402–5410, Oct. 2014.

[7] B. Zhao, Q. Song, W. Liu, and Y. Xiao, "Next-generation multi-functional modular intelligent UPS system for smart grid," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3602–3618, Sep. 2013.

[8] H. Qin and J. W. Kimball, "Solid-state transformer architecture using AC-AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.

[9] B. Zhao, Q. Song, and W. Liu, "Experimental comparison of isolated bidirectional DC–DC converters based on all-Si and All-SiC power devices for next-generation power conversion application," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1389–1393, Mar. 2014.

[10] X. Pan and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated dc/dc converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[11] J. L. Duarte, M. Hendrix, and M. G. Simoes, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 480–487, Mar. 2007.

[12] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional DC–DC converter with decoupled power flow management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443–2453, Sep. 2008.

[13] S. Kim, H. Song, and K. Nam, "Idling port isolation control of three-port bidirectional converter for EVs," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2495–2506, May 2012.

[14] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011.

[15] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol.24, no. 7, pp. 1826–1838, Jul. 2009.

[16] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[17] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC–DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

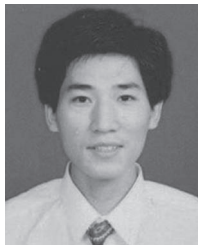
[18] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional DC–DC converter with dual- phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, May 2013.
[19] H. Wen, W. Xiao, and X. Su, "Nonactive power loss minimization in a bidirectional isolated DC–DC converter for distributed power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822–6831, Dec. 2014.
[20] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.
[21] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.
[22] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual active bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1424–1442, Jul./Aug. 2009.
[23] X. He, Z. Zhang, Y. Cai, and Y. Liu, "A variable switching frequency hybrid control for ZVS dual active bridge converters to achieve high efficiency in wide load range," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2014, pp. 1095–1099.
[24] F. Z. Peng, H. Li, G. Su, and J. S. Lawler, "A new ZVS bidirectional DC–DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.
[25] D. Xu, C. Zhao, and H. Fan, "A PWM plus phase-shift control bidirectional DC–DC converter," *IEEE Trans. Power Electron.*, vol.19, no. 3, pp. 666–675, May 2004.
[26] D. Liu and H. Li, "A ZVS bi-directional DC–DC converter for multiple energy storage elements," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1513–1517, Sep. 2006.
[27] Z. Wang and H. Li, "An integrated three-port bidirectional DC–DC converter for PV application on a DC distribution system," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4612–4624, Oct. 2013.
[28] Z. Ding, C. Yang, Z. Zhang, C. Wang, and S. Xie, "A novel soft-switching multiport bidirectional DC–DCc converter for hybrid energy storage system," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1595–1609, Apr. 2014.
[29] Y. Shi, L. Liu, H. Li, and Y. Xue, "A single-phase grid-connected PV converter with minimal dc-link capacitor and low-frequency ripple-free maximum power point tracking," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp 2385–2390.
[30] L. Liu, H. Li, Y. Xue, and W. Liu, "Decoupled active and reactive power control for large-scale grid-connected photovoltaic systems using cascaded modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 10, no. 1, pp. 176–187, Jan. 2015.
[31] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phased-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.
[32] Z. Wang and H. Li, "Optimized operating mode of current-fed dual half bridges DC–DC converters for energy storage applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 731–737.

**Yuxiang Shi** (S'13) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2007 and the M.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL, USA.

From 2010 to 2011, he was an Electrical Engineer with Philips Lighting Electronics, Shanghai, China. His research interests include bidirectional dc–dc converters, grid-tied photovoltaic systems with a wide-bandgap device, and cascaded multilevel inverters.

**Rui Li** (S'10–M'11) was born in Qingdao, China, in 1980. He received the B.S. degree in electrical engineering from Qingdao University, Qingdao, in 2002, the M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2005, and the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010.

Since December 2010, he has been with the Department of Electrical Engineering, School of Electronics, Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China, where he is currently an Associate Professor. From September 2008 to August 2009, he was an Academic Guest with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland. Since July 2014, he also has been with the Center for Advanced Power Systems, Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL, USA, as a Postdoctoral Research Scholar. His current research interests include applications of power electronics in renewable energy conversion.



**Yaosuo Xue** (M'03–SM'12) received the B.S. degree in electrical engineering from East China Jiaotong University, Nanchang, China, in 1991 and the M.S. degree in electrical engineering from the University of New Brunswick, Fredericton, NB, Canada, in 2004.

From 1991 to 2000, he was a Professional Engineer and took charge of the research and development of traction power-supply systems with the Third Survey and Design Institute, Chinese Ministry of Railways. In 2005 and 2006, he worked with the Capstone Turbine Corporation, Chatsworth, CA, USA, as a Lead Power Electronics and Systems Engineer. From 2006 to 2008, he was a Natural Sciences and Engineering Research Council of Canada Postgraduate (Doctor) Scholar with the University of New Brunswick. Since 2009, he has been with Siemens Corporate Technology, Princeton, NJ, USA, as a Power Electronics Manager. His current research interests include multilevel topologies and controls for utility and industry applications.

**Hui Li** (S'97–IM'00–SM'01) received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, in 1992 and 1995, respectively, and the Ph.D. degree from the University of Tennessee, Knoxville, TN, USA, in 2000, all in electrical engineering.

She is currently a Professor with the Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL, USA. Her research interests include photovoltaic converters applying a wide-bandgap device, bidirectional dc–dc converters, cascaded multilevel inverters, and power electronics applications in hybrid electric vehicles.