Sensorless Predictive Current Controlled DC–DC Converter With a Self-Correction Differential Current Observer

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***Abstract*—For a sensorless predictive current controlled boost dc–dc converter, its small-signal model that contains a number of parasitic parameters, is derived in this paper. This model indicates that the type of system becomes type 0 even with the correction of voltage loop proportional–integral controller, leading to the existence of output voltage steady-state error. Then a self-correction differential current observer (SDCO) is proposed to eliminate this steady-state error and gain high transient response speed. The self-correction part of the SDCO makes the system become type 1 to achieve no steady-state error for output voltage, whereas the differential part can guarantee that the intermediate calculation results do not overflow. By carrying out a series of simulation verifications, further investigation proves that the proposed algorithm has good robustness. Finally, the effectiveness of the proposed algorithm is verified by experimental results.**

***Index Terms*—DC–DC converter, differential current observer, self-correction, sensorless.**

I. Introduction

In RECENT years, the current mode controlled dc–dc converter has become a hot research topic [1]–[6]. Compared with voltage mode control, it has higher response speed and larger loop gain bandwidth. However, the extra current detecting module, which includes the current sensor, the voltage level shifting circuit, and the analog-to-digital converter (ADC), brings extra cost and unreliability. Thus, the sensorless current controlled dc–dc converter, which acts in current control mode with all the aforementioned advantages but without needing a current detecting module, has got great potentials in both academic and industrial applications.

As an advanced current control strategy, the predictive current control (PCC) has the characteristics of high robustness and high response speed. It can be combined with the current observer to realize sensorless PCC (SPCC). Both the PCC and current observer technologies have been widely investigated. For the PCC, an algorithm was investigated in [7] to eliminate the inductor current disturbance in one switching cycle in peak, average, and valley current control modes. However, in order to maintain the current control loop stability, the specific combination of current control mode with pulsewidth modulation (PWM) modulation scheme should be obeyed, and it restrains the flexibility of system design. Lai and Yeh further investigated PCC-based peak current mode control in [8]. The effectiveness to eliminate the disturbance in limit cycle by PCC with leading-edge PWM modulation scheme was verified by theoretical derivation. Then, in [9], Lai *et al.* proposed a family of PCC methods to adapt leading-edge, trailing-edge, and triangular modulation schemes under boundary current mode control. Although the zero-current detection and the high-frequency ADC can be eliminated from the system, an additional ADC is required for online inductance tuning. All the aforementioned PCC research work have already built solid basement for the research on SPCC.

In order to realize sensorless current control, the current observer is chosen to fulfill the task. The performance of the current observer is decided by the accuracy of its modeling [10]. In [11], an accurate system model was established for current-observer-based senseless current control. However, the implementation of this strategy is far too complex. An input voltage feedforward current observer was proposed in [12], which is easy to implement in terms of computational complexity. The input voltage feedforward module can help in effectively avoiding the impact of the input voltage variations, but the current estimation error is relatively large because of the ignorance of the parasitic parameters. To improve the current estimation accuracy, an extended-Kalman-filter-based current observer was investigated in [13]. An explicit model predictive control was implemented to improve the current control performance, and a piecewise affine method was used to obtain the optimal control parameters. However, the parameter tuning process can only be carried out in offline mode due to its high calculation complexity. Shen *et al.* proposed an SPCC algorithm aiming at reducing the cross regulation for single-inductor multiple-output converters [14]. The parasitic parameters' effect on current estimation is considered, but the voltage loop steady-state error and parameter variation issues are not addressed. In [15], with the consideration of a number

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of parasitic parameters, the current estimation is relatively accurate, but an additional signal sampling module is required for the switch node voltages sampling to determine the parasitic parameters. In spite of that, the parasitic parameter variation compensation has to rely on the load resistance, which normally varies with working conditions.

With the aforementioned research achievements, the effect of component parasitic parameters has not yet been deeply investigated. There are two important related issues. One is the output voltage steady-state error. If the parasitic parameters are involved to get a more accurate small-signal model, the integration effect of the voltage loop proportional–integral (PI) controller is negated by the zero at the origin introduced from the PCC controller. Eventually, the output voltage steady-state error cannot be eliminated. The other issue is that the variation of parasitic parameters can cause the system model to change over time. This brings an extra current estimation error, even leading to the system being unstable because the current observer relies on modeling with parasitic parameters to realize accurate sensorless current control. In theory, the issue can be solved by online parameter estimation [16]–[18]. However, to simultaneously identify all the parasitic parameters online is not practical due to the high calculation complexity.

Aiming at finding out solutions for the two issues aforementioned, this paper is organized as follows. In Section II, an SPCC algorithm is designed for peak current mode controlled boost converter. Then, a proper modeling scheme for the SPCC-based boost converter small-signal model, which contains a number of parasitic parameters, is proposed. It is found out that the output voltage steady-state error cannot be eliminated even with the correction of the voltage loop PI controller. In Section III, an self-correction differential current observer (SDCO) is investigated. It has the advantage that it can eliminate the zero at the origin produced by the PCC controller to achieve no output voltage steady-state error without considering any parasitic parameters. Further investigations on its control parameter tuning and the system robustness analysis are covered in Section IV. Finally, the experimental results and their analysis are given in Section V.

II. SPCC and Its Small-Signal Model

A. Basic Current Observer and SPCC

To implement the proposed algorithm, the boost converter is chosen as an example. The structure of a conventional SPCC-based boost converter is shown in Fig. 1. The system is composed of two control loops. The outer loop is a voltage control loop, using a PI controller to output a current reference. The inner loop is a current control loop, using senorless current control in peak current mode.

The increasing slope of inductor current in the kth switching cycle is $M_1(k)$, and the decreasing slope absolute value is $M_2(k)$, then

$$M_1(k) = \frac{V_{IN}(k)}{L} \tag{1}$$

$$M_2(k) = \frac{V_O(k) - V_{IN}(k)}{L}. \tag{2}$$

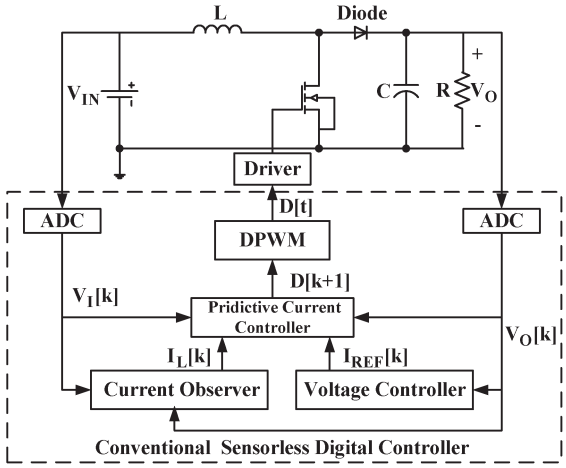

Fig. 1. Structure of conventional sensorless current control for a boost converter.

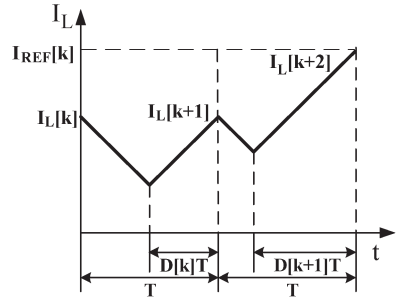

Fig. 2. Inductor current waveform of peak current control mode.

The differential equation of estimated inductor current $I_L(k)$ in the time domain is

$$I_L(k+1) = I_L(k) - M_2(k)D'(k)T + M_1(k)D(k)T \tag{3}$$

where $D(k)$ is the duty ratio in the kth switching cycle, and $D'(k)$ is $1 - D(k)$. If $I_L(k)$ represents the estimated peak inductor current, this is a digital first-order observer for inductor current estimation.

The PCC-based regulating process of the inductor current is presented in Fig. 2. The duty ratio of the next switching cycle is derived from the error between the reference and estimated currents, making the estimated current I_L reach the reference current I_{REF} in two control cycles. Suppose that $M_1(k) \approx M_1(k+1)$ and $M_2(k) \approx M_2(k+1)$. Then the relationship between $I_L(k)$ and I_{REF} is described in

$$I_L(k) + M_1(k)\left[D(k) + D(k+1)\right]T - M_2(k)\left[D'(k) + D'(k+1)\right]T = I_{\mathrm{REF}}(k). \tag{4}$$

From (1), (2), and (4), the SPCC control law for peak current control mode can be derived as

$$D(k+1) = \frac{L\left[I_{\mathrm{REF}}(k) - I_L(k)\right] - 2V_{IN}(k)T}{V_O(k)T} + 2 - D(k). \tag{5}$$

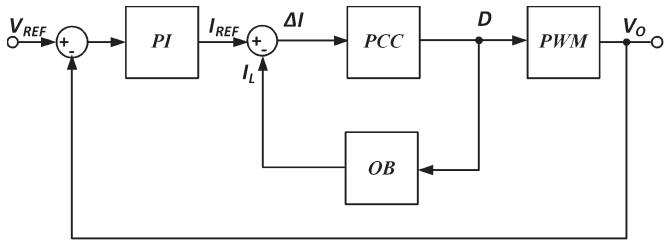

Fig. 3. Closed-loop small-signal model of the SPCC boost converter.

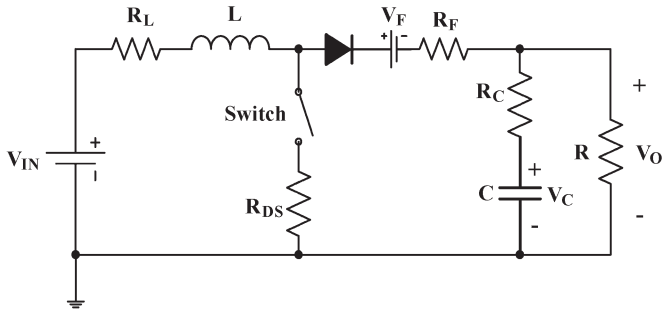

Fig. 4. Equivalent model of a boost converter with a number of parasitic parameters.

B. Small-Signal Model for SPCC

Until now, there has not yet been a proper model with parasitic parameters for the SPCC-based system in published literature. Aiming at this issue, a small-signal modeling method for SPCC is investigated.

The closed-loop small-signal model in continuous time domain is shown in Fig. 3, where ΔI is equal to $(I_{\rm REF} - I_L)$. Assuming $I_{\rm REF}$ and I_L are sampled at the beginning of each switching cycle, then I_L strictly follows $I_{\rm REF}$ with two switching cycle delay. Therefore, in discrete time domain, the relationship between $I_{\rm REF}$ and I_L is

$$I_L(k) = I_{\rm REF}(k)z^{-2}. \tag{6}$$

Substituting I_L into (5) by (6), then

$$D(k+1)(1+z^{-1}) = \frac{\left[I_{\rm REF}(k) - z^{-2}I_{\rm REF}(k)\right]L + 2\left[V_O(k) - V_{IN}(k)\right]T}{V_O(k)T}. \tag{7}$$

By using Tustin approximation, (7) can be transferred from discrete time domain to continuous time domain, i.e.,

$$D\left(\frac{4}{2+sT}\right) = \frac{8s}{(2+sT)^2}\frac{I_{\rm REF}L}{V_O} + 2\frac{V_O - V_{IN}}{V_O}. \tag{8}$$

Because the crossover frequency is always much lower than the switching frequency, then with the approximation $2 + sT \approx 2$, (8) can be simplified to

$$D = s\frac{I_{\rm REF}L}{V_O} + 1 - \frac{V_{IN}}{V_O}. \tag{9}$$

Equation (9) is the regulating rule in continuous time domain. In this control diagram, V_{IN} is regarded as constant. Imposing small-signal disturbances $\hat{I}_{\rm REF}$, $\hat{D}$, and $\hat{V}_O$ onto $I_{\rm REF}$, D, and V_O, respectively, and then substituting them into (9), then

$$(V_O + \hat{V}_O)(D + \hat{D}) = sL(I_{\rm REF} + \hat{I}_{\rm REF}) + V_O + \hat{V}_O - V_{IN}. \tag{10}$$

After eliminating the dc elements and higher order infinitesimals, the small-signal model transfer function from $I_{\rm REF}$ to D can be obtained, i.e.,

$$\frac{\hat{D}}{\hat{I}_{\rm REF}} = sL\frac{1}{V_O - \frac{\hat{V}_O}{\hat{D}}(1-D)}. \tag{11}$$

Supposing $G_{VI}(s)$ is the transfer function from $I_{\rm REF}$ to V_O, then

$$G_{VI}(s) = \frac{\hat{V}_O}{\hat{I}_{\rm REF}} = \frac{\hat{D}}{\hat{I}_{\rm REF}}\frac{\hat{V}_O}{\hat{D}} = sL\frac{\frac{\hat{V}_O}{\hat{D}}}{V_O - \frac{\hat{V}_O}{\hat{D}}(1-D)}. \tag{12}$$

$G_{VD}(s)$ is the classical boost converter transfer function from D to V_O without any parasitic parameters, which is shown as

$$G_{VD}(s) = \frac{\hat{V}_O}{\hat{D}} = \frac{(1-D)V_O\left(1 - \frac{Ls}{(1-D)^2R}\right)}{LCs^2 + \frac{L}{R}s + (1-D)^2}. \tag{13}$$

Substituting (13) into (12), the following can be deduced:

$$G_{VI}(s) = \frac{\hat{V}_O}{\hat{I}_{\rm REF}} = \frac{R(1-D)^2 - Ls}{(RCs+2)(1-D)}. \tag{14}$$

As can be seen from (14), without any parasitic parameters, $H_{IV}(s)$ for SPCC mode is exactly the same as that part of the conventional current control mode with a current sensor.

$G_{\rm PI}(s)$ is the transfer function of the PI controller; whereas K_P and T_I are the proportional and integral parameters, respectively. Then the open-loop transfer function of the SPCC boost converter is

$$T(s) = \frac{R(1-D)^2 - Ls}{(RCs+2)(1-D)}K_P\left(1 + \frac{1}{sT_I}\right). \tag{15}$$

According to (15), it is a type-1 system; thus, there is no output voltage steady-state error with a step-type reference voltage. However, the system type is changed when the parasitic parameters are included in the model.

The equivalent circuit diagram of a boost converter with a number of parasitic parameters is presented in Fig. 4, where R_L, R_{DS}, R_F, V_F, and R_C represent the parasitic resistance of the inductor, the MOSFET conducting resistance, the diode equivalent conducting resistance, the diode conducting voltage drop, and the capacitor equivalent serial resistance, respectively.

When R_C is included in the small-signal model, V_O is no longer equal to the voltage of the output capacitor V_C. Thus, the difference between them should be considered during the derivation process of the small-signal model.

When the switch is on, the output capacitor discharges supply energy to the load. Therefore

$$V_O = V_C - \frac{V_O}{R}R_C. \tag{16}$$

Differentiating (16), the following can be obtained:

$$C\frac{dV_C}{dt} = \frac{R+R_C}{R}C\frac{dV_O}{dt}. \tag{17}$$

During switching on period, the capacitor average discharging current is $-V_O/R$. The system state function during this period is

$$\begin{cases} L\frac{dI_L}{dt} = V_{IN} - I_L R_L - I_L R_{DS} \\ C\frac{dV_O}{dt} = -\frac{V_O}{R+R_C}. \end{cases} \tag{18}$$

When the switch is off, the inductor current charges the capacitor and supplies the load. During this period, the relationship between V_O and V_C is

$$V_C = V_O - \left(I_L - \frac{V_O}{R}\right)R_C. \tag{19}$$

Differentiating (19), the following can be obtained:

$$C\frac{dV_C}{dt} = \frac{R+R_C}{R}C\frac{dV_O}{dt} - CR_C\frac{dI_L}{dt}. \tag{20}$$

During $(1-D)T$, the capacitor average charging current is $I_L - V_O/R$. Thus, the system state function is

$$\begin{cases} L\frac{dI_L}{dt} = -(V_O - V_{IN}) - I_L R_L - I_L R_F - V_F \\ C\frac{dV_O}{dt} = \frac{R}{R+R_C}\left(I_L - \frac{V_O}{R} + CR_C\frac{dI_L}{dt}\right). \end{cases} \tag{21}$$

First, multiply (18) and (21) with DT and $(1-D)T$, respectively. Then, adding them together, the average state functions of the whole switching cycle can be obtained, i.e.,

$$\begin{cases} L\frac{dI_L}{dt} = V_{IN} - V_O(1-D) - I_L R_L - I_L R_{DS} D \\ \qquad\qquad - (I_L R_F + V_F)(1-D) \\ C\frac{dV_O}{dt} = -\frac{V_O}{R+R_C} + \frac{R(1-D)}{R+R_C}I_L + \frac{R(1-D)CR_C}{R+R_C}\frac{dI_L}{dt}. \end{cases} \tag{22}$$

Impose small-signal disturbances $\hat{I}_{\mathrm{REF}}$, $\hat{D}$, and $\hat{V}_O$ onto I_{REF}, D, and V_O, respectively, and then substitute them into (22). After getting rid of dc elements and high-order infinitesimals, then

$$\begin{cases} Ls\hat{I}_L = V_O\hat{D} - \hat{V}_O(1-D) - \hat{I}_L R_L - \hat{I}_L R_{DS} D \\ \qquad - I_L R_{DS}\hat{D} + I_L R_F\hat{D} - \hat{I}_L(1-D)R_F + V_F\hat{D} \\ Cs\hat{V}_O = -\frac{\hat{V}_O}{R+R_C} + \frac{R}{R+R_C}\left[\hat{I}_L(1-D) - I_L\hat{D}\right] \\ \qquad - \frac{RCR_C s}{(R+R_C)}\left[\hat{I}_L(1-D) - I_L\hat{D}\right]. \end{cases} \tag{23}$$

Let $a = R_L + DR_{DS} + R_F(1-D)$ and $b = R_F - R_{DS}$, the inductor current part of (23) can be simplified as

$$\hat{I}_L = \frac{V_O\hat{D} - \hat{V}_O(1-D) + I_L b\hat{D} + V_F\hat{D}}{Ls+a}. \tag{24}$$

Eliminating $\hat{I}_L$ from (23), $G_{VD}(s)$ can be obtained, and it is shown as

$$G_{VD}(s) = \frac{(1-D)R(R_C Cs+1)\frac{V_O + I_L b + V_F}{sL+a} - I_L R(R_C Cs+1)}{1+(R+R_C)Cs + R(R_C Cs+1)\frac{(1-D)^2}{sL+a}}. \tag{25}$$

The relationship between V_O and I_L is

$$V_O = I_L(1-D)R. \tag{26}$$

Z_O is the output impedance, which consists of R_C, C, and R. Therefore, Z_O can be described as

$$Z_O = \frac{RR_C Cs + R}{RCs + R_C Cs + 1}. \tag{27}$$

Substituting (26) and (27) into (25), then

$$G_{VD}(s) = \left[1 - \frac{Ls + a - b(1-D)}{R(1-D)^2} + \frac{V_F}{V_O}\right] \times \frac{V_O Z_O(1-D)}{Ls + a + Z_O(1-D)^2}. \tag{28}$$

It can be verified that, when all the parasitic parameter values are zero, i.e., $a = b = R_C = V_F = 0$, (28) and (13) are the same.

Substituting (28) into (12), a zero at the origin can be found in $G_{VI}(s)$, which is shown as (29). It can be also verified that (29), shown at the bottom of the page, and (14) are equal when all the parasitic parameter values are zero.

For the open-loop transfer function, this zero at the origin eliminates the pole at the origin brought by the PI controller. Thus, the SPCC-based boost converter becomes a type-0 system, and the elimination of output steady-state error cannot be realized through voltage loop PI controller.

III. SDCO

A. Self-Correction Module

According to the analysis in Section II, for the basic current observer, an integral self-correction module can be added to the system for voltage loop steady-state error elimination. As shown in Fig. 5, in the integral self-correction module, I'_L multiplies K/s, and the result is subtracted by I_L; the relationship between I'_L and I_L is

$$I'_L = I_L\left(\frac{s}{s+K}\right). \tag{30}$$

In the following, the open-loop transfer function with the self-correction module is derived. First, the equation of the basic

$$G_{VI}(s) = \frac{\left[(1-D)^2 - \frac{Ls+a-b(1-D)}{R} + \frac{V_F}{V_O}(1-D)^2\right]}{(Ls+a)(RCs + 2R_C Cs + 2) - \left[b(1-D) + \frac{V_F}{V_O}R(1-D)^2\right](R_C Cs+1)}\frac{RR_C Cs + R}{1-D}Ls \tag{29}$$

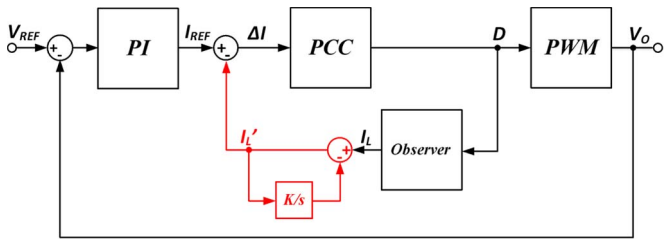

Fig. 5. Block diagram of the current controller with self-correction.

current observer without self-correction can be described as

$$I_L(k+1) = I_L(k) + \frac{T}{L}\left\{V_{IN}(k) - V_O(k)\left[1 - D(k)\right]\right\}. \tag{31}$$

Transferring (31) into continuous domain, then

$$I_L = \frac{1}{sL}\left[V_{IN} - V_O(1-D)\right]. \tag{32}$$

Impose small-signal disturbances $\hat{I}_{\rm REF}$, $\hat{D}$ and $\hat{V}_O$ onto $I_{\rm REF}$, D and V_O, respectively, and then substitute them into (32). After eliminating dc elements and higher order infinitesimals, the following can be obtained:

$$\frac{\hat{I}_L}{\hat{D}} = \frac{1}{sL}\left[V_O - \frac{\hat{V}_O}{\hat{D}}(1-D)\right]. \tag{33}$$

$G_{ID}(s)$ is the transfer function from D to I'_L. Combining the self-correction module with the current observer, $G_{ID}(s)$ is

$$G_{ID}(s) = \frac{\hat{I}'_L}{\hat{D}} = \frac{1}{(s+K)L}\left[V_O - \frac{\hat{V}_O}{\hat{D}}(1-D)\right]. \tag{34}$$

From (5), the relationship between ΔI and D can be derived, i.e.,

$$\left[D(k+1)+D(k)\right]V_O(k)T = L\Delta I(k) - 2V_{IN}(k)T + 2V_O(k)T. \tag{35}$$

Equation (35) represents the regulating rule of PCC. Then $G_{\rm PCC}(s)$, i.e., the transfer function from ΔI to D, can be obtained by the same method, i.e.,

$$G_{\rm PCC}(s) = \frac{L}{2T}\frac{1}{V_O - \frac{\hat{V}_O}{\hat{D}}(1-D)}. \tag{36}$$

Combining (28), (34), and (36), $G_{VI}(s)$ is presented as (37), shown at the bottom of the page.

Comparing (37) with (29), the zero at origin of $G_{VI}(s)$ is eliminated after the introduction of the self-correction module. Therefore, the system type changes from type 0 to type 1, and there should be no output voltage steady-state error.

B. Differential Current Observer

After involving the self-correction module into the current observer, the output voltage steady-state error can be eliminated, and I'_L tends to be constant. However, the problem still exists in two respects. First, the predicted current I_L is still increasing, eventually leading to the calculation result overflowing. More importantly, the influences on the parasitic parameters, e.g., device aging, will diverge I'_L from the actual inductor current.

As shown in Fig. 5, in order to deduce $D(k+1)$, it is only necessary to calculate ΔI rather than I_L. After extracting common factor $1/sT$, ΔI becomes

$$\Delta I = I_{\rm REF} - I_L = \frac{1}{sT}(\Delta I_{\rm REF} - \Delta I_L) = \frac{1}{sT}\Delta I'. \tag{38}$$

In (38), $\Delta I_{\rm REF}$ and ΔI_L are the differential values of $I_{\rm REF}$ and I_L, respectively. When the system reaches its steady state, both of them converge to zero, and the calculation overflow can be effectively avoided. The current observer equation in the continuous domain can be converted from (3), i.e.,

$$I_L = \frac{1}{sT}\frac{T}{L}\left[V_{IN} - V_O(1-D)\right]. \tag{39}$$

Then the differential current observer is

$$\Delta I_L = \frac{T}{L}\left[V_{IN} - V_O(1-D)\right] \tag{40}$$

whereas $\Delta I_{\rm REF}$ can be calculated by

$$\Delta I_{\rm REF} = K_P\left(1 + \frac{1}{sT_I}\right)sT. \tag{41}$$

The block diagram of the current controller with differential observer is shown in Fig. 6. Compared with Fig. 5, additional modules are added, as marked in red.

When the common factor $1/sT$ is extracted from the PI controller, the PI controller becomes a proportional–derivative controller. The model with differential observer is shown in Fig. 7. The computational complexity of the algorithm does not increase with the modification of the control structure.

$$\begin{aligned} G_{VI}(s) &= \frac{G_{\rm PCC}(s)}{1 + G_{\rm PCC}(s)G_{ID}(s)}G_{VD}(s) \\ &= \frac{\left[(1-D)^2 - \frac{Ls+a-b(1-D)}{R} + \frac{V_F}{V_O}(1-D)^2\right]}{(Ls+a)(RCs+2R_CCs+2) - \left[b(1-D) + \frac{V_F}{V_O}R(1-D)^2\right](R_CCs+1)} \\ &\quad \times \frac{RR_CCs+R}{1-D}\frac{L(s+K)}{1+2Ts+2KT} \end{aligned} \tag{37}$$

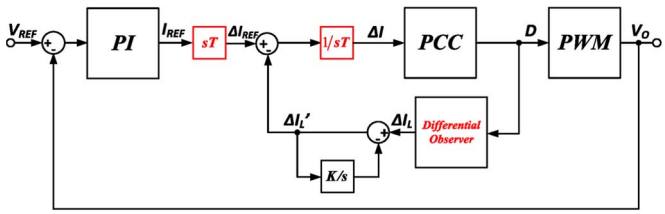

Fig. 6. Block diagram of the current controller with differential observer.

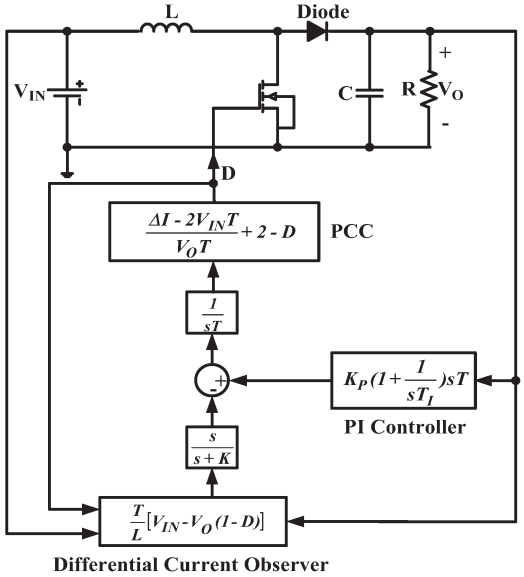

Fig. 7. Block diagram of SPCC with differential current observer.

IV. Self-Correction Coefficient Tuning and Robustness Analysis

After introducing the SCDO, the system robustness should be clarified, and the effect on the system stability by the variations of self-correction coefficient K should be investigated. At first, the value of K should be optimized.

A. Self-Correction Coefficient Tuning

The open-loop transfer function $G_{\mathrm{LOOP}}(s)$ can be described as (42), shown at the bottom of the page, where $G_{VI}(s)$ can be derived from (37).

TABLE I
Poles and Zeros of the Open-Loop Transfer Function

Poles	Zeros
0	$-\frac{1}{T_I}$
$-\frac{RCa+2L}{LRC}$	$-K$
$-\frac{2a-b(1-D)-\frac{V_F}{V_O}R(1-D)^2}{RCa+2L}$	$\frac{R}{L}(1-D)^2$
$-\frac{2KT+1}{2T}$	$-\frac{1}{R_cC}$

In (42), there are four zeros and four poles in $G_{\mathrm{LOOP}}(s)$, and the polynomials, which include a or b, in the denominator part of $G_{\mathrm{LOOP}}(s)$ are quite complicated. Substituting $a = R_L + DR_{DS} + R_F(1-D)$ and $b = R_F - R_{DS}$ into (42), it is very hard to derive the poles directly. Thus, some reasonable simplifications are necessary.

At first, assume that one of the poles is (43), shown at the bottom of the page.

When R is much larger than R_C, (50) can be simplified as

$$\omega_{p1} \approx -\frac{RCa+2L}{LRC}. \tag{44}$$

Substituting (44) into the second-order polynomial includes a and b. Another pole can be obtained as

$$\omega_{p2} \approx -\frac{2a-b(1-D)-\frac{V_F}{V_O}R(1-D)^2}{RCa+2L}. \tag{45}$$

Finally, four zeros and four poles of $G_{\mathrm{LOOP}}(s)$ can be derived, as shown in Table I.

After obtaining all the zeros and poles, K can be fixed according to the desired phase margin and crossover frequency.

In order to find out the optimal value of K, a boost converter simulation system was built in Simulink. The input voltage is 6 V, whereas the expected output voltage is 12 V. The main inductor is 50 μH; the switching frequency is 100 kHz. The parasitic parameters are $R_C = 50$ mΩ, $R_D = 100$ mΩ, $R_L = 100$ mΩ, $R_{DS} = 11$ mΩ, and $V_D = 0.7$ V. When K is 3800, the open-loop Bode plot is as shown in Fig. 8. With these parameters, the crossover frequency is 3.68 kHz, which is

$$\begin{aligned} G_{\mathrm{LOOP}}(s) &= G_{\mathrm{PI}}(s)G_{VI}(s) \\ &= \frac{\left[(1-D)^2 - \frac{Ls+a-b(1-D)}{R} + \frac{V_F}{V_O}(1-D)^2\right]}{(Ls+a)(RCs+2R_CCs+2) - \left[b(1-D)+\frac{V_F}{V_O}R(1-D)^2\right](R_CCs+1)} \\ &\quad \times \frac{RR_CCs+R}{1-D}\,\frac{L(s+K)}{1+2Ts+2KT}\,\frac{K_P+K_PT_Is}{T_Is} \end{aligned} \tag{42}$$

$$\omega_{p1} = -\frac{a(RC+2R_CC) - b(1-D)R_CC - \frac{V_F}{V_O}RR_CC(1-D)^2 + 2L}{LRC+2LR_CC} \tag{43}$$

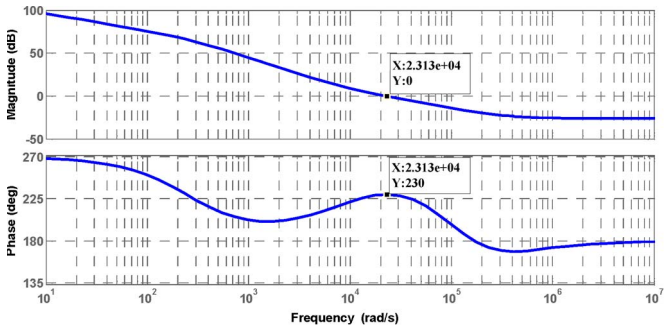

Fig. 8. Open-loop Bode plot of the system when $K = 3800$.

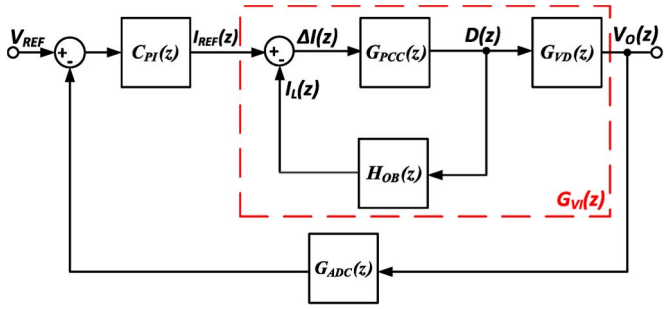

Fig. 9. Control diagram of a closed-loop digital-controlled boost converter.

about one fifth of right-half-plane zero, and the phase margin is 50°. With these settings, the controller can guarantee that the performance of the system is pretty good.

B. Robustness Analysis in Discrete Time Domain

In order to analyze the closed-loop stability of the system, it is necessary to describe the closed-loop model in the discrete time domain (z-domain). The control diagram of a closed-loop digital-controlled converter is shown in Fig. 9. Then the transfer function of each module is deduced as follows.

First, the transfer function of the boost converter should be transferred from the s-domain to the z-domain. The following can be obtained by using bilinear transform to (28), i.e.,

$$G_{VD}(z) = \frac{V_O}{1-D}\frac{(F_1-2L)z+F_1+2L}{z+1} \times \frac{(2R_CC+T)z^2+2Tz-2R_CC+T}{(F_2+F_3+F_4)z^2+(-2F_2+2F_4)z+F_2-F_3+F_4} \quad (46)$$

where

$$\begin{aligned} F_1 &= (1+V_F/V_O)R(1-D)^2T+[-a+b(1-D)]\,T \\ F_2 &= 4LC(R+R_C) \\ F_3 &= 2T\left[L+aC(R+R_C)+(1-D)^2RR_CC\right] \\ F_4 &= T^2\left[(1-D)^2R+a\right]. \end{aligned} \quad (47)$$

Then, the transfer function of the current observer in the z-domain can be deduced from (34), i.e.,

$$I_L(z)(z-1) = \frac{T}{L}\frac{z-1}{(1+KT)z-1} \times \{V_{IN}(z)-V_O(z)\,[1-D(z)]\}. \quad (48)$$

The small-signal model of the current observer in the z-domain can be obtained by using the similar approach in the s-domain, i.e.,

$$\hat{I}_L(z) = \frac{T}{L}\frac{1}{z+KTz-1}\left[\hat{D}(z)V_O(z)+D(z)\hat{V}_O(z)-\hat{V}_O(z)\right]. \quad (49)$$

The transfer function of the PCC controller in the z-domain can be derived from (5). Then its small-signal model in the z-domain can be obtained, i.e.,

$$\left[\hat{D}(z)V_O(z)+\hat{V}_O(z)D(z)\right](z+1) = \frac{\left[\hat{I}_{\rm REF}(z)-\hat{I}_L(z)\right]L+2\hat{V}_O(z)T}{T}. \quad (50)$$

According to (46), (49), and (50), the transfer function from $I_{\rm REF}$ to V_O in the z-domain can be derived by (51), shown at the bottom of the page, where $\alpha = 1+KT$. In addition, the expression of the PI controller in the z-domain is

$$C_{\rm PI}(z) = K_P + \frac{K_P}{T_I}\frac{Tz}{z-1}. \quad (52)$$

In addition, the effect of sample and hold, together with the ADC conversion time, should be considered. The transfer function of the ADC can be derived by [9]

$$G_{\rm ADC}(z) = \frac{2^N-1}{V_{\rm REF,ADC}}\frac{z+1}{\left(1+\frac{2\tau}{T}\right)z+\left(1-\frac{2\tau}{T}\right)} \quad (53)$$

where τ is the ADC conversion time, and N is the number of bits.

Finally, the system closed-loop transfer function in the z-domain can be obtained, i.e.,

$$T(z) = \frac{G_{VI}(z)C_{\rm PI}(z)}{1+G_{VI}(z)C_{\rm PI}(z)G_{\rm ADC}(z)}. \quad (54)$$

To analyze the system stability with a group of K values, the zero and pole migration plot of the closed-loop transfer function is plotted in Fig. 10. When K is 20 000, all the closed-loop poles are inside of the unit circle, and the system is stable. When K increases to 31 500, the pole approaches to the unit circle boundary. As K increases further, the pole moves out of the unit circle. Thus, the system becomes unstable.

In addition, the variations of the parasitic parameters can also affect the system robustness. To analyze the stability, the migration of poles and zeroes with a varying R_L value is plotted in Fig. 11. As the figure shows, R_L is set to 0.01, 0.1, 0.2, 0.3,

$$G_{VI}(z) = \frac{L}{T}\frac{(\alpha z-1)G_{VD}(z)}{(\alpha z^2+KTz)V_O(z)+\left[\alpha Dz^2+(KTD-2\alpha)z+1\right]G_{VD}(z)} \quad (51)$$

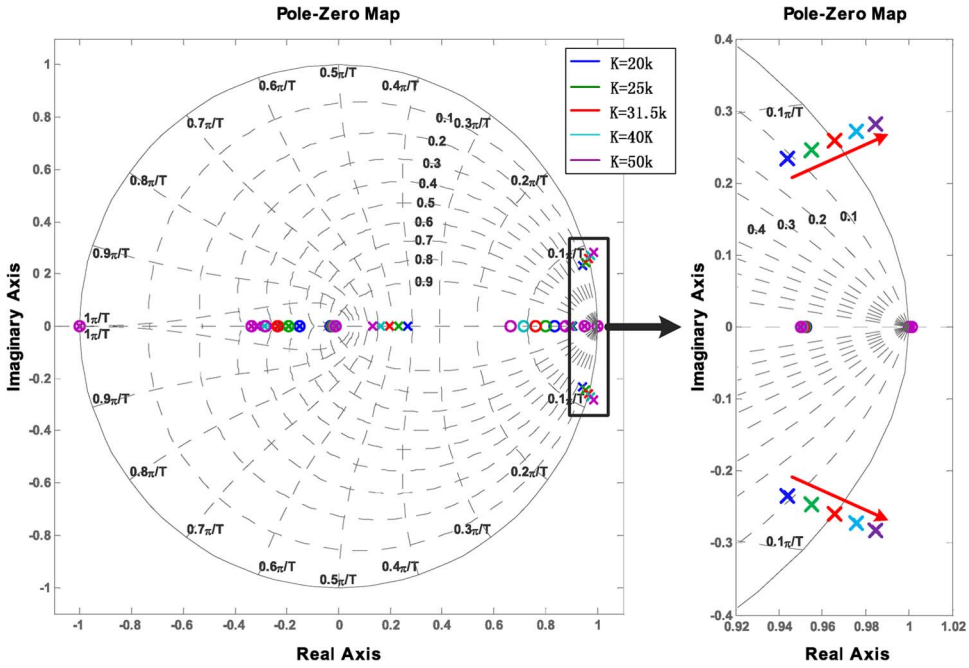

Fig. 10. Migration of poles/zeros of the digital controlled system according to the variation of K.

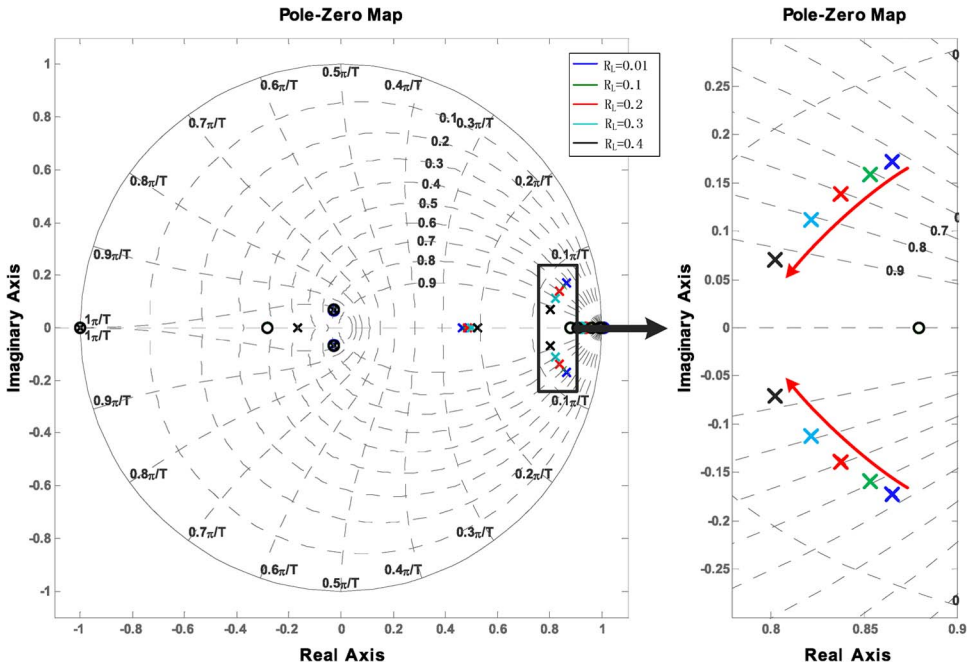

Fig. 11. Migration of poles/zeros of the digital controlled system according to the variation of R_L.

and 0.4 Ω, respectively. With the increasing of the R_L value, all of the closed-loop poles are inside of the unit circle. Thus, the digital control system remains stable. In addition, the damping ratio of the digital control system increases, and the frequency of the dominant poles does not change too much. It means that the system stability is enhanced and its bandwidth does not change much. Thus, the system stability can be guaranteed even with the variations of R_L.

The inductor value L plays an important role in the current estimation result. Suppose that the actual value of inductance is not the same as its setting one. Setting the inductance value used in the controller to be L_{ob}, then L should be replaced by L_{ob} in (49) and (50), whereas $G_{VD}(s)$ remains unchanged. In this case, the new transfer function from I_{REF} to V_O is

$$G'_{VI}(z) = \frac{L_{ob}}{L} G_{VD}(z). \tag{55}$$

Then (54) should be modified to

$$T(z) = \frac{G'_{VI}(z) C_{\mathrm{PI}}(z)}{1 + G'_{VI}(z) C_{\mathrm{PI}}(z) G_{\mathrm{ADC}}(z)}. \tag{56}$$

In order to investigate the inductance variation effect on the current loop control performance, the inductance L used for the circuit modeling is fixed to 25 μH, whereas the inductance for

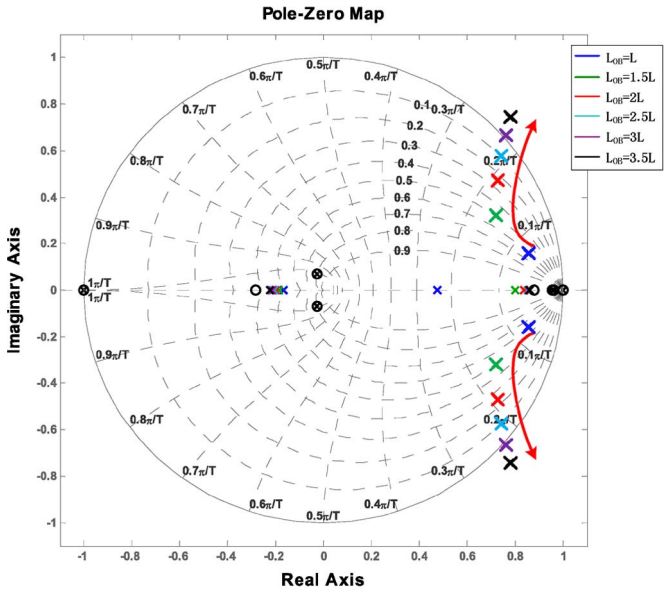

Fig. 12. Migration of poles/zeros of the digital controlled system according to the variation of L_{ob}.

TABLE II
SPECIFICATIONS OF THE TESTED BOOST CONVERTER

Input voltage	*6V*
Output voltage	*12V*
Rated output current (ROC)	*0.5A*
Voltage ripple under ROC	*1%*
Switching frequency	*100kHz*

current observer and PCC controller L_{ob} is subject to change. As shown in Fig. 12, when $L_{ob} = L = 25$ μH, all the closed-loop poles are inside of the unit circle. Thus, the system is stable. With the increasing of L_{ob}, the damping ratio of the system decreases, the pole approaches closer to the boundary of the unit circle. Thus, the system becomes more vulnerable when the disturbance happens. When $L_{ob} = 3L = 75$ μH, the pole moves out of the unit circle, the system becomes unstable. However, as long as the inductance is less than three times of its nominal value, the system stability can be guaranteed.

V. EXPERIMENTAL RESULTS

To verify the proposed algorithm, experiments are carried out with a digital controlled boost converter. Its specifications are shown in Table II.

A. Experimental Settings

The system hardware contains a control board and a power board. A Texas Instruments digital signal processor (DSP) TMS320F2812 is the core part of the control board. The control algorithm is implemented in it. The power board includes the boost converter and the signal level shifting circuits. The switching device is an Infineon BSZ110N6NS3 MOSFET. The output capacitor type is Panasonic EEHZCIE101XP. In addition, a four-channel 12-bit ADC AD7934-6 is chosen for input and output voltages sampling. Since the maximum clock frequency of the TMS320F2812 DSP is 150 MHz and the switching frequency is 100 kHz, the digital PWM (DPWM) resolution is 1500, which is between 10 and 11 bits. In order to avoid limit cycle oscillations, a dead zone with a constant threshold to the voltage sampling is implemented. By this approach, the ADC resolution can be reduced to 9 bits, which is compatible with DPWM resolution.

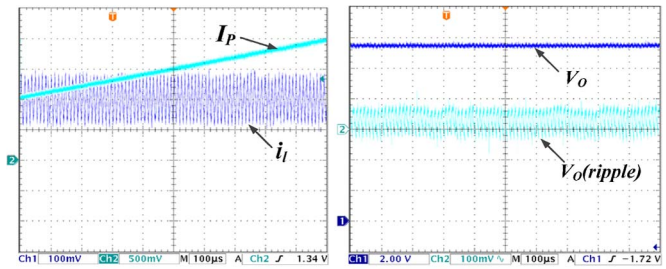

Fig. 13. (a) Estimated and actual current waveforms of the conventional current observer. (b) Output voltage waveform of the conventional current observer.

For monitoring, the estimated peak current I_P, the estimated differential current, and the actual differential current are synchronously output by a 12-bit digital-to-analog converter (DAC) TVL5616, respectively. The actual inductor current i_l is measured by a Rogowski current probe PEM CWT015 with a resolution of 200 mV/A and sampled by the ADC for actual differential current calculation.

B. Results and Analysis

1) Conventional Current Observer: Fig. 13(a) shows the waveforms of the measured inductor current i_l in channel 1 and the estimated peak current I_P in channel 2, respectively. The DAC resolution is set as 200 mV/A. The estimated current does not converge with the measured inductor current, whose peak value is 1.45 A, but has a linear upward trend. Fig. 13(b) shows the output voltage in two scales. Channel 1 is a coarse one at 2 V/div, and channel 2 is a fine one at 100 mV/div showing its ripple. As it can be seen, the average value of the output voltage is 11.46 V. The steady-state error is 0.54 V, i.e., 4.5% compared with the reference voltage.

These results prove that the PI controller does not guarantee the elimination of ΔV_O, which makes the current reference continuously increase so that the current estimation also increases in a linear upward nonconverging trend.

2) Experimental Results With SDCO: In order to verify the proposed algorithm and its robustness, experiments are carried out under impact load and line voltage disturbance conditions. For comparison, the system with conventional voltage mode is also tested under the same condition.

Fig. 14(a) shows the results with the proposed algorithm when the load changes from 24 to 18 Ω (33% increases in current). Compared with Fig. 13(b), the steady-state value of V_O changes from 11.46 to 12 V. This means that the steady-state error of V_O is successfully eliminated by the introduction of an SDCO. When the load increases, the output voltage decreases to 11.75 V and then returns to 12 V after 160 μs. When the line voltage steps down from 6 to 5 V, the waveforms are shown in Fig. 14(b). The output voltage drops to 11.72 V after the line voltage changes and then returns to 12 V in 200 μs.

The differential observer outputs are shown in Fig. 15. For comparison, the actual differential current is also presented at

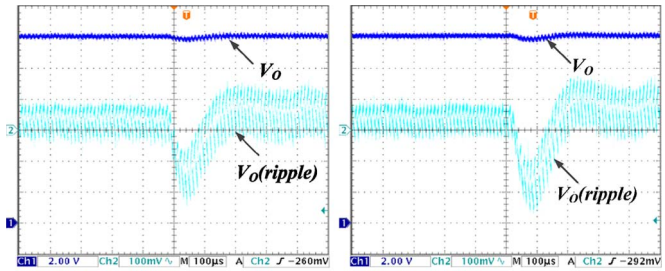

Fig. 14. Transient response waveforms with the proposed algorithm. (a) Load disturbance condition. (b) Line voltage disturbance condition.

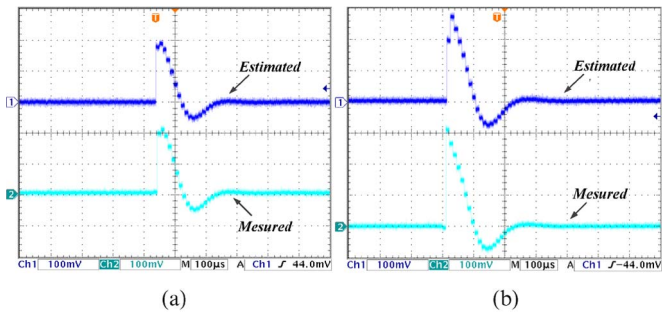

Fig. 15. Output of the differential current observer together with actual differential current. (a) Load disturbance condition. (b) Line voltage disturbance condition.

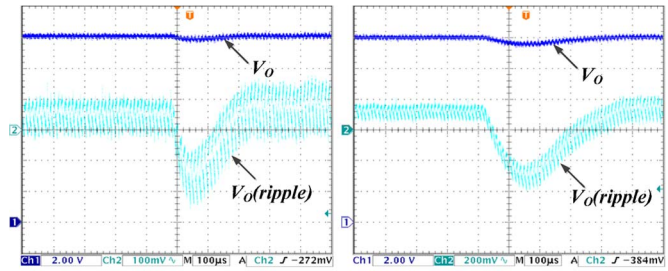

Fig. 16. Transient response waveforms with conventional voltage control. (a) Load disturbance condition. (b) Line voltage disturbance condition.

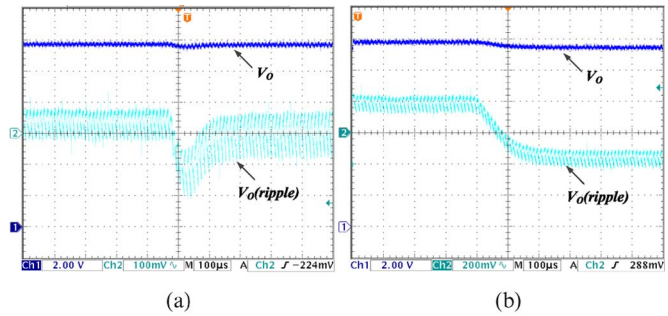

Fig. 17. Transient response waveforms with the conventional current observer without self-correction part. (a) Load disturbance condition. (b) Line voltage disturbance condition.

the same time. The scaling of the DAC output is set to 1 V/A. As shown in Fig. 15(a), the output of the differential observer jumps to 0.2 A after the load stepping up point and returns to convergence state in 160 μs, i.e., the same time length as the voltage restabilization process. On the other hand, the actual differential current jumps to 0.22 A at the same time, which is 10% larger than the estimated differential current. However, it also converges to steady state in about 160 μs.

The differential observer output under line voltage disturbance is shown in Fig. 15(b). It jumps to 0.28 A after line voltage steps down point and converges close to zero in 200 μs, i.e., also the same response speed as the transient response of voltage. In addition, the actual differential current jumps to 0.32 A, which is 14.2% larger than the estimated differential current. However, it also converges to steady state in about 200 μs.

According to the results shown in Fig. 15, the estimated differential current is quite close to the actual differential current.

The results of conventional voltage mode control under load disturbance are shown in Fig. 16(a), where the output voltage drops to 11.74 V and then returns to 12 V in 240 μs. Compared with the proposed algorithm, although the transient voltage drop stays the same, the response time is 50% longer. Under the line voltage disturbance, the waveforms are shown in Fig. 16(b). The output voltage decreases to 11.42 V and then converges in 500 μs. This process takes 150% longer, and the voltage decrease is 162% more than in the proposed algorithm.

The results of the conventional current observer without self-correction part under load disturbance are shown in Fig. 17(a), where the output voltage drops from 11.75 to 11.5 V and then returns to 11.72 V in 175 μs. Compared with the proposed algorithm, although the transient voltage drop stays the same, the output voltage steady-state error always exists, and the response time is 9.4% longer. Under the line voltage disturbance, the waveforms are shown in Fig. 17(b). The output voltage decreases to 11.78 V and then converges in 11.34 V in 220 μs. Again, the output voltage steady-state error always exists, and it enlargers further after the line disturbance happens. In addition, the transient process takes 10% longer than the proposed algorithm.

According to the preceding experimental results, even when the system is subject to sudden load and line voltage disturbances, it is able to respond quickly and converge to a new steady state with no output voltage steady-state error. With the proposed algorithm, the system shows good robustness.

VI. Conclusion

The basic cause of output voltage steady-state error in a sensorless current controlled boost converter has been established in theory. On this basis, the system small-signal model, including the parasitic parameters, is constructed and analyzed. Then an SCDO is proposed. Simulation shows that the proposed algorithm is very robust. In addition, its computational complexity is low and easy to implement. With the proposed algorithm, the system ultimately achieves no voltage steady-state error with good transient performance despite parasitic parameters variation. Experimental results show that the control algorithm proposed in this paper is accurate and effective and has a good theoretical and practical application potential.

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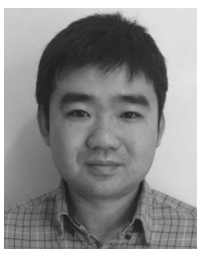

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