Sensorless Predictive Peak Current Control for Boost Converter Using Comprehensive Compensation Strategy

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***Abstract*—For a sensorless predictive-peak-current-controlled boost converter, the output voltage steady-state error cannot be eliminated by voltage loop PI controller. The basic cause for this is investigated through analysis and theoretical approaches. To eliminate the voltage steady-state error and achieve high-accuracy current estimation, a comprehensive compensation strategy is proposed. First, a compensation algorithm for output voltage sampling is introduced. It can not only effectively eliminate the output voltage steady-state error but also guarantee current observer convergence. The compensation schemes for component parasitic parameter effects and switching delay are also investigated. With this comprehensive compensation strategy, both the system transient response and current estimation accuracy are greatly improved. Finally, the effectiveness of the proposed algorithm is verified by experimental results.**

***Index Terms*—Boost converter, comprehensive compensation strategy, predictive peak current control, sensorless.**

I. Introduction

In RECENT years, digital control for a boost converter has become one of the research hot topics [1]–[8]. Compared with the voltage control mode, the current control mode has higher response speed and larger loop gain bandwidth. However, in current control mode, when the pulsewidth modulation (PWM) duty ratio is higher than 50%, a slope compensation circuit becomes necessary to maintain system stability [9].

Due to its high robustness and high response speed, predictive current control (PCC) has been brought into boost converter current control loop design and has been widely investigated. In PCC mode, the inductor current of the next switching cycle should be predicted, and the duty ratio for the next switching cycle can be calculated according to the reference current and predicted current. The inductor current can only be sampled once in each switching cycle, which is normally equal to the control period in a digital control boost converter system. In addition, PWM duty ratio calculation is carried out once in each switching cycle. A high-response digital PCC strategy was proposed by Chen *et al.* [10], where the disturbance of inductor current can be eliminated in the following switching cycle in valley, peak, and average current control modes. The authors verified that system stability can be guaranteed by combining the peak, average, or valley current control mode with the specific PWM scheme and that the compensation circuit can be eliminated. Bibian *et al.* investigated a high-performance PCC based on a dead beat digital control strategy in [11]. The biggest advantage of this control strategy is the low calculation complexity, but its response speed is low due to its error elimination once in every four switching cycles. Lai and Yeh further investigated PCC for the peak current control mode in [12]. The effectiveness of the limit cycle elimination by PCC with the leading edge PWM modulation scheme was verified by theoretical derivation.

For conventional PCC of a boost converter system, precise current sampling is necessary. There are three most common current sampling types. The first type uses a shunt resistor in series with the switching component, the second type uses current mirror to reconstruct the switch component current, and the third type uses a Hall current sensor. The third is the most accurate, but the price of Hall current sensors is relatively high, and the additional current sampling module reduces system reliability. The sensorless current control can maintain the advantages of current mode control without using the current sensor. Therefore, combining the sensorless current control with PCC for boost converter system design has very good potential for both academic and practical applications. For sensorless current control, the current observer is normally used for its current estimation.

The current observer is built on the basis of accurate system modeling [13]–[15]. Midya *et al.* proposed a sensorless current control strategy based on a current observer in 2001 [16], where the inductor current estimation relied on sampled input and output voltages. However, for real-time digital control, the implementation of this strategy is far too complex. A less complex algorithm using a feedforward current observer based on the input voltage was published in 2004 [17]; the input voltage feedforward was introduced to the observer, and it can avoid the impact of the output voltage variations on the current observer. However, in this algorithm, the influence of the parasitic parameters was not considered, and the current estimation error is relatively large. To improve control accuracy,

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Beccuti *et al.* introduced a current observer based on the extended Kalman filter [18]. The explicit model predictive control was implemented, and a piecewise affine method was used to obtain the optimal control parameters. The optimization tuning process can only be carried out in offline mode due to its high calculation complexity. Qahouq and Arikatla published a paper on sensorless adaptive voltage positioning for a buck converter [19]. This algorithm is easy to implement as it relies only on the signals used in conventional voltage control mode. However, the assumption of the constant equivalent resistance from the input side to the output side is not accurate enough because the equivalent resistance changes with load variations. This kind of assumption can affect the performance of current control. Qiu *et al.* proposed an average current mode observer in 2010 [20]. Due to considering the impact of a number of parasitic parameters, the current estimation accuracy is higher but still has potential to be improved, and the switch node voltage needs to be sampled to determine the parasitic parameters, requiring an additional signal sampling module.

However, all the published sensorless current control strategies have not addressed the issue of the output voltage steady-state error. For sensorless current control, the PI controller of the voltage control loop cannot guarantee the elimination of the output voltage steady-state error. This issue can be theoretically verified. The voltage sampling compensation to eliminate the effect of output capacitor equivalent series resistance (ESR) affection was not considered in the former publications. This would lead to low accuracy or convergence problems of current estimation and even system instability. In particular, when the output current is high, this compensation becomes more essential. In addition, if the passive components, parasitic parameters, and switch turn-on and turn-off delays are not properly considered, the expected performance cannot be achieved. All of the above items are the main issues in this paper.

This paper is organized as follows: In Section II, a first-order current observer and the PCC algorithm are proposed for sensorless peak current control mode. When the inductor current disturbance occurs, only one switching cycle is needed to eliminate the error between the reference current and the actual inductor peak current. In Section III, a detailed theoretical analysis of the output voltage steady-state error is carried out in a sensorless PCC (SPCC) system, and its calculation formulas are derived. Based on this, in Section IV, the output voltage sampling compensation algorithm is proposed. It not only effectively eliminates the output voltage steady-state error but also eliminates the current estimation error caused by the offset of the sampling point. Meanwhile, a variety of parasitic parameters are introduced into the system small signal model, adding compensation to eliminate the switching delay. With these comprehensive compensation approaches, current observer accuracy can be greatly improved. Finally, the experimental results and analysis are presented.

II. Sensorless Peak Current Control

The structure of conventional sensorless current control for a boost converter is shown in Fig. 1. Inductor current and PWM duty cycle are deduced according to the input and output

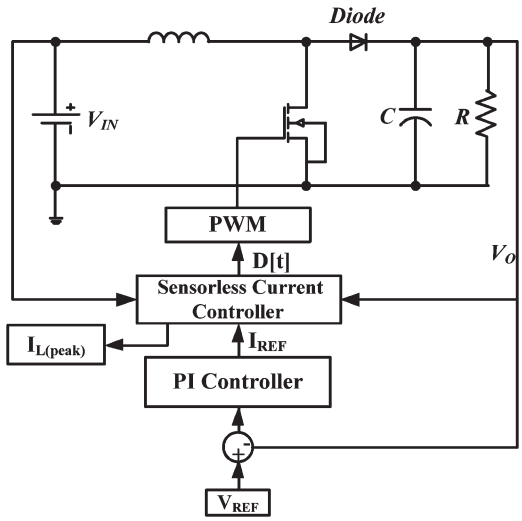


Fig. 1. Structure of conventional sensorless current control for a boost converter.

voltages. The system is comprised of two control loops. The outer loop is a voltage control loop using a PI controller and outputting a current reference. The inner loop is a current control loop using sensorless predictive peak current control mode. The voltage PI controller design can be referenced from [11]. The current control loop design is the main issue in this paper.

Working in continuous current mode (CCM), without consideration of the parasitic parameters of inductor L and output capacitor C, using average inductor current $I_L(t)$ and average output voltage $V_O(t)$ as state variables, the state equations are

$$\frac{dI_L(t)}{dt} = \frac{V_{\rm IN}(t)}{L} - \frac{(1-D)V_O(t)}{L} \tag{1}$$

$$\frac{dV_O(t)}{dt} = \frac{(1-D)I_L(t)}{C} - \frac{V_O(t)}{RC} \tag{2}$$

where D is the duty ratio, R is the equivalent load, and $V_{\rm IN}(t)$ is the input voltage. Equations (1) and (2) are the basic boost converter state equations from which the observer can be derived.

A. First-Order Current Observer

According to (1) and (2), when the boost converter works under CCM, the system is observable. The inductor current can be estimated by using current observer. In the actual system, voltage sampling, predictive current calculation, and duty ratio updating should be finished in one switching cycle. In order to precisely control the sampling value and leave enough time for algorithm calculation, input and output voltage sampling is done at the beginning of the switching cycle and the sampled values used for inductor current estimation. The deducing process for the first-order current observer in discrete format is as follows.

The positive slope of inductor current in the kth switching cycle is $M_1(k)$, and the negative slope absolute value in the

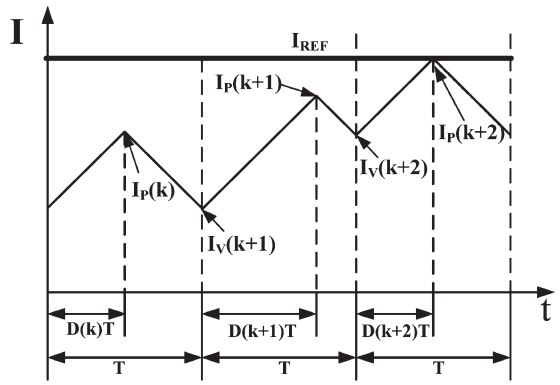


Fig. 2. Inductor current waveform of peak current control mode.

same switching cycle is $M_2(k)$, then

$$M_1(k) = \frac{V_{\rm IN}(k)}{L} \tag{3}$$

$$M_2(k) = \frac{V_O - V_{\rm IN}(k)}{L}. \tag{4}$$

The differential equation in the time domain for inductor current $I_L(k)$ is

$$I_L(k+1) = I_L(k) - M_2(k)D'(k)T + M_1(k)D(k)T \tag{5}$$

where $D'(k)$ is $1 - D(k)$. Equation (5) is the observer equation. The inductor peak current of each switching cycle can be estimated by $I_P(K+1) = I_P(k) - M_2(k)D'(k)T + M_1(k)D(k)T$, where $I_P(k)$ is the estimated peak current.

B. Peak Current Control Mode

Fig. 2 shows the inductor current waveform under peak current control mode by using the "trailing edge PWM" scheme. When the output voltage is disturbed, the voltage loop output is $I_{\rm REF}$, which is the reference current. In order to eliminate the disturbance, the PWM duty ratio of the $k+1$th cycle is regulated to make the system achieve the steady state in the $k+2$th cycle while the inductor peak current will be equal to $I_{\rm REF}$. The slopes of the continuous three switching cycles can be regarded as constant because the switching cycle is short. Hence, $M_1(k) \approx M_1(k+1) \approx M_1(k+2)$ and $M_2(k) \approx M_2(k+1) \approx M_2(k+2)$.

$I_v(k+1)$ and $I_v(k+2)$, which represent the $k+1$th and the $k+2$th cycle starting point inductor currents, are deduced from $I_P(k)$ and $I_{\rm REF}$. Thus

$$I_V(k+1) = I_P(k) - M_2\left[1 - D(k)\right]T \tag{6}$$

$$I_V(k+2) = I_{\rm REF} - M_1 D(k+2)T$$

$$= I_{\rm REF} - \frac{M_1 M_2}{M_1 + M_2}T. \tag{7}$$

From (5), the PWM duty ratio of the $k+1$th cycle is

$$D(k+1) = \frac{I_V(k+2) - I_V(k+1) + M_2 T}{(M_1 + M_2)T}. \tag{8}$$

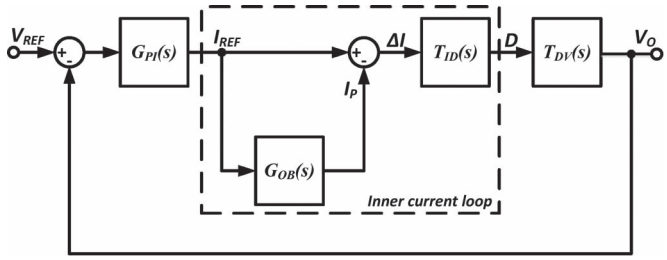


Fig. 3. Closed-loop small-signal model of the SPCC boost converter.

If the disturbance happens during a switching cycle in steady state, the duty ratio can be derived according to $D(k) = M_2/(M_1 + M_2)$. Using this equation together with (6) and (7) and substituting them into (8), the following equation can be deduced:

$$D(k+1) = \frac{I_{\rm REF} - I_P(k) + M_2 T}{(M_1 + M_2)T} \tag{9}$$

which indicates that $D(k+1)$ is proportional to the difference between reference current and estimated current of the kth cycle.

$D(k+1)$ is the control variable of the system. As shown in Fig. 2, the disturbance can be eliminated in one switching cycle; hence, the response speed of the above control strategy is quite high.

However, there are two types of errors that lower the performance of the sensorless current control. One is the output voltage steady-state error. Because there is no pole at the origin in the open-loop transfer function, the error increases with increasing output current. The other is the steady-state error of the current estimation caused by the low accuracy of observer modeling. In the following sections, these errors are investigated and addressed.

III. Output Voltage Steady-State Error Analysis

For a current-mode-controlled boost converter with a current sensor, the voltage loop PI controller is able to eliminate ΔV_O, which is the steady-state error of the output voltage, by providing a pole at the origin. However, this conclusion does not necessarily apply for the SPCC because the pole at the origin from the PI controller's integration part is eliminated by the zero at the origin from SPCC. When there is no pole at the origin in the open-loop transfer function, the integration effect of the PI controller is nullified, and hence, the output voltage may have a steady-state error.

A. Basic Cause of ΔV_O

The closed-loop small-signal model in continuous time domain is shown in Fig. 3, where $G_{\rm PI}(s)$, $G_{\rm OB}(s)$, $T_{\rm ID}(s)$, and $T_{\rm DV}(s)$ are the transfer functions of the PI controller, $I_{\rm REF}$ to I_P, ΔI to duty ratio, and duty ratio to output voltage, respectively. Moreover, ΔI is equal to $(I_{\rm REF} - I_P)$. Assuming $I_{\rm REF}$ and I_P are sampled at the beginning of each switching cycle, then I_P strictly follows $I_{\rm REF}$ with two switching cycle delays.

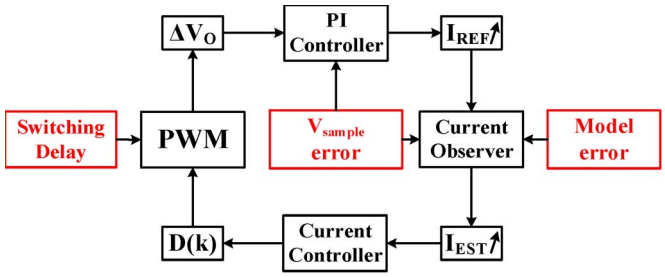


Fig. 4. Generating process of the output voltage steady-state error.

Therefore, in discontinuous time domain, the relationship between $I_{\rm REF}$ and I_P is

$$I_P = I_{\rm REF} z^{-2}. \tag{10}$$

Then, the transfer function from $I_{\rm REF}$ to ΔI is

$$T_{II}(z) = \frac{\Delta I}{I_{\rm REF}} = \frac{(z-1)(z+1)}{z^2}. \tag{11}$$

According to Euler transformation, $z-1$ generates the zero at the origin in the continuous time domain since $s = (z-1)/T$. Therefore, (11) in continuous time domain is

$$T_{II}(s) = \frac{sT(sT+2)}{(sT+1)^2}. \tag{12}$$

Moreover, $G_{\rm PI}(s)$ in continuous time domain is

$$G_{PI}(s) = K_P\left(1 + \frac{1}{sT_I}\right) \tag{13}$$

where K_P and T_I are the proportional and integral coefficients, respectively.

From (12) and (13), the pole at the origin of the PI controller is eliminated by the zero at the origin provided by $T_{II}(s)$. Therefore, the elimination of the output steady-state error cannot be guaranteed by the voltage loop PI controller. This phenomenon has not been considered in published SPCC research papers.

The process of generating ΔV_O is shown in Fig. 4. A variety of nonideal factors (such as the parasitic resistance of the inductor) will cause some drop in the output voltage. In this situation, the PI controller generates a continually increasing $I_{\rm REF}$, and the current loop forces the predictive current to follow the rising $I_{\rm REF}$. According to (9), this increasing inductor current finally stabilizes the duty ratio and ΔV_O. If the diode-conducting voltage drop V_D is considered, the theoretical value of ΔV_O is given below.

B. Calculation of ΔV_O

Let I'_P be the actual inductor peak current. When the system is in its steady state, the variation of I'_P between the two neighboring switching cycles is zero. Including v_D, this peak current differential equation can be described in

$$\begin{aligned}\Delta I'_P &= I'_P(k+1) - I'_P(k) \\ &= \frac{V_{\rm IN}}{L}T - \frac{V_O}{L}D'(k)T - \frac{V_D}{L}D'(k)T = 0.\end{aligned} \tag{14}$$

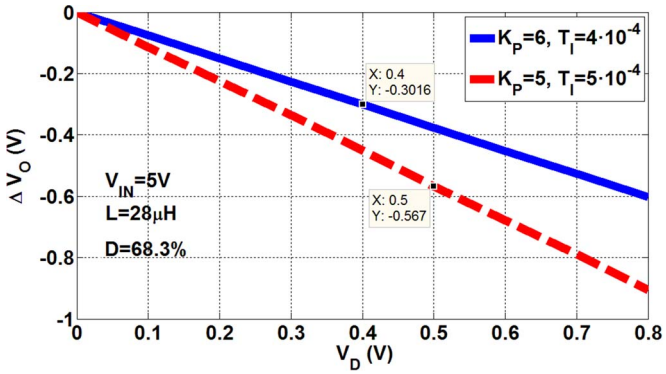


Fig. 5. Simulation results of modified ΔV_O versus different V_D values under two sets of PI controller parameters.

However, based on (5), the variation of I_P is

$$\Delta I_P = I_P(k+1) - I_P(k) = \frac{V_{\rm IN}}{L}T - \frac{V_O}{L}D'(k)T. \tag{15}$$

From (14), the equation $V_{\rm IN}T/L - V_O D'(k)T/L = V_D D'(k)T/L$ can be obtained. Substituting it into (15), then the following equation can be derived:

$$\Delta I_P = \frac{V_D}{L}D'(k)T. \tag{16}$$

As $\Delta V_O = V_{\rm SAMPLE} - V_{\rm REF}$, the negative ΔV_O leads the reference current to increase at a constant slope. According to the transfer function of the PI controller, the variation of $I_{\rm REF}$ in the two neighboring switching cycles is

$$\Delta I_{\rm REF} = -\frac{K_P T}{T_I}\Delta V_O. \tag{17}$$

Compared with the actual inductor current, the estimated inductor current has two switching cycle delays because of the digital control character. Hence, in the steady state, $\Delta I_{\rm REF} = \Delta I_P$, ΔV_O can be obtained from (16) and (17) as

$$\Delta V_O = -\frac{D'T_I}{LK_P}V_D. \tag{18}$$

According to (16) and (18), ΔI_P and ΔV_O are proportional to V_D. In order to verify this conclusion, a simulation system of the boost converter was built under Simulink. The input voltage is 5 V, whereas the expected output voltage is 15 V. The main inductor is 28 μH, and V_D varies from 0 to 0.8 V. The current loop control algorithm is based on (8), whereas the voltage loop is the PI controller. The simulation results of different V_D versus ΔV_O under two sets of PI controller parameters are shown in Fig. 5. The simulation results, as marked on the curves, are exactly the same as the results calculated by (18).

The parasitic resistance of the inductor R_L, the MOSFET-conducting resistance $R_{\rm DS}$, diode-equivalent conducting resistance R_D, and other parasitic factors can have a similar effect on the output voltage steady-state error as V_D does. If all these parasitic factors are considered, ΔV_O is

$$\begin{aligned}\Delta V_O = \frac{T_I}{LK_P}\{&I_{\rm AV}(k)\left[R_D D'(k) + R_L + R_{\rm DS}D(k)\right] \\ &+ D'(k)V_D\}\end{aligned} \tag{19}$$

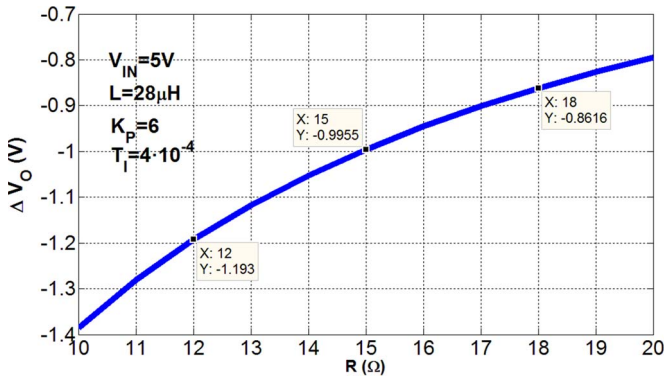


Fig. 6. Simulation results of modified ΔV_O versus load.

where $I_{\rm AV}(k)$ is the estimated average inductor current. Thus, $I_{\rm AV}(k)$ is deduced from $I_P(k)$ in Fig. 2 as

$$I_{\rm AV}(k) = I_P(k) + \frac{T}{2} \times \left[M_1(k)D^2(k) - M_2(k)D'(k) - M_2(k)D(K)D'(k)\right]. \quad (20)$$

According to (19), ΔV_O enlarges with increasing inductor current, which is decided by the load. For better understanding, setting the parasitic parameters as $R_C = 30$ mΩ, $R_D = 100$ mΩ, $R_L = 50$ mΩ, $R_{DS} = 11$ mΩ, and $V_D = 0.7$ V, the simulation was carried out to find out the precise relationship between ΔV_O, and the results are shown in Fig. 6. As can been seen from the marked points, the simulation results fit well with (19).

Hence, for a high-current boost converter, this error becomes unacceptable.

In addition, although the inductance is prone to offset and the system clock may also deviate from setting values, from (5) and (8), the changes in these parameters do not generate ΔV_O.

IV. Comprehensive Compensation Strategy

The compensation strategy consists of two parts, namely, output voltage sampling compensation and system nonlinear factors compensation.

A. Compensation Strategy For Output Voltage Sampling

1) Compensation Strategy For Current Control Loop: The output voltage has a great impact on the estimation value of the inductor current. Because there is ripple in the output voltage, the error caused by voltage sampling needs to be considered.

As described in (4) and (5), the inductor current is affected by the output voltage only during the $(1-D)T$ period. Hence, the correct output voltage value to calculate the inductor current is the average voltage V_A during $(1-D)T$. Because of the capacitor ESR effect, the output voltage curve does not continuously change. V_A is not equal to the average output voltage $\overline{V_O}$ of the whole control cycle. Fig. 7 shows the output voltage affected by the capacitor ESR. Point A is the ideal sampling time point that is equal to V_A. In the actual system, the position of A varies with the PWM duty ratio; hence, point A in Fig. 6 is only for demonstration.

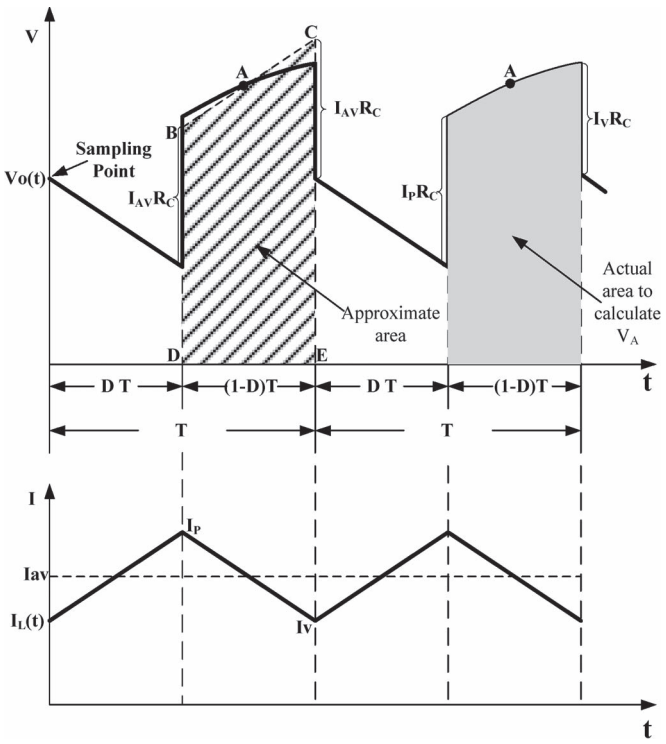


Fig. 7. Output voltage and inductor current waveforms affected by ESR in steady state.

However, in the actual system, the output voltage is sampled at the beginning of each switching cycle; hence, it is necessary to compensate the sampled value $V_{\rm SAMPLE}$ to V_A.

As shown in Fig. 7, due to the decreasing inductor current during $(1-D)T$ while the output current is constant, the capacitor charging current should decrease, and the output voltage becomes a second-order curve during the $(1-D)T$ period. The slope of the curve during $(1-D)T$ is related to R_C and dI_L/dt. For example, by choosing a low ESR capacitor, the slope as Fig. 7 shows, is positive. On the other hand, if the ESR is large enough, the slope will be negative.

In order to deduce V_A, the area shaded in gray value should be calculated. The output voltage function in the time domain during $(1-D)T$ can be described by (21). The derivation is given in the Appendix. Thus

$$V_O(t) = V_{\rm SAMPLE} - V_{\rm PP} + I_L(t)R_C + \frac{I_P t - I_{\rm AV}(1-D)t - M_2 t^2}{C} \quad (21)$$

where $V_{\rm PP}$ is the peak-to-peak value of the output capacitor voltage. The equation for $V_{\rm PP}$ calculation is

$$V_{\rm PP} = \frac{I_O D}{fC} = \frac{I_{\rm AV} D' D}{fC}. \quad (22)$$

However, to calculate the integration value according to (21) is far too complex. In the actual system, the calculation of the area shaded in gray can be replaced by calculating the trapezoidal area BCDE. The length of CE is

$V_{\mathrm{SAMPLE}} + I_{\mathrm{AV}} R_C$, whereas the length of BD is $V_{\mathrm{SAMPLE}} - V_{\mathrm{PP}} + I_{\mathrm{AV}} R_C$. Therefore, the average voltage is

$$\begin{aligned} V_A &= V_{\mathrm{SAMPLE}} + I_{\mathrm{AV}} R_C - \frac{V_{\mathrm{PP}}}{2} \\ &= V_{\mathrm{SAMPLE}} + I_{\mathrm{AV}} R_{\mathrm{COMP}} \end{aligned} \tag{23}$$

where $R_{\mathrm{COMP}} = R_C - D'D/2fC$ is the equivalent compensation resistor. $R_C > D'D/2fC$ is guaranteed according to the actual electrical parameters of the system; hence, R_{COMP} can always be a positive value.

The difference between the actual average voltage and the value calculated by (23) is $V_{PP}/30D$, which can be ignored compared with the actual average value. The detailed derivation is given in the Appendix.

As can be seen from (23), when the ESR value R_C is higher, R_{COMP} will be larger. If the average current is high, the compensation cannot be ignored. In this case, the voltage sampling compensation plays a key role in system performance improvement.

ΔV_O can be eliminated by output voltage compensation. By substituting R_{COMP}, the following equation can be deduced from (15) and (17):

$$-\frac{K_P}{T_I}\Delta V_O(k)T = \frac{V_{\mathrm{IN}}}{L}T - \frac{V_O + I_{\mathrm{AV}}(k)R_{\mathrm{COMP}}}{L}D'(k)T. \tag{24}$$

Then, the following equation can be derived from (24):

$$\begin{aligned} &\Delta V(k+1) - \Delta V_O(k) \\ &\qquad = \frac{[I_{\mathrm{AV}}(k+1) - I_{\mathrm{AV}}(k)]\,T_I R_{\mathrm{COMP}}}{K_P L} D'(k). \end{aligned} \tag{25}$$

As shown in the analysis in Section III, if the actual output voltage is lower than expected, i.e., ΔV_O is negative, whereas $I_{\mathrm{AV}}(k)$ is rising, the right side of (25) is positive, indicating that ΔV_O continues to increase, eventually converging to zero. Elimination of ΔV_O means that the reference current can be kept constant so the estimated value of the inductor current will converge. By introducing the output voltage compensation mechanism, (14) is amended to

$$\begin{aligned} \Delta I_P = 0 = \frac{V_{\mathrm{IN}}}{L}T - \frac{V_O + I'_{\mathrm{AV}}(k)R_{\mathrm{COMP}}}{L}D'(k)T \\ - \frac{V_D}{L}D'(k)T \end{aligned} \tag{26}$$

where $I'_{\mathrm{AV}}(k)$ is the average current value under the actual V_D value.

Now, the error caused by V_D can be compensated using the estimated value of the inductor current. From (24) and (26), (27) can be deduced as follows:

$$I_{\mathrm{AV}}(k) - I'_{\mathrm{AV}}(k) = \frac{V_D}{R_{\mathrm{COMP}}}. \tag{27}$$

As shown in (27), when the system parasitic parameters change, the system model changes as well. However, the compensation strategy proposed in this paper can effectively eliminate the steady-state error of the output voltage by adjusting the estimated value of the inductor current.

2) Voltage Compensation Strategy of Voltage Control Loop: Similarly, the voltage sampling compensation is also necessary for the voltage control loop. Because the voltage control loop reference is set as the average output voltage, the feedback voltage should be the average voltage of the whole control cycle, and this feedback voltage can be derived from the sampled voltage with compensation.

The average voltage is equal to the average voltage of output capacitor; hence, the compensation process can be divided into two steps.

In the first step, the sampled voltage value is compensated to the capacitor voltage value that is the peak voltage value at the sampling moment. The compensated value is

$$V_{\mathrm{COMP1}} = V_{\mathrm{SAMPLE}} + I_{\mathrm{AV}}(1-D)R_C. \tag{28}$$

In the second step, the peak voltage value of the capacitor is compensated as its average value, i.e.,

$$V_{\mathrm{COMP2}} = V_{\mathrm{COMP1}} - \frac{1}{2}V_{\mathrm{PP}}. \tag{29}$$

Therefore, the total compensation value is

$$V_{\mathrm{COMP}} = V_{\mathrm{SAMPLE}} + I_{\mathrm{AV}}(1-D)R_C - \frac{I_{\mathrm{AV}}D'D}{2fC}. \tag{30}$$

Compensating the sampled output voltage by using (30), the feedback voltage will be the average output voltage.

By using the above compensation scheme, ΔV_O can be eliminated. However, there are other parasitic parameters and nonlinear factors in the actual system, and these items can cause an error in the current estimation.

B. Compensation Strategy For System Nonlinear Factors

According to the above investigations, the control structure of the system after the output voltage sampling compensation is shown in Fig. 8. Because no current sensor is used in this system, there is no direct way to correct the current estimation. In this case, the accuracy of the estimated current entirely depends on the accuracy of the observer. If the parasitic parameters and various nonlinear factors are not considered, the estimated current will have a certain amount of error. When a disturbance or a load change occurs, the inductor current estimation error can cause the system to take longer to converge, resulting in a significant decline in the system dynamic performance.

After considering the compensation of parasitic parameters and output voltage sampling, the calculation functions for $M_1(k)$ and $M_2(k)$ become

$$M_1(k) = \frac{V_I(k) - I_{\mathrm{AV}}(k)(R_{\mathrm{DS}} + R_L)}{L} \tag{31}$$

$$M_2(k) = \frac{V_O(k) - V_I(k) + V_D + I_{\mathrm{AV}}(k)(R_D + R_L + R_{\mathrm{COMP}})}{L}. \tag{32}$$

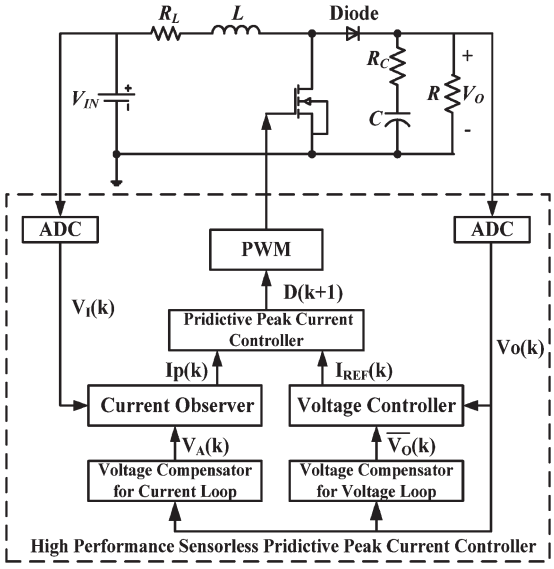


Fig. 8. Digital system block diagram of the proposed controller.

Using (31) and (32) to modify (15), the more accurate scheme for inductor peak current estimation can be deduced as

$$I_p(k+1) - I_p(k) = \frac{V_{\rm IN}}{L}T - \frac{V_o}{L}D'(k)T - \frac{I_{\rm AV}(k)T}{L}R_T - \frac{V_D}{L}D'(k)T \quad (33)$$

where $R_T = (R_{\rm COMP} + R_D)D'(k) + R_L + R_{\rm DS}D(k)$; R_T is the overall equivalent compensation resistance.

If the parasitic parameters change with the environment and other factors, the actual equivalent resistance is ΔR_T larger than the compensated equivalent resistance, and diode voltage drop is ΔV_D larger than the value used in the observer. As described in (25), ΔV_O still can converge to zero. Then, $I'_P(k)$ can be obtained by the following equation:

$$I'_P(k+1) - I'_P(k) = \frac{V_{\rm IN}}{L}T - \frac{V_O}{L}D'(k)T - \frac{I'_{\rm AV}(k)T}{L}(R_T + \Delta R_T) - \frac{V_D + \Delta V_D}{L}D'(k)T. \quad (34)$$

In steady-state condition, (33) and (34) are equal to zero. Then, the inductor current estimation error caused by parasitic parameter variation can be deduced from

$$\Delta I_P(k) = \frac{I'_{\rm AV}(k)\Delta R_T + \Delta V_D D'(k)}{R_T} \quad (35)$$

where $\Delta R_T = (\Delta R_C + \Delta R_D)D'(k) + \Delta R_L + \Delta R_{\rm DS}D(k)$.

In order to investigate the affection on system robustness by parasitic parameter variations, a mixed-signal simulation system has been built. Using the same control parameters, the initial parasitic parameters are $R_C = 30$ mΩ, $R_D = 100$ mΩ, $R_L = 50$ mΩ, $R_{\rm DS} = 11$ mΩ, and $V_D = 0.7$ V. If one of them changes, it can cause an error between the actual peak inductor current and estimated value. Setting the estimation error limitation as 20%, Table I shows the simulation results on each parasitic parameter variation degree (percentage based on its initial value) at this estimation error limitation.

TABLE I
VARIATION DEGREE OF EACH PARASITIC PARAMETER AT 20% ESTIMATION ERROR OF INDUCTOR CURRENT

Parasitic parameters	*Variation degree (percentage)*
R_C	*332%*
R_D	*111%*
R_L	*65%*
R_{DS}	*409%*
V_D	*39%*

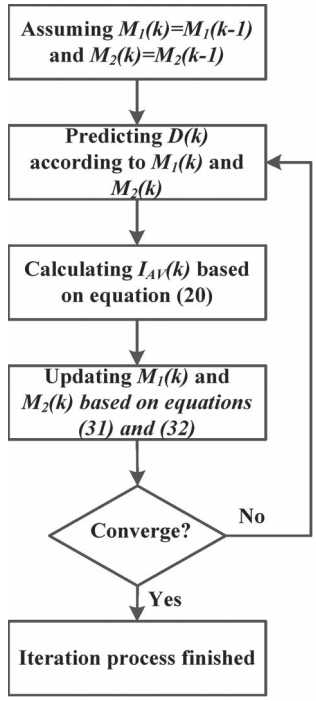


Fig. 9. Iteration process to calculate $I_{\rm AV}(k)$, M_1k, and M_2k.

There are R_C, R_D, R_L, and $R_{\rm DS}$ involved in R_T; hence, its value is relatively large. However, because the change in one specific parasitic parameter gives only a small change ΔR_T, the effect on inductor estimation error should be very limited.

As can be seen from (20), (31), and (32), there is an iterative relationship between $I_{\rm AV}(k)$, $M_1(k)$, and $M_2(k)$, as shown as Fig. 9. During each iterative process, first, $D(k)$ is derived according to $M_1(k)$ and $M_2(k)$. Then, $I_{\rm AV}(k)$ can be obtained based on (20). Finally, $M_1(k)$ and $M_2(k)$ are updated according to (31) and (32), respectively. In addition, the above iteration process keeps going until the converging condition is satisfied. It can be very time consuming to finish one iteration process, but it can be reasonably simplified. As previously mentioned, the slopes of the inductor current do not change during the two neighboring switching cycles. Thus, $M_1(k) \approx M_1(k-1)$, $M_2(k) \approx M_2(k-1)$, and (20) can be converted to

$$I_{\rm AV}(k) = I_P(k) + \frac{T}{2}\left[M_1(k-1)D^2(k) - M_2(k-1)D'(k) - M_2(k-1)D(k)D'(k)\right]. \quad (36)$$

According to (36), when the duty ratio of the kth cycle is decided, $I_{\rm AV}(k)$ can be calculated according to the slopes of the

TABLE II
SPECIFICATIONS OF TESTED BOOST CONVERTER

Input voltage	*5V*
Output voltage	*15V*
Rated output current (ROC)	*1A*
Voltage ripple under ROC	*1.5%*
Switching frequency	*100kHz*

previous cycle. The entire calculation process can be completed in the $k-1$th cycle, leaving more time margin for other control algorithms. However, using the conventional algorithm according to (20), (31), and (32), the iterative calculation process can only be activated after the analog-to-digital conversion of the kth cycle. It is not satisfactory as it is both complex and time consuming.

Besides these parasitic parameters, the delay of the switching devices also needs to be compensated [21], [22]. In order to eliminate the impact of the switch component, delay compensation should be considered, and the compensation formula is given by

$$D^*(k) = D(k) + \frac{T_{\mathrm{COM}} - T_{\mathrm{ON}} + T_{\mathrm{OFF}}}{T} \tag{37}$$

where $D^*(k)$ is the duty ratio after compensation, and T_{COM} is the compensation time. T_{ON} and T_{OFF} are known from the component datasheet, and T_{COM} can be derived according to $(T_{\mathrm{COM}} - T_{\mathrm{ON}} + T_{\mathrm{OFF}})/T = 0$ in (37). After the compensation, the actual duty ratio is equal to the ideal duty ratio. For the synchronous rectifier converter, the effect of the dead time T_d, which is used to prevent the two switches conducting at the same time, should be considered.

Above all, (23), (30), (33), and (37) together form the comprehensive compensation strategy. With this comprehensive compensation strategy, the current estimation becomes more accurate, and the two main issues for SPCC of a boost converter have been solved in theory.

V. EXPERIMENT AND RESULTS

The above sections finished the theoretical derivation and proof for the proposed algorithm. A real-time boost converter system is constructed to implement the algorithm. Here, the experimental settings, which include the boost converter design specifications and the hardware platform, are first introduced, and then, the test results are presented and analyzed.

A. Experimental Settings

The boost converter design specifications are shown in Table II.

The system hardware consists of control and power sections. The core of the control section is a Texas Instruments digital signal processor (DSP) TMS320F2812. The control algorithm and all other software features are implemented through this DSP. The power section includes the main power stage and signal sampling circuits. The switching device of the power stage is an Infineon BSZ110N06NS3 MOSFET, the output capacitor is Panasonic EEHZC1E101XP, and the diode is Liteon SB350. The specifications for these are shown in Table III. After the level converting circuit, the input and output voltages are sampled by a four-channel 12-bit AD converter chip (AD7934-6).

TABLE III
SPECIFICATIONS OF HARDWARE PLATFORM

Inductance of the power inductor	*28μH*
Inductor winding resistance	*50mΩ*
Capacitance of the output capacitor	*100μF*
ESR value of the output capacitor	*30mΩ*
MOSFET threshold voltage	*3.5V*
MOSFET R_{DS}	*11mΩ*
MOSFET turn on delay time	*10ns*
MOSFET turn off delay time	*14ns*
Diode forward Voltage	*0.7V*
Diode forward resistance	*100 mΩ*

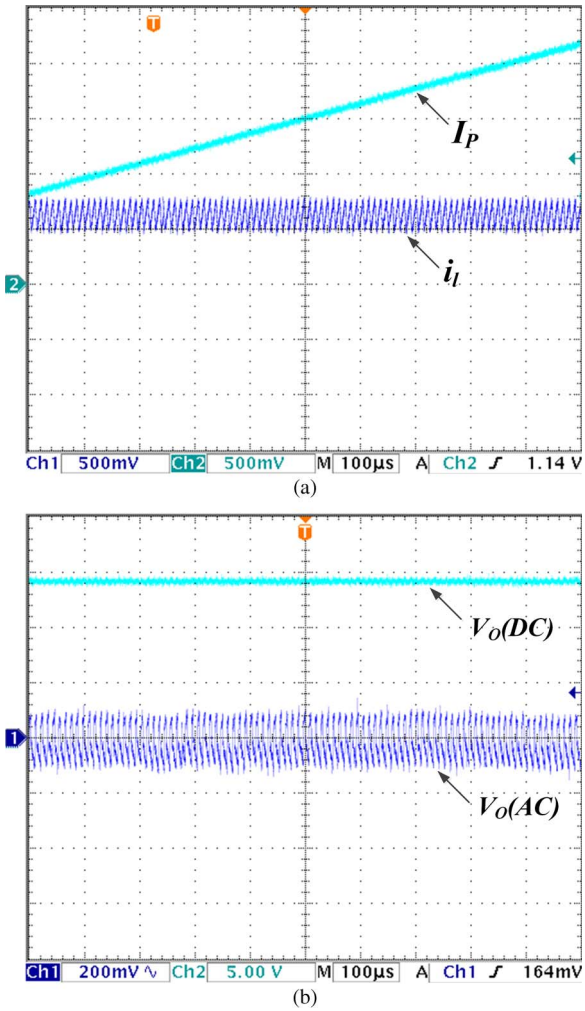


Fig. 10. (a) Estimated and actual current waveforms under basic current observer. (b) Output voltage waveform under basic current observer.

I_P was output in synchronization with the 12-bit DA chip (TLV5616). The actual inductor current i_L was measured using a Rogowski current probe (PEM CWT015).

B. Experimental Results and Analysis

1) Experiment by Using Basic Current Observer: Fig. 10(a). shows the waveforms of the estimated peak current and the measured inductor current. Channel 1 is i_l, whereas channel 2 is the waveform of I_P. The resolution of the Rogowski current probe is 200 mv/A. For easy comparison, the

resolution of the DA output was also set to 200 mv/A. All the following experimental results use the same resolution settings.

As shown in Fig. 10(a), the current observer does not converge but has a linear upward trend, whereas the actual inductor peak current is 3.69 A. Fig. 10(b) includes both the dc and ac components of the output voltage. As can be seen from the waveforms, the average value of the output voltage is 14.43 V. The steady-state error is 0.57 V, i.e., 3.8% compared with the reference voltage.

The experimental results can verify the analysis of ΔV_O in Section III. The voltage control loop PI controller cannot guarantee the elimination of ΔV_O. Because there is no compensation on output voltage sampling and component parasitic parameters, the output voltage is lower than the reference, and the steady-state error is negative. The negative voltage error caused the current reference to continuously increase; hence, the current estimation also increased in a linear upward nonconverging trend.

In the following experiment, the output voltage sampling compensation strategy is implemented both in current and voltage control loops.

2) Experiment With Output Voltage Sampling Compensation: Fig. 11(a) shows the waveforms of i_l and I_P after output voltage sampling compensation. Although the current observer output eventually converges to 7.53 A, the measured inductor peak current is 3.85 A. The voltage output waveforms are shown in Fig. 11(b); the steady-state error of the output voltage has been eliminated. The output voltage is approximately equal to the reference value of 15 V.

Compared with the experimental results of the basic current observer, ΔV_O can be eliminated, and the current observer can eventually converge. However, the observer estimated inductor peak current is nearly twice of the actual peak current.

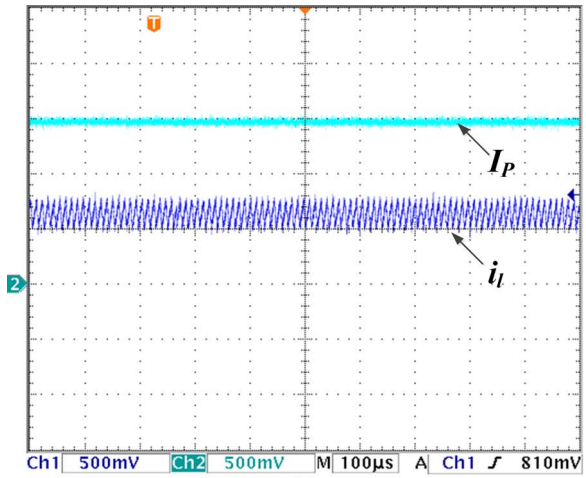
According to the previous analysis, if these parasitic and nonlinear factors are not involved in system modeling, the current estimation accuracy will be affected. After comprehensive compensation for all the factors, the results are as follows.

3) Experiment After Comprehensive Compensation: Fig. 12 presents waveforms of i_l and I_P after implementing the comprehensive compensation strategy. Compared with Fig. 9(a), the steady-state value of the current observer output changes from 7.5 to 4.03 A. The actual inductor peak current is 3.85 A. The estimated results are quite close to the actual value with only a 4.7% difference. The output voltage is almost 15 V without the steady-state error.

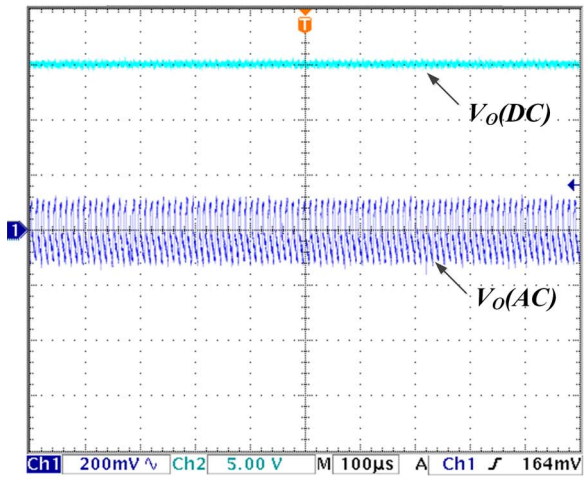
As shown in Fig. 12, after the compensation of output voltage sampling, parasitic parameters, and nonlinear factors, the current observer output can satisfy the actual application requirements.

4) Experiment For System Robustness Verification: In order to verify the robustness of the proposed algorithm, the experiments were carried out subject to load and line voltage disturbance conditions. In addition, for performance comparison, the conventional voltage-control-mode-based system subject to the same disturbance conditions was also tested.

Fig. 13(a) and (b) shows the current and voltage waveforms of the proposed algorithm when the load changes from 15 to 10 Ω (33% increase). As Fig. 13(a) shows, the estimated peak inductor current changes from 4.03 to 5.82 A within 180 μs. The estimated current and the measured inductor peak current synchronized error is less than 5%. As shown in Fig. 13(b), when the load increases, the output voltage decreases to



(a)



(b)

Fig. 11. (a) Estimated and actual current waveforms after output voltage sampling compensation. (b) Output voltage waveforms after output voltage sampling compensation.

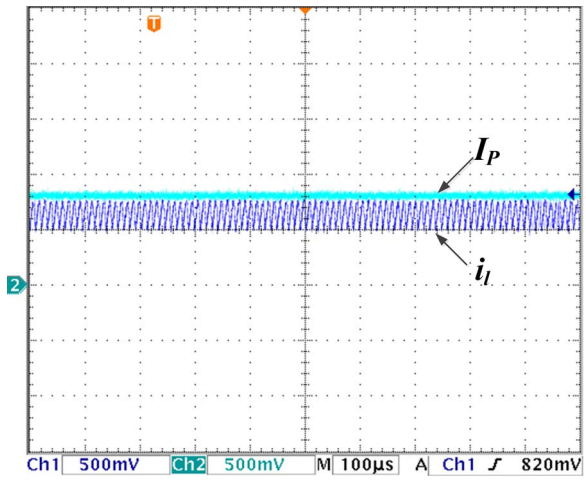


Fig. 12. Estimated and actual current waveforms after comprehensive compensation.

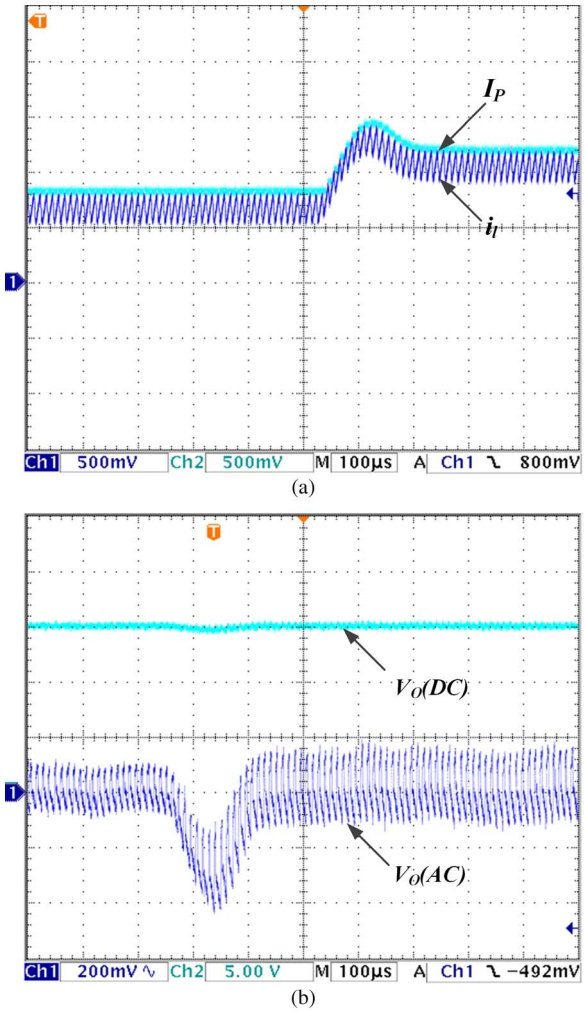


Fig. 13. (a) Current transient response due to load changes from 15 to 10 Ω with the proposed algorithm. (b) Output voltage transient response due to load changes from 15 to 10 Ω with the proposed algorithm.

14.61 V for a short time. After 180 μs, the output voltage restabilizes at 15 V.

With conventional voltage control mode, when the load changes from 15 to 10 Ω, the output voltage waveform is shown in Fig. 14. It drops to 14.64 V and then returns to the steady state, the total restabilizing process takes 400 μs. Compared with the proposed algorithm, the voltage drops are at the same level, but its response time is 122% longer. It means that the proposed algorithm has much better load regulation performance under load disturbance condition.

When the line voltage changes from 5 to 6 V, for the proposed algorithm, the current and voltage waveforms are shown in Fig. 15(a) and (b), respectively. As shown in Fig. 15(a), the estimated peak inductor current changes from 4.03 to 3.47 A within 200 μs. The synchronized error between the estimated and measured inductor peak current is less than 5%. In addition, the output voltage in Fig. 15(b) rises to 15.15 V and then returns to steady state in 200 μs. The voltage overshoot is only 0.15 V.

With the conventional voltage control mode, when the line disturbance happens (changing from 5 to 6 V), its output voltage waveform is shown in Fig. 16, the output voltage rises to 15.39 V, and the restabilizing process takes 500 μs. The

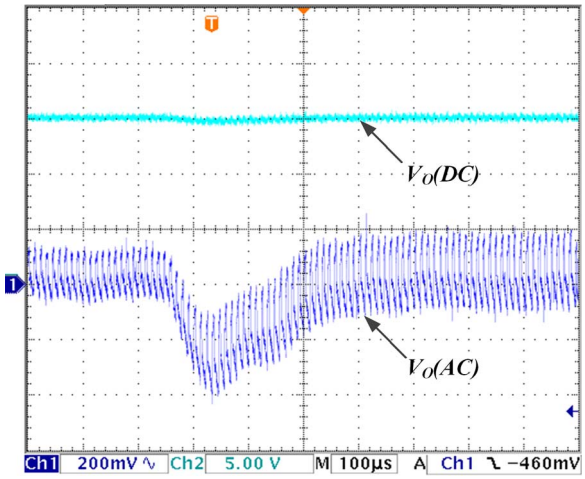


Fig. 14. Output voltage transient response due to load changes from 15 to 10 Ω with voltage control mode.

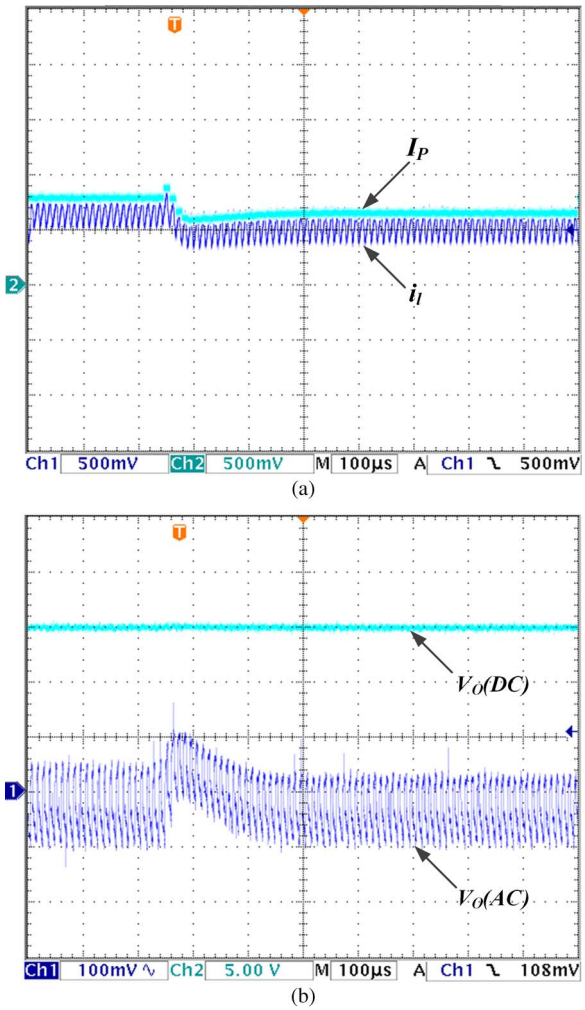


Fig. 15. (a) Current transient response due to line voltage changes from 5 to 6 V with the proposed algorithm. (b) Output voltage transient response due to line voltage changes from 5 to 6 V with the proposed algorithm.

response speed is 150% lower, and voltage overshoot is 160% more than the proposed algorithm.

As the experimental results show, even the system is subject to sudden load and line voltage disturbances, with the proposed

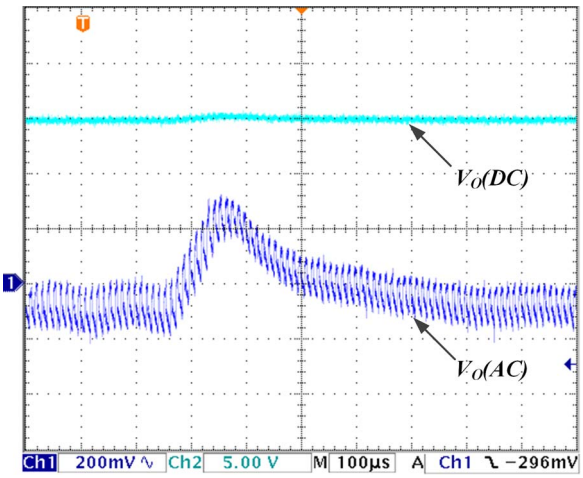


Fig. 16. Output voltage transient response due to line voltage changes from 5 to 6 V with voltage control mode.

algorithm, it will still be able to quickly respond and track to a new steady state. The difference between the estimated value and the actual value of the peak current is always less than 5%, the output voltage steady-state errors are almost zero, and the system has strong robustness. In addition, compared with conventional voltage control mode, the proposed algorithm has much better transient performance in both load and line voltage disturbance conditions.

VI. Conclusion

The basic cause of the output voltage steady-state error in a sensorless current-controlled boost converter has been proved through theoretical derivations. On this basis, the compensation strategy for output voltage sampling in both current loop and voltage loop has been proposed. In addition, the system modeling error caused by the parasitic parameters and nonlinear factors has been also compensated. The system ultimately achieves high-precision sensorless predictive peak current control without the voltage steady-state error with the comprehensive compensation strategy. Experimental results show that the control algorithm proposed in this paper is accurate and effective and has good potential for both theoretical and practical applications.

Appendix

V_A can be deduced from the sampled voltage $V_{\rm SAMPLE}$, the process can be divided into five steps as follows (see Fig. 17).

1) The valley value of output voltage $V_{\rm LOW}$: During the DT period, the output capacitor discharges with almost constant speed, and the discharging current is $I_{\rm AV}(1-D)$. Therefore, the output voltage decreases with a constant slope, and the output voltage valley value is

$$V_{\rm LOW} = V_{\rm SAMPLE} - \frac{I_{\rm AV}(1-D)DT}{C} = V_{\rm SAMPLE} - V_{\rm PP}. \tag{A1}$$

2) At the switching-off point, the starting voltage, which is on the second-order curve, after the voltage jumping is $V_{\rm START}$.

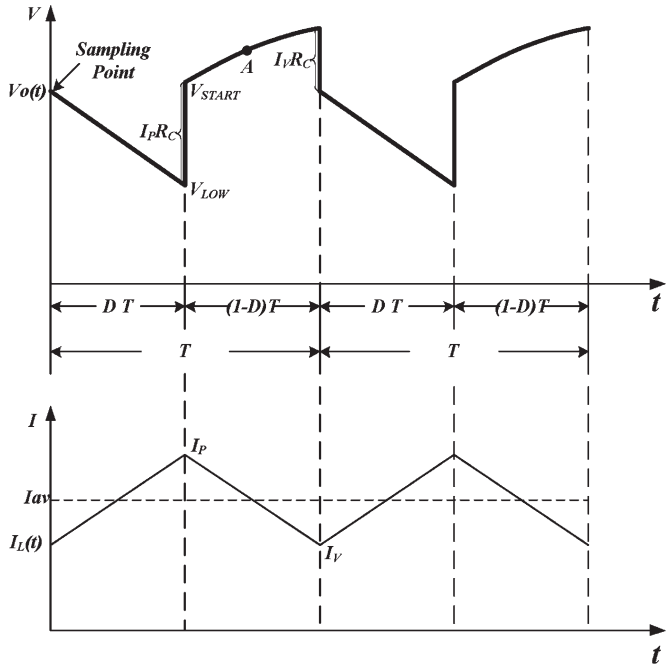


Fig. 17. Waveforms of output voltage and inductor current.

When the switch is on, the capacitor discharging current is $I_{\rm AV}(1-D)$. After switching off, inductor current $I_L(t)$ charges the capacitor and supplies the load current at the same time. Hence, the capacitor charging current is $I_L(t) - I_{\rm AV}(1-D)$. At the switching-off point, the inductor current is at its peak value I_P. Hence, $V_{\rm START}$ is

$$V_{\rm START} = V_{\rm SAMPLE} - V_{\rm PP} + I_P R_C. \tag{A2}$$

3) In the $(1-D)T$ period, the capacitor charging current is $I_{\rm CHARGE}(t)$.

After switching off, the inductor current is

$$I_L(t) = I_P - M_2 t. \tag{A3}$$

The charging current of the capacitor can be obtained from the inductor current minus the load current, i.e.,

$$I_{\rm CHARGE}(t) = I_L(t) - I_{\rm AV}(1-D) = I_P - M_2 t - I_{\rm AV}(1-D). \tag{A4}$$

4) The output voltage function during the $(1-D)T$ period.

To calculate the output voltage during the $(1-D)T$ period, in addition to the capacitor charging current, the effect of ESR should be considered as well. The capacitor charging current decreases under the M_2 slope; hence, the voltage across ESR also decreases, and its value is $[I_P - I_L(t)]R_C$. Finally, the output voltage function is

$$\begin{aligned} V_O(t) &= V_{\rm START} + \frac{\int_0^t I_{\rm CHARGE}(t)dt}{C} - [I_P - I_L(t)]\,R_C \\ &= V_{\rm SAMPLE} - \frac{I_{\rm AV}(1-D)DT}{C} \\ &\quad + I_L(t)R_C + \frac{I_P - I_{\rm AV}(1-D)}{C}t - \frac{M_2 t^2}{2C}. \end{aligned} \tag{A5}$$

5) The average output voltage V_A during $(1-D)T$. Thus

$$V_A = \frac{\int_0^{(1-D)T} V_O(t)dt}{(1-D)T}$$
$$= V_S - V_{\rm PP} + I_{\rm AV}R_C + \frac{I_P - I_{\rm AV}(1-D)}{2C}(1-D)T - \frac{M_2(1-D)^2T^2}{6C}. \quad \text{(A6)}$$

Comparing (A6) with (18), the difference between them should be established. When the system is in steady state, the relationship between the peak current and the average current is

$$I_P = I_{\rm AV} + \frac{M_2(1-D)T}{2}. \quad \text{(A7)}$$

Using (A7) in (A6), the equation will be

$$V_A = V_S - \frac{V_{\rm PP}}{2} + I_{\rm AV}R_C + \frac{M_2(1-D)^2T^2}{12C}. \quad \text{(A8)}$$

Comparing (A8) with (18), the difference between them is

$$\varepsilon = \frac{M_2(1-D)^2T^2}{12C}. \quad \text{(A9)}$$

$\Delta I = M_2(1-D)T$ is the maximum inductor current difference in one control cycle. Thus

$$\varepsilon = \frac{M_2(1-D)^2T^2}{12C} = \frac{\Delta I_P}{12D}\frac{D(1-D)T}{C}. \quad \text{(A10)}$$

Normally, the inductor current ripple ratio is 0.4, and $r = 0.4 = \Delta I_P/I_{\rm AV}$, $\Delta I_P \approx 2/5 I_{\rm AV}$, substituting them in (A10). Thus

$$\varepsilon = \frac{\Delta I_P}{12D}\frac{D(I-D)T}{C} = \frac{I_{\rm AV}}{30D}\frac{D(1-D)T}{C} = \frac{V_{\rm PP}}{30D}. \quad \text{(A11)}$$

As can be seen from (A11), the difference between (A8) and (14) is very small. Hence, using (A8) instead of (14) is reasonable. The complexity of calculation can be greatly reduced.

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