A Fiber-Optic-Less 50-MHz Single Transformer Isolated Gate Driver With Fault Feedback for 10-kV SiC MOSFETs

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***Abstract*—This article presents a novel fiber-optic-less 50-MHz single transformer isolated gate driver (GD) for medium voltage (MV) SiC MOSFETs. A unique edge-interval-OFF modulation scheme is proposed to allow signal and power simultaneously transmitted through a single transformer with minimal power switches and voltage sources. The proposed GD can also transmit the fault signal from the GD secondary side to primary side, eliminating the requirement for fiber-optic (FO) communication for fault feedback. The proposed GD offers a low propagation delay and can respond to short pulsewidths, as well as supports an ultra-wide duty-cycle range including 0% and 100% duty-cycle operation. Furthermore, it utilizes solid dielectrics to achieve a compact footprint of 61 mm $\times$ 24 mm $\times$ 30 mm and meet MV insulation requirements with a partial discharge (PD) inception voltage $>$ 13.5 kV_{RMS} under 60-Hz ac voltage and a PD-free operation under 100-kHz, 5-kV PWM voltage with a *dv/dt* of 100 V/ns. The proposed GD achieves an ultra-low coupling capacitance of 1.9 pF and a common-mode transient immunity (CMTI) $>$ 100 V/ns, making it preferable to drive MV SiC MOSFETs with high *dv/dt*. The proposed GD eliminates the need for both FOs and bulky GD power supplies, resulting in a more than 10-fold reduction in size compared to conventional 10-kV isolated GDs and has the potential to be integrated into MV SiC device packages. Experimental results on 10-kV SiC MOSFETs validate the effectiveness of the proposed GD.**

***Index Terms*—Common-mode transient immunity (CMTI), fiber-optic-less (FOL), isolated gate driver (GD), medium voltage (MV) SiC MOSFET , partial discharge (PD), signal-power integrated transmission.**

I. Introduction

RECENT advancements in medium voltage (MV) SiC devices offer substantial benefits in MV power conversion, including increased power density, enhanced efficiency, and simplified system complexity [1]. Isolated gate drivers (GDs) are critical for MV SiC devices, as they provide insulation strength and common mode transient immunity (CMTI) required for high voltage (HV) and high *dv/dt* applications [2], [3]. Conventional MV isolated GDs separate signal and power transmissions. PWM and fault signals are usually transmitted using fiber optics (FOs), while GD power is delivered by the isolated MV GD power supplies (GDPSs) that have a large form factor to maintain the sufficient insulation distance and low coupling capacitance (C_{cp}) [4], [5], [6]. As a result of using FOs and bulky MV-isolated GDPSs, conventional 10-kV isolated GDs have a large overall footprint and increase system cost. Moreover, FO transceivers are sensitive to high temperatures and thus hard to integrate into device package.

Pulse-transformer GDs have potential to achieve a smaller footprint and lower cost by transferring the signal and power simultaneously through the transformer [7], [8], [9], [10], [11]. However, most commonly used pulse-transformer GDs operate at PWM frequency, resulting in a high voltage-second and requiring a large magnetic core. They also have a narrow duty-cycle range and cannot accommodate fast duty-cycle changes [7], [8]. To obtain a low voltage-second, edge-triggered pulse-transformer GDs utilize bipolar narrow pulses instead of complete PWM voltage pulses, which allows for a smaller magnetic core, a wide duty-cycle range, and fast duty-cycle changes [9], [10]. However, in the case of constant ON or OFF PWM input, all the pulse-transformer GDs in [7], [8], [9], and [10] fail to transfer GD power, causing shutdown of GD secondary circuits, especially the protection circuit. This is undesirable for SiC device applications that require uninterrupted protection. To address this issue, a 1-MHz bi-level modulated pulse-transformer GD is proposed by alternating between full-bridge and half-bridge modes [11]. Nonetheless, the hard-switching operation limits the modulation frequency, resulting in a severe propagation delay and duty-cycle distortion.

The pulse-transformer GDs in [7], [8], [9], [10], and [11] are designed for low voltage (LV) applications, leaving a gap in fulfilling the insulation requirement for MV SiC applications. Importantly, MV insulation schemes affect the overall size of pulse-transformer GDs. The insulation schemes developed for MV-isolated GDPSs can provide valuable references in this aspect. Air-insulated GDPSs utilize the air gap as an isolation

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barrier, but the low dielectric strength of air (<3 kV/mm) requires a large clearance distance [12], [13]. PCB-insulated GDPSs employ PCB substrates as isolation barriers, allowing for a smaller isolation barrier thickness due to the higher dielectric strength (40–50 kV/mm) [14], [15]. However, a minimum creepage distance should be maintained to prevent surface discharge and/or flashover. This can be further addressed by applying silicone or epoxy encapsulation [16], [17]. The insulation schemes for MV-isolated GDPSs in [12], [13], [14], [15], [16], and [17] have been validated under hi-pot dc tests, partial discharge (PD) or breakdown tests at 60-Hz ac voltage. However, their performance under PWM voltage excitation is still not well characterized and requires further investigation.

Recently, the first pulse-transformer GD for 10-kV SiC MOSFETs to transfer both PWM signal and GD power is proposed in [18]. By implementing a soft-switching topology and on-off-key modulation scheme for two identical transformers operating complimentarily, 20 MHz with a low propagation delay of 50 ns is achieved. However, it has not implemented the fault feedback signal transmission from the GD secondary side to the primary side using the same transformer. In addition, dual transformers are beneficial for full duty-cycle range operation, but C_{cp} is doubled compared to that of a single transformer.

This article presents a novel pulse-transformer GD for 10-kV SiC MOSFETs. First, an edge-interval-OFF (EIO) modulation scheme is proposed which requires only a single transformer to operate over an ultra-wide duty-cycle range, including 0% and 100% duty-cycle operation. In addition, the operation frequency of the transformer is raised to 50 MHz, which reduces transformer winding geometry and enables an ultra-low C_{cp} of 1.9 pF. This new modulation scheme eliminates extra switches and/or voltage sources required for magnitude modulation. Second, unlike existing pulse-transformer GDs, the proposed GD transmits fault feedback signal from GD secondary side to primary side through the same transformer, eliminating the need of FOs for both PWM and fault signal transmission. Third, solid dielectrics are utilized in the proposed GD to achieve a compact size while meeting insulation requirements with a PD inception voltage (PDIV) of 13.5 $\mathrm{kV_{RMS}}$ under 60-Hz ac voltage excitation and PD-free under 100-kHz, 5-kV PWM voltage with a *dv/dt* of 100 V/ns. The proposed GD has passed both static and dynamic CMTI tests, indicating a CMTI >100 V/ns.

The rest of this article is organized as follows. Section II presents the operation principle and circuit schematic of the proposed GD. The timing characteristics of the proposed GD are analyzed in Section III, in terms of the propagation delay time, minimum pulse width limitation, and duty-cycle range. The insulation scheme and PD characterization of the proposed GD are discussed in Section IV. Section V provides experimental verifications, and Section VI concludes this article.

II. Operation Principle and Circuit Schematic of Proposed FOL-Isolated GD

The operation principle of the proposed GD is illustrated in Fig. 1, consisting of the function block diagram in Fig. 1(a) and the modulation scheme in Fig. 1(b). An isolated dc–dc converter

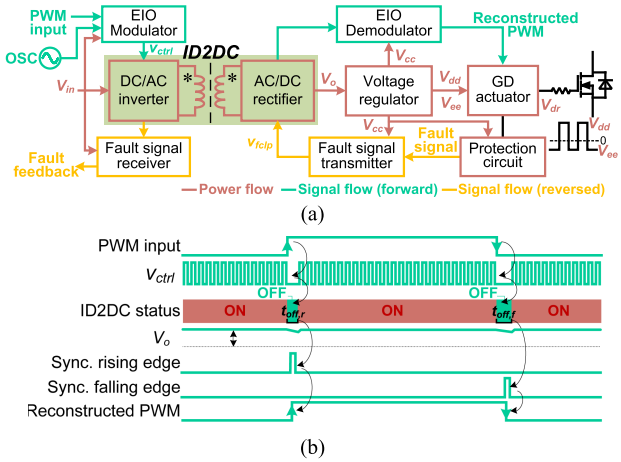

Fig. 1. Proposed fiber-optic-less (FOL)-isolated GD. (a) Block diagram. (b) Proposed EIO modulation/demodulation scheme.

(ID2DC) performs the dual function of delivering GD power and modulating the transmission of PWM and fault feedback signals. The PWM input is modulated with an oscillator (OSC), and the resulting control signal v_{ctrl} regulates ON/OFF status of the ID2DC's inverter stage with the proposed EIO modulation scheme. As shown in Fig. 1(b), the ID2DC remains ON except during short intervals ($t_{\mathrm{off},r}$ and $t_{\mathrm{off},f}$) at the rising and falling edges of PWM input. The ID2DC's ON/OFF status is detected and demodulated at its rectifier stage to reconstruct the PWM signal. To identify the rising and falling edges of the PWM signal, OFF intervals are intentionally set to be unequal, i.e., $t_{\mathrm{off},r} \neq t_{\mathrm{off},f}$. Since OFF intervals are short ($\leq$100 ns), the ripple of ID2DC output voltage, V_o, is negligible and GD secondary circuits are continuously power-ON without interruption. Unlike existing magnitude-based modulation, the proposed EIO modulation does not require extra switches or voltage sources. Once the GD secondary-side protection circuit (such as DESAT and UVLO) is activated, the fault signal transmitter can clamp the ID2DC's rectifier stage, after which a fault feedback signal is generated by detecting the ID2DC's inverter stage. At the GD secondary side, dc–dc voltage regulators are used to supply positive/negative rail voltages, V_{dd}/V_{ee}, for the GD actuator, as well as V_{cc} for the PWM signal demodulator, fault signal transmitter, and protection circuits. With the reconstructed PWM signal, the GD actuator outputs a driving voltage v_{dr} to drive the MV SiC device.

To ensure a low propagation delay time, high duty-cycle resolution, and wide duty-cycle range as well as a compact footprint, a 50-MHz class-E resonant flyback converter (RFC) with coreless transformer is selected to implement ID2DC due to its soft-switching feature and minimum component count.

The circuit implementation of the proposed EIO modulator/demodulator and ID2DC is illustrated in detail in Fig. 2(a). The PWM input and OSC signal are used as data and clock inputs of a D flip-flop to generate a complementary pair of signals, *pwm* and *npwm*. Both *pwm* and *npwm* are processed by one-shots and then inverted buffers to generate *pulse,r* and *pulse,f*, respectively, which are combined by an AND gate to

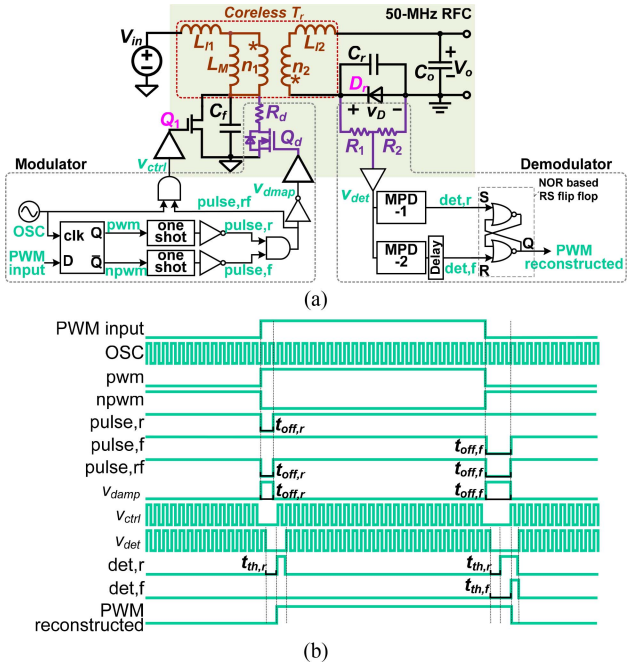

Fig. 2. Proposed EIO-based modulator and demodulator. (a) Circuit schematic. (b) Key waveforms.

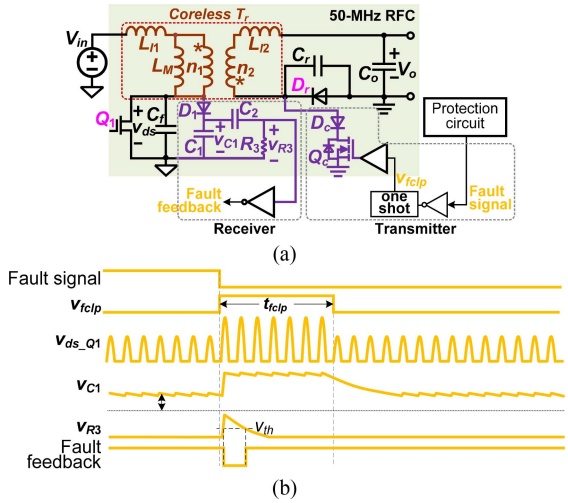

Fig. 3. Proposed fault signal transmitter and receiver. (a) Circuit schematic. (b) Operational waveforms.

produce *pulse,rf*. The OSC signal and *pulse,rf* are combined by an AND gate to generate $v_{\rm ctrl}$ that controls the gate signal of the main switch Q_1 of class-E RFC. The voltage across diode D_r, v_D, is sensed by a resistive divider comprised of R_1 and R_2. The scaled voltage is then buffered as $v_{\rm det}$, which exhibits pulse voltage profiles when the class-E RFC is ON. During OFF intervals of class-E RFC, v_D will decay below the buffer's low-level threshold and result in missing pulses of $v_{\rm det}$. $v_{\rm det}$ is processed by two missing pulse detectors (MPDs), which generate rising and falling edge detection signals (*det,r* and *det,f*) when the pulses in $v_{\rm det}$ are absent for a specified time interval. Both *det,r* and *det,f* are sent into a NOR-gatebased RS flip–flop, as set and reset signals, respectively, to reconstruct PWM signal. To accelerate the decay of v_D during OFF intervals of class-E RFC, a damping branch consisting of resistor R_d and switch Q_d is activated by a control signal complementary to *pulse,rf*, by which R_d is paralleled with Q_1 to hasten the damping of resonant tank and v_D decays rapidly. Fig. 2(b) presents key waveforms of the proposed modulator and demodulator. The one-shot pulse width for *pulse,r* and *pulse,f* is denoted as $t_{{\rm off},r}$ and $t_{{\rm off},f}$, respectively. $t_{{\rm off},f}$ is set longer than $t_{{\rm off},r}$ to distinguish the rising and falling edges of the PWM signal. When the interval of missing pulses in $v_{\rm det}$ exceeds threshold values, $t_{{\rm th},r}$ or $t_{{\rm th},f}$, MPD-1 or -2 is activated to set *det,r* or *det,f* to high. At the rising edge of the PWM input, only *det,r* is set to high to reconstruct the rising edge of the PWM signal. At the falling edge of PWM input, *det,r* and det,*f* are successively set to high, which reconstructs the falling edge of the PWM signal due to the higher priority of reset signal in NOR-gate-based RS flip-flop. To ensure the falling edge of *det,f* lag that of *det,r*, a delay block with several nanoseconds is inserted after MPD-2.

To transmit the fault status of GD secondary side to the primary side, a fault signal transmitter is used to intentionally short-circuit the rectifier stage of RFC for a short interval (i.e., t_{fclp}). A fault signal receiver, therefore, can generate the fault feedback signal by detecting the voltage variation of the inverter stage of RFC. Fig. 3 presents the circuit schematic and operational waveforms of the proposed fault signal transmitter and receiver, which are simplified and represented by orange boxes in Fig. 1(a). The fault signal (activated from GD secondary-side protection circuits) is processed by an inverted buffer and one-shot to generate the control signal v_{fclp} for the clamping switch Q_c, which is antiseries with a clamping diode D_c to provide a bidirectional blocking capability. When Q_c is ON during t_{fclp}, V_o is reflected to the transformer primary winding, the peak value of the drain-source voltage of Q_1, $v_{{\rm ds}\_Q1}$, therefore increases and can be detected using an envelope detector formed by D_1 and C_1. Once the peak value of $v_{{\rm ds}\_Q1}$ increases during t_{fclp}, the envelope voltage v_{C1} has a step-rising edge and it is extracted by an RC differential circuit comprised of C_2 and R_3. The extracted step rising edge signal is then buffered as a negative pulse on the fault feedback signal, which can provide the fault status to MCU and/or other control logics.

III. Propagation Delay Time, Minimum Pulse Width, and PWM Duty-Cycle Range of Proposed GD

Timing diagrams of proposed modulation and demodulation processes are essential for analyzing the propagation delay time, minimum pulse width, and PWM duty-cycle range, which are derived and demonstrated in Fig. 4. The corresponding breakdown of subintervals in modulation and demodulation processes is listed in Table I.

As shown in Fig. 4, the negative pulse-width of pulse,*r* and pulse,*f* (i.e., $t_{{\rm off},r}$ and $t_{{\rm off},f}$) result in missing pulses in $v_{\rm ctrl}$ and $v_{\rm det}$. The numbers of missing pulses in $v_{\rm ctrl}$ at PWM rising and falling edges are denoted as $N_{m,r}$ and $N_{m,f}$, respectively. Determined by the response speed of v_D after OFF intervals,

TABLE I
BREAKDOWN OF TIME INTERVALS IN THE PROPOSED MODULATION AND DEMODULATION PROCESSES

Time interval		Source	Estimated length
t_1–t_x	time delay from OSC to v_{ctrl}	AND gate: SN74LVC1G08	2.5 ns
t_1–t_2	time delay from PWM input to *pwm* or *npwm*	D flip-flop: SN74LVC2G74	2.8 ns
t_x–t_3	time delay from v_{ctrl} to v_{det}	Determined by RFC and measured in experiments	~9 ns
t_3–t_4	overlapped interval of v_{ctrl} and v_{det}	(t_4-t_3)= ½ T_{osc} - (t_3-t_2)	1 ns
t_2–t_5	time delay from *pwm* to *pulse,r* (or from *npwm* to *pulse,f*)	One-shot: LTC6993-2, inverted buffer: SN74LVC1G02	12 ns + 2.5 ns
t_5–t_6	time delay from *pulse,r* (or *pulse,f*) to *pulse,rf*	AND gate: SN74LVC1G08	2.5 ns
t_7–t_8	time delay from *det,r* (or *det,f*) to reconstructed PWM	RS flip-flop: SN74LVC2G02	2.5 ns ×2
t_{delay}	delay time of "*delay* block" after MPD-2	Set by RC filter	~5 ns

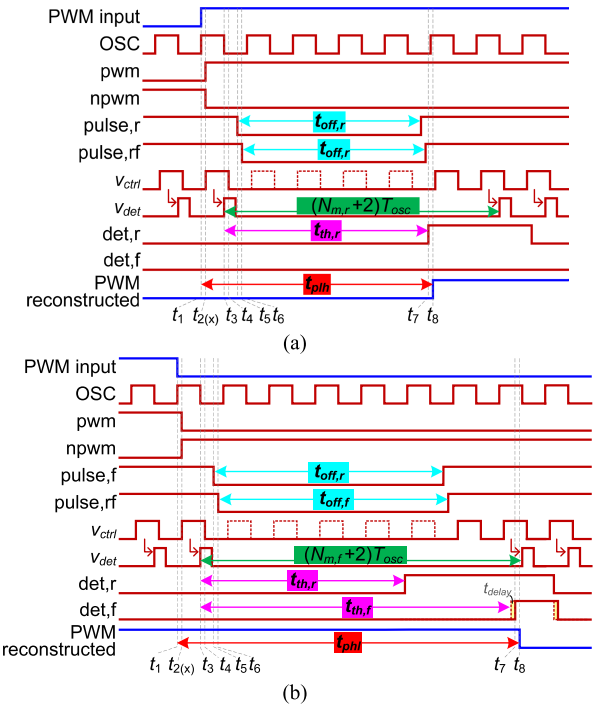

Fig. 4. Timing diagrams of proposed modulation and demodulation processes during (a) PWM rising edge and (b) PWM falling edge.

v_{det} has $(N_{m,r}+1)$ and $(N_{m,f}+1)$ missing pulses at PWM rising and falling edges, respectively. To maintain desired positive pulsewidths for v_{ctrl} (i.e., half of the OSC cycle period) without any slivers, it is essential to meet constraints (1)–(3)

$$(t_x - t_1) + \frac{1}{2}T_{osc} < (t_6 - t_1) < (t_x - t_1) + T_{osc} \quad (1)$$

$$(t_x - t_1) + \left(N_{m,r} + {}^1\!/_2\right) T_{osc} < (t_6 - t_1) + t_{off,r} < (t_x - t_1) + (N_{m,r} + 1)\, T_{osc} \quad (2)$$

$$(t_x - t_1) + \left(N_{m,f} + {}^1\!/_2\right) T_{osc} < (t_6 - t_1) + t_{off,f} < (t_x - t_1) + (N_{m,f} + 1)\, T_{osc} \quad (3)$$

where T_{osc} is the OSC cycle period (i.e., 1/50 MHz = 20 ns). $(t_6$–$t_1)$ is the propagation delay time from the rising edge of OSC to the falling edge of pulse,*rf*, and it is the sum of propagation delay times of D flip–flop $(t_2$–$t_1)$, one-shot and inverted buffer $(t_5$–$t_2)$, and AND gate $(t_6$–$t_5)$. $(t_x$–$t_1)$ is the propagation delay time from the rising edge of OSC to the rising edge of v_{ctrl}. According to Table I, $(t_6$–$t_1) = 19.8$ ns, $(t_x$–$t_1) = 2.5$ ns. In this article, $N_{m,r}$ is set as 4 and $N_{m,f}$ is set as 5. The values of $t_{off,r}$ and $t_{off,f}$ are specified as 80 and 100 ns, respectively.

In addition, threshold values, $t_{th,r}$ and $t_{th,f}$, of MPDs must satisfy (4) to properly activate det,*r* and det,*f*

$$\begin{cases} t_{th,r} < (N_{m,r} + 2)\, T_{osc} \\ t_{th,r} < t_{th,f} < (N_{m,f} + 2)\, T_{osc} \end{cases} \quad (4)$$

where $t_{th,r}$ is set as 90 ns and $t_{th,f}$ is set as 130 ns in this article.

Equations (1)–(4) are design guidelines derived from the timing diagrams to generate the correct reconstructed PWM signal. The timing characteristics of the proposed GD, including the propagation delay time, minimum pulse width, and PWM duty-cycle range, are analyzed based on the timing diagram of Fig. 4 and presented as follows.

A. Propagation Delay Time

As shown in Fig. 4, when the OSC and PWM input are synchronized, the propagation delay time from low to high t_{pdlh} and that from high to low t_{pdhl} are expressed as

$$\begin{cases} t_{pdlh} = (t_x - t_1) + (t_3 - t_x) + t_{th,r} \\ t_{pdhl} = (t_x - t_1) + (t_3 - t_x) + t_{th,f} + t_{delay} \end{cases} \quad (5)$$

where $(t_3$–$t_x)$ is the propagation delay time from the rising edge of v_{ctrl} to the rising edge of v_{det}, and t_{delay} is the delay time of the delay block after MPD-2.

According to (5) and Table I, t_{pdlh} = 101.5 ns and t_{pdhl} = 146.5 ns. The difference between t_{pdlh} and t_{pdhl} results in a pulse width distortion (PWD = $|t_{pdhl}$-$t_{pdlh}|$) for the reconstructed PWM signal. This PWD can be compensated by adding a rising-edge delay block after the RS flip-flop to delay the rising edge of the reconstructed PWM signal by PWD value. The propagation delay times and PWD of the proposed GD are comparable with commercially isolated GDICs. Note that when the OSC and PWM inputs are asynchronized, a propagation jitter < 20 ns may occur. In real applications, the effects of PWD and propagation jitter (only for asynchronized mode) should be considered for setting the dead time for a phase leg circuit.

B. Minimum Pulse Width Limitation

The minimum allowable positive and negative pulsewidths of PWM input, t_{pw,pos_min} and t_{pw,neg_min}, are determined by (6),

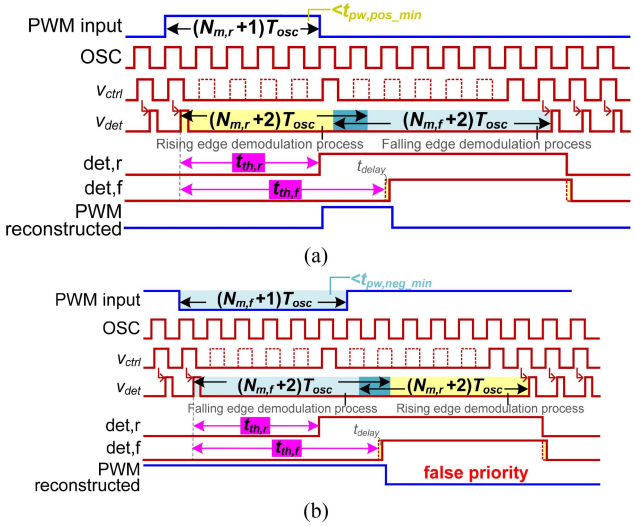

Fig. 5. Timing diagrams with (a) actual positive pulse width $<$ $t_{\mathrm{pw,pos\_min}}$ and (b) actual negative pulse width $<$ $t_{\mathrm{pw,neg\_min}}$.

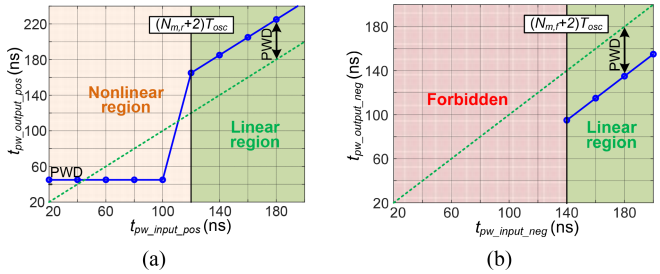

Fig. 6. (a) $t_{\mathrm{pw\_output\_pos}}$ versus $t_{\mathrm{pw\_input\_pos}}$. (b) $t_{\mathrm{pw\_output\_neg}}$ versus $t_{\mathrm{pw\_input\_neg}}$.

resulting in $t_{\mathrm{pw,pos\_min}} = 120$ ns and $t_{\mathrm{pw,neg\_min}} = 140$ ns

$$\begin{cases} t_{\mathrm{pw,pos\_min}} = (N_{m,r}+2)\,T_{\mathrm{osc}} \\ t_{\mathrm{pw,neg\_min}} = (N_{m,f}+2)\,T_{\mathrm{osc}} \end{cases}. \tag{6}$$

As shown in Fig. 5, when the actual positive/negative pulsewidths of PWM input are shorter than $t_{\mathrm{pw,pos\_min}}$/$t_{\mathrm{pw,neg\_min}}$, the overlap of rising and falling edge demodulation processes causes distortion or error in the reconstructed PWM output. In Fig. 5(a), when the actual positive pulse width is shorter than $t_{\mathrm{pw,pos\_min}}$, the pulse width of the reconstructed PWM signal is clamped to PWD. In Fig. 5(b), when the actual negative pulse width is shorter than $t_{\mathrm{pw,neg\_min}}$, the reconstructed PWM signal is set to low and remains in that state, causing a false output priority. Fig. 6 plots the relationship of pulsewidths of the reconstructed PWM signal ($t_{\mathrm{pw\_output\_pos}}$ and $t_{\mathrm{pw\_output\_neg}}$) and pulsewidths of PWM input ($t_{\mathrm{pw\_input\_pos}}$ and $t_{\mathrm{pw\_input\_neg}}$). When $t_{\mathrm{pw\_input\_pos}} > t_{\mathrm{pw,pos\_min}}$, $t_{\mathrm{pw\_output\_pos}}$ can track $t_{\mathrm{pw\_input\_pos}}$ linearly. When $t_{\mathrm{pw\_input\_neg}} > t_{\mathrm{pw,neg\_min}}$, $t_{\mathrm{pw\_output\_neg}}$ can track $t_{\mathrm{pw\_input\_neg}}$ linearly. It is important to note that the actual negative pulse width should be longer than $t_{\mathrm{pw,neg\_min}}$, which can be achieved with a little penalty on the control accuracy for MV converters.

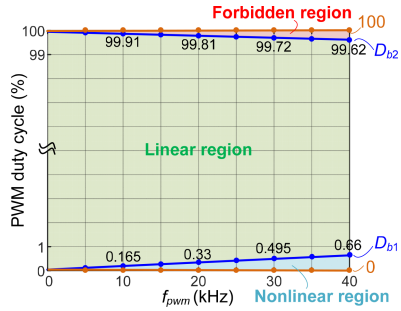

Fig. 7. Achieved PWM duty-cycle range with the varying f_{pwm}.

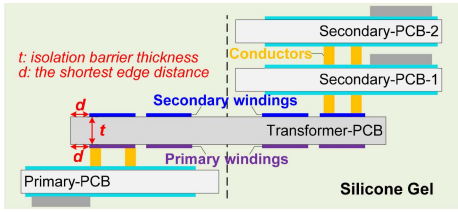

Fig. 8. Proposed insulation scheme using solid dielectrics.

C. PWM Duty-Cycle Range

Despite the minimum pulse width limitation, the proposed GD can operate reliably when PWM input remains constantly either high or low, representing a duty cycle of 100% or 0%, respectively. Therefore, the PWM duty-cycle range supported by proposed GD is $\{0\%\}\cup[D_{b1}, D_{b2}]\cup\{100\%\}$. D_{b1} and D_{b2} are the boundaries of linear PWM duty-cycle range, which are determined by $t_{\mathrm{pw,pos\_min}}$ and $t_{\mathrm{pw,neg\_min}}$ as (7) and (8)

$$D_{b1} = (t_{\mathrm{pw,pos\_min}} + \mathrm{PWD})\, f_{\mathrm{pwm}} \times 100\% \tag{7}$$

$$D_{b2} = (1 - (t_{\mathrm{pw,neg\_min}} - \mathrm{PWD})\, f_{\mathrm{pwm}}) \times 100\%. \tag{8}$$

Fig. 7 illustrates the achieved PWM duty-cycle range with the varying PWM frequency f_{pwm}. For example, the achieved PWM duty-cycle range is $\{0\%\}\cup[0.66\%, 99.62\%]\cup\{100\%\}$ at $f_{\mathrm{pwm}} = 40$ kHz, which is acceptable to control MV converters.

IV. Proposed Insulation Scheme and Its Validation

A. Proposed Solid-Dielectrics-Based Insulation Scheme

To meet MV insulation and maintain a compact footprint, a solid-dielectrics-based insulation scheme, shown in Fig. 8, is proposed. With the designed PCB stack structure, transformer-PCB dielectric serves as the isolation barrier of the proposed GD, and the entire GD circuit is potted in the silicone gel to prevent surface flashover and discharge. In this article, the transformer-PCB dielectric material is DiClad-880 with a dielectric strength of 45 kV/mm and relative permittivity (ε_r) of 2.2. The silicone gel adopted is SilGel 612 with a dielectric strength of 23 kV/mm and $\varepsilon_r = 2.8$. Compared to FR4 dielectric material ($\varepsilon_r = 4.4$–4.6), the use of DiClad-880 reduces C_{cp} of the proposed GD due to its lower ε_r. In addition, the ε_r of DiClad-880 is closer to that of SilGel 612, leading to lower electric-field stress [19].

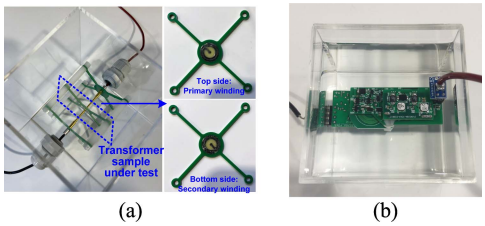

Fig. 9. DUT pictures. (a) Transformer sample #4. (b) GD circuit sample.

TABLE II
CONFIGURATION OF TRANSFORMER SAMPLES

Sample #	1	2	3	4
PCB dielectric	FR4	FR4	DiClad-880	DiClad-880
Gel potting?	No	Yes	No	Yes

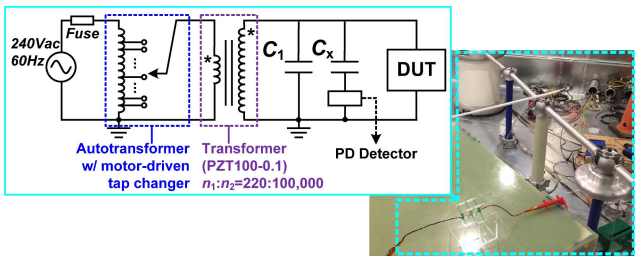

Fig. 10. HV test setup with 60-Hz ac voltage.

The high dielectric strength of these solid dielectrics enables a thinner isolation barrier thickness (denoted as t) and a smaller shortest edge distance (denoted as d) to achieve a compact GD footprint. In this article, the values of t and d are set to 1.6 and 2 mm, respectively.

This article also aims to quantitatively validate the proposed insulation scheme by characterizing its PD performance, which serves as an early indicator of insulation degradation and the onset of insulation failure. The PD characterization is conducted under both 60-Hz ac voltage and high frequency, high *dv/dt* PWM voltage excitations. In the PD tests, both the transformer itself and GD circuit are tested as devices under test (DUT), shown in Fig. 9(a) and (b), respectively. Four different transformer samples are built with the configurations in Table II, where transformer sample #1–#3 are for comparison purpose. The gel potting process is performed in a vacuum pump to remove air pockets and bubbles, by which their effect on the potential electric-field enhancements can be minimized.

B. PD Characterization Under 60-Hz AC Voltage

Fig. 10 shows the HV test setup for the PD test under 60-Hz ac voltage. The PDIV is obtained by increasing ac voltage through a motor-driven tap changer until PD reaches a threshold of 10 pC. The PD results of transformer sample #4 and GD circuit sample are presented in Fig. 11, with measured PDIVs of 14.37 kV_{RMS} and 13.57 kV_{RMS}, respectively. PDIVs of transformer samples #1–#3 are 2.5, 14.1, and 3.3 kV_{RMS}, respectively. Due

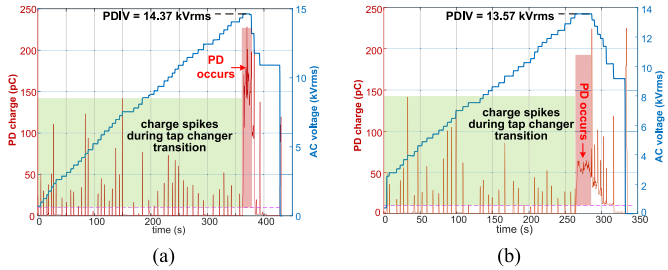

Fig. 11. PD results of (a) transformer sample #4 and (b) GD circuit sample under 60-Hz ac voltage.

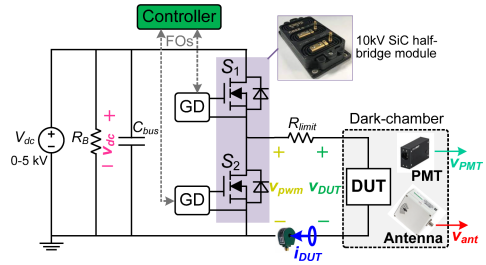

Fig. 12. PD test platform with PWM voltage excitation.

to the gel potting, the PDIV of sample #2 (#4) is higher than that of #1 (#3). Due to the ε_r of DiClad-880 being closer to that of silicone gel, the PDIV of sample #3 (#4) is slightly higher than that of sample #1 (#2). Please note that the tap changer in the HV test setup can induce charge spikes which will naturally disappear after each tap changer transition, making them easily distinguish from actual PD events.

C. PD Characterization Under PWM Voltage

A PD test platform with PWM voltage excitation is built as Fig. 12, where a PWM voltage generator supports continuous PWM voltage pulses at a frequency of 100 kHz, and duty cycle D of 50%. PWM voltage pulses have a *dv/dt* up to 100 V/ns, and the magnitude can be adjusted within 0–5 kV. A coordinated detection strategy is implemented using different PD detectors simultaneously, including photomultiplier tube (PMT), ultra-high-frequency antenna, and high-frequency current transformer. To mitigate the external light interference, DUT and PMT are enclosed in a dark chamber. The PD testing procedure in [20] is followed, and PDIV is defined as the plateau magnitude of the PWM voltage pulse when PD event is detected. PMT is effective in detecting PD when PD coincides with *dv/dt* transients, as its PD signal magnitude is higher than spikes caused by PWM switching interferences [20]. As shown in Fig. 13(a), the PDIV of transformer sample #1 is measured as 4.6 kV with a *dv/dt* exceeding 90 V/ns. Different PD events are identified during the PWM voltage plateau as well as within the falling and rising *dv/dt* transients. In contrast, no PD occurs for transformer samples #2–#4, even when the PWM voltage is increased to the maximum value of 5 kV with a *dv/dt* exceeding 100 V/ns, indicating a PDIV $>$ 5 kV. Fig. 13(b) presents the PD result of transformer sample #4 under 5-kV PWM voltage with

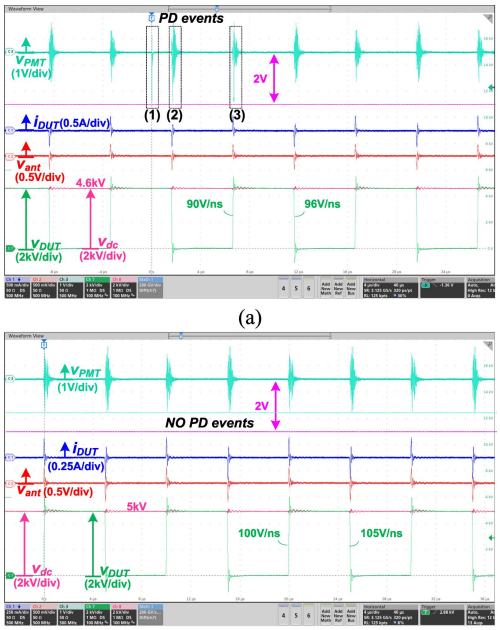

Fig. 13. PD results of transformer samples. (a) #1 (FR-4 dielectric without gel potting) under 4.6-kV PWM voltage. (b) #4 (DiClad-880 dielectric with gel potting) under 5-kV PWM voltage.

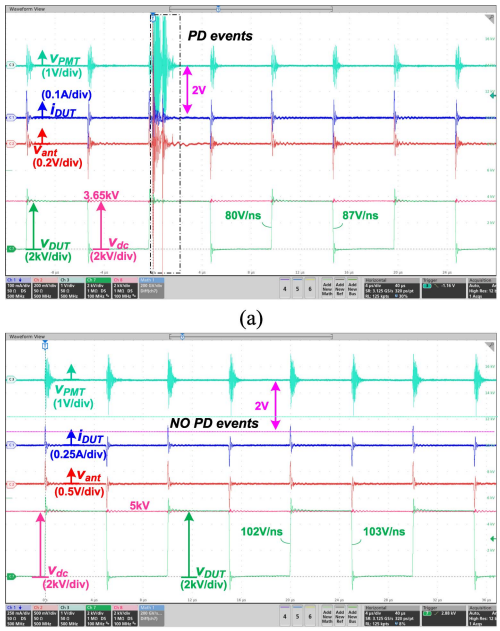

Fig. 14. PD results of GD circuit sample. (a) Before gel potting at 3.65-kV PWM voltage. (b) After gel potting at 5-kV PWM voltage.

a *dv/dt* of 100–105 V/ns. To determine the PDIVs of transformer samples #2–#4, higher PWM voltage pulses are needed. Fig. 14 shows PD results of GD circuit sample before and after gel potting. Before gel potting shown in Fig. 14(a), intense PD signals are captured by all three PD sensors at 3.65-kV PWM voltage, with a rising and falling *dv/dt* of 80 and 87 V/ns. After gel potting shown in Fig. 14(b), no PD occurs at 5-kV PWM voltage with a rising and falling *dv/dt* of 102 and 103 V/ns,

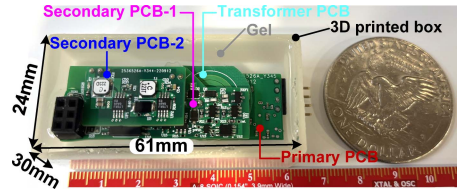

Fig. 15. Photo of the proposed GD hardware.

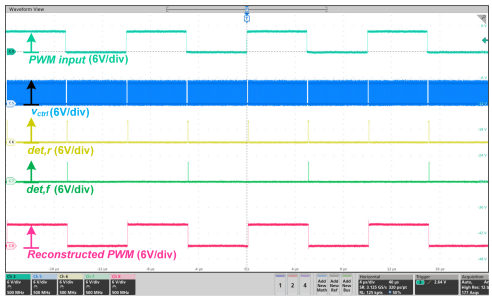

Fig. 16. Experimental waveform of PWM signal transmission.

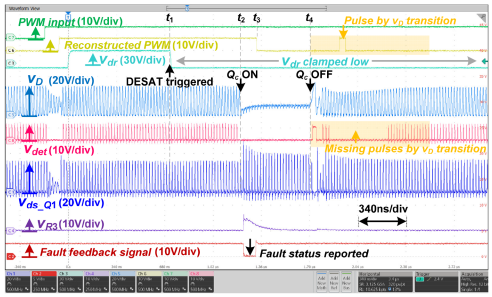

Fig. 17. Experimental waveform of fault feedback signal transmission.

indicating a PDIV >5 kV. It is concluded that the proposed GD has a PDIV of 13.57 kV_{RMS} under 60-Hz ac voltage and a PDIV >5 kV under 100 kHz PWM voltage with a high *dv/dt* >100 V/ns.

V. Experimental Results

The proposed GD hardware has been developed in the lab and is shown in Fig. 15. It follows a vertical PCB stack structure shown in Fig. 8. A 3-D printed box with dimensions of 61 mm $\times$ 24 mm $\times$ 30 mm is designed to house the GD PCB stacks and silicone gel.

A. Functionality and Timing Characteristics Verification

Fig. 16 presents the experimental waveform of PWM signal transmission by proposed GD at $f_{\rm pwm} = 100$ kHz and $D = 50\%$, where the EIO modulation is demonstrated.

Fig. 17 shows the experimental waveform of fault feedback signal transmission by the proposed GD, where a DESAT fault is intentionally emulated (by disconnecting the GD from SiC MOSFET) at the GD secondary side. After $v_{\rm dr}$ goes off in response to DESAT fault at t_1, Q_c is ON during t_2–t_4 to increase the peak voltage of $v_{\rm ds\_}{}_{Q1}$, which is detected by v_{R3} to trigger

Fig. 18. Propagation delay time measurement. (a) t_{pdlh} and (b) t_{pdhl}.

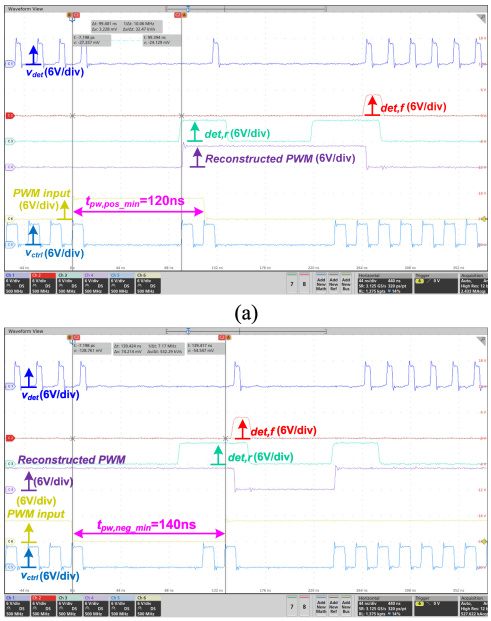

Fig. 19. Measured minimum pulsewidths. (a) $t_{\mathrm{pw,pos\_min}}$ and (b) $t_{\mathrm{pw,neg\_min}}$.

a negative pulse on the fault feedback signal. Therefore, it has been validated that the fault status of the GD secondary side can be successfully transmitted to the primary side using the same transformer. Although the reconstructed PWM signal may be affected during the fault feedback signal transmission, its impact on the GD actuator output (i.e.,v_{dr}) has been eliminated using a latch circuit to clamp v_{dr} at -5 V.

The propagation delay times of the proposed GD are measured in Fig. 18, which are $t_{\mathrm{pdlh}} = 98.5$–100.2 ns, and $t_{\mathrm{pdhl}} = 146.3$–$148.0$ ns, with negligible variations. The minimum allowable PWM pulsewidths are shown in Fig. 19, which are $t_{\mathrm{pw,pos\_min}} = 120$ ns and $t_{\mathrm{pw,neg\_min}} = 140$ ns. The measured propagation delay times and minimum PWM pulsewidths are consistent with the theoretical analysis in Section III.

B. CMTI Characterization

The CMTI of the proposed GD is characterized experimentally using the test setup shown in Fig. 20. A CM pulse generator

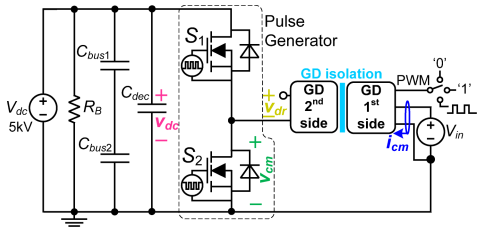

Fig. 20. CMTI test setup.

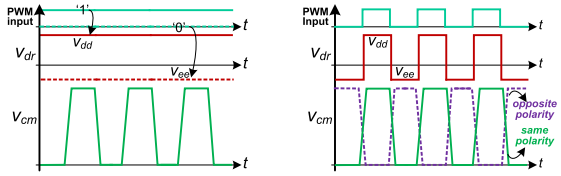

Fig. 21. Timing diagrams of CMTI test. (a) Static CMTI with PWM = "1" or "0." (b) Dynamic CMTI with the same or opposite polarity of v_{cm} and v_{dr}.

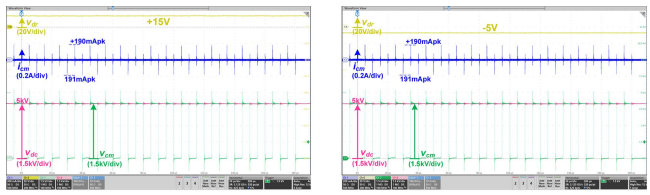

Fig. 22. Static CMTI testing waveforms. (a) PWM = "1." (b) PWM = "0."

generates 100-kHz, 5-kV CM voltage pulses v_{cm} with $D = 50\%$ and $dv/dt = 100$ V/ns. v_{cm} is applied across the primary and secondary sides of the proposed GD, resulting in the CM current i_{cm} flowing through the isolation barrier of the proposed GD. The proposed GD passed both static and dynamic CMTI tests with timing diagrams shown in Fig. 21. In static CMTI tests, PWM input is set to either high or low, keeping v_{dr} at a constant level of either V_{dd} or V_{ee}. In dynamic CMTI tests, PWM input is toggled between high and low to alternate v_{dr} between V_{dd} and V_{ee}, where the rising and falling v_{dr} transition occurs during the rising and falling or during the falling and rising transients of v_{cm}. Fig. 22 shows static CMTI testing waveforms. Zoomed-in dynamic CMTI testing waveforms with v_{dr} transition during v_{cm} rising/falling or falling/rising transients are shown in Fig. 23(a)–(d), respectively. The rising and falling dv/dt of v_{cm} are measured as $+100.2$ and -101 V/ns, respectively, and the peak i_{cm} reaches $+190$ and -191 mA, respectively, by which C_{cp} of proposed GD is estimated to be 1.9 pF. This value is competitive with SOA MV-isolated GDs. Despite the high dv/dt transients of v_{cm}, v_{dr} of the proposed GD remains clear and stable, without high or low errors, missing or false pulses, or the output latch issue. It is concluded that the proposed GD has a CMTI > 100 V/ns at 5-kV CM voltage, which is suitable for MV SiC MOSFET applications.

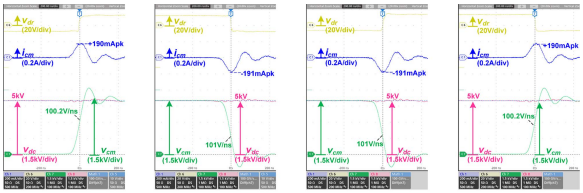

Fig. 23. Dynamic CMTI testing waveforms. (a) Rising $v_{\rm dr}$ during $v_{\rm cm}$ rising transient. (b) Falling $v_{\rm dr}$ during $v_{\rm cm}$ falling transient. (c) Rising $v_{\rm dr}$ during $v_{\rm cm}$ falling transient. (d) Falling $v_{\rm dr}$ during $v_{\rm cm}$ rising transient.

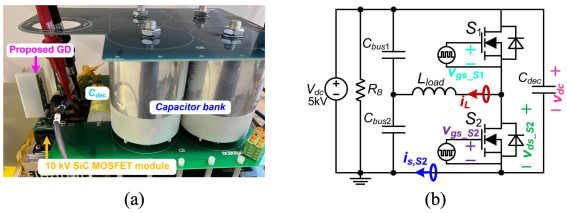

Fig. 24. Continuous test platform. (a) Hardware. (b) Schematic.

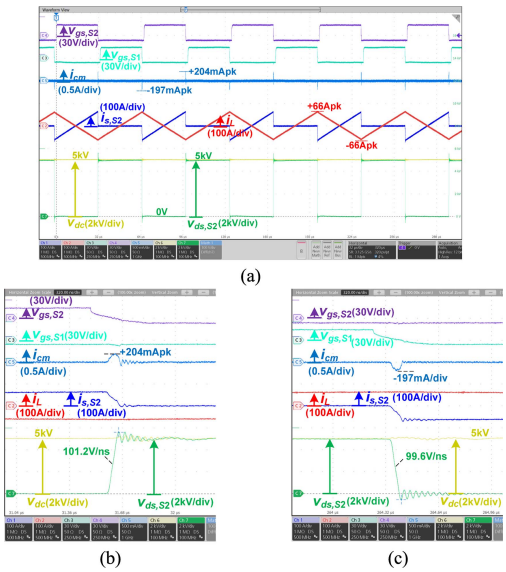

Fig. 25. Continuous testing waveforms for 10-kV SiC MOSFET at $V_{\rm dc}$ = 5 kV with *dv/dt* up to 100 V/ns. (a) Overall waveform. (b) S_2 turn-off transients. (c) S_1 turn-off transients.

C. Dynamic Switching Verification on 10-kV SiC Device

The continuous test is conducted to verify the effectiveness of the proposed GD in driving 10-kV SiC MOSFET with dynamic switching operation. The photo and schematic of the continuous test platform are presented in Fig. 24(a) and (b), respectively. The continuous testing waveform on 10-kV SiC MOSFET half-bridge module is shown in Fig. 25(a), where $V_{\rm dc}$ = 5 kV, peak-to-peak inductor current $i_{L,\rm pp} = 132$ A, $R_{\rm gon} = R_{\rm goff} = 2\,\Omega$, $L_{\rm load} = 590\,\mu$H. Switches S_1 and S_2 are switched complementarily at 15 kHz. Zoomed-in switching transients are shown in Fig. 25(b) and (c), where the CM current through upper GD reaches + 204 mA as the rising *dv/dt* reaches 101.2 V/ns, and −197 mA as the falling *dv/dt* reaches 99.6 V/ns. It is demonstrated that the proposed GD can continuously drive 10-kV SiC MOSFET at 5-kV dc-link voltage and a high *dv/dt* up to 100 V/ns, without false-triggering, missing pulses, or undesired delays, showcasing robust noise immunity.

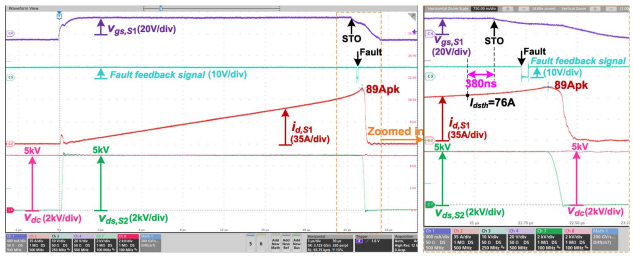

Fig. 26. Experimental DESAT protection waveform on 10-kV SiC MOSFET and fault feedback signal transmission.

The functionalities of DESAT protection and fault feedback signal transmission are verified on the upper switch S_1 at 5-kV dc-link voltage. The experimental waveform is presented in Fig. 26, where DESAT protection is triggered when S_1 current reaches the protection threshold of 76 A. After a response time of 380 ns, S_1 starts soft-turning-off. Subsequently, after 400 ns, the fault feedback signal at the GD primary side has a narrow negative width to indicate the fault status.

VI. Conclusion

The pulse-transformer-based GD offers the advantages of smaller footprint and lower cost due to its capability to enable integrated signal-power transmission. However, most of the pulse-transformer GDs are designed for LV power devices. The first MHz pulse-transformer-based GD for 10-kV SiC MOSFETs has been introduced recently which uses dual transformer configuration to achieve the full duty-cycle range operation. This article presents a novel isolated GD for 10-kV SiC MOSFETs based on a single pulse transformer. The proposed GD utilized a 50-MHz class-E RFC with a unique EIO modulation scheme to simultaneously transmit both PWM and GD power without FOs. In addition, by intentionally short-circuiting the transformer secondary winding, the GD secondary-side fault status was monitored by detecting the peak voltage variation of the primary-side switch of class-E RFC without FOs. The timing characteristics of the proposed GD were competitive with commercially isolated GDICs. It can operate over an ultra-wide duty-cycle range, including 0% and 100% duty cycles, with a low propagation delay < 150 ns, but the negative pulse width < 140 ns should be prohibited. The proposed insulation scheme was experimentally characterized under both 60-Hz ac voltage and high frequency, high *dv/dt* PWM voltage. The proposed GD has a CMTI > 100 V/ns and an ultra-low $C_{cp} < 2$ pF, ensuring the driving reliability for 10-kV SiC MOSFETs. The proposed GD has a small footprint of 61 mm × 24 mm × 30 mm, which can be further integrated into 10-kV SiC device packages to improve reliability and switching performance. The proposed GD can also be applied to other MV power semiconductor devices.

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