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Optimal Utilization of Battery Sources in Cascaded H-Bridge Inverter by Coordinated Sequence Selection

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***Abstract*—With ever increasing grow of inverter-based generation, energy storage systems that can support the grid during load and generation disturbances become vital for stable and resilient operation of the grid. Battery energy storage systems (BESS) are one of the promising candidates to provide grid support during disturbances. Using secondhand batteries which are retired from electric vehicles can alleviate the cost of BESS requirements for grid applications. However, this high number of secondhand batteries have diverse state of the charges (SOCs), which should stay in a predefined range to avoid failure or malfunction of BESS. This article proposes a control scheme for BESS interfaced to a cascaded H-bridge inverter for grid-integration. The proposed scheme is based on a model predictive control (MPC) embedded with coordinated battery cell selection which determines the contribution of each battery to the overall power injection to the grid according to its SOC. The process starts with classification of batteries into subsets according to their SOCs, then sequence matrices are constructed based on the subsets to optimize the power drawn from each cell to comply with battery's SOC. The proposed MPC scheme determines the optimal switching array according to the coordinated battery cells sequence selection. Several experimental case studies are provided that validate the proposed scheme's impact and theoretical expectations. Furthermore, the computational burden and the performance of the proposed scheme are compared with the other algorithms to show the merits of the proposed method.**

***Index Terms*—Battery energy storage system (BESS), cascaded multilevel inverter, distributed energy resources, model predictive control (MPC), state of charge balancing.**

I. Introduction

BATTERY energy storage systems (BESS) can support the voltage and frequency of the grid during undesired events which becomes more critical as the penetration of renewable energy sources increases [1], [2]. BESS is realized by connecting several numbers of individual cells in series and/or parallel with each other to meet a certain charge capability for the whole battery package. With ongoing increasing demand for backup energy storage for the microgrids, supplying this large number of battery cells would cause environmental and ecological risks [3], [4]. On the other hand, electric vehicles (EVs) are growing exponentially in automotive market across the globe to meet the green mandates and reduce greenhouse gas emissions. Batteries from retired EVs can be given a second life for utilities and power grid applications as a low-cost energy storage system [5], [6]. However, due to the diversity of state of the charge (SOC) in worn EV batteries, proper measures should be taken to manage the amount of drawn energy from each battery when they are forming a large-scale BESS for medium or high voltage grid application. Implementing algorithms for drawing power from the battery cells according to their available energy will ensure longer performance of the BESS.

Cascaded H-bridge (CHB) inverters prove themselves as a reliable solution for interfacing distributed energy resources with medium to high voltage grid that can offer high number of benefits including less voltage stress across the semiconductors, reduced *dv/dt* stress, and lower electromagnetic interference which can be further decreased by selecting optimized switching sequences [7], [8], [9]. Furthermore, the CHB topology enables more flexible control on power drawn from dc-sources, such as battery cells. Thus, literature proposes different control schemes with the goal of balancing the power drawn from individual dc-sources of CHB. For instance, in [10], model predictive control (MPC) is combined with a phase-shifted pulse width modulation to balance the power drawn from each phase as well as each cell. Yet, this algorithm does not consider unequal power sharing when the available energy of the dc sources are unequal. In [11], the authors proposed a method to change the phase difference between the carrier signals of the CHB cells to mitigate the harmonics around twice the carrier frequency when the input dc voltage of the cells are different. In [12], three variation of phase-shifted carrier pulsemidth modulation (PWM) techniques is compared in terms of total harmonic distortion and harmonic spectrum under different conditions of dc voltage magnitude and modulation indices. In [13], Alcaide et al. proposed a method for phase-shifted PWM that forms groups

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from the CHB cells to eliminate harmonic content around twice carrier frequency while mitigating harmonics around $4f_c$ in each group when the magnitude of the dc voltages in each CHB cell is not equal. In [14], the idea of the variable phase angle carrier PWM is generalized to consider all the harmonics by minimizing a cost function. Although the proposed algorithms using variable phase-shifted carrier PWM can satisfactorily decrease harmonic content when the magnitude of dc sources are not identical, it cannot provide the ability to draw all the possible combination of input power for each cell which enables us to use all the batteries for longer time without reaching their lower SOC limit. In [15], a single phase CHB with battery balancing capability is proposed. The controller decides suitable switching angles to total harmonic distortion and battery balancing. However, the proposed algorithm in this article is described for fundamental frequency switching when all the batteries have different SOC. Thus, the main shortcoming of this approach is when two or more battery cells have similar SOC which impacts the proper balancing using the proposed approach. In [16], the authors proposed pseudoopen circuit voltage to estimate the SOC of the batteries in the cells by using idle time in each cell and using cell model without focus on SOC balancing itself. In [17], Liang et al. proposed a balancing algorithm that considers the active power constrain of each cell in CHB structure. The algorithm defines the required power to balance the cells considering three active power constraints which avoid drawing power from the cells more than their rated values. Nonetheless, the SOC balancing approach is not well addressed in detail, and it has similar shortcomings as previous approaches. Furthermore, all these approaches are carrier based with multi-nested loop PI controllers that requires tuning efforts.

This article proposes a MPC scheme with the capability of coordinated battery cell sequence selection in horizon of time according to their SOCs for optimal utilization of BESS interfaced with CHB for grid integration. MPC empowers the selection of the next converter's state based on the multiobjective optimization approach to attain the desired value for the control variables providing the system with rapid dynamic response in a single loop [18]. However, conventional MPC schemes do not consider the status of dc-sources for switching array selection, a challenge that is amplified if the dc-sources are battery cells with arbitrary set of SOC for aged batteries such as the considered application in this article. The inherent characteristics of MPC allows for multiobjective constraint optimization that is well suited for the objective of this article to create a coordinated battery cell sequence selection in a straightforward manner without tuning effort. This article proposes a generalized method to select the sequence of batteries in each sampling time using MPC which ensures optimal utilization of dc sources in each level of the output voltage according to their SOC.

The proposed MPC scheme begins with generating feasible cost functions according to the present voltage level. Then, battery cells are classified into subsets according to the distribution of their SOCs. According to the created subsets and considering the present voltage level based on subset of cost functions generated, a sequence of battery cells for forming the desired voltage levels in horizon of time are determined and used for optimal switching array generation each sample time. The proposed scheme is summarized in Fig. 1. The coordinated cells selections ensure energy drawn from individual cells according to their SOCs under any SOC diversity which is not well addressed in the prior works. Furthermore, it addresses the limitation of conventional MPC scheme for CHBs with unbalanced or uncontrolled power drawn from individual cells. Thus, the main contribution of this article can be summarized as follows.

1) A new MPC scheme that considers the status of dc-sources (e.g., battery cells) for optimal switching array generation. Thus, eliminating the need of controller tuning and complex modulation schemes while considering the dc-source status of CHBs for switching signal generation using MPC.
2) An algorithm that considers diverse distribution of battery cells' SOCs at each voltage level of CHB to addresses the need of optimal power distribution between CHB cells with different combination of SOCs.
3) Enabling the optimal utilization of secondhand battery cells retired from EVs for power grid applications.

The rest of the article is organized as follows: Section II provides an overview of the CHB and groundwork of MPC formulation. Section III explains the detail of the proposed battery cell classification and subset creation for power drawn scheduling according to their SOCs. Furthermore, the requirements that should be met in battery cell sequence selection are discussed. Section IV provides determination approach of the sequence matrices and augmented sequence matrices according to the present voltage level and content of the created subsets in Section III. Section V compares the computational burden of the proposed scheme with the finite-set MPC. Section VI provides the experimental results and case studies. Finally, Section VII concludes this article.

II. MPC Scheme Formulation for CHB

The structure of the studied MPC is shown in Fig. 1. the power stage of the converter is composed of N_{cell} H-bridge cells which are cascaded with each other and connected to the grid after an inductive filter denoted by L_f. The dc-link of each cell is connected to a battery. In order to control the CHB, an MPC controller is implemented in the $\alpha\beta$ frame. Second order generalized integrator is used to generate quadrature axis, which improves the performance of the controller when the grid voltage is affected by distortion [19], [20]. Assuming that P_k and Q_k are the reference active and reactive power in k^{th} step of running the controller, respectively, the reference currents in dq frame is obtained as following:

$$\begin{aligned} i_{d,k}^{\text{ref}} &= \frac{2(P_k V_{d,k}+Q_k V_{q,k})}{V_{d,k}^2+V_{q,k}^2} \\ i_{q,k}^{\text{ref}} &= \frac{2(P_k V_{q,k}-Q_k V_{d,k})}{V_{d,k}^2+V_{q,k}^2} \end{aligned} \tag{1}$$

where, $V_{d,k}$ and $V_{q,k}$ are the grid voltage in d- and q-axis, respectively. For charging the dc sources active power should be extracted from the grid. Therefore, the value of the extracted active power should be used with negative sign in (1). By transferring the reference currents to $\alpha\beta$ frame, the following

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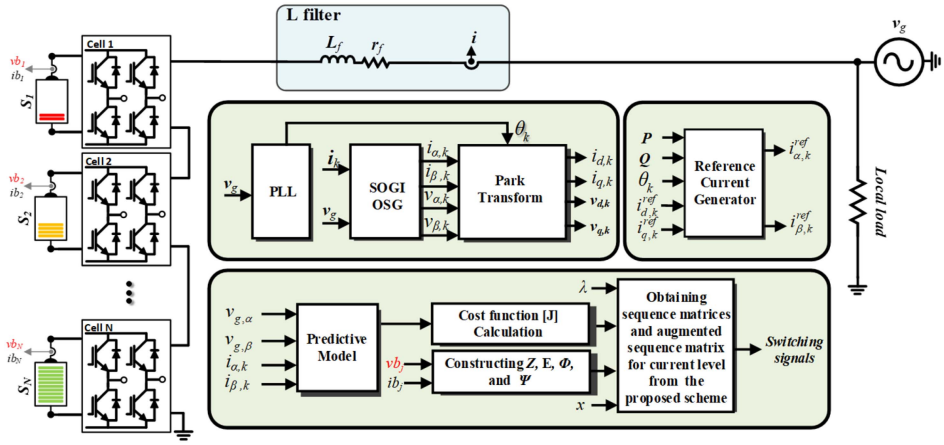

Fig. 1. Proposed MPC with coordinated sequence selection scheme for optimal utilization of battery sources.

equations is obtained for reference currents:

$$\begin{aligned} i_{\alpha,k}^{\text{ref}} &= i_{d,k}\sin(\theta_k) \\ i_{\beta,k}^{\text{ref}} &= i_{q,k}\cos(\theta_k) \end{aligned} \tag{2}$$

where θ_k is the grid voltage angle in k^{th} step. The voltage of the CHBs, v_{CHB}, is related to the inverter output voltage, v_g, via the following relation:

$$v_{\text{CHB}} = L_f\frac{di}{dt} + r_f i + v_g \tag{3}$$

where L_f and r_f are the output filter inductance and resistance of the output filter, respectively. The value of the calculated parameters in the current sampling time is k^{th} step, which is denoted by k subscript. In order to predict the current in the $\alpha\beta$ frame in the next sampling time denoted as $(k+1)$th step, using the Euler forward method, the following equations can be written:

$$\begin{aligned} i_{\alpha,k+1} &= \tfrac{T_s}{L_f}[v_{\text{CHB},\alpha} - v_{g,\alpha} - i_{\alpha,k}r_f] + i_{\alpha,k} \\ i_{\beta,k+1} &= \tfrac{T_s}{L_f}[v_{\text{CHB},\beta} - v_{g,\beta} - i_{\beta,k}r_f] + i_{\beta,k} \end{aligned} \tag{4}$$

where T_s is the sampling time of the current and voltage sensors. The current is predicted based on all the possible switching arrays that make the cascaded bridge voltage. In this article, the predicted current is used to select a subset of feasible switching array in the next time step. This subset of switching arrays which minimize the cost function given by

$$J = \left|i_{\alpha,k}^{\text{ref}} - i_{\alpha,k+1}\right| + \left|i_{\beta,k}^{\text{ref}} - i_{\beta,k+1}\right|. \tag{5}$$

In fact, in this article, (5) provides a subset of feasible switching arrays whose corresponding battery cell sources should be evaluated to be complied with the augmented sequence matrices as explained in the Sections III and IV. Thus, unlike conventional MPC, (5) does not directly determine the switching array every sampling time.

III. Proposed Battery Cells Subset Creation and Power Sharing Mechanism

In order to share the power among the batteries based on their SOCs, the controller should have a specific power sharing scheme for every possible combination of SOCs in the batteries. Z is defined as the set of all batteries used in the CHB structure

$$Z = \{S_i | 1 < i < N\} \tag{6}$$

where S_i denotes the battery of ith cell in the CHB structure. We can then define two sets A and B such that $A \cap B = \emptyset$ and $A \cup B = Z$. A and B can be represented as follows:

$$A = \{S_j \in Z | \forall S_x \in A, \text{SOC}_x = \text{SOC}_j\} \tag{7}$$

$$B = \{S_k \in Z | \forall S_y \in B, y \neq k, \text{SOC}_y \neq \text{SOC}_k\} \tag{8}$$

where SOC_x, SOC_y, SOC_i, and SOC_j are the values of SOC in S_x, S_y, S_i, and S_j, respectively. The $m \times 1$ vector E which includes members of A can be represented as follows:

$$\text{E} = [\varepsilon_i] | 1 \leq \forall i \leq m, S_i \in A \tag{9}$$

B can be separated into two subsets, namely *SUT* and *SUB*, for which $SUT \cap SUB = \emptyset$ and $SUT \cup SUB = B$ as following:

$$SUT = \{S_i | S_i \in B, \text{SOC}_i > \Gamma\} \tag{10}$$

$$SUB = \{S_i | S_i \in B, \text{SOC}_i < \Gamma\} \tag{11}$$

where Γ is the SOC of each member of A. Depending on the value of Γ, only one, both or none of the *SUT* and *SUB* set can be null set. Assuming that none of the *SUB* and *SUT* sets are null set, by sorting the batteries based on their SOC in descending order Φ and Ψ vectors can be defined as follows:

$$\Phi = [\varphi_i] | 1 \leq \forall i \leq q, S_{\varphi_i} \in SUT, \text{SOC}_{\varphi_i} > \text{SOC}_{\varphi_{i+1}} \tag{12}$$

$$\Psi = [\psi_i] | 1 \leq \forall i \leq p, S_{\psi_i} \in SUB, \text{SOC}_{\psi_i} > \text{SOC}_{\psi_{i+1}} \tag{13}$$

where q and p are the number of rows in Φ and Ψ, respectively. If $\text{E} \neq \emptyset$ Depending on which of *SUT* and *SUB* sets is equal to null set, four situation to determine the power that should be drawn from each batteries can be considered as following:

$$\text{If E} \neq \emptyset \begin{cases} SUB = \emptyset, SUT = \emptyset & (\Omega_1) \\ SUT = \emptyset, SUB \neq \emptyset & (\Omega_2) \\ SUB = \emptyset, SUT \neq \emptyset & (\Omega_3) \\ SUB \neq \emptyset, SUT \neq \emptyset & (\Omega_4) \end{cases}. \tag{14}$$

The first situation which is denoted as Ω_1 is the situation in which all the dc sources are equal. The fourth condition marked

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as Ω_4 happens when there are some batteries with more SOC than the sources inside E, and there are some batteries with less SOC than the sources inside E. In order for the controller to share the power between the batteries based on their SOCs, the following relations should be met for each case described earlier

$$\text{For } (\Omega_1)\ \forall S_i, S_j \in A, \overline{E_{S_i}} = \overline{E_{S_j}} \tag{15}$$

$$\text{For } (\Omega_2) \begin{cases} \forall S_i, S_j \in A, \overline{E_{S_i}} = \overline{E_{s_j}} = \chi, \overline{E_{s_{\psi_1}}} \leq \chi \\ \forall S_i \in SUB, i < p, \overline{E_{S_{\psi_i}}} \geq \overline{E_{S_{\psi_{i+1}}}} \end{cases} \tag{16}$$

$$\text{For } (\Omega_3) \begin{cases} \forall S_i, S_j \in A, \overline{E_{S_i}} = \overline{E_{S_j}} = \chi, \chi \leq \overline{E_{S_{\varphi_q}}} \\ \forall S_i \in SUT, i < q, \overline{E_{S_{\varphi_i}}} \geq \overline{E_{S_{\varphi_{i+1}}}} \end{cases} \tag{17}$$

$$\text{For } (\Omega_4) \begin{cases} \forall S_i, S_j \in A, \overline{E_{S_i}} = \overline{E_{S_j}} = \chi, \overline{E_{S_{\psi_1}}} \leq \chi \leq \overline{E_{S_{\varphi_q}}} \\ \forall S_i \in SUT, i < q, \overline{E_{S_{\varphi_i}}} \geq \overline{E_{S_{\varphi_{i+1}}}} \\ \forall S_i \in SUB, i < p, \overline{E_{S_{\psi_i}}} \geq \overline{E_{S_{\psi_{i+1}}}} \end{cases} \tag{18}$$

When all the SOC are different than each other, i.e., $\mathrm{E} = \emptyset$, the following relation for the power drawn from each battery should be met by the controller:

$$(\Omega_5) \begin{cases} \forall S_i \in SUB, i < p, \overline{E_{S_{\psi_i}}} \geq \overline{E_{S_{\psi_{i+1}}}} \\ \forall S_i \in SUT, i < q, \overline{E_{S_{\varphi_i}}} \geq \overline{E_{S_{\varphi_{i+1}}}} \geq \overline{E_{S_{\psi_1}}} \end{cases} \tag{19}$$

where $\overline{E_{s_i}}$ is the energy delivered to the grid from S_i, and χ is considered to be the power drawn from sources that have equal SOC. For a specific number of batteries in a CHB structure, at the beginning of the CHB operation the batteries can have arbitrary SOC and the SOC of the batteries would change during the operation of the CMI, thus, the value of Γ and vectors E, Ψ, Φ can change. The controller should cover all the possible situation of SOC for a particular number of batteries to ensure the controller can maintain the balance of SOCs or balancing the batteries' SOC if they are unbalanced. For charging the dc sources, assuming that $\overline{E_{s_j}}$ is the power absorbed by the dc sources, the controller regulates the energy absorbed by $\overline{E_{S_{\Psi_1}}}$ to be less than the other sources in Ψ and more than χ. Furthermore, the controller should adjust $\overline{E_{S_{\Phi_1}}}$ to be less than the other sources in Φ and χ.

This mathematical formulation for battery cells classification and subset creation for power sharing is graphically illustrated in Fig. 2 for all possible SOC situations for three battery cells as a case study. As illustrated in Fig. 2, in the first up to sixth situation, none of the batteries are equal, which corresponds to $E = \emptyset$. In the first case the controller draws more power from battery one than that of battery two and three, whereas it draws more power from the third battery than that of the other batteries in the sixth situation. In rows 7 to 13 situation in Fig. 2, only two batteries are equal in SOC and the other battery has higher or lower SOC than the SOC of the equal ones. In this situation, the controller draws equal energy from the two equal batteries while the other battery can deliver higher or lower energy to the grid considering its SOC. Next, the sequence matrices and augment sequence matrix for battery cells will be constructed for generating the optimal switching arrays.

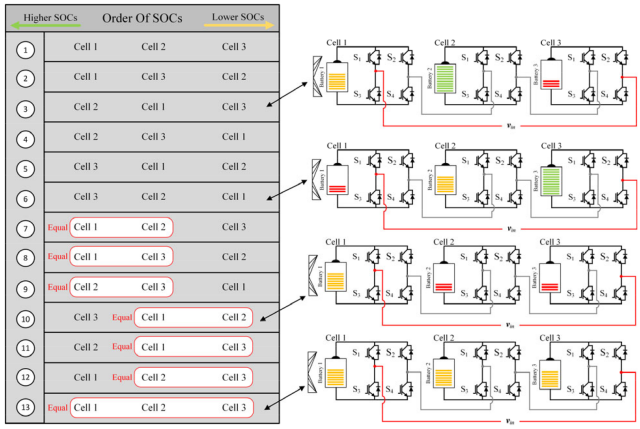

Fig. 2. Feasible combinations of SOC when the number of cells is three.

IV. Proposed Sequence Selection Method

The absolute value of energy exchanged between grid and S_α which is selected by the controller to deliver energy to the grid during a sampling time can be calculated as follows:

$$\hat{E}_{stp,S_\alpha}(\lambda) = \int_{\lambda}^{\lambda+\Delta\theta_{smp}} V_{\mathrm{DC},\alpha} I \left|\mathrm{Sin}\,\tau\right| d\tau \quad 0 \leq \lambda \leq 2\pi \tag{20}$$

where λ is the angle of injected current at which a sampling time period starts. $\Delta\theta_{smp}$ is the phase difference corresponds to the T_s, respectively. Furthermore, I is the maximum value of the output current, and $V_{\mathrm{DC},\alpha}$ is the voltage of S_α. Using the first order Taylor expansion in one sampling time, (20) can be expressed as follows:

$$\hat{E}_{stp,S_\alpha}(\lambda) = \begin{cases} I_{\mathrm{out}} V_{\mathrm{DC}} \Delta\theta_{smp} \sqrt{1 + \frac{\Delta\theta_{smp}}{4}}\, \mathrm{Sin}(\lambda + \beta) & 0 \leq \lambda \leq \pi \\ -I_{\mathrm{out}} V_{\mathrm{DC}} \Delta\theta_{smp} \sqrt{1 + \frac{\Delta\theta_{smp}}{4}}\, \mathrm{Sin}(\lambda + \beta) & \pi < \lambda \leq 2\pi \end{cases} \tag{21}$$

where $\tan(\beta) = 0.5\Delta\theta_{smp}$. According to (21), the energy exchanged between grid and a specific battery which conduct current during a sampling time varies in a sinusoidal manner. As a result, as λ increase the energy exchanged between the battery and grid in a sampling time will increase before $\pi/2$ in the first half cycle and $3\pi/2$ in the second half cycle. After $\pi/2$ and $3\pi/2$ increase in λ will result in decrease in the exchanged power during one sampling period.

Depending on the instantaneous desired current, different number of batteries are connected in series with each other to make an inverter voltage that can minimize the cost function (5). In each T_s, the MPC can select a particular set of battery sources to make the desired output current. At the first level, the controller has N ways to select one battery from N batteries. At the x^{th} level, the controller should select x batteries from N to make the output voltage. At level $+N$ or $-N$ of the bridge voltage all the battery sources are connected to each other, which implies

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that there is only one combination of sources that can make $\pm N$ level.

To share the power between the batteries with the proposed coordinated sequence selection, at each voltage level, the controller implements a particular scheme to select x number of batteries out of N in each sampling time such that the power drawn from each source meet the conditions described in Section III. The sources selected by the controller in a specific sampling time to generate a specific level of the output voltage is arranged in a vector. In the level x, i.e., output voltage of xV_{DC}, the element of each vector is x number of sources connected together to make the output voltage. By arranging these vectors corresponding to consecutive sampling times which make a specific level, a sequence matrix is created. To satisfy the conditions described in Ω_1 to Ω_5, two sequence matrix U_x and V_x will be defined in the following sections for each level x. The augmented sequence matrix is created by concatenating U_x and V_x according to x. Each vector in the augmented sequence matrix is composed of the sources which should deliver power to the source in each sampling time. The augmented sequence matrix can be defined as follows:

$$SQ_x = \begin{cases} [V_x] & x \le q \\ \begin{bmatrix} U_x \\ V_x \end{bmatrix} & x > q \end{cases}. \tag{22}$$

The U_x provides a sequence that meets the condition described in Ω_1 to Ω_4 for E members. The V_x provides a sequence which meets conditions explained in Ω_3 and Ω_4 for *SUT* and *SUB* members. When $x \le q$ the conditions described for the sources inside *SUB* in Ω_2 and Ω_4 is met by drawing zero power from the sources inside *SUB*. When the present level number, i.e., x, is less than the number of sources in *SUT*, the controller draws no power from the sources in E and *SUB*. Hence, the augmented sequence matrix is made up of V_x. On the other hand, when $x \ge q$, depending on x, the sources in *SUT* and/or E deliver power to the grid.

Fig. 3 graphically illustrates the sequence matrices construction and its impact on the power delivered power of each cell in the third and fourth level of a 15-level inverter for a given *Z*, E, Φ and Ψ, which are determined according to the (6), (9), (10), and (11). Furthermore, Fig. 3 shows the instantaneous power delivered to the grid by E members for a given 48 sampling time period. For each battery in E, each bar shows the power delivered to the grid by that battery in a sampling time. The sampling times for which each battery in E delivers power is denoted by κ_1 to κ_9. The proposed scheme tries to maintain the balance between batteries in E by arranging the power delivery sampling times in a symmetrical manner around specific times which corresponds to W_1 to W_5 in Fig. 3. As depicted in Fig. 3, κ_1 is located in sampling times 1 and 15 for S_1, 3 and 13 for S_2. Furthermore, for S_6, κ_1 is placed in sampling time 5 and 11 and sampling time 7 and 9 for S_7. Therefore, the all the sampling time denoted by κ_1 is symmetrically placed around W_1 for all the dc sources inside *E*. Similarly, for the batteries in E, the sampling times denoted by κ_2, κ_3 are located symmetrically around W_2 and W_3, respectively. The κ_4 is located in sampling times 24 and 2 for both S_1 and S_2. Meanwhile, it is in sampling time 4 and 22 for S_6 and sampling time 12 and 14 for S_7, which shows symmetry around W_4. Similarly, the sampling times denoted by κ_5, κ_6 are located symmetrically around W_4 and the sampling times denoted by κ_7, κ_8, κ_9 are located symmetrically around W_5. By adopting this arrangement, the proposed scheme ensures that the energy delivered to the grid by the batteries in E is close together. On the other hand, as shown in the figure, the coordinated sequence selection ensures that the energy delivered to the grid by the sources in *V* is higher than energy delivered by each source in E.

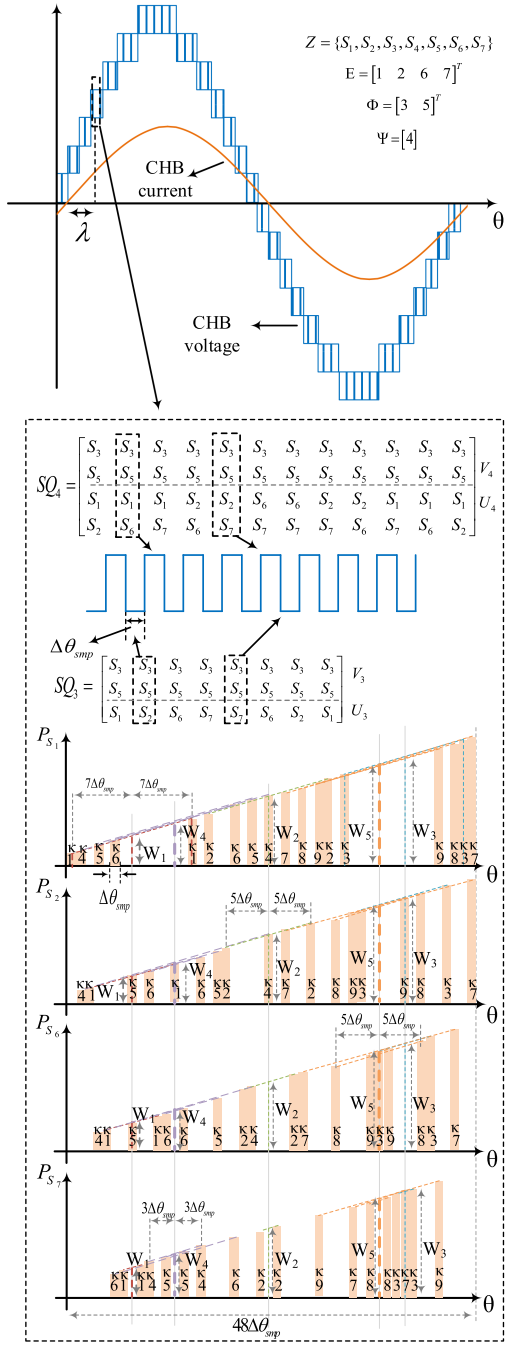

Fig. 3. Illustration of delivered power of each source in E with selected sequence in an interval for a given Z, *E*, *Φ*, and Ψ in a 15-level CMI.

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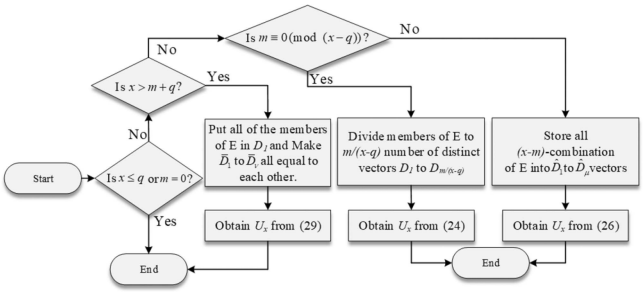

Fig. 4. Flowchart to obtain U_x.

A. Definition of U_x

Fig. 4 shows the flow chart for obtaining U_x. To obtain the sequence matrix, U_x and V_x are combined together depending on the value of x and q. As depicted in Fig. 4, to obtain U_x, depending on the present voltage level of the CMI, three general situations should be considered. In each condition, the number of column vectors inside U_x is different. In the second condition, the number of column vectors is denoted by η, which can be calculated via (25). In the third condition, the number of column vector inside U_x is denoted by ν which can be calculated via (30). The number of column vectors is dependent on the length of *E*, Φ, and Ψ. These conditions are implemented via three conditional blocks in Fig. 4, which can be described as follows.

1) When $x \le q$ or $m = 0$ because the batteries in *SUT* should deliver more power to the gird, the controller will select all the sources from *SUT*. Thus, the U_x matrix does not exist.
2) When $x > q$, two situations should be considered:
   i) if the members of E can be divided into $\frac{m}{x-q}$ distinct subset, i.e., $\frac{m}{x-q}$ is an integer number, where each subset C_j can be represented as $C_j : 1 \le j \le \frac{m}{x-q}$ such that

$$\bigcup_{j=1}^{m/(x-q)} C_j = A, \quad \bigcap_{j=1}^{m/(x-q)} C_j = \emptyset \tag{23}$$

then U_x matrix is comprised of column vectors that is selected from C_j members which can be defined as follows:

$$U_x = [D_1 \quad D_2 \quad \cdots \quad D_{m/(x-q)} D_{m/(x-q)} \quad D_{(m/(x-q))-1} \quad \cdots \quad D_1] \tag{24}$$

where the column vectors inside U_x, i.e., D_i, can be made from the following relation:

$$D_i = [d_j] | 1 \le \forall j \le \frac{m}{x-q}, d_j \in C_i. \tag{25}$$

   ii) if E members cannot be dividable into distinct subsets to meet (25), i.e., $m \not\equiv 0 \pmod{x-q}$, U_x can be defined as follows:

$$U_x = [\hat{D}_1 \quad \hat{D}_2 \quad \cdots \quad \hat{D}_\mu \hat{D}_\mu \quad \hat{D}_{\mu-1} \quad \cdots \quad \hat{D}_1] \tag{26}$$

where μ is the number of all *(x-q)*-combination of E members which can be calculated as follows:

$$\mu = \binom{m}{x-q} \tag{27}$$

where $\hat{D}_i : 1 \le x \le \mu$ is a column vector which is composed of a combination without repetition of x sources from sources inside E.

The number of column vectors in U_x when $x \le m+q$ can be calculated as follows:

$$\eta = \begin{cases} \frac{2m}{x-q} & m \equiv 0 \pmod{x-q} \\ 2\mu & m \not\equiv 0 \pmod{x} \end{cases}. \tag{28}$$

3) *When* $x > m+q$

If $x > m+q$ all the batteries in E are selected to be in U_x to deliver power to the grid by the controller. U_x has ν number of columns, and can be defined as follows:

$$U_x = [\bar{D}_1 \quad \bar{D}_2 \quad \cdots \quad \bar{D}_\nu] \tag{29}$$

whereν can be calculated as follows:

$$\nu = \binom{p}{x-(m+q)}. \tag{30}$$

To charge the dc sources, conditions 1 and 2 described in this section should be modified to make the dc sources inside *SUB* absorb more energy than the sources inside E. When $x > m+\mathrm{p}$, all the sources inside E are selected to absorb power.

B. Definition of V_x

The sequence matrix V_x is made by the members of *SUT* or *SUB*. When $x \le q$ the control should select x source out of q sources in *SUT* in each sampling time for which the condition for *SUT* members in Ω_3 and Ω_4 hold. The number of column vectors in V_x is denoted by σ which changes according to the value of x and q. When the number of sources inside E is not zero, σ is calculated from (32). Otherwise, (33) is used to determine the number of column vectors inside V_x. Because each source in *SUT* should deliver more power to gird than the sources inside E, each source in *SUT* should conduct more than at least ν times in V_x. V_x can be obtained from the following relations:

$$V_x = \begin{cases} [F_1 \quad F_2 \quad \ldots \quad F_\sigma] & \lambda \le \frac{\pi}{2} \\ [F_\sigma \quad F_{\sigma-1} \quad \ldots \quad F_1] & \lambda > \frac{\pi}{2} \end{cases}. \tag{31}$$

Fig. 5 shows the flowchart to obtain F_i $1 \le i \le \sigma$. In this flowchart, σ is the number of columns in V_x. When $m \neq 0$, σ can be calculated from the following relation:

$$\sigma = \begin{cases} \binom{q}{x} & x \le q \\ \eta & q < x \le m+q \\ \binom{p}{x-(m+q)} & x > m+q \end{cases}. \tag{32}$$

When $m = 0$, the number of E members is zero. As a result, all the batteries have unequal SOCs. In this situation, σ can be

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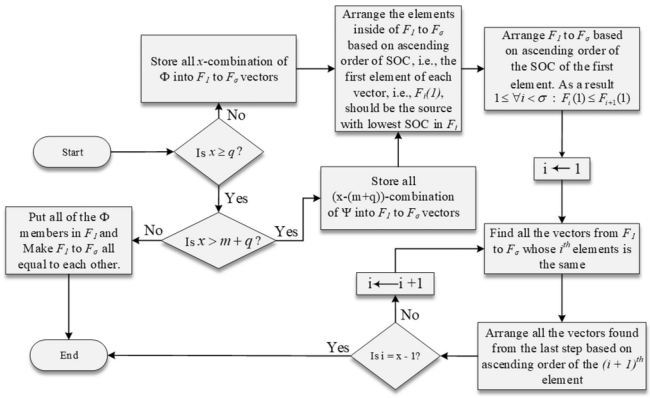

Fig. 5. Flowchart to obtain column vectors inside V_x.

obtained from the following relation:

$$\sigma = \begin{cases} \binom{q}{x} & x \le q \\ \binom{p}{x-q} & x > q \end{cases}. \tag{33}$$

If charging the dc sources is desired, σ should be modified to meet Ω_1 to Ω_5. When $m = 0$, the sources inside *SUB* should be charged. In this case, the sources to be charged are selected from *SUB* if x is less than p.

V. Comparison of the Computational Burden and Required Memory for Implementing the Proposed Scheme and Finite Set MPC

In this section, the computational burden and the required memory for implementing the proposed scheme is compared with the finite set MPC. Fig. 6(a) shows the variation of the number of floating points, flops, of the proposed scheme and finite set MPC when the number of cells changed from one to ten. The number of flops is used as a criterion to compare the computational burden of the proposed scheme and finite set MPC. It should be noted that the finite set MPC does not have the ability of optimal utilization of dc sources during the operation of CHB converter. For the proposed scheme the reference value of current in $\alpha\beta$ frame is calculated in each sampling time. Then, according to (4), the predicted value of the current and associated cost function in $\alpha\beta$ frame is calculated based on the grid and CHB voltage and output filter current for different possible values of output voltage level. Unlike the finite set MPC, the optimization of cost function based on the output voltage level causes significant reduction in the number of iterations which should be done by the processor to find the current vector that minimizes the cost function in each sampling time. As shown in Fig. 6(a), for the finite set MPC the number of flops increases exponentially as the number of cells increases. However, the trend of increase in the number of flops is more linear. Fig. 6(b) shows the minimum required memory to run the proposed scheme and finite set MPC. As shown in this figure, the required memory in KB for both algorithms have an exponential trend when the number of cells increases. However, the rate of increase for the proposed algorithm with optimal

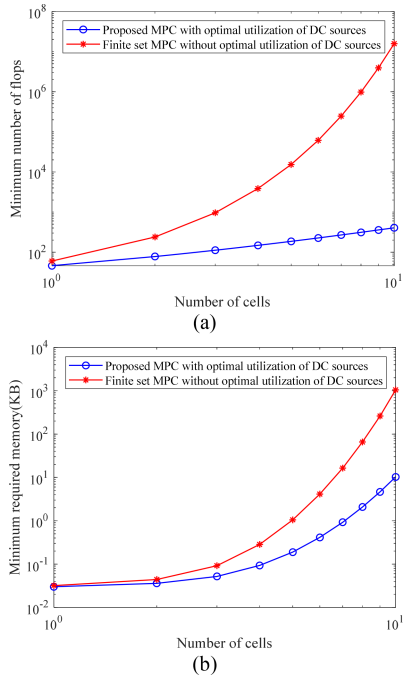

Fig. 6. (a) Minimum number of flops for the proposed scheme and finite set MPC versus number of cells. (b) Minimum required memory in KB for the proposed scheme and finite set MPC versus number of cells.

utilization of the dc sources is less than that of finite set MPC without optimal utilization of dc sources. In finite set MPC all the switching arrays which correspond to all the vectors that are evaluated for cost function minimization are stored in the memory. After selecting the vector that minimizes the cost function, the relative switching array is sent to the gate drive. In the proposed scheme, the selection of the proper vector based on the level and construction of switching array according to the augmented sequence matrix decreases the occupied memory.

VI. Experimental Validation

To prove the feasibility of the proposed scheme, the proposed scheme is prototyped on a seven-level grid following CMI hardware. dSPACE MicroLabBox is used to implement the controller. The sampling time of the controller is 20 μs with a turnaround time of around 12.4 μs which demonstrates low computational effort and feasible implementation of the proposed control scheme on majority off the shelf digital controllers. The turnaround time is a criterion provided by dSPACE platform which shows the amount of time required for the device to perform all the instructions required to run the controller in real time. Although the value of turnaround time is affected by multiple factors other than computational burden of the proposed control, it can provide a comparative metric for the burden of the proposed scheme, whose value for the proposed scheme shows the successful implementation of the proposed scheme on hardware. SKM75GB12T4 is used for the H-bridge switches. A 550 nS deadtime is placed between two consecutive falling and rising edges of the control signals of the switches belonging to the same leg. The CMI is connected to the grid and local load via

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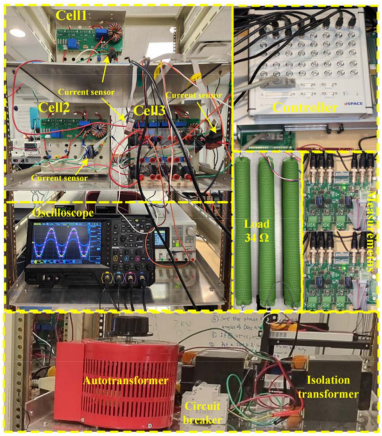

Fig. 7. Configuration of experimental setup.

TABLE I
CHARACTERISTIC OF THE EMULATED BATTERIES

K_1	K_2	G	H	Capacity (Ah)	Nominal voltage (V)
80.24	1.11	6.23	122.12	0.5	75
103.77	1.03	7.77	122.13	0.5	95

an inductive filter of 3 mH. A 34 Ω resistive load is connected to the output of the CMI in parallel with the grid. Fig. 7 shows different parts of the experimental setup. The voltage of the grid is connected to an autotransformer whose output is connected to an isolation transformer. A circuit breaker is placed between the output of the isolation transformer and the output of the CMI to open or close the connection to the grid. The voltage of the grid is 113 v after the isolation transformer for case study 1 to 3. The behavior of the batteries is emulated using dSPACE MicroLabBox and EA power supply. To emulate the batteries, the following expression is evaluated to determine the voltage value of each dc supply [21], [22]

$$v_s = K_1 - K_2\frac{Q}{Q-q'}(\bar{i}_s + q') + Ge^{-Hq'} \tag{34}$$

where Q is the capacity of the emulated battery, q' is the consumed capacity, and $\bar{i}_s$ is the average cell current. Furthermore, K_1, K_2, G, and H are constant values which are determined based on the characteristics of the emulated battery. The value of the current for each cell is obtained by the current sensors and measurement boards. The consumed capacity of each cell in coulombs is calculated as follows:

$$q'(t) = \int_0^t i_s(t)dt \tag{35}$$

where $i_s(t)$ is instantaneous current of each cell. After evaluating (34) during the operation of the CHB, dSPACE MicroLabBox sends a command to set the value of the voltage in each dc power supply to emulate the characteristic of a battery. Table I shows the value of the constant used for the emulation of battery. The emulated batteries for all the cells are lithium-ion batteries.

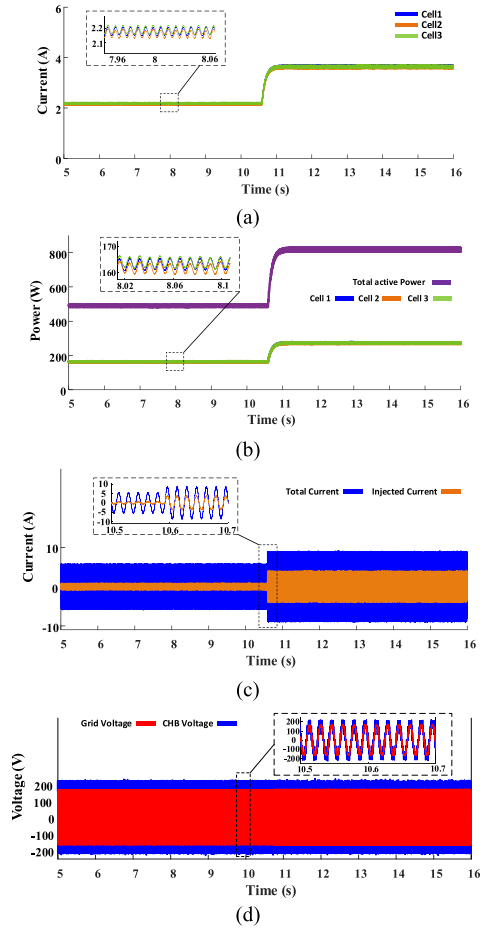

Fig. 8. Case study 1: Experimental result for step change of active power reference of 450 to 720 W. (a) Cell average input current. (b) Average input power of each cell and total average input power of CMI. (c) CMI total output current and injected current to the grid. (d) Grid voltage and the output voltage of the CMI before filter.

The experimental validation is conducted through four case studies which will be described in the following sections. The presented values in the first row of Table I are used for case study 1 to 3 and the presented values in the second row of Table is used for case study 4.

1) Case Study 1: In this case study, the ability of the controller for sharing equal power between the cells is examined via a step change in the controller reference value of the injected active power from 480 to 720 W which occurs at the time of 10.59 s. No reactive power is injected to the grid in this case study. Fig. 8(a) shows the waveforms of the average input current for each cell. As shown in Fig. 8, the average input currents of all the H-bridge cells are equal before and after the step change is applied. Fig. 8(b) shows the total average input power of the CMI and the average input power of each cell. As shown in this figure the total average input power of the system is equally shared between the H-bridge cells. Fig. 8(c) shows the CMI total average input current and the current which is injected to the grid. Due to the change of the reference power, the injected current to the grid increased at 10.59 s. Fig. 9 shows the output current harmonics spectrum after the output power reached 720 W. The

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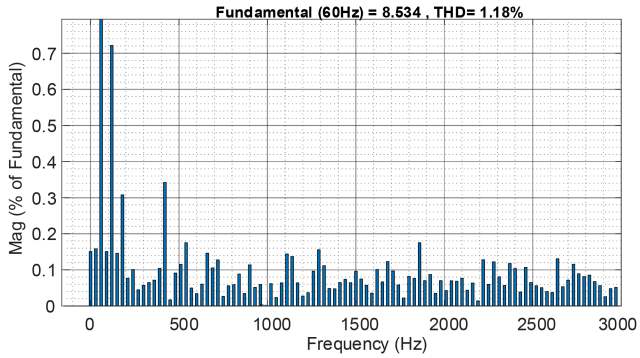

Fig. 9. Output current harmonic spectrum for case study 1 after output power reach 720 W.

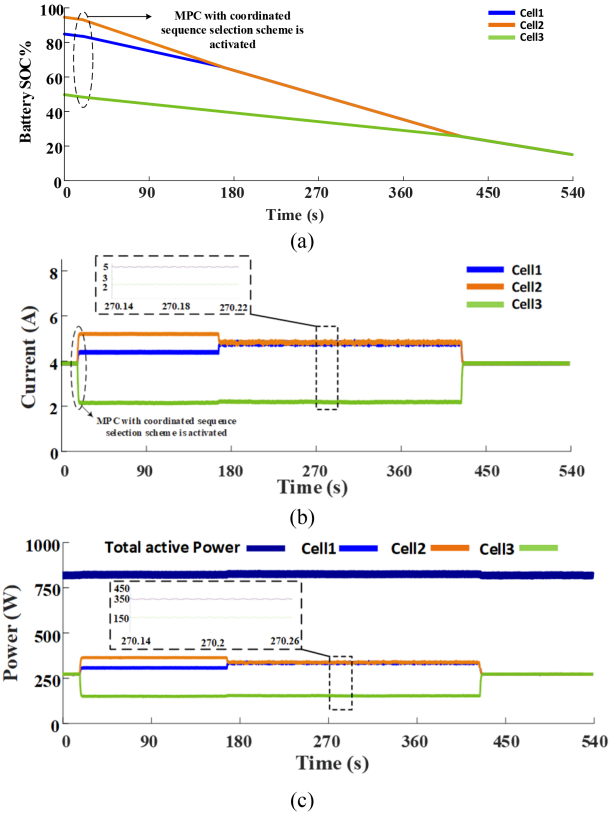

Fig. 10. Case study 2: Experimental result for unequal power sharing when all the SOCs are different, the proposed scheme is triggered at time $t = 20$ s. (a) SOC of the batteries. (b) Cell average input current. (c) Average input power of each cell and total average input power of CHB.

value of the total harmonic distortion for the output current is 1.18%. The percentage of each individual harmonic whose frequency is higher than 500 Hz is less than 0.18%. For other harmonics, the percentage of each harmonic is less than 0.72%.

2) Case Study 2: In this case study, the ability of the proposed controller to utilize the dc sources according to their SOC is examined. The SOC of the dc sources is different at the beginning. In this case study, the total active power output of the converter is 780 W and no reactive power is injected to the grid. The second cell has more SOC than the other sources and the SOC of the third cell is less than the other. Fig. 10(a) shows

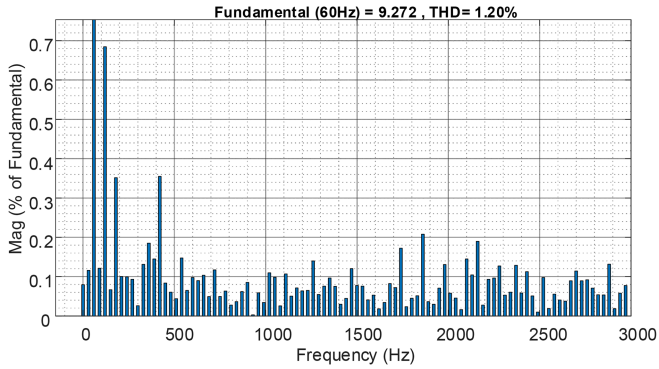

Fig. 11. Output current harmonic spectrum in case study 2 during the operation of the proposed scheme.

the SOC of the dc sources. At 20 s the proposed controller is activated. Fig. 10(b) and (c) show the average current and the average power drawn from each cell, respectively. The power drawn from cell 2 is more than that of cell one and cell three after the operation of the proposed scheme started. As shown in Fig. 10(c) the total power drawn from all the cells remains equal during the operation of the proposed scheme. After 146 s, when the SOC of cell one and cell two becomes equal, the proposed scheme draws equal power from cell one and cell two while the power drawn from cell three is lower. After 415 s, the SOC of all the supplies becomes equal and the proposed scheme shares the power between the cells equally. During the operation of the proposed scheme, the augmented sequence matrix is changed to accommodate the change of the SOC. As a result, for each situation of cell's SOC, the proposed scheme adopts a procedure to calculate the U_x, V_x, and SQ_x matrices to optimally utilize the dc sources. Fig. 11 shows the output current harmonics spectrum during the operation of the proposed scheme. The total harmonic distortion of the output current is 1.2%. The percentage of each individual harmonic whose frequency is higher than 500Hz is less than 0.22%. For other harmonics, the percentage of each harmonic is less than 0.7%.

3) Case Study 3: This case study studies the ability of the proposed controller to share the power between two cells when one of the cells fails to deliver power. In this situation, the proposed controller shares the power between the remaining cells according to their SOCs. The setpoint of active and reactive power in this case study is 630 W and 50 VAR in the beginning of the converter operation. Fig. 12(a) shows the SOC of the dc sources. Two of the dc sources share the same SOC and one of the dc sources has more SOC than the others. Fig. 12(b) and (c) show the average current and power drawn from each cell. After the activation of the proposed scheme, at 17 s, the power drawn from cell two and cell one become equal, and the power drawn from cell three is higher than that of equal cells. At 122 s, one of the batteries is disconnected due to a failure. As a result, the proposed control shares the power between the two dc remaining sources. The proposed control draws more power from cell three than cell one due to the higher SOC of the cell three. The value of active and reactive power after 122 s are 480 W and 50 VAR, respectively. After 323 s, the SOC of the two remaining dc

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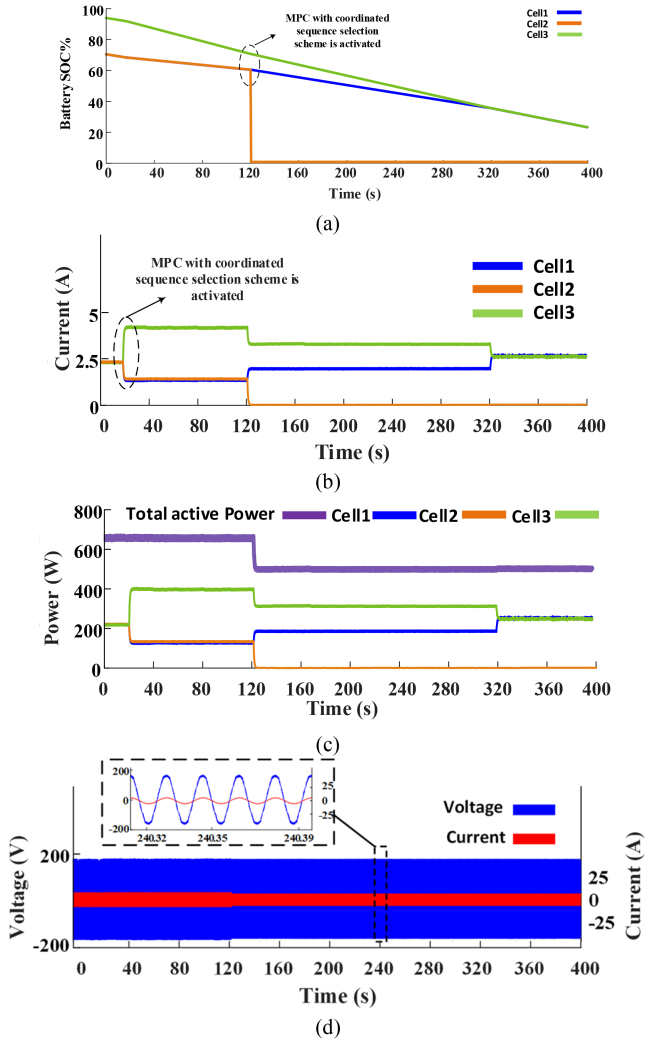

Fig. 12. Case study 3: Experimental result for unequal power sharing when two batteries have the same SOC and one of the batteries fails, the proposed scheme is triggered at time $t = 120$ s. (a) SOC of the batteries. (b) Cell average input current. (c) Average input power of each cell and total average input power of CHB. (d) Grid voltage and output current of the proposed scheme.

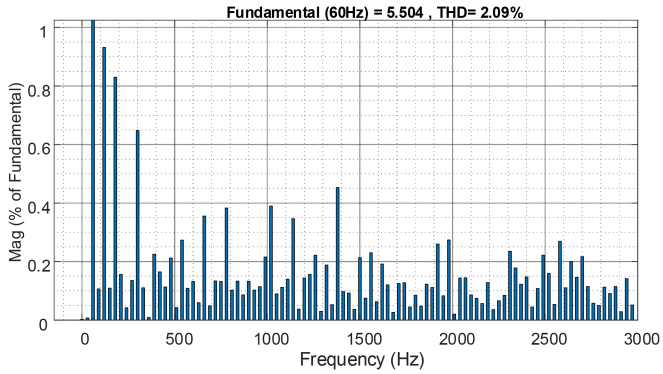

Fig. 13. Output current harmonic spectrum in case study 3 after battery failure.

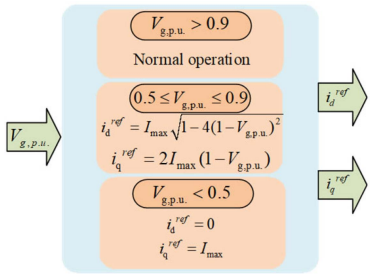

Fig. 14. Case study 4: Constant peak current operation diagram.

sources become equal. At this point, the proposed control shares the power equal between them. The optimal sequence selection via augmented sequence matrix can optimally utilize the dc sources with different situations. Fig. 12(d) shows the voltage of the grid and the output current of the converter. The output current of the converter lags the grid voltage due to the reactive power injection. Fig. 13 shows the output current harmonics spectrum when power is shared between two batteries by the proposed scheme. The total harmonic distortion of the output current is 2.09%. The percentage of each individual harmonic with higher than 11 order is less than 0.45%. For other harmonics orders, the percentage of each harmonic is less than 0.95%.

4) Case Study 4: In this case study, the ability of the controller to maintain optimal utilization of the dc sources during low voltage ride through (LVRT) is studied in which the output reactive and active power of the converter are changed according to the grid voltage. After a voltage sag in the grid, the inverter supports grid's voltage through the LVRT operation. During LVRT, the inverter injects reactive power to the grid to support the grid voltage. There are different methods to perform LVRT during the grid voltage drop such as constant active current, constant average active power, and constant peak current (CPC). In this article, CPC strategy is implemented to test the ability of the proposed algorithm to support the grid and maintain the coordinated sequence selection (i.e., Ω_1 to Ω_5). In CPC method, the controller changes the output active and reactive injected power in such a way that the LVRT operation keeps the peak of output current constant. Fig. 14 shows the calculation of the reference currents in dq frame in CPC mode. In this figure, $V_{g,p.u}$,$I_{\max}$ are per-united grid voltage with grid respect to nominal grid rms voltage, and maximum peak current during CPC mode [23]. For this case study, before the LVRT operation starts, the controller references for active and reactive output power are 600 W and zero, respectively. To test the LVRT operation, the point of common coupling (PCC) voltage of the CHB is being decreased to 0.9 p.u. by means of changing the output voltage of the autotransformer. Fig. 15(a) shows the input average current of each cell before, during and after CPC LVRT. Although the converter performs LVRT to support the grid side, the proposed scheme can share the power between the dc sources equally. At 17.76 s, the voltage starts to decrease. As the CPC operation starts when the voltage is less than 0.9 p.u., the controller increases the output current to keep the output power the same as the reference value. As shown in Fig. 15(b), during this period, due to the increase of the output current, the input average power of the CHB increases. At 20.45 s, the

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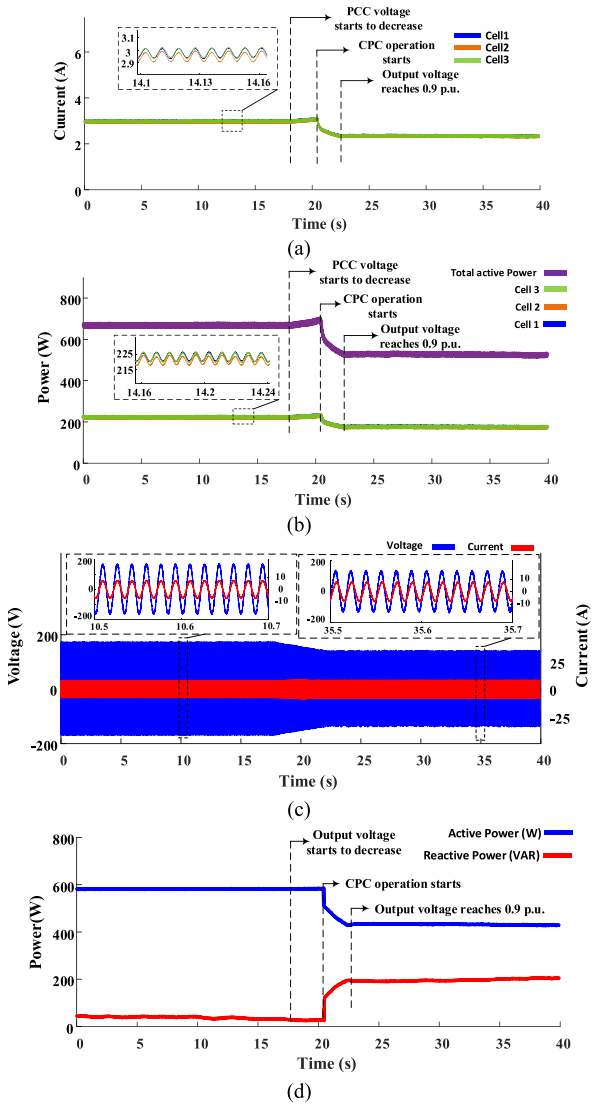

Fig. 15. Case study 4: Experimental result for coordinated sequence selection power sharing during LVRT. (a) Average input current of the batteries. (b) Average input power of the batteries. (c) PCC voltage and output current of the CHB. (d) Output average active and reactive power of CHB.

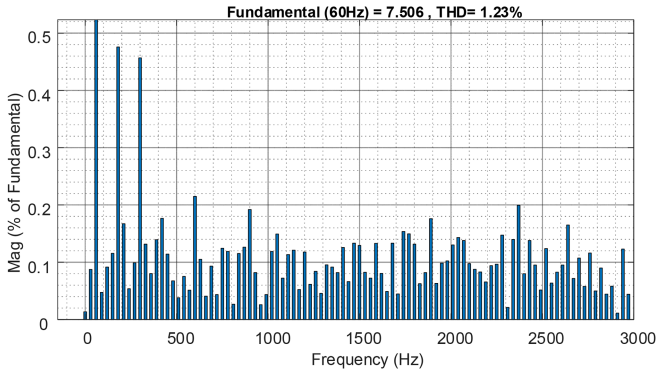

Fig. 16. Output current harmonic spectrum for case study 4 during LVRT.

PCC voltage goes below 0.9 p.u. of grid rms voltage. At this moment, the CPC mode starts to decrease the average output active power and injecting reactive power until the rms of PCC voltage reaches 0.9 p.u. as shown in Fig. 15(d). Fig. 15(c) shows the PCC voltage and the output current of the CHB for this case study. As shown in this figure, after the CPC, when the voltage reaches 0.9 p.u., the current lags the voltage due to the reactive power injection. As seen in Fig. 15(c), during LVRT, the CPC algorithm maintains the peak of CHB's output current constant. Fig. 13 shows the output current harmonics spectrum during LVRT using the proposed algorithm. The total harmonic distortion of the output current is 1.23%. The percentage of each individual harmonic with the frequency of lower than 1000 Hz is less than 0.48%. For other harmonics orders, the percentage of each harmonic is less than 0.48%.

VII. Comparison of the Proposed Scheme With Other Control Methods

In this section the proposed scheme is compared with the phase shifted PWM (PS-PWM) and finite set MPC. Fig. 17 shows the simulation results for the comparison which was conducted in MATLAB/Simulink. The number of dc sources in the CHB structure is three and the dc sources used for the comparison are 75 V lithium-ion batteries with 3 Ah of capacity. The output active and reactive power setpoint which is injected to the grid is 2 kW and zero respectively for all the control methods. Fig. 17(a) and (b) shows the average current of the cells and their SOCs for the proposed scheme. The SOC of the first cell is higher than the other cells, and the third cell has the lowest SOC among the cells. Before 480 s, the proposed scheme draws more current from the first cell and lowest current from the third cell. Between 480 and 510 s, because of equal SOC for second and third cells, the current drawn from cell one is more than cell two and three, while the current drawn from cells 2 and 3 are equal. After 510 s, the proposed control draws equal power from all the dc sources because the SOC of all the dc sources is the same. Fig. 17(c) and (d) shows the average current and SOC of the dc sources for the PS-PWM control method. The current which is drawn from the dc sources is equal in the PS-PWM regardless of the situation of the dc sources. Therefore, all the rate of change of SOC for all the dc sources are the same. Fig. 17(e) and (f) show the average current and SOC of the dc sources for the finite set MPC. In the finite set MPC, the switching array that minimizes the cost function is selected by the controller. As shown in Fig. 17(e) and (f), although the SOC of the first cell is more, the finite set MPC draws more power from the second cell. The time span during which all the dc sources operate with more than a critical limit, say, 10% of their SOC, is 560 s for the proposed scheme, 275s for the PS-PWM, and 366 s for finite set MPC. As a result, the proposed scheme can increase the safe operation time of the all the batteries. Because the operation of the BESS is restricted by healthy operation of all the all batteries in its structure, the proposed scheme can increase the time the BESS can deliver power to the grid.

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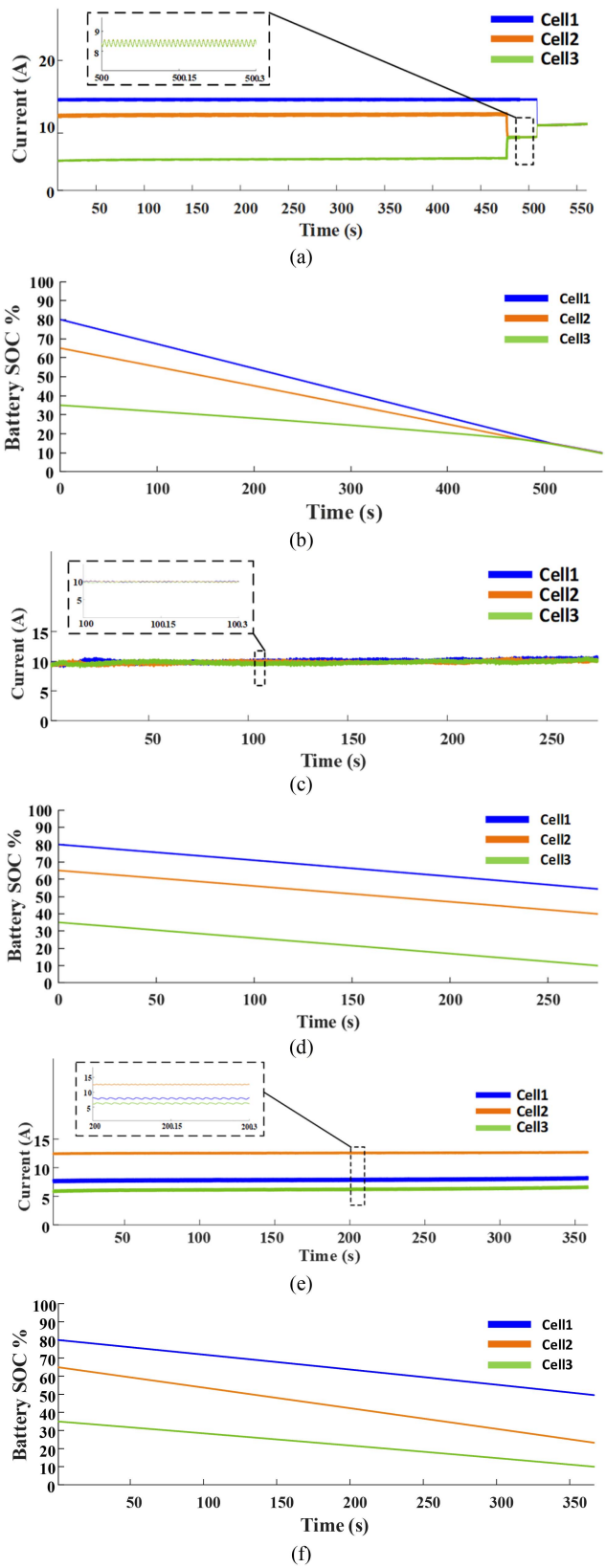

Fig. 17. Comparison of the proposed scheme with the other control methods. (a) Average current drawn from each dc sources.(b) SOC of the dc sources during the operation of the proposed scheme. (c) Average current.(d) SOC of each DC sources for PS-PWM. (e) Average current. (f) SOC of the dc sources using finite set MPC.

VIII. Conclusion

In conclusion, this article proposes a new MPC scheme embedded with a coordinated sequence selection for optimal utilization of the dc sources in grid interactive CHBs. The proposed scheme modifies the switching arrays selection by the MPC cost function in each sampling time in comparison to conventional MPC schemes that determines the switching arrays by directly optimizing the cost function. This approach was based on the developed coordinated sequence selection of battery cells in horizon of time that leads to optimal utilization of battery sources. Thus, the proposed scheme addresses two main challenges for battery sources interfaced CHB: deriving specific procedure to address different situations of SOCs individually that was implemented by categorizing the dc sources according to their SOC and augmented sequence matrix and improved MPC scheme that considers the dc-sources status for switching array selection which realizes a control scheme without tuning requirement and complex modulation schemes while maintaining optimal utilization of battery sources or generally other dc-sources in broader range of applications. To validate the proposed scheme, extensive experimental case studies were conducted that demonstrate the practicality as well as impact of the proposed controller for optimal utilization of BESS and grid-integration. The comparison of the computational burden and required memory of the proposed topology and finite set PWM shows lower required resources for implementing the proposed scheme. The impact of the proposed topology on the SOC of the dc sources was compared to the finite-set MPC and phase shifted PWM, respectively, to show the merit of the proposed topology to prolong the operation of the converter and batteries within the safe area was presented. Furthermore, the harmonic spectrum and THD of the output current complies with tables 26 and 27 of IEEE 1547-2018 standard that shows low harmonic content of the proposed topology.

Acknowledgment

The statements made herein are solely the responsibility of the authors.

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