Multithreaded State Controller for Grid-Connected Converter With Imposed Limits

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Abstract—**This article proposes an innovative approach to control a grid-connected converter. The method combines the versatility and high-quality control offered by the state-feedback controllers for linear plants with the ease of imposing limits on the controlled variables offered by the cascaded control systems. The method is groundbreaking in its ability to bridge the gap between the elegance of the full-state-feedback control structure and its lack of popularity among power electronics engineers and possibly also other groups of practitioners. A multithreaded state controller is proposed in the form of three state controllers: one to control grid currents and dc-link voltage if limits of the currents are not reached, and two state controllers that are put into the closed loop if one of the current limits is reached. A complete design procedure is proposed, including the selection of all gains present in the three state-feedback controllers using the pole placement method. An algorithm of soft switching between the three control signals is also developed. Sharing the desired dynamics between the threads is fulfilled thanks to the eigenstructure assignment introduced to overcome the problem of multiple solutions by choosing the most orthogonal eigenvectors. The proposed control system is then verified in a simulation, and its high practicality is demonstrated experimentally.**

Index Terms—**Current constraints, full state feedback (FSF), grid converter, multithreaded state controller (MTSC), state feedback control.**

I. INTRODUCTION

STATE-FEEDBACK controllers (SFCs) are one of the most widely used groups of advanced control structures for grid-connected converters [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. These control structures, also called full state feedback (FSF), allow a very good control quality [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. However, in most systems, an SFC does not encompass all the control tasks that have to be performed by the grid converter control system. The state-feedback concept is usually applied only to the grid current control, without the primary process of dc voltage control [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. This article deals with a problem that is the main reason for that state of affairs and proposes an innovative method of control that cope with the challenges arising when dc voltage control is included in the SFC scope of operation.

Fig. 1 shows a concept comparison of control systems implemented in a rotating reference frame for grid-connected converters [see Fig. 1(a)]. Fig. 1(b) presents the cascade control structure [19], [20], [21], [22], [23], [24].

The main advantage of such a solution is a possibility of limiting the set value of the grid current components. Since the value of i_q^{ref} is known at all times, imposing the current limitation comes down to imposing restrictions on the i_d^{ref} signal. Fig. 1(c) illustrates the concept with a state-feedback current controller (SFCC) and a voltage controller in the outer control loop [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. This concept assumes a simplified description of the object excluding v_{dc} as the state variable, at the stage of designing the SFCC. Similarly to the circuit presented in Fig. 1(b), this solution allows imposing of constraints through a limitation on the output signal of the voltage controller. On the other hand, Fig. 1(d) presents the control system with the state feedback, where the reference signals correspond to dc voltage v_{dc} and current component i_q [25], [26], [27], [28]. This control structure has good control properties, but it does not allow the direct imposition of the current limitations through d-axis current set point due to the lack of such a signal in the control structure. The proposed name, a state-feedback voltage controller (SFVC), is conventional and refers to the primary purpose of control, which is to maintain the desired dc voltage at the converter output. In fact, the system with an SFVC has a second reference signal, which determines the desired current component in the q-axis.

The innovative multithreaded state controller (MTSC), whose concept was first presented in [29], allows taking advantage of an FSF with a current limiting method that is simple to implement.
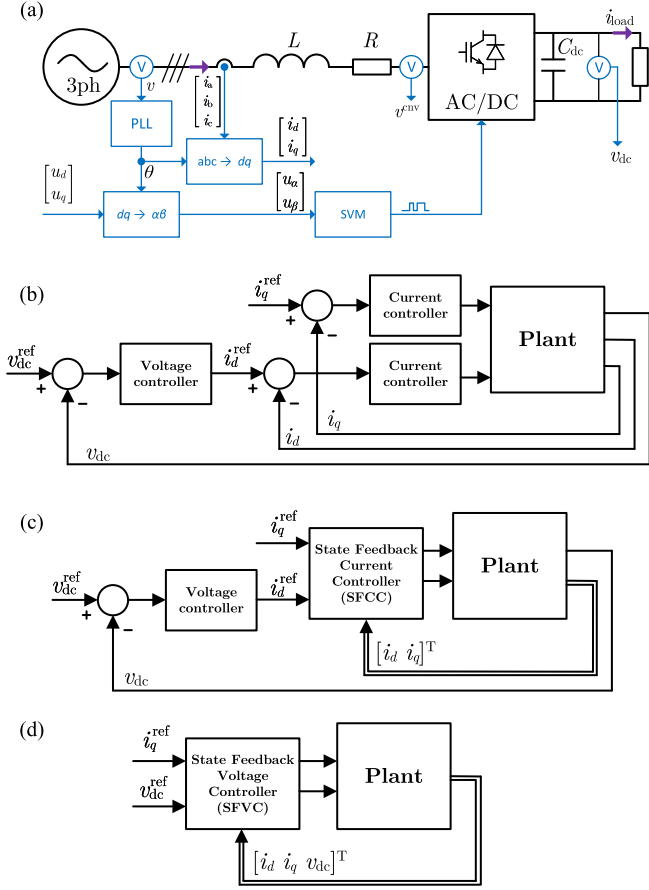
Fig. 1. Simplified block diagrams of the control structure for the grid converter. (a) Schematic diagram of the plant. (b) Cascade output feedback control. (c) Cascade control with the SFCC. (d) SFVC.

The idea is to use different structures of the state controller, depending on the control mode. The concept of two parallel operating SFCs was previously used only for a doubly fed induction generator to synchronize the system in the transition between stand-alone and grid operation [30]. That solution was used to change the control structure depending on the plant configuration. The MTSC extends this idea by the cooperation of parallel control threads to ensure the right timing of transition between particular control modes.

The research presented in [29] elaborates on methods for imposing limits on state variables. Plant augmentation according to the internal model principle to get zero steady-state error for constant references and disturbances is discussed there. A complete design procedure, including analytical gain tuning and deriving the back-calculation formula to enable soft switching between the threads of the controller, is presented as well. The research also includes a numerical comparison between the cascade control system and the state-feedback control system as well as results for a hardware-in-the-loop simulation of the converter-fed dc machine.

This article presents an innovative implementation of the MTSC for a grid converter and presents the full experiment results for any MTSC application. Section II introduces a multithreaded SFC for a grid-connected converter. A distinguishing
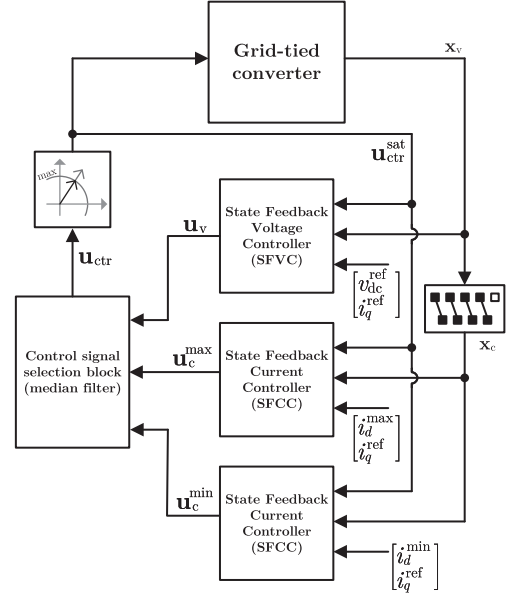

Fig. 2. Block diagram of the MTSC for a grid converter.

feature of the presented structure, compared to the most popular approaches using SFC [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], is the control of dc-link voltage and grid currents with the use of a parallel structure. The controller design procedure is described in Section III. The design includes controller tuning with the use of the eigenstructure assignment theorem—this is to address the nonuniqueness of the eigenvalue assignment using state-feedback control for linear time-invariant multi-input multi-output systems. The simulation and experimental results in a physical 10-kVA grid-connected converter are presented in Sections IV and V, respectively. Finally, Section VI concludes this article.

II. MULTITHREADED STATE CONTROLLER

The idea of the MTSC for the grid converter is presented in Fig. 2. It uses three control threads with state feedback. The main control thread is the state-feedback control loop for dc voltage v_{dc} control (SFVC). The other two control threads are the grid current control loops (SFCC). Reference signals i_d^{max} and i_d^{min} for the SFCCs indicate the maximum and minimum values of the d-axis current component, respectively.

At each step of the algorithm, all the control threads are calculated. When the control signals have been determined in each of the three threads, the signal selector chooses a signal passed as an input to the plant. The SFVC is considered as the main thread because it fulfills the primary purpose of the control, which is the control of v_{dc}, and if the system does not enter the operation region where the current or control signal should be limited, the control signal applied to the object is equal to $\mathbf{u_v}$, the output of SFVC. The operation scheme of signal selection consists in comparing the lengths of vectors $\mathbf{u_v}$, $\mathbf{u_c^{min}}$, and $\mathbf{u_c^{max}}$ and choosing the middle value. Considering the negative plant gain—which will be described in the next section—between the inputs and outputs of i_d and i_q, in the case
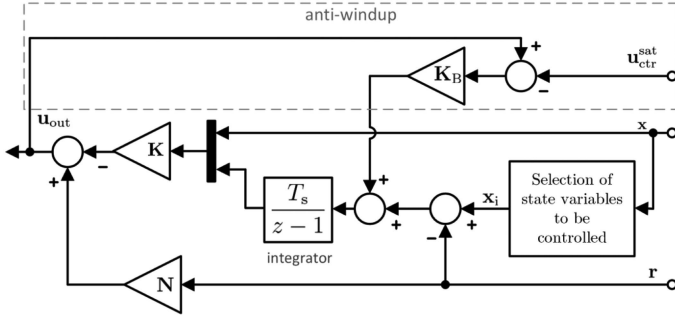
Fig. 3. Interior diagram of the SFC blocks in Fig. 2.

TABLE I
GRID CONVERTER PARAMETERS

Parameter	Symbol	Value
Nominal line-to-line grid voltage	$V_{\mathrm{g}}^{\mathrm{nom}}$	400 V RMS
Nominal dc voltage	$V_{\mathrm{dc}}^{\mathrm{nom}}$	700 V
DC–link capacity	C_{dc}	750 µF
Nominal load current	$I_{\mathrm{load}}^{\mathrm{nom}}$	15 A RMS
Nominal grid current	I_{nom}	15.2 A RMS
Maximum grid current amplitude	I_{max}	25 A
Nominal pulsatance of the input voltage	ω	$100\,\pi/\mathrm{s}$
Input filter inductance	L	2.2 mH
Input filter resistance	R	0.2 Ω
Switching frequency	f_{sw}	10 kHz
Sampling time	T_{s}	100 µs

of $\mathbf{u_c^{min}} > \mathbf{u_v} > \mathbf{u_c^{max}}$, the circuit transitions to the operating points where $i_d^{\min} < i_d < i_d^{\max}$. Since the linear operating range of the converter is considered, it is known from the superposition principle that in situations where $\mathbf{u_c^{max}} > \mathbf{u_v}$, the SFVC tends to force i_d values greater than the current controller with a reference equal to the upper threshold value. The same rule is true for $\mathbf{u_v} > \mathbf{u_c^{min}}$ and the lower threshold value. Therefore, the choice of the median value of $[\mathbf{u_c^{min}}, \mathbf{u_v}, \mathbf{u_c^{max}}]$ as a control signal allows the implementation of current limitations in the grid converter system. Owing to the limited range of grid converter output voltages at a given dc voltage, the value of the control signal is limited to the linear operating range of the modulator [31]. The SFCs whose outputs are not selected at a given time as the plant control signal operate in an open loop. It means that the loop is broken in the selection or the saturation block. No more than one SFC selected by means of the median filter operates in a closed loop.

The structure of SFCs [32] is presented in Fig. 3. To ensure zero steady-state error at constant disturbance condition, integral terms of control errors are incorporated to the control structure. This, in turn, requires an antiwindup mechanism for integral terms to provide expected control performance. The antiwindup aims to adjust the state of integrators in an open-loop operation of a given SFC. The problem of adjusting augmented states in state-feedback control structures at the transition between two control modes is also addressed in [30]. However, the concept, presented there, of using an additional controller to match control signals of different controller types cannot be applied to the MTSC. This is because such a mechanism does not allow the selection of control modes based on control signal as the control signal selection block (CSSB) does. In [29], it has been demonstrated that the back-calculation loop with a gain $\mathbf{K_b} = \mathbf{N^{-1}}$ keeps the integrator state at the desired level and provides the desired response of the system when a transition between open- and closed-loop operations of the given controller takes place.

III. CONTROLLER DESIGN

The design of an MTSC comes down to designing the state-feedback gains $\mathbf{K_c}$ and $\mathbf{K_v}$ and feedforward gains $\mathbf{N_c}$ and $\mathbf{N_v}$ for current and voltage SFCs. This section provides all the steps of the design and selection of control structure parameters. The presented numerical results are provided for the grid converter system characterized by parameters listed in Table I. For the purpose of designing SFCs, the linearized plant model at the

nominal operation point is considered. In the continuous time domain, the grid converter system is described by the following state-space equations:

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) + \mathbf{E}\mathbf{z}(t) \\ \mathbf{y}(t) = \mathbf{x}(t) \end{cases} \tag{1}$$

$$\mathbf{A} = \begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ -\omega & -\frac{R}{L} & 0 \\ \frac{3V_{\mathrm{g}}^{\mathrm{nom}}}{2C_{\mathrm{dc}}V_{\mathrm{dc}}^{\mathrm{nom}}} & \frac{3\sqrt{2}\omega L I_{\mathrm{nom}}}{2C_{\mathrm{dc}}V_{\mathrm{dc}}^{\mathrm{nom}}} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \\ \frac{3\sqrt{2}I_{\mathrm{nom}}}{2C_{\mathrm{dc}}V_{\mathrm{dc}}^{\mathrm{nom}}} & 0 \end{bmatrix},$$

$$\mathbf{E} = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{C_{\mathrm{dc}}} \end{bmatrix}, \mathbf{x} = \begin{bmatrix} i_d \\ i_q \\ v_{\mathrm{dc}} \end{bmatrix}, \mathbf{u} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} \mathbf{z} = \begin{bmatrix} v_d \\ v_q \\ i_{\mathrm{load}} \end{bmatrix},$$

where $\mathbf{A}$ is the state matrix, $\mathbf{B}$ is the control matrix, $\mathbf{E}$ is the disturbance matrix, $\mathbf{x}$ is the state vector, $\mathbf{u}$ is the control vector, and $\mathbf{z}$ is the disturbance vector.

A. Current SFC

To design the SFCC, a discretized and simplified model of the plant, including only two state variables i_d and i_q, is taken into consideration. It is described in the discrete time domain as follows:

$$\begin{cases} \mathbf{x_1}(k+1) = \mathbf{F_1}\mathbf{x_1}(k) + \mathbf{G_1}\mathbf{u}(k) + \mathbf{E_1}\mathbf{z_1}(k) \\ \mathbf{y_1}(k) = \mathbf{x_1}(k) \end{cases} \tag{2}$$

where $\mathbf{x_1} = [i_d \quad i_q]^{\mathrm{T}}$ and $\mathbf{z_1} = [v_d \quad v_q]^{\mathrm{T}}$.

The discretization is done based on the zero-order hold (ZOH) method (i.e., match to the step response) according to the following relations:

$$\mathbf{F_1} = e^{\mathbf{A}[\mathbf{1:2,1:2}]T_{\mathrm{s}}}$$

$$[\mathbf{G_1} \quad \mathbf{E_1}] = \mathbf{A}[\mathbf{1:2,1:2}]^{-1}(e^{\mathbf{A}[\mathbf{1:2,1:2}]T_{\mathrm{s}}}$$
$$- \mathbf{I}_{2\times2})[\mathbf{B}[\mathbf{1:2,:}] \quad \mathbf{E}[\mathbf{1:2,:}]]. \tag{3}$$

In order to provide zero steady-state tracking errors $e_d = i_d - i_d^{\mathrm{ref}}$ and $e_q = i_q - i_q^{\mathrm{ref}}$ for constant reference and disturbance signals, the control structure includes integrators (see Fig. 3), which results in plant augmentation by two states p_d
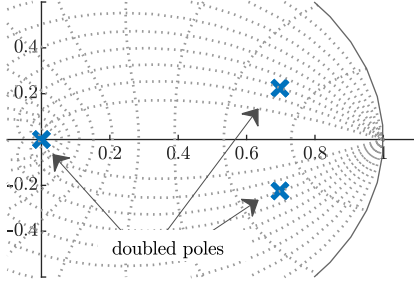
Fig. 4. Closed-loop poles for the current SFC.

and p_q [3], [4], [27]. Additional two state variables representing the output voltage of the converters u_d^{cnv} and u_q^{cnv} are included in the state vector when the unit delay resulting from the digital controller operation is considered in the plan description [6], [10]. Thus, the subsequent plant model used for the design is as follows:

$$\begin{cases} \mathbf{x_c}(k+1) = \mathbf{F_c}\mathbf{x_c}(k) + \mathbf{G_c}\mathbf{u}(k) + \mathbf{E_c}\mathbf{z_c}(k) \\ \mathbf{y_c}(k) = \mathbf{x_c}(k) \end{cases} \tag{4}$$

where $\mathbf{F_c} = \begin{bmatrix} \mathbf{F_1} & \mathbf{0} & \mathbf{G_1} \\ \mathbf{I_{2\times2}}T_s & \mathbf{I_{2\times2}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}$, $\mathbf{G_c} = \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{I_{2\times2}} \end{bmatrix}$,

$\mathbf{E_c} = \begin{bmatrix} \mathbf{E_1} & \mathbf{0} \\ \mathbf{0} & \mathbf{I}T_s \\ \mathbf{0} & \mathbf{0} \end{bmatrix}$, $\mathbf{x_c} = \begin{bmatrix} i_d & i_q & p_d & p_q & u_d^{cnv} & u_q^{cnv} \end{bmatrix}^T$,

and

$\mathbf{z_c} = \begin{bmatrix} v_d & v_q & i_d^{ref} & i_q^{ref} \end{bmatrix}^T$.

The feedback gain $\mathbf{K_c}$ is calculated using the pole placement method. There are six desired closed-loop pole locations on the z plane to be defined. Two of the open-loop poles that are introduced by state variables u_d^{cnv} and u_q^{cnv} are already in the preferred position. They are in the origin and represent the unit delay. The next two pairs of closed-loop poles are dominant and determine the response of the control system. Initially, the location of the poles is set in the s plane. The closed-loop bandwidth is chosen at $\omega_{cur} = 2\pi f_{cur}$ ($f_{cur} = 700$ Hz) and the damping ratio $\zeta = \frac{\sqrt{2}}{2}$, which is a typical tradeoff between the speed of the response and the accompanying overshoot for current control systems

$$p_{s1} = -\zeta\omega_{cur} + \omega_{cur}\sqrt{\zeta^2 - 1}$$
$$p_{s2}; = -\zeta\omega_{cur} - \omega_{cur}\sqrt{\zeta^2 - 1}. \tag{5}$$

Afterward, z plane poles are calculated by using the definition of z as follows:

$$p_{z1} = e^{p_{s1}T_s}$$
$$p_{z2} = e^{p_{s2}T_s}. \tag{6}$$

Assuming the same dynamic for i_d and i_q, the desired closed-loop poles (see Fig. 4) are as follows:

$$p_{cur}^{CL} = \begin{bmatrix} 0 & 0 & p_{z1} & p_{z2} & p_{z1} & p_{z2} \end{bmatrix}.$$

The reference input matrix $\mathbf{N_c}$ is defined as follows:

$$\mathbf{N_c} = \mathbf{K_c}[1:2, 3:4]T_s \tag{7}$$

which results in placing the zeros introduced by the reference feedforward in the z plane origin. This compensates the poles placed there.

The response of the current controller is presented in Fig. 5. In accordance with the selected damping ratio for a step reference signal, the system responds with an overshoot of approximately 4%. The results also demonstrate good disturbance rejection properties of the controller, which is noticeable at time 10 and 25 ms when a grid voltage step change of 25 V occurs.

B. Voltage SFC

To design the discrete voltage SFC, a discrete form of the plant [see (2)] is used

$$\begin{cases} \mathbf{x}(k+1) = \mathbf{F_2}\mathbf{x}(k) + \mathbf{G_2}\mathbf{u}(k) + \mathbf{E_2}\mathbf{z}(k) \\ \mathbf{y}(k) = \mathbf{x}(k) \end{cases} \tag{8}$$

where $\mathbf{F_2}$, $\mathbf{G_2}$, and $\mathbf{E_2}$ come from ZOH equivalent discretization

$$\mathbf{F_2} = e^{\mathbf{A}T_s}$$
$$[\mathbf{G_2} \quad \mathbf{E_2}] = \mathbf{A}^{-1}(e^{\mathbf{A}T_s} - \mathbf{I_{3\times3}})[\mathbf{B} \quad \mathbf{E}]. \tag{9}$$

Similarly to the steps performed for the current controller in Section III-A, the plant is augmented by states u_d^{cnv} and u_q^{cnv} and integral of control error p_v and p_q, respectively, for the control of v_{dc} i_q. The plant in this design stage is formulated as follows:

$$\begin{cases} \mathbf{x_v}(k+1) = \mathbf{F_v}\mathbf{x_v}(k) + \mathbf{G_v}\mathbf{u}(k) + \mathbf{E_v}\mathbf{z_v}(k) \\ \mathbf{y_v}(k) = \mathbf{x_v}(k) \end{cases} \tag{10}$$

where $\mathbf{F_v} = \begin{bmatrix} \mathbf{F_2} & \mathbf{0} & \mathbf{G_2} \\ \begin{smallmatrix} 0 & 0 & T_s \\ 0 & T_s & 0 \end{smallmatrix} & \mathbf{I_{2\times2}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}$, $\mathbf{G_c} = \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{I_{2\times2}} \end{bmatrix}$,

$\mathbf{E_v} = \begin{bmatrix} \mathbf{E_2} & \mathbf{0} \\ \mathbf{0} & \mathbf{I}T_s \\ \mathbf{0} & \mathbf{0} \end{bmatrix}$, $\mathbf{x_v} = \begin{bmatrix} i_d & i_q & v_{dc} & p_d & p_q & u_d^{cnv} & u_q^{cnv} \end{bmatrix}^T$,

and $\mathbf{z_v} = \begin{bmatrix} v_d & v_q & i_{load} & i_d^{ref} & i_q^{ref} \end{bmatrix}^T$.

This SFC requires seven closed-loop pole locations to be defined. It should be pointed out here that the final goal is to use the voltage state controller as a part of the MTSC; thus, the freedom of selection of pole location is limited. In other words, the dynamics of SFVC must be associated with the dynamics of the SFCC. Two poles are placed in the z plane origin for the previously mentioned reason. The same dynamics of i_q control for both the voltage and current SFCs is expected to be achieved, and this is why two poles, p_{z1} and p_{z2}, of the closed-loop system are placed in the same location as the current controller poles (see Fig. 6). The last three pole locations are selected to achieve a desired control performance of i_d and v_{dc} states. One less dominant pole is placed on the real axis at the
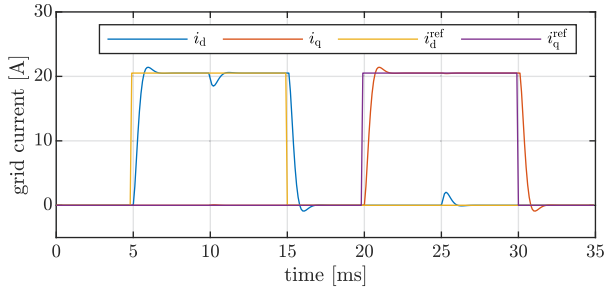
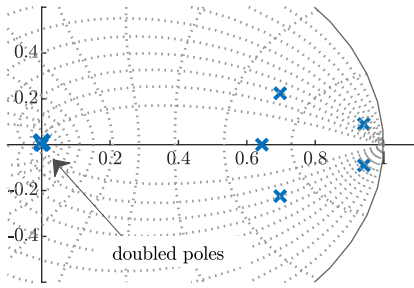Fig. 5. Numerical results showing the theoretical performance of the designed SFCC.

Fig. 6. Closed-loop poles for voltage SFC.

point corresponding to the ω_{cur} frequency. This set of conditions should be met to ensure that the control signal selection block adequately switches between the operation modes. Moving this pole to the right side reduces dynamics and causes belated transition to the current control mode when a current saturation is needed. On the other hand, moving toward the origin might cause unnecessary transients to the current control mode and reduce the robustness of the system. The last two dominant poles p_{z4} and p_{z5} are selected as z plane equivalent to s plane poles p_{s3} and p_{s4}

$$p_{z4} = e^{p_{s4}T_{\mathrm{s}}}$$

$$p_{z5} = e^{p_{s5}T_{\mathrm{s}}} \qquad (11)$$

where p_{s3} and p_{s4} correspond to the natural frequency $\omega_{\mathrm{vol}} = 0.25\omega_{\mathrm{cur}}$ and damping ratio $\zeta_{\mathrm{vol}} = 0.5$. That gives us the set of closed-loop poles (see Fig. 6) as follows:

$$p_{\mathrm{vol}}^{\mathrm{CL}} = \begin{bmatrix} 0 & 0 & p_{z1} & p_{z2} & p_{z3} & p_{z4} & p_{z5} \end{bmatrix}.$$

Having selected the poles of a closed system, it should be pointed out that for the multi-input plant, as analyzed here, there are many solutions for feedback gains, which allow obtaining the desired position of the poles. These possible solutions are not equivalent [33], [34]. For an object with a large difference in dynamics between d-axis and q-axis, the `place` command in MATLAB does not ensure getting the expected dynamics for specific outputs. To be more specific, there is a possibility that in the closed-loop system with poles $p_{\mathrm{vol}}^{\mathrm{CL}}$, the control dynamic for i_q will be affected not only by 0, p_{z1}, and p_{z2} poles but also by some or all of the remaining poles p_{z3}, p_{z4}, and p_{z5}, which would be undesired. Therefore, the eigenstructure assignment

theorem is applied to design the feedback matrix [35], [36], [37].

C. Eigenstructure Assignment

Let us denote the eigenvalue of closed-loop state matrix $[\mathbf{F_v} - \mathbf{G_v}\mathbf{K_v}]$ by $\lambda_i = p_{\mathrm{vol}}^{\mathrm{CL}}[i]$ and eigenvector associated with λ_i by $\mathbf{v}_i$, where $i = 1\ldots7$. Then, there exists the following equation:

$$(\lambda_i\mathbf{I} - \mathbf{F_v} + \mathbf{G_v}\mathbf{K_v})\mathbf{v}_i = \mathbf{0}. \qquad (12)$$

Set a matrix $\mathbf{S}_i$ associate with each λ_i

$$\mathbf{S}_i = \begin{bmatrix} \lambda_i\mathbf{I} - \mathbf{F_v} & \mathbf{G_v} \end{bmatrix} \qquad (13)$$

and a compatibly partitioned matrix

$$\mathbf{P}_i = \begin{bmatrix} \mathbf{L}_i \\ \mathbf{M}_i \end{bmatrix} \qquad (14)$$

whose columns form a basis for the kernel of $\mathbf{S}_i$.

Equation (12) can be formulated using partition matrix as

$$\begin{bmatrix} \lambda_i - \mathbf{F_v} & \mathbf{G_v} \end{bmatrix} \begin{bmatrix} \mathbf{v}_i \\ \mathbf{K_v}\mathbf{v}_i \end{bmatrix} = \mathbf{0}. \qquad (15)$$

Since columns of $\mathbf{P}_i$ constitute a basis for the kernel of $\mathbf{S}_i$, it means that $\mathbf{v}_i \in \mathrm{span}\{\mathbf{L}_i\}$; thus, $\mathbf{v}_i$ can be expressed as $\mathbf{v}_i = \mathbf{L}_i\mathbf{k}_i$ for some vectors $\mathbf{k}_i \in \mathbb{C}^2$. For $\mathbf{M}_i\mathbf{k}_i = \mathbf{K_v}\mathbf{v}_i$, the relation in (12) is satisfied. In [35], it is proved that the feedback matrix can be constructed based on the following equation:

$$\mathbf{K_v}\begin{bmatrix} \mathbf{v}_1 & \mathbf{v}_2 & \ldots & \mathbf{v}_7 \end{bmatrix} = \begin{bmatrix} \mathbf{w}_1 & \mathbf{w}_2 & \ldots & \mathbf{w}_7 \end{bmatrix} \qquad (16)$$

where $\mathbf{w}_i = \mathbf{M}_i\mathbf{k}_i$.

If all the eigenvalues are real numbers, $\mathbf{K_v}$ is calculated directly from

$$\mathbf{K_v} = \begin{bmatrix} \mathbf{w}_1 & \mathbf{w}_2 & \ldots & \mathbf{w}_7 \end{bmatrix}\begin{bmatrix} \mathbf{v}_1 & \mathbf{v}_2 & \ldots & \mathbf{v}_7 \end{bmatrix}^{-1}. \qquad (17)$$

For complex eigenvalues, some minor adjustments must be calculated to ensure that the feedback matrix contains only real numbers [35]. In the case of a pair of conjugate eigenvalues $\lambda_i = \lambda_{i+1}^*$, we have $\mathbf{v}_i = \mathbf{v}_{i\Re} + j\mathbf{v}_{i\Im} = \mathbf{v}_{i+1}^*$ and $\mathbf{w}_i = \mathbf{w}_{i\Re} + j\mathbf{w}_{i\Im} = \mathbf{w}_{i+1}^*$. Then, in (17), $\mathbf{v}_i$ and $\mathbf{v}_{i+1}$ are replaced by $\mathbf{v}_{i\Re}$ and $\mathbf{v}_{i\Im}$, respectively. The same rule is applied to the pairs of vectors $\mathbf{w}_i$, $\mathbf{w}_{i+1}$ and $\mathbf{w}_{i\Re}$, $\mathbf{w}_{i\Im}$.

For the two analyzed input systems, there are two independent solution vectors $\mathbf{v}_i$, which belong to the kernel of $\mathbf{S}_i$, and two corresponding vectors $\mathbf{w}_i$. Therefore, for a given set of closed-loop poles $p_{\mathrm{vol}}^{\mathrm{CL}}$, there is no uniquely defined $\mathbf{K_v}$. The designer has the freedom of selecting one of the possible closed-loop eigenvector sets. In the analyzed system with two inputs and seven state variables, there is $2^7 = 128$ possible combinations of eigenvector set. Because there is a need to minimize the interaction between state variables, in other words, to make the dynamics of i_q independent of the most dominant closed-loop poles, the designer should select the set with the most orthogonal eigenvectors. This set can be easily numerically found by searching the minimum value of eigenvector dot product for all the possible sets.
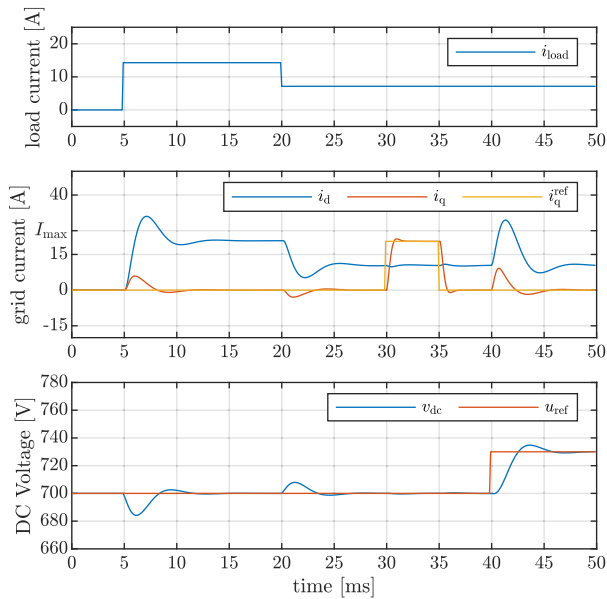
Fig. 7. Numerical results showing the theoretical performance of the designed SFVC.

TABLE II
STABILITY MARGIN VARIATION

Input resistance	Input inductance		
	80 % L	L	120 % L
80 % R	5.69 dB, 5.63 dB	7.88 dB, 7.59 dB	8.53 dB, 5.45 dB
	35.1°, 34.8°	46.0°, 44.7°	48.9°, 33.8°
R	5.71 dB, 5.64 dB	7.92 dB, 7.68 dB	8.58 dB, 5.52 dB
	35.2°, 34.8°	46.2°, 44.1°	49.2°, 34.2°
120 % R	5.72 dB, 5.65 dB	7.96 dB, 7.77 dB	8.64 dB, 5.60 dB
	35.3°, 34.9°	46.4°, 44.5°	48.4°, 34.6°

Next, after calculating $\mathbf{K_v}$ from (17), using zero-pole compensation at the z plane origin, $\mathbf{N_v}$ is defined as follows:

$$\mathbf{N_v} = \mathbf{K_v}[1:2, 4:5]T_s. \qquad (18)$$

D. Voltage Controller Dynamic

The performance of the designed voltage controller is presented in Fig. 7. In the period from 5 to 15 ms, there is a pulse of load current. At the v_{dc} plot, we can observe the desired disturbance rejection properties. The system has the same dynamic as current controller in terms of i_q control, which is shown at step changes of i_q^{ref} in 20 and 25 ms. The compliance with the assumed controller bandwidth is also visible at the reference step response in time instance 30 ms. The consequences of the demand for such high dynamics are large instantaneous values of current in transient states (7 and 42 ms). Because the peak current exceeds the I_{max} value, this provides a strong justification for applying the multithreaded control concept.

IV. SIMULATION RESULTS OF MTSC FOR DISCRETE LINEAR PLANT

The MTSC for the grid-connected converter (see Fig. 2) has been verified in a simulation study. The results are provided in Fig. 8. The ability of the system to correctly impose the limits on the current component i_d and the control signal has been presented for the test scenario, which includes the following:
1) step changes of load current i_{load} (at time 5, 40, 75, and 90 ms);
2) a grid voltage sag in the period from 20 to 35 ms;
3) step changes of i_q^{ref} at time 50 and 65 ms.

In Fig. 8, the operation mode of the converter is presented. In time marked with blue color, the controller is in the voltage control mode. It means that the control signal applied to the plant is the signal produced by the SFVC $\mathbf{u_v}$. This happens for the majority of the system operation time. However, in the transient states, the mode might be changed to impose the predefined constraints. The intervals marked with red color correspond to the current control mode. This means the realization of the current saturation for the grid converter. The control signal applied to the plant comes from one of SFCCs and is either $\mathbf{u_c^{min}}$ or $\mathbf{u_c^{max}}$, depending on whether the lower or upper current threshold is reached. In time intervals marked with yellow color, the system goes into the control signal saturation mode. This result shows that the final dynamics of the system is the combination of the dynamics designed for the current and voltage controllers. For example, in a period just after the load step at 5 ms (see Fig. 8), the response corresponds to the one presented in Fig. 5 at 5 ms. In turn, just after the load step at 90 ms, the response corresponds to the one presented in Fig. 7 at 20 ms.

Since the stability criterion was not taken into account at the tuning stage, the system should also be analyzed in this respect. Table II shows the results of a stability analysis at the plant inputs, showing the sensitivity to plant parameters' variation. Two values are provided for each case. The first one corresponds to the SFCC and the second one to the SFVC. The control system robustness directly results from the robustness of the FSF controllers implemented as parallel subsystems. The robustness is not weakened by the limitation mechanism of the state variable range itself. In addition, there is no negative inverse impact, i.e., the change in the plant parameters does not affect the ability to impose limits. The proposed method is not based on the plant model, which distinguishes it from other methods of imposing limits in FSF controllers [38].

V. EXPERIMENTAL RESULTS

The experimental validation of the proposed control structure was carried out at the laboratory setup consistent with the parameters provided in Table I. The view of the setup is shown in Fig. 9. Two three-phase voltage source converters with a common dc circuit have been used in the experimental setup. The first one was operated as a grid-side converter, and
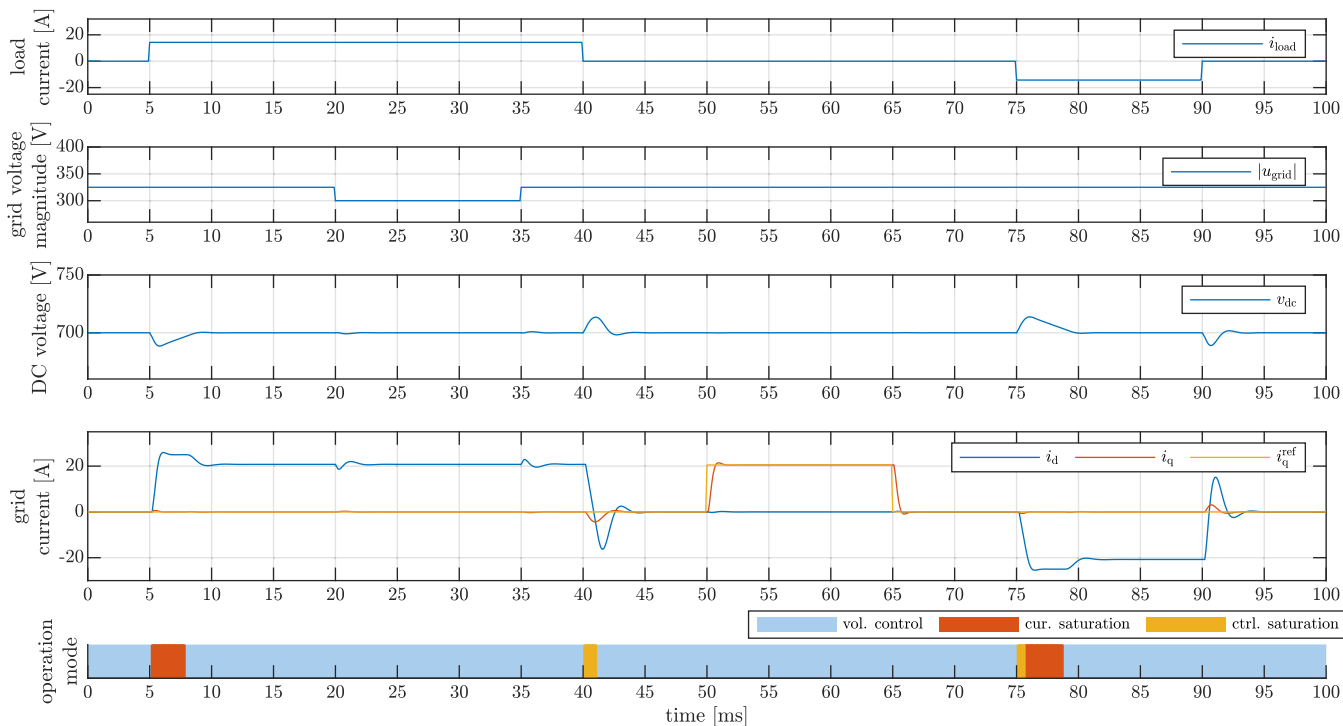
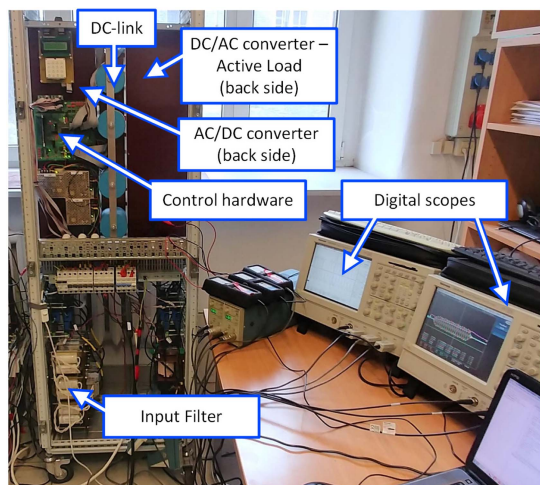Fig. 8. Numerical results of MTSC for discrete linear plant.

Fig. 9. View on laboratory setup.

Fig. 10. Experimental results for a load pulse. (a) Grid line to line voltages. (b) Phase currents. (c) DC-link voltage.

the second one was used an active load. Both the converters were controlled by a control board with the TMS320F28335 microcontroller.

The MTSC performance at the step load condition is illustrated in Fig. 10. At time 5 ms, a load current pulse lasting 60 ms starts. In the period between 6 and 11 ms, the system goes into the current control mode, using SFCC, to impose the current limitation. The amplitude of the phase current matches the predefined threshold in the transient state. During that time, v_{dc} increases at a constant rate. The described design of the MTSC ensures that the system goes back to the voltage control thread in the right time and with the appropriate state of
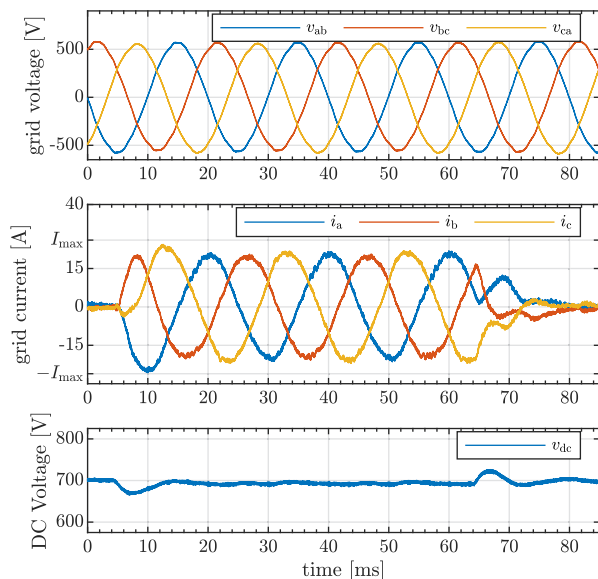
integral term; therefore, the character of response remains as desired.

A longer phase of operation in the current saturation mode is presented for the grid voltage dip case in Fig. 11. At time 30 ms, grid voltage starts to decrease, and this, in turn, causes an increase in grid current. At time 70 ms, the grid current reaches the maximum value. The consequence of imposing current saturation is the drop in output voltage v_{dc}.
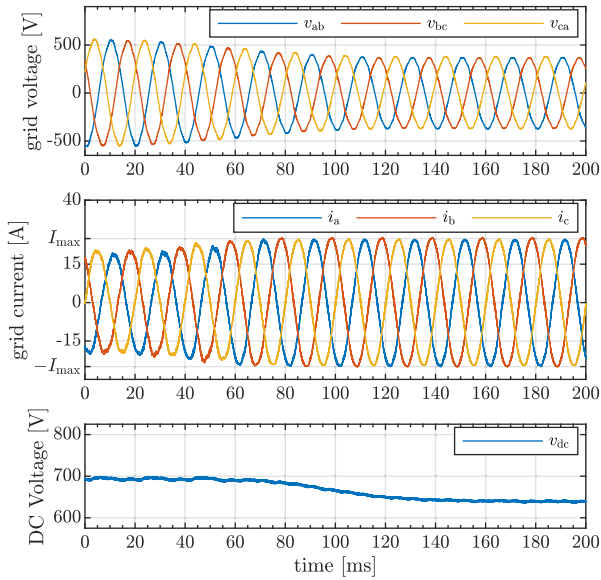
Fig. 11. Experimental results for a voltage sag. (a) Grid line to line voltages. (b) Phase currents. (c) DC-link voltage.
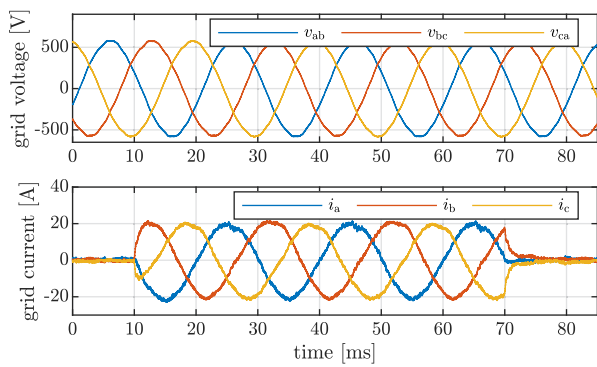

Fig. 12. Experimental results for pulse of i_q^{ref}. (a) Grid line-to-line voltages. (b) Phase currents.

The effect of the independent design of i_q current dynamics not coupled with the v_{dc} dynamics is presented in Fig. 12. In this case, the system remains on the main thread using SFVC. Thanks to the selection of eigenvectors with high orthogonality, the dynamics of i_q for SFVC and SFCC is the same.

The presented experimental results demonstrate the accomplishment of all the targets for the described controller.

VI. CONCLUSION

The SFC is a very effective solution from the control theory point of view. Unfortunately, its standard implementation with a single instance of such a controller suffers from a lack of straightforward methods of imposing constrains on the state variables. In most practical applications, this is prohibitive and, hence, is less popular among practitioners, who often discard this kind of controller in favor of a cascaded control structure.

Often, the tuning cascaded control structure has its limitations coming from the fact that the bandwidth of the outer loop has to be significantly lowered with respect to the bandwidth of the inner control loop, if tuned in the loop-at-a-time fashion, which is standard practice. This restriction does not apply to the state controller, which is of a parallel structure, and all the feedback loops are at the same hierarchy level. Control quality, in terms of achieving the desired step-response character and disturbance rejection properties, can then outcompete the one offered by the cascaded controllers.

The proposed MTSC retained all the benefits of an FSF controller and, at the same time, imposed limits on the state variables as well as on control signals. This made it practical in real-life engineering control tasks. We believed that this is a bridging technology toward transitioning from cascaded to parallel control structures in many industrial applications, including power electronics and drives. Moreover, the control structures of FSF architecture were also fully capable of being extended to accommodate oscillatory terms, if this was required by a specific application.

The developed algorithm was verified experimentally, and the obtained results confirmed its efficacy. This was the very first fully fledged demonstration of the viability of the algorithm in a physical control system. However, the topology of the proposed multithreaded state control was not application specific, i.e., the number of state controllers may vary with the application as it is directly linked to the number of limits one needs to impose, but the overall concept stays the same. Further research will be directed toward the implementation of the algorithm in a physical drive system and a grid converter with an LCL filter. There are potential significant benefits for the system with the LCL filter, resulting from the usage of the MTSC instead of classical methods, i.e., there is a possibility of effective imposing restrictions in dynamic states on the capacitor voltage and currents at both the inductors.

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