Corrections to "Countering Load-to-Use Stalls in the NVIDIA Turing GPU"

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In our article titled "Countering load-to-use stalls in the NVIDIA turing GPU,"[1] references [9] and [10] need to be corrected. Reference [9] should be: S. Z. Gilani, N. S. Kim, and M. J. Schulte, "Power-efficient computing for compute-intensive GPGPU applications," in *Proc. High Performance Comput. Archit.*, 2013, pp. 330–341.

Reference [10] should be: J. Kim, C. Torng, S. Srinath, D. Lockhart, and C. Batten, "Microarchitectural mechanisms to exploit value structure in SIMT architectures," in *Proc. Int. Symp. Comput. Archit.*, 2013, pp. 130–141.

REFERENCES

1. R. Rangan, N. Turakhia, and A. Joly, "Countering load-to-use stalls in the NVIDIA turing GPU," *IEEE Micro*, vol. 40, no 6, pp. 59–66, Nov./Dec. 2020.

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