FROM THE EDITOR-IN-CHIEF

Connectivity—More Needed Than Ever Before

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Welcome to the first issue of *IEEE Micro* of the new year 2021, a Special Issue on Hot Interconnects! The importance of interconnections cannot be emphasized as we think of 2020. The world just wound down an unprecedented year where survival of mankind depended on connected devices. As COVID took us to a "new normal," that normalcy included online classrooms, online conferences, virtual doctors visit, virtual wedding celebrations, virtual baby showers, virtual family meets, etc. Without the modern connectivity, the COVID sheltering and isolation would have been much more devastating.

Connectivity is important at all levels—between transistors in chips, between chips in systems, and between systems that are far apart. It is also commonly thought that the superior energy efficiency of brain compared to silicon chips is largely due to the higher connectivity of neurons. Computer chips for accelerating machine learning will likely be more effective if more connectivity can be provided between compute units.

This special issue presents a collection of articles on interconnect technologies circa 2020, based on the Hot Interconnects Conference of 2020. Seven papers are presented with the Hot Interconnect theme. Ryan Eric Grant from Sandia National Labs and Manjunath Gorentla Venkata of NVIDIA served as guest editors for this special issue. An overview of the seven articles can be obtained from the comprehensive introductory message written by Grant and Venkata. The seven articles are on topics such as interface architectures for die-to-die chiplets, lossy data center networks, configurable network accelerators using FPGAs, GPU-FPGA heterogeneous accelerators for deep learning, PCI-Express 6.0 using PAM-4 signaling, reliable time-efficient virtual network function placement, etc. I would like to express my special gratitude to guest editors Grant and Venkata who worked hard on identifying these excellent papers from the Hot Interconnects Conference, and taking them through a rigorous review/revision process, resulting in the excellent articles that you are presented with.

The seven articles from the Hot Interconnects theme are accompanied by two General Interest articles and a Micro Economics column by Shane Greenstein.

In the first of the General Interest articles, Tsiokanos and Karakonstantis present ExHero, a fully automated framework that performs dynamic timing analysis considering the execution history of a number of in-flight instructions. This article is important for timing analysis of nanometer devices, which are heavily prone to timing errors. In modern microarchitectures, it is not sufficient to only consider the data-dependent excitation of paths; it is also important to consider the impact of concurrently executed instructions on error occurrence. ExHero considers the order and type of instructions within sequences that have length equal to the pipeline depth and improves the estimation of errors using execution history.

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In the second General Interest article, Bertozzi *et al.* present a cost-effective and flexible asynchronous interconnect technology for globally asynchronous locally synchronous (GALS) systems. Although asynchronous Networks on Chips (NoCs) bring several potential advantages compared to their synchronous counterparts, they suffer from challenges in optimizations, scaling, and flexibility. This article first presents a novel asynchronous switch architecture that uses two-phase or transition signaling protocols and bundled data encoding. Then, it presents a complete synthesis flow for such designs built on top of mainstream industrial CAD tools. The article demonstrates the ability

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of the tool flow to correctly instantiate a complete network topology for a GALS system.

In the Micro Economics article, "Technology Policy Dilemmas in the New Administration," Shane Greenstein discusses potential policy changes in the economy, trade, immigration, and commercial policy with the new administration in the United States. These policies will shape costs and opportunities for firms, and result in economic implications for managers and investors.

The article, "A Hardware–Software Blueprint for Flexible Deep Learning Specialization," authored by T. Moreau, T. Chen, L. Vega, J. Roesch, E. Yan, L. Zheng, J. Fromm, Z. Jiang, L. Ceze, C. Guestrin, and A. Krishnamurthy, has been awarded the 2019 Best Paper Award from *IEEE Micro* by the IEEE Computer Society Publications Board. This article, originally published in the September/October 2019 issue, proposed an end-to-end framework with versatile tensor accelerator (VTA) paired with a capable JIT compiler and runtime to support evolving ML workloads on hardware accelerators. The work demonstrated how a well-integrated hardware/software stack can enable full-stack optimization, and automatic compilation to FPGAs.

IT IS ONLY APPROPRIATE THAT WE HAVE AN ISSUE DEDICATED TO INTERCONNECTS AS THE WORLD JUST FINISHED WITH A YEAR WHERE CONNECTIVITY PROVED TO BE EXTREMELY IMPORTANT FOR SURVIVAL, WHETHER IT WAS WORKING REMOTELY FROM HOME OR STAYING CONNECTED WITH YOUR LOVED ONES VIA TECHNOLOGY.

Congratulations to the University of Washington team who won the best paper award. The papers in *IEEE Micro*, except the Top Picks articles, were considered for the award. I wish to express my gratitude to the selection committee consisting of John Kim, Tulika Mitra, Vijaykrishnan Narayanan, and R. Iris Bahar that evaluated the 2019 papers in order to select the winners. I am specially indebted to John Kim for serving as the Chair of the committee.

Readers of *IEEE Micro* will continue to get articles on emerging chip technologies and architectures as we go into the coming year. This Hot Interconnects Issue will be followed by a Hot Chips Issue in March/April. The subsequent issues will be Top Picks from architecture conferences, and special issues on FPGA Computing, Quantum Computing, and In-Memory Computing. Please check out the Call for Papers at:

- https://www.computer.org/digital-library/magazines/mi/call-for-papers-special-issue-on-fpgas-in-computing
- https://www.computer.org/digital-library/magazines/mi/call-for-papers-special-issue-on-quantum-computing-2

In addition to the Special Issue articles, *IEEE Micro* is always interested in submissions on any aspect of chip/system design or architecture. Please consider submitting articles to *IEEE Micro* and remember these articles are eligible for the best paper award, which will be given annually.

I wish all readers a very happy 2021 both professionally and personally. Enjoy this issue on Hot Interconnects! It is only appropriate that we have an issue dedicated to interconnects as the world just finished with a year where connectivity proved to be extremely important for survival, whether it was working remotely from home or staying connected with your loved ones via technology. Wishing you more connectivity in 2021 in your chips and in your lives!

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