



Architectures for the Post-Moore Era

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Moore's law is a techno-economic model that has enabled the \$4 trillion worldwide IT industry¹ to nearly double the performance and functionality of digital electronics roughly every two years within a fixed cost and area. And, simply put, our innovation-driven economy has come to rely on this technological pace to transform economic competitiveness, national security, energy, and quality of life. However, recent reports illustrate that classical technological drivers that have underpinned Moore's law for the past 50 years are already failing, and they predict that they will plateau by 2025.²⁻⁵ That is, within a decade, the technological underpinnings for Moore's law will end.

Propelling computer performance beyond the scaling limits of Moore's law will likely require a comprehensive rethinking of technologies—from materials to devices, circuits, and architectures. Innovative new technologies like quantum, neuromorphic, approximate, and stochastic computing may provide solutions to these challenges, while new

integration strategies such as 3D stacking are maturing to provide additional architectural options.

This special issue of *IEEE Micro* examines these new technologies for a post-Moore era. Submissions were solicited in January 2017 and underwent peer review, and the committee then selected six articles for publication.

In the first article, “Heterogeneous Computing Meets Near-Memory Acceleration and High-Level Synthesis in the Post-Moore Era,” Nam Sung Kim and his colleagues describe a conceptual architecture for heterogeneous computing near memory that can improve both performance and energy efficiency. The article also discusses the need for using a high-level synthesis approach for designing such architectures.

In “A Resistive CAM Processing-in-Storage Architecture for DNA Sequence Alignment,” Roman Kaplan and his colleagues describe a processing-in-storage (PRinS) architecture based on resistive content addressable memory (ReCAM). The article motivates the architecture with a specific evaluation on the problem of DNA sequence alignment, and the authors compare their results to field-programmable gate arrays (FPGAs), Xeon Phi, and GPUs. The results show an improvement in throughput and power.

“In-Memory Intelligence” by Tim Finkbeiner and his colleagues takes another look at memory-centric computing in the form of in-memory intelligence (IMI). In this work, the architecture includes a massive array of SIMD computing elements on pitch with the memory array. The work is evaluated with several important kernels, including image and hashing algorithms.

In “Solving Mesoscale Atmospheric Dynamics Using a Reconfigurable Dataflow Architecture,” Lin Gan and his colleagues revisit the opportunities for reconfigurable computing by mapping a complex Euler stencil kernel for mesoscale atmospheric dynamics into a single FPGA chip. The authors compare the design to other accelerators, and their evaluation shows that this design can outperform several other technologies in terms of both time to solution and energy to solution.

“Exploiting Dark Fluorophore States to Implement Resonance Energy Transfer

Pre-Charge Logic” by Craig LaBoda and his colleagues investigates the opportunities for resonance energy transfer (RET) logic composed of self-assembled networks of fluorescent molecules. The authors propose a new form of RET logic design that yields a library of nonlinear logic gates that can be composed into more complex integrated molecular circuits.

Finally, in “Building Maze Solutions with Computational Dreaming,” Scott M. Jackson and JoAnn M. Paul investigate a meta-algorithm for cognition called *computational dreaming*, which is inspired by the cerebral cortex’s “day phases” and “dream phases.” The authors find that this technique can be applied successfully to finding maze solutions, and its solutions can match those generated by other well-known algorithms such as BFS and DFS.

We thank all those who submitted papers to this issue and the anonymous reviewers for their efforts. We hope readers will enjoy this special issue of *IEEE Micro*. ■■■

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Assoc. and Semiconductor Research Corp., 2015.

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