A Power-Efficient CMOS Multi-Band Phased-Array Receiver Covering 24–71-GHz Utilizing Harmonic-Selection Technique With 36-dB Inter-Band Blocker Tolerance for 5G NR

Yi Zhang, *Graduate Student Member, IEEE*, Jian Pang, *Member, IEEE*, Zheng Li, *Graduate Student Member, IEEE*, Minzhe Tang, *Student Member, IEEE*, Yijing Liao, Ashbir Aviat Fadila, *Graduate Student Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Senior Member, IEEE*

***Abstract*— This article introduces a power-efficient 24.25–71-GHz multi-band phased-array receiver supporting all allocated fifth-generation mobile network new radio (5G NR) frequency range 2 (FR2) bands at 24/28/39/47 GHz and the potential 5G NR-U bands in unlicensed 57–71 GHz. A novel harmonic-selection technique is introduced to extend the operating bandwidth with low power consumption. By switching between the fundamental-selected mode, the second-harmonic-selected mode, and the third-harmonic-selected mode, only signals in the desired bands can be preserved, while the unselected mixing components are rejected. A dual-mode multi-band low-noise amplifier (LNA) based on a configurable transformer is adopted to realize broadband operation with minimized power consumption and noise figure (NF). The Hartley architecture is employed to further improve the image rejection performance. A hybrid-type polyphase filter (PPF) with a detector-based high-precision calibration block is utilized in this work to realize the Hartley operation with reduced insertion loss (IL). The proposed phased-array receiver is fabricated in a standard 65-nm bulk CMOS process. With the concerted efforts of all components, the proposed multi-band receiver can support 5G standard-compliant OFDMA-mode modulated signals up to 256QAM with a 400-MHz channel bandwidth from 24 to 71 GHz. Better than 36-dB inter-band blocker rejections can be maintained by this work. With existing of 0-dBc inter-band blockers at worst case frequencies, this receiver shows EVMs of −33.3, −30.9, −31.6, and −28.5 dB at 28, 39, 47.2, and 60.1 GHz, respectively. The power consumptions for a single receiver channel are 36, 32, 51, and 71 mW at 28, 39, 47.2, and 60.1 GHz, respectively.**

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The authors are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan (e-mail: yi@ssc.pe.titech.ac.jp; pangjian@ssc.pe.titech.ac.jp).

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***Index Terms*— Blocker tolerance, CMOS, fifth-generation (5G) new radio frequency range 2 (FR2), harmonic selection, image rejection ratio (IRR), multi-band, phased array.**

I. Introduction

MILLIMETER-WAVE (mmW) communication is indispensable in the next-generation network to satisfy the exponentially growing data traffic between massive devices. To further improve the data rate and channel capacity, the fifth-generation mobile network new radio (5G NR) bands keep scaling toward frequencies over 100 GHz. The frequency allocations for 5G usage in various countries are shown in Fig. 1 [1]. The frequency resources in 28-, 39-, and 47-GHz bands have already been regulated in 5G standard. The 60-GHz spectrum is also under discussion. To realize global application and cross-standard communication, multi-band compatibility is necessary for user devices in 5G NR networks. As indicated in Fig. 1, the necessary operating frequency range with complete support of 5G NR bands mentioned previously should be at least 24.25–71 GHz. Phased-array architecture is essential in 5G NR communications to improve signal quality at mmW frequencies. 5G NR phased-array systems with competitive receiver performance have been published with narrowband designs recently [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. However, multiple chips are necessary to support the multi-band operation, which increases the system size and complexity. To realize compact user devices with low cost, several studies have demonstrated wideband phased-array receivers supporting multiple 5G NR frequency range 2 (FR2) bands with minimized system dimensions in recent years [15], [16], [17], [18], [19], [20], [21], [22]. However, the operating frequency range of these works is still limited and difficult to be scaled to more 5G NR FR2 bands. In addition, multi-band operation also exposes the receiver to more cluttered and rapid-changing electromagnetic (EM) environments. Power-efficient and wideband receiver architecture with enough rejections to inter-band blockers will, hence, be required for such receivers.

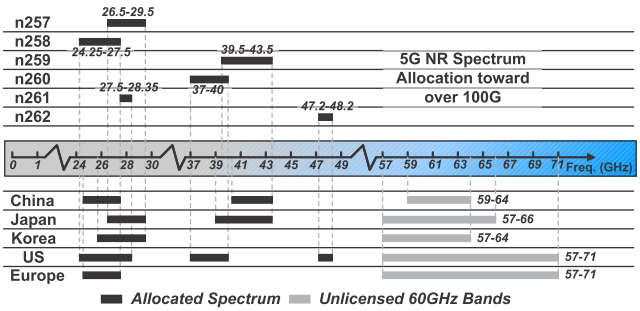


Fig. 1. Latest 5G NR FR2 bands and global licensed/potential spectrum allocation for now and future.

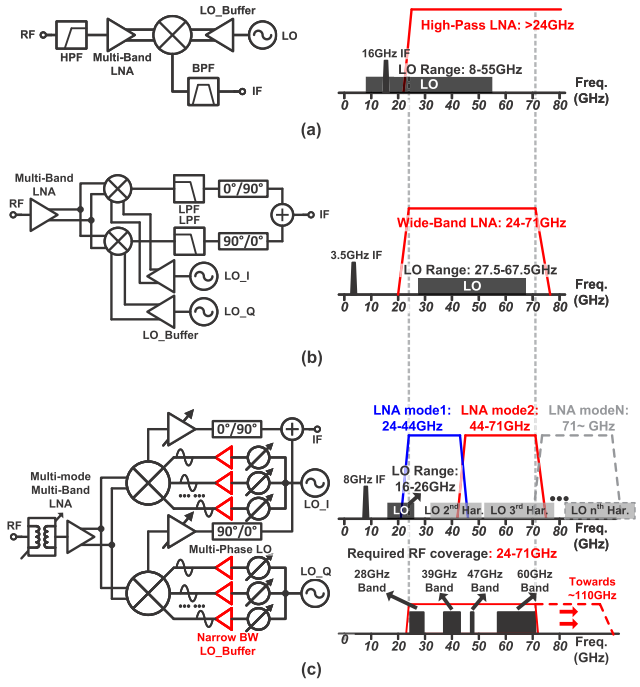


Fig. 2. (a) Conventional multi-band superheterodyne receiver [20], [21]. (b) Conventional multi-band configurable Hartley receiver [18]. (c) Proposed multi-band Hartley receiver utilizing the harmonic-selection technique.

This work introduces a CMOS multi-band phased-array receiver covering 24.25–71 GHz. Complete 5G NR FR2 bands can be covered. A harmonic-selection technique is proposed to extend the operating bandwidth with low power consumption. Improved inter-band blocker tolerance can also be maintained by this work. This article, which is an extension of [23], is organized as follows. Section II introduces the system consideration of the proposed multi-band phased-array receiver. The proposed harmonic-selection technique and the detailed circuit implementations are explained in Section III. Section IV presents the measurement results. Finally, the conclusion is drawn in Section V.

II. System Consideration

As mentioned previously, the 24.25–71-GHz operation is necessary to be covered for supporting complete 5G NR FR2 band operation. The frequency plans of conventional and proposed multi-band receivers with 24–71-GHz radio frequency (RF) coverage are shown in Fig. 2. As shown in Fig. 2(a), the conventional multi-band receiver based on the superheterodyne architecture achieves multi-band operation with wideband signal path design [20], [21]. With high intermediate frequency (IF), the images can be completely removed from the passband of the low-noise amplifier (LNA). However, the fractional bandwidth of the local oscillator (LO) path will be much larger when the RF frequency coverage scales to 24–71 GHz. The power consumption of both RF and LO will become incredibly large to guarantee the required conversion gain (CG). Moreover, the image frequency will also be inevitably overlapped with the passband of LNA; even a high IF frequency is used. To tackle with this issue, the Hartley architecture is adopted to provide full-band image rejection in multi-band receivers [17], [18], as shown in Fig. 2(b). Conventional multi-band receiver employs the configurable Hartley architecture to select the desired sideband. Therefore, 24.5–43.5-GHz RF frequency coverage can be realized with a high image rejection ratio (IRR) [18]. A single multi-band LNA is also utilized for providing wideband signal amplifying. However, the noise figure (NF) of such a system will be degraded by around 3 dB since the images are still located in the passband of the LNA. When the RF frequency coverage is extended to 24–71 GHz, the LO frequency range will be also enlarged. Quadrature LO generation will be required to be maintained over an ultra-wide frequency range. Therefore, the bandwidth of such multi-band receiver architecture can hardly be extended with small circuit area and power consumption overheads.

To realize multi-band receiver achieving band selectivity across a wide frequency range with low power consumption and high inter-band blocker rejection, the scalable harmonic-selection technique is introduced in this work. The block diagram of a harmonic-selection receiver is shown in Fig. 2(c). By applying multi-phase LO to a mixer, the desired mixing component can be selected from the harmonics. Assuming that there are totally N mixing paths in the harmonic-selection receiver, and they are driven by N-phase LOs, the resulted mixing components could be represented with the following equation:

$$\begin{aligned} V_{\mathrm{IF}k\mathrm{th}} &= \frac{1}{2}A_{\mathrm{SIG}}A_{\mathrm{LO}}\sum_{i=1}^{N}\cos\left[(k\omega_{\mathrm{RF}}\pm\omega_{\mathrm{LO}})+\frac{2ki\pi}{N}\right] \\ &= \frac{1}{2}A_{\mathrm{SIG}}A_{\mathrm{LO}}\left[\cos(k\omega_{\mathrm{RF}}\pm\omega_{\mathrm{LO}})\sum_{i=1}^{N}\cos\left(\frac{2ki\pi}{N}\right)\right. \\ &\qquad \left. -\sin(k\omega_{\mathrm{RF}}\pm\omega_{\mathrm{LO}})\sum_{i=1}^{N}\sin\left(\frac{2ki\pi}{N}\right)\right] \\ &= \begin{cases} 0, & k<N \\ \dfrac{k}{2}A_{\mathrm{SIG}}A_{\mathrm{LO}}\cos(k\omega_{\mathrm{RF}}\pm\omega_{\mathrm{LO}}), & k=N. \end{cases} \end{aligned} \tag{1}$$

In the equation, $V_{\mathrm{IF}k\mathrm{th}}$ represents the mixing component with the kth harmonic of LO. It can be found that only the Nth harmonic mixing component will be enhanced, while the other mixing components will be rejected by applying an N-phase LO with $2\pi/N$ phase interval. With this feature, any mixing components generated by kth ($k <= N$) order

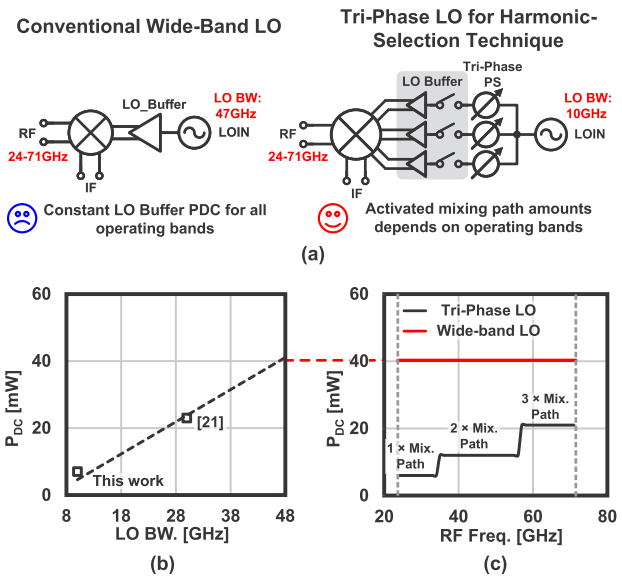


Fig. 3. (a) Comparison of conventional and proposed LO path for 24–71-GHz multi-band operation. (b) Estimated LO buffer power consumption against LO bandwidth. (c) Power consumption of tri-phase LO path for the proposed harmonic-selection technique with three mixing paths and conventional wideband LO paths.

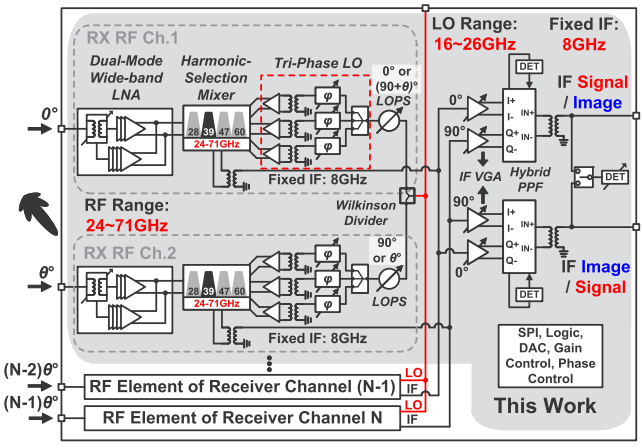


Fig. 4. Block diagram of the proposed multi-band phased-array receiver with harmonic-selection technique.

harmonic of the LO can be realized by applying an appropriate LO phase assignment to an k-path harmonic-selection mixer. It can be considered that the RF signal is mixed with an equivalent harmonic of the LO with the harmonic-selection mixer. Therefore, the operating frequency range of the receiver can be significantly extended without a wideband LO. The power consumption can be minimized with scalable RF frequency coverage. According to the equation, the harmonic-selection technique also provides rejections against the inter-band blockers generated by the unwanted harmonics. Collaborate with the LNA bandpass filtering and the Hartley receiver architecture; the proposed technique can realize high inter-band blocker rejection with suppressed system NF and minimized power consumption.

To realize the required 24–71-GHz RF coverage, three mixing paths with a tri-phase assignment are required for the proposed harmonic-selected technique, as shown in Fig. 3(a). For an RF amplifier, since the matching loss of the matching network tends to increase proportionally along with its bandwidth, a larger transistor size or more stages are required to compensate for the matching loss, which will significantly increase the power consumption. Therefore, it can be roughly assumed that the power consumption (P_{dc}) of the LO buffer is proportional to the LO bandwidth for a certain LO budget. An estimated P_{dc} of LO buffer against LO bandwidth is shown in Fig. 3(b) based on the measured and reported P_{dc} of this work and conventional work in Fig. 3(a) [21]. P_{dc} of LO buffer could be up to 40 mW for conventional wideband LO path to support the required 24–71-GHz RF coverage. According to (1), only k mixing paths are required for the harmonic-selection mixer to select the desired kth harmonic mixing component. As shown in Fig. 3(c), theoretically, only one and two mixing paths are activated at fundamental- and second-harmonic-selected modes, separately. Therefore, lower power consumption can be realized on lower operating bands. On the contrary, the power consumption of conventional wideband LO is constant on all operating bands. Since the harmonic-selection technique depends on the nonlinearity of the mixer, the higher order mixing components tend to be weaker than the fundamental mixing component. However, as explained in (1), multi-phase mixing paths in the proposed harmonic-selection technique also result in a k-times CG, which can compensate for the loss of higher order harmonic mixing components effectively.

III. Circuit Implementation

The block diagram of the proposed 24.25–71-GHz multi-band phased-array receiver based on the harmonic-selection technique is shown in Fig. 4. Considering the required RF frequency coverage, a tri-phase LO is utilized in this work to drive the mixer. Thanks to the proposed harmonic-selection technique, the required LO frequency range is reduced to 16–26 GHz. The IF frequency is fixed at 8 GHz for better selectivity. Besides, the 8-GHz narrowband design can prevent IF from the influence of LO spurious and leakage. With the improved tolerance to LO leakage, the LO can be generated with a mature sub-6-GHz frequency synthesizer following by the frequency multiplier theoretically [24], [25], [26]. Totally two receiver channels are included in the proposed chip. Each receiver channel consists of a dual-mode multi-band LNA, a harmonic-selection mixer with a tri-phase LO generating circuit, and an LO phase shifter. LO phase shifting architecture is chosen for this work to realize precise beam steering across a wide frequency range [11], [27]. Each channel in this work is designed with 360° phase-shifting coverage. The dual-mode multi-band LNA in this work can be configured to cover 24–44 or 44–71 GHz. Configurable Hartley receiver architecture is also adopted in the proposed receiver for sideband selection and image rejection. Since the phased array already provides sufficient spatial selectivity, the Hartley architecture in this work is designed for the situation where the desired and undesired signals arrive with the same phase. The quadrature LO is generated by the LO phase shifters in different receiver

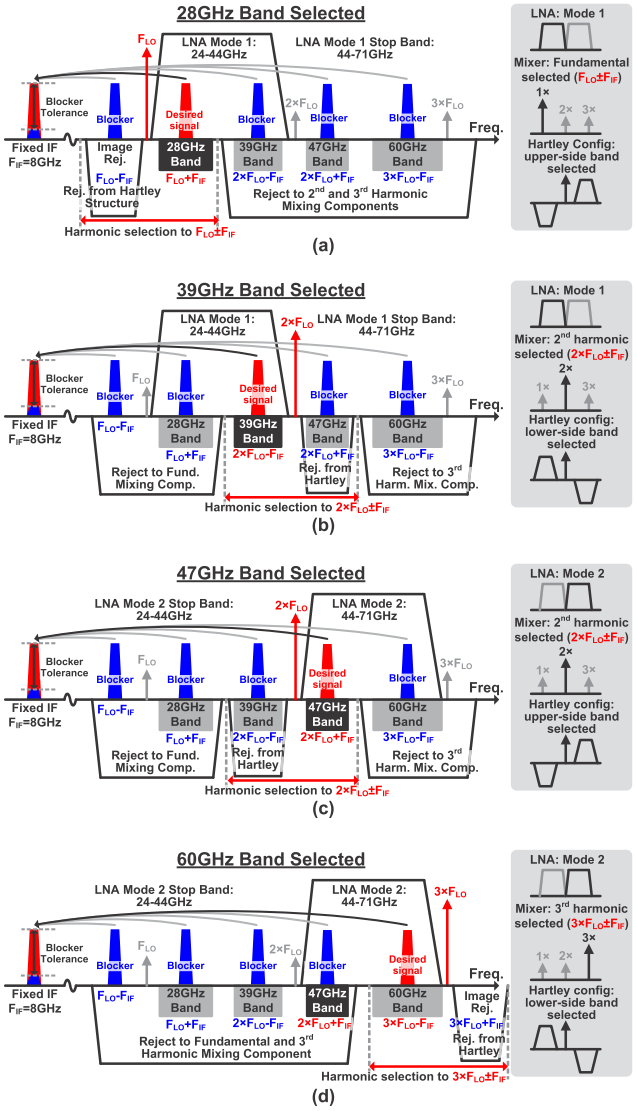


Fig. 5. Frequency plan and inter-band blockers analysis of the proposed receiver on (a) 28-GHz band mode, (b) 39-GHz band mode, (c) 47-GHz band mode, and (d) 60-GHz band mode.

channels. A hybrid-type polyphase filter (PPF) is inserted into the IF part for summarizing the received signals in quadrature.

Based on the system implementation, the detailed frequency plan of the proof-of-concept harmonic-selection receiver is shown in Fig. 5. There are totally four operating modes for the receiver. Frequencies configurations of $F_{\mathrm{LO}} + F_{\mathrm{IF}}$, $2 \times F_{\mathrm{LO}} - F_{\mathrm{IF}}$, $2 \times F_{\mathrm{LO}} + F_{\mathrm{IF}}$, and $3 \times F_{\mathrm{LO}} - F_{\mathrm{IF}}$ are assigned to 28-GHz band, 39-GHz band, 47-GHz band, and 60-GHz band operations, respectively. When the receiver is in 28-GHz band operation, the harmonic-selection mixer will be configured in fundamental-selected mode, and the LNA will be configured to cover 24–44 GHz. The upper sideband is selected by the Hartley operation in this mode, while the lower sideband is rejected. In the 39-GHz band and 47-GHz band operations, the harmonic-selection mixer is in the second-harmonic-selected mode. Because the 39-GHz band and 47-GHz band operations are image frequencies with each other, they are distinguished by the sideband-selection function provided by the Hartley architecture. The LNA will be in the 24–44-GHz mode for the 39-GHz band operation and in the 44–71-GHz mode for the 47-GHz operation. Therefore, enough isolation could be provided between these two modes for a maximized IRR and a minimized system NF. In the 60-GHz band operation, the harmonic-selection mixer is in third-harmonic-selected mode, and the LNA is configured with the 44–71-GHz mode. The lower sideband is selected by the Hartley operation. Within the four modes mentioned above, the desired signal could be selected by the proposed receiver, while the unwanted inter-band blockers at harmonic frequencies and image frequencies could be rejected by the proposed harmonic-selection technique, the LNA bandpass filtering, and the Hartley receiver architecture. In actual application, non-ideal mismatches, such as the LO phase error and phase offset between desired and undesired signals, may affect the performance of the Hartley operation or harmonic-selection operation, which will be analyzed in the following part. However, the harmonic-selection technique, LNA bandpass filtering and the Hartley operation always cooperate with each other to reject the undesired signals, which guarantees the receiver performance despite various mismatches.

A. Harmonic-Selection Mixer and Tri-Phase LO Generation

The proposed harmonic-selection technique greatly reduces the required LO frequency coverage while still realizing multi-band down-conversion. The operation principle of the proposed down-conversion technique in the fundamental-selected mode, the second-harmonic-selected mode, and the third-harmonic-selected mode is explained in Fig. 6. The proposed harmonic-selection mixer is driven by the configurable tri-phase LO generation circuits. It consists of three differential mixing paths. Each mixing path is independently driven by an LO signal with proper phase assignment according to the desired mixing component. By applying LOs with different phase assignments to the mixer, the resulted mixing components in each mixing path behave constructively for the desired component and destructively for the undesired harmonics. A differential-/common-mode selector based on the transformer is also implemented at the mixer output side. Additional signal filtering and better matching can be, therefore, provided.

In the fundamental-selected mode, only two mixing paths are activated. The LO path to the closed mixing path is also turned down for saving power. The differential-mode output is selected in this mode, and the proposed mixer now behaves as a conventional double-balanced mixer. The CG of the fundamental mixing component is enhanced by the double-balanced topology, while the unwanted second- and third-harmonic mixing components are rejected. The second-harmonic-selected mode keeps the same LO phase assignment as the fundamental-selected mode. Nonetheless, the mixer output is switched to a common-mode connection in this mode. Therefore, only the second-harmonic mixing component is retained. The differential fundamental- and third-harmonic mixing components are canceled. The balanced topology of

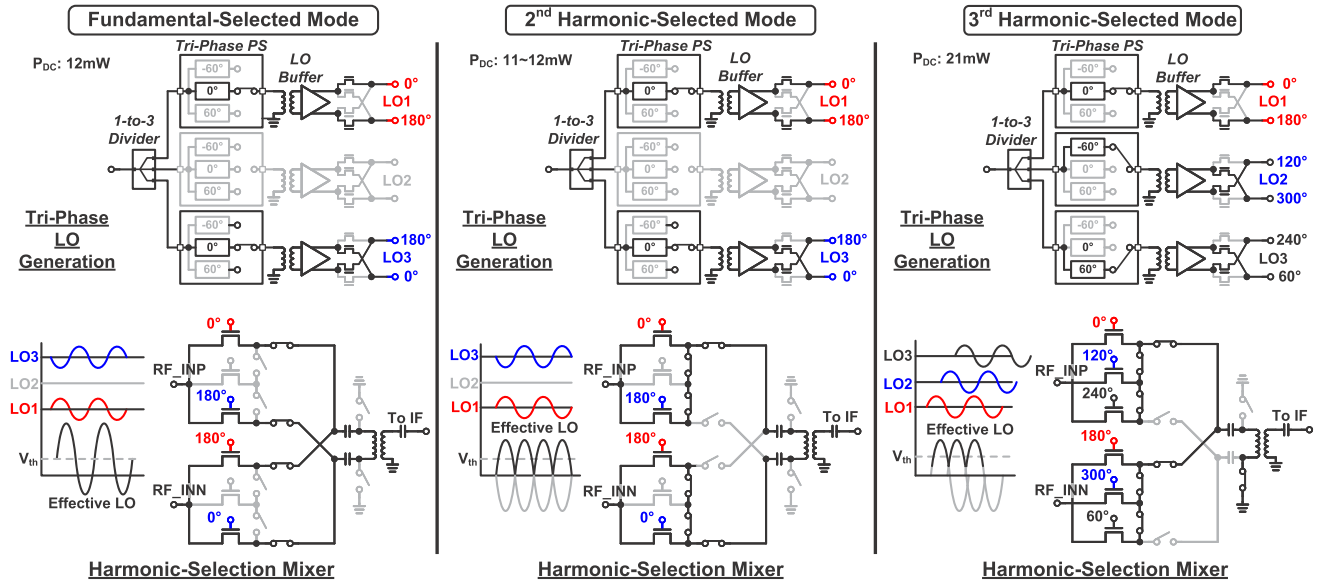


Fig. 6. Operating principle of proposed harmonic-selection mixer with configurable tri-phase LO at each mode.

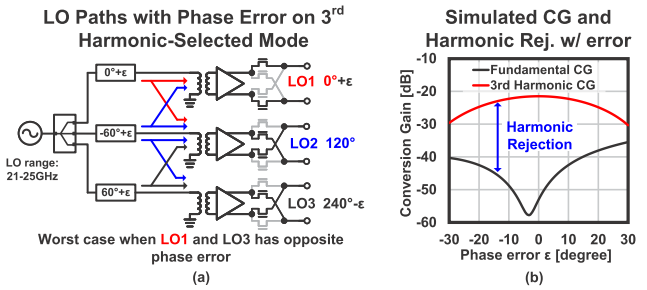


Fig. 7. (a) Phase error of LO paths on third-harmonic-selected mode. (b) Simulated CG and harmonic rejection on third-harmonic-selected mode with phase error.

fundamental- and second-harmonic-selected modes can eliminate the LO leakage effectively. In the third-harmonic-selected mode, three mixing paths are fully activated and driven by tri-phase LOs with 120° phase difference. The fundamental- and second-harmonic mixing components are canceled by the 120° interval tri-phase LO, as analyzed in Section II. The output connection of the mixer is switched to differential mode to further reject the common-mode second-harmonic mixing component. Therefore, the third-harmonic mixing component is, finally, preserved at the output. In an actual circuit, the tri-phase LO may deviate from the desired phase due to the imperfect frequency characteristic of tri-phase LO generation and coupling between mixing paths. For fundamental- and second-harmonic-selected modes, mixing paths on two sides are selected to avoid coupling and keep the circuit symmetrical. The phase error will only slightly degrade CG with a balanced mixer topology. This issue could be more obvious in the third-harmonic-selected mode, as shown in Fig. 7(a). Nonetheless, the simulation result in a worst case in Fig. 7(b) shows that the harmonic-selection technique has a high tolerance to the phase error.

In this work, the compact tri-phase LO generation is designed with low power consumption. The detailed circuit schematic of the LO is shown in Fig. 9. After the LO phase shifter for beamforming, the LO signal is divided into three paths by a compact 1-to-3 Wilkinson divider, which ensures isolation between each path. The bulky λ/4 wavelength transmission lines in the Wilkinson divider are replaced by area-efficient CLC networks to significantly reduce the effective footprint [28], [29]. After that, a tri-phase phase shifter is employed in each path to realize the corresponding LO phase assignment for each harmonic-selection mode. As shown in Fig. 9(b), the proposed tri-phase phase shifter consists of a −60° phase shifting path, a 60° phase shifting path, and a 0° through the path. The −60° and 60° phase shiftings are realized by a phase-lagging low-pass network and a phase-leading high-pass network, respectively, for a compact circuit area. A differential LO buffer with 180° phase-flipping function, as shown in Fig. 9(c), is inserted after the tri-phase phase shifter [30], [31]. Together with the tri-phase phase shifter, the phase assignment for all the operating modes could be generated with a minimized circuit overhead, as shown in Fig. 6. Transformer matching with capacitors is utilized in the LO buffers for broadening the operating bandwidth. Since the harmonic mixing is realized by the non-linearity of the mixer rather than the harmonic distortion of the LO buffer, the LO buffer consumes the same power on all operating modes, which is only around 7 mW.

The measured CG and harmonic rejections of the proposed harmonic-selection mixer along with the tri-phase LO are presented in Fig. 8. The IF frequency is fixed at 8 GHz in this measurement. As shown in the figure, the flat CG characteristic is obtained in all the harmonic-selection modes. More than 20-dB rejections to the undesired harmonic components are also achieved in each operating band by the proposed mixer. The CG offset between each operating mode is less than 5 dB, which can be compensated by variable gain without causing an NF degradation. It should be noted that the rejections could be further improved by the LNA bandpass filtering and the Hartley receiver architecture.

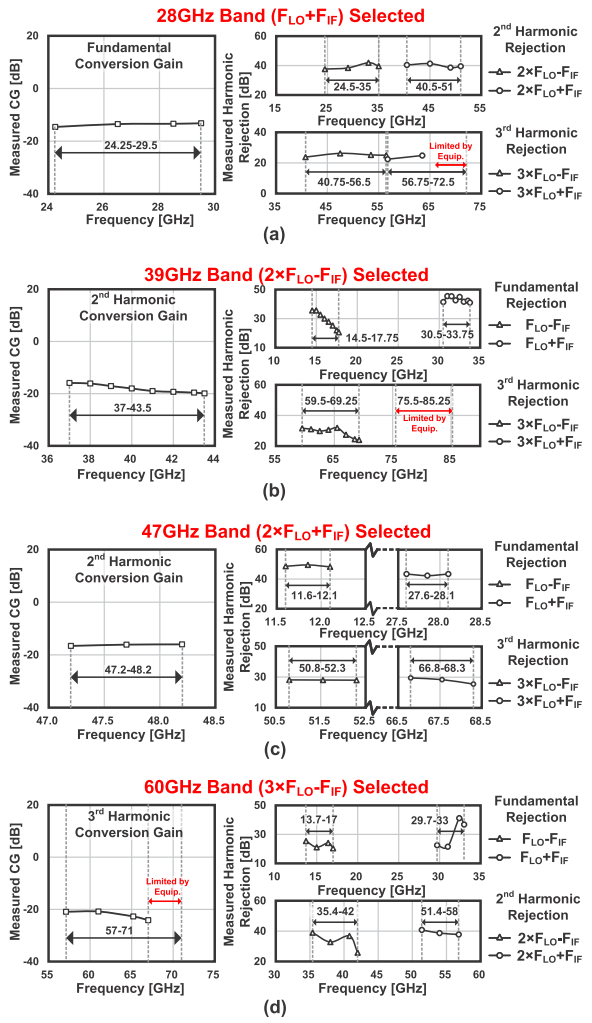


Fig. 8. Measured CGs and harmonic rejections of the proposed mixer on (a) 28-GHz band mode, (b) 39-GHz band mode, (c) 47-GHz band mode, and (d) 60-GHz band mode.

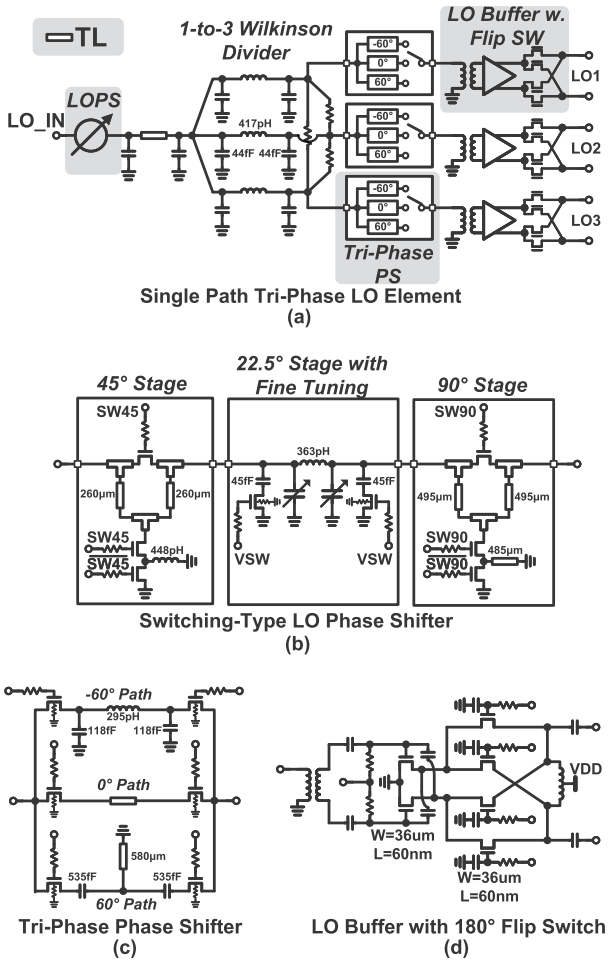


Fig. 9. (a) Block diagram of the tri-phase LO generating path. Circuit implementation of (b) STPS, (c) tri-phase phase shifter, and (d) LO buffer.

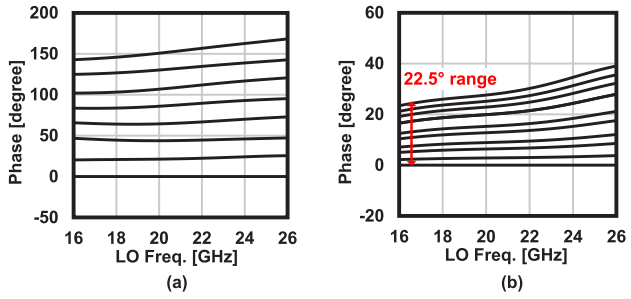


Fig. 10. (a) Simulated relative phase response of the LO STPS. (b) Simulated relative phase coverage of the fine-tuning stage in LO STPS [tuned by 10-bit resistive digital-to-analog converter (RDAC)].

Fig. 9(d) shows the LO phase shifter for beamforming. With 4-bit phase resolution, the switching-type phase shifter (STPS) employed in this work consumes only 0.1-mm^2 chip area while achieving wide bandwidth and great linearity without additional power consumption. It consists of a 90° stage, a 45° stage, and a 22.5° with fine-phase tuning. Along with the 180° phase-flipping function in the LO buffer, 360° phase coverage could be covered. The 45° and 90° stages in this work are designed with bridged-T architecture, which realizes stable and precise phase shifting with small gain variation [32], [33], [34]. Nonetheless, the phase error is difficult to be eliminated in a wide LO frequency range. The simulated relative phase response of the STPS is shown in Fig. 10(a). The remaining phase error may cause LO I/Q mismatch and degrade the performance of the Hartley receiver operation. Therefore, the 22.5° stage with CLC topology shown in Fig. 9(b) also plays the role of the fine-tuning stage by employing varactors [35]. As shown in Fig. 10(b), the fine-tuning realizes at least 22.5° coverage, which is sufficient to compensate for the LO phase error.

B. Dual-Mode Multi-Band LNA

In recent years, although many attractive blocker rejection methods have been proposed, LNA is still the front line to undertake the impact of blockers. In conventional multi-band receivers, a single LNA is designed with a wideband frequency response to cover all the desired bands. The power consumption of the LNA will scale against the bandwidth for maintaining enough gain and linearity. The inter-band blocker rejection of such a method is also limited due to the lack of bandpass filtering. In order to improve the power efficiency

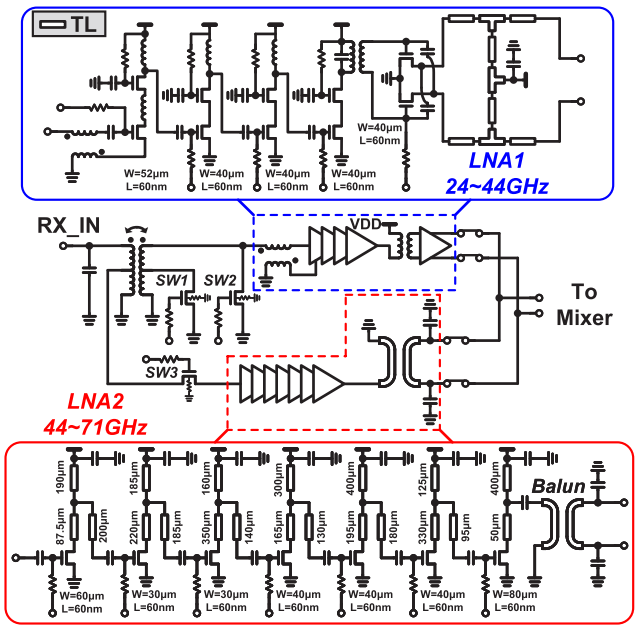


Fig. 11. Block diagram of the proposed dual-mode wideband LNA and its detailed core circuits.

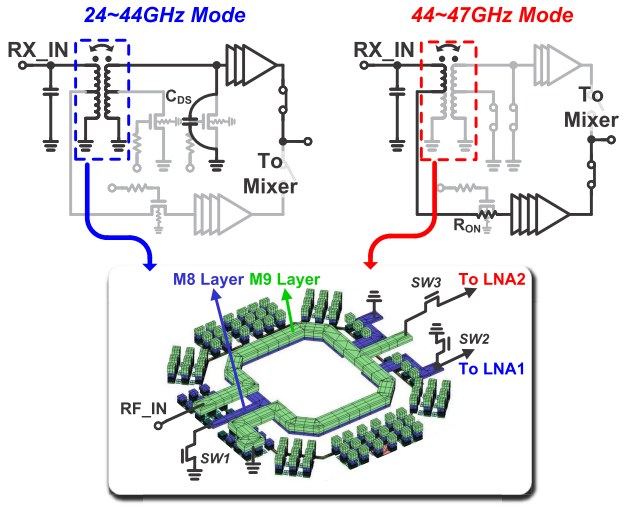


Fig. 12. Operation explanation of dual-mode LNA at the 24–44-GHz mode and the 44–71-GHz mode with a reconfigurable transformer.

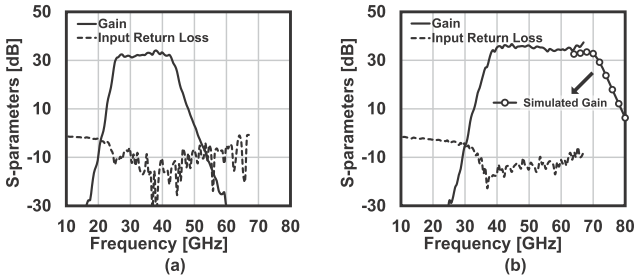


Fig. 13. Measured frequency responses of a single proposed dual-mode multi-band LNA in (a) 24–44-GHz mode and (b) 44–71-GHz mode.

and inter-band blocker tolerance, a dual-mode multi-band LNA is proposed in this work, as shown in Fig. 11. The proposed LNA consists of two LNA elements, which are the lower band LNA covering 24–44 GHz and the upper band LNA covering 44–71 GHz. The frequency coverage of the LNA elements is selected considering the system image rejection and the LNA circuit performance. With the help of the configurable matching network shared between two operating mode, the proposed dual-mode multi-band LNA structure takes a good balance between chip area and circuit performance. The band-pass filtering of the LNA also leads to high isolation between the fundamental- and third-harmonic mixing components of the harmonic-selection mixer. The detailed compositions of the two LNA elements are also demonstrated in Fig. 11. The lower band LNA employs four cascode stages to achieve high gain while maintaining a low NF [36]. The input stage is source degenerated with an inductor coupled and integrated with the input series inductor [37]. A compact footprint is realized with improved matching and linearity. The upper band LNA introduces seven common-source (CS) stages to ensure enough power gain. Transmission-line-based interstage matching is chosen to improve the area efficiency.

Typically, the required passive values for the matching are inversely proportional to the operating frequency. Based on this characteristic, a reconfigurable transformer is employed at the input to combine the two LNA elements. As shown in Fig. 12, the upper band LNA is connected to the center tap of the primary coil. When the lower band LNA is operating, the input transformer forms a high-order wideband matching network with C_{gs} from SW2 to cover 24–44 GHz. During the operation of the upper band LNA, the secondary transformer coil will be grounded. The upper band LNA will, hence, be matched with the approximate half-inductance value of the primary transformer coil. At the output side, the two LNA elements are combined with a single-pole–double-throw (SPDT) switch for better isolation.

A stand-alone dual-mode multi-band LNA is fabricated for on-wafer evaluation. The measured performance of the LNA in the lower band mode and the upper band mode is presented separately in Fig. 13. The −3-dB bandwidth in the lower band and upper band modes realizes coverage of 24–44 and 44–71 GHz, as expected. The measured gains of the proposed LNA in the 24–44-GHz mode and the 44–71-GHz mode are around 32 and 35 dB, respectively. During the measurement, the input return loss in both modes keeps lower than −10 dB in the passband.

C. Hartley Receiver and Hybrid-Type PPF

The IRR performance of multi-band receivers is essential due to their wide frequency coverage. The proposed receiver utilizes the Hartley receiver architecture to improve image rejections. A 90°-shifted LO is used at the adjacent channel, and −90° is again applied in IF PPF to realize the Hartley operation. The insertion loss (IL) of passive multistage PPFs increases significantly with more stages, which degrades the system CG and NF. Therefore, a single-stage PPF is utilized in this work. Generally, the PPF topology can be classified into two types, as shown in Fig. 14(a) [38]. For Type-I PPF, the I and Q signals are orthogonal at all frequencies. However,

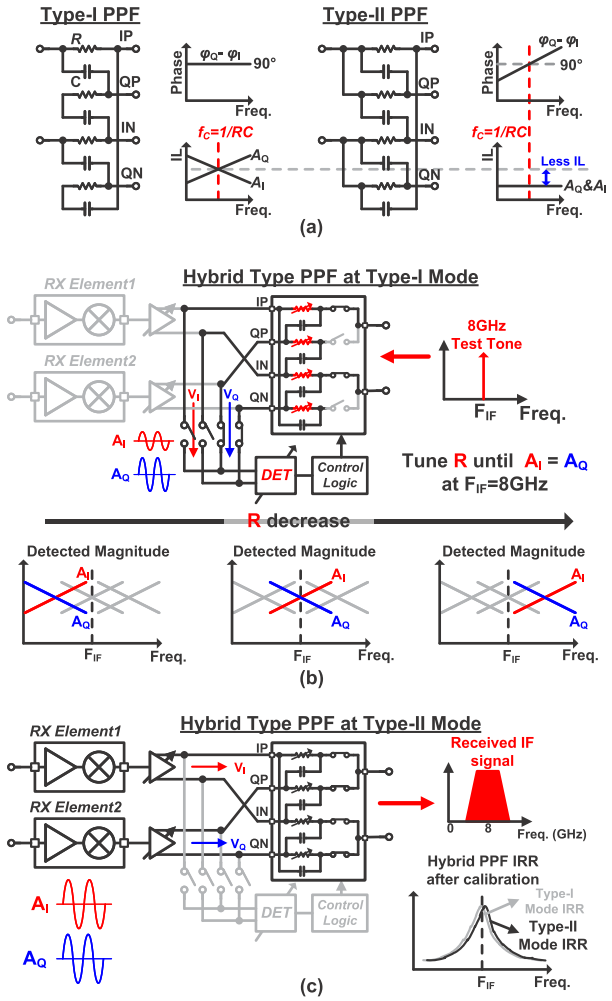


Fig. 14. (a) Frequency responses of Type-I and Type-II PPFs. (b) Calibration of the hybrid-type PPF. (c) IF circuits configuration after IRR calibration at the normal receiver operation.

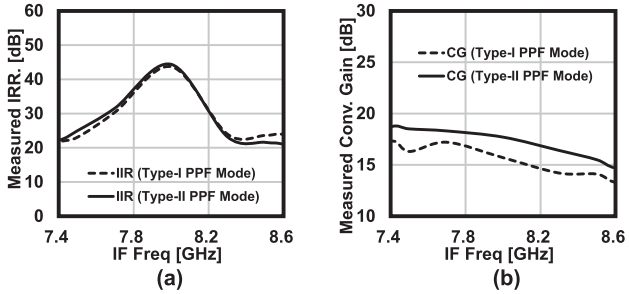


Fig. 15. Measured system (a) IRR and (b) CG with the proposed hybrid-type PPF operating in Type-I and Type-II modes separately.

the amplitude of I and Q signals will be the same only at the pole frequency $f_C = 1/2\pi RC$ of the PPF. On the contrary, the amplitude of I and Q signals in Type-II PPF is identical at all frequencies but will be orthogonal only at the pole frequency f_C. Typically, Type-II PPF is preferred in conventional designs since its IL is 3 dB theoretically better than Type-I topology. However, regarding the IRR degradation caused by PVT variations, Type-II PPF generally requires complicated and bulky phase calibration [16], [39], [40]. The

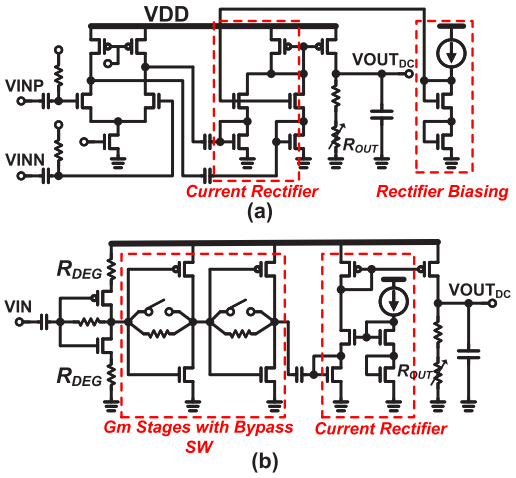


Fig. 16. Schematic of (a) proposed differential voltage detector for hybrid PPF calibration and (b) high-dynamic detector for IF power level detection.

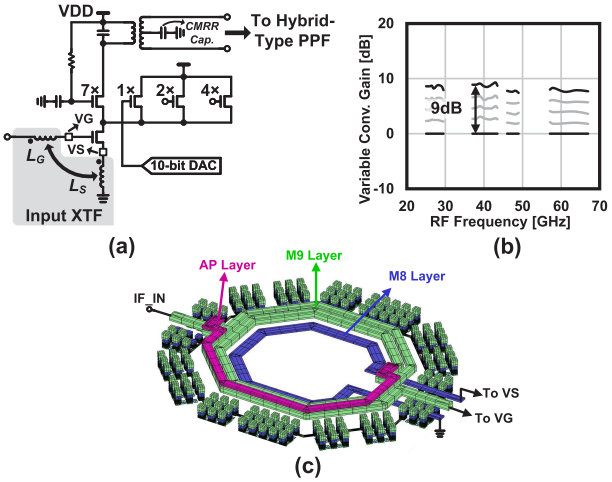


Fig. 17. (a) Circuit schematic of the proposed 3-bit IF VGA. (b) Measured normalized receiver variable gain in all operating bands. (c) Input XTF of IF VGA.

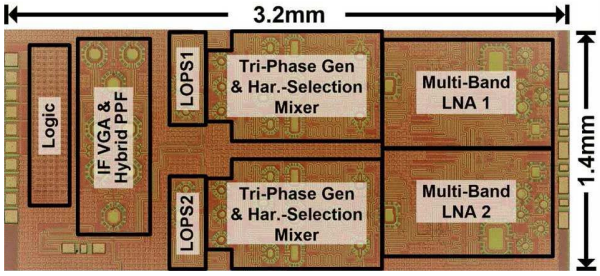


Fig. 18. Chip micrograph.

corresponding calibration accuracy is usually limited, and the power consumption is usually high. On the contrary, the IRR of Type-I PPF can be easily calibrated by simple and high-accuracy magnitude detections. Therefore, this work introduces a hybrid-type PPF to achieve both accurate

Selected Band	28GHz ($F_{LO}+F_{IF}$)	39GHz ($2\times F_{LO}-F_{IF}$)	47GHz ($2\times F_{LO}+F_{IF}$)	60GHz ($3\times F_{LO}-F_{IF}$)
LO Freq. Range	16-27GHz	21.5-26GHz	18-24.5GHz	21-25GHz

(a)

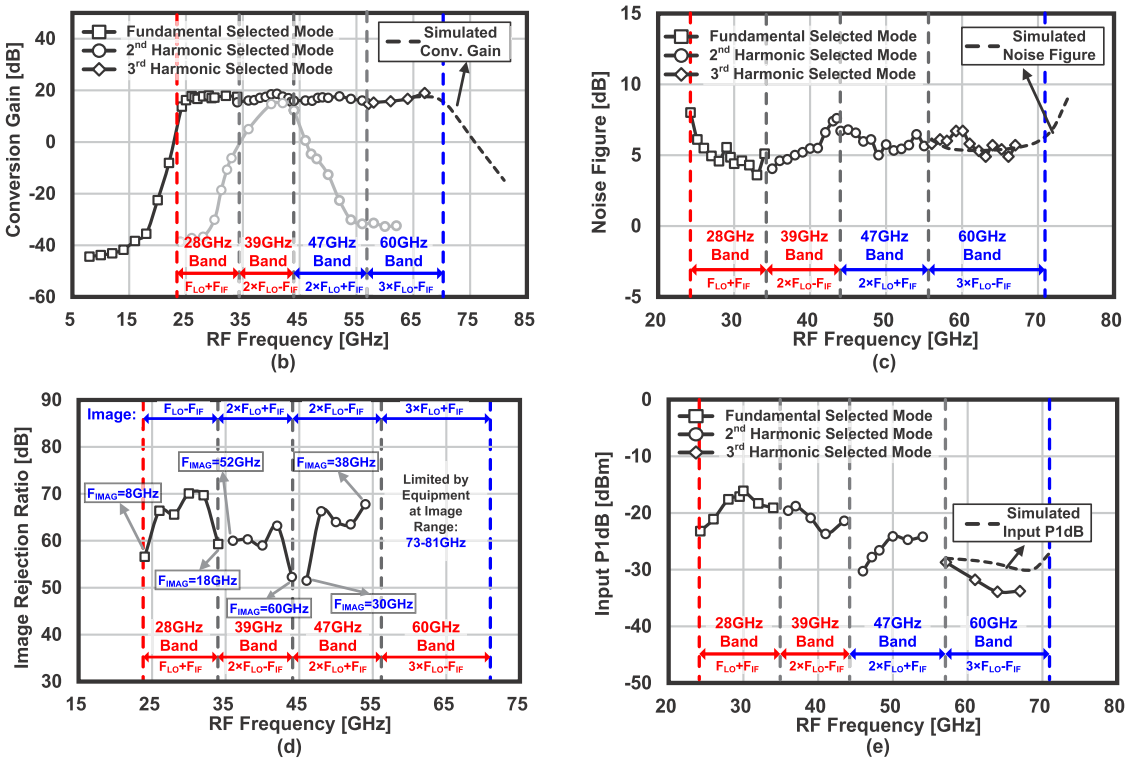


Fig. 19. (a) Required LO frequency range of the proposed receiver at all operating bands. (b) Measured and simulated CG with the single receiver channel. (c) Measured and simulated NF of the single receiver channel. (d) Measured and simulated input P1dB of the single receiver channel. (e) Measured IRRs of the proposed multi-band receiver at all operating bands.

IRR calibration and low IL

$$\mathrm{IRR}_{\mathrm{Type-I}} = \mathrm{IRR}_{\mathrm{Type-II}} = \left(\frac{f+f_C}{f-f_C}\right)^2. \tag{2}$$

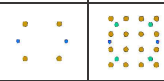
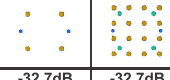
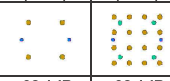
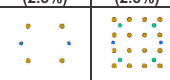
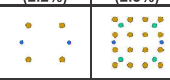
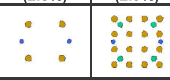
As explained in (2) [38], [41], Type-I and Type-II PPFs have identical IRR with peak frequency located at $f_C = 1/2\pi RC$ when R and C values are the same. The hybrid-type PPF can be reconfigured between Type-I and Type-II topologies while maintaining the same R and C values. The operation principle of the hybrid-type PPF is detailedly explained in Fig. 14. The hybrid-type PPF will be first configured in Type-I mode for IRR calibration. An 8-GHz test-tone signal is an input from the IF output node, while the I and Q ports of the hybrid-type PPF are connected to a magnitude detector. The R value is tuned to calibrate the I/Q magnitude imbalance depending on the readout value of the detector. Since Type-I and Type-II PPFs share the same IRR peak frequency f_C, the proposed PPF will keep the calibrated R value and directly switches to Type-II mode. Lower IL during normal operation could be, therefore, achieved, as shown in Fig. 14(c). f_C of the PPF is steered by tuning R_{on} of a triode-region transistor. With the help of analog-to-digital converter (ADC), RDAC, and serial peripheral interface (SPI) integrated into the digital block, the hybrid PPF calibration can operate automatically. The measured IRRs of the proposed PPF in both Type-I mode and Type-II mode are shown in Fig. 15(a) after calibration in Type-I mode. As demonstrated in the figure, the IRRs in Type-I and Type-II modes match with each other very well. As expected, Fig. 15(b) shows that the measured CG achieves a 2-dB improvement with the proposed hybrid-type PPF operating in Type-II mode.

The proposed hybrid-type PPF is calibrated with an on-chip differential detector, as shown in Fig. 16(a). The I/Q ports of the PPF share one magnitude detector to avoid mismatch. The differential detector senses the input voltage by an input transconductance stage followed by a current rectifier. The rectified current is then amplified and filtered to generate a dc voltage $\mathrm{VOUT}_{\mathrm{dc}}$ [42]. Another detector is applied at the IF output node to indicate the output power of the receiver, which is shown in Fig. 16(b). To extend the input dynamic range, multiple transconductance stages with bypass switches are introduced. Larger than 20-mV/dBm sensitivity can be achieved across a 40-dB signal power range in the simulation.

An IF VGA is inserted between before PPF and mixer to provide variable gain and isolation. The detailed circuit of the proposed phase-invariant IF VGA is shown in Fig. 17(a). The IF VGA is designed based on the current-steering topology with 3-bit coarse tuning and 10-bit fine-tuning [43], [44]. The IF selectivity can be improved by IF VGA with a fixed IF frequency at 8 GHz. A source degeneration inductor L_s is coupled and integrated with the input series inductor L_g, as shown in Fig. 17(a), to realize improved matching with compact area [37]. A transformer with capacitors at a center

TABLE I

MEASURED CONSTELLATIONS AND EVMS OF PROPOSED MULTI-BAND RECEIVER AT ALL BANDS

Modulation*			QPSK (MCS4)	16QAM (MCS10)	64QAM (MCS19)	256QAM (MCS27)
Mode			OFDMA	OFDMA	OFDMA	OFDMA
BW_c			400MHz	400MHz	400MHz	400MHz
Freq.	24.25GHz	Constellation				
		EVM (RMS)**	-32.0dB (2.5%)	-31.8dB (2.6%)	-31.6dB (2.6%)	-31.4dB (2.7%)
	28GHz	Constellation				
		EVM (RMS)**	-32.7dB (2.5%)	-32.7dB (2.3%)	-33.4dB (2.1%)	-33.5dB (2.1%)
	39GHz	Constellation				
		EVM (RMS)**	-32.1dB (2.5%)	-32.1dB (2.5%)	-31.9dB (2.5%)	-31.6dB (2.6%)
	47.2GHz	Constellation				
		EVM (RMS)**	-33.0dB (2.2%)	-32.7dB (2.3%)	-32.5dB (2.4%)	-32.4dB (2.4%)
	60GHz	Constellation				
		EVM (RMS)**	-30.9dB (2.8%)	-30.7dB (2.9%)	-30.5dB (3.0%)	-30.3dB (3.1%)
	71GHz	Constellation				
		EVM (RMS)**	-29.1dB (3.5%)	-29.0dB (3.5%)	-28.9dB (3.6%)	-28.9dB (3.6%)

*5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0).
**Measured EVMs are referred to the RMS magnitude.

TABLE II

POWER BREAKDOWN OF SINGLE RECEIVER CHANNEL OF THE PROPOSED MULTI-BAND RECEIVER AT ALL OPERATING MODES

Building Block	Dual-Mode Multi-band LNA	Harmonic-Selection Mixer	Tri-Phase LO	IFVGA	P_{DC}/Path
28GHz Band Mode	20mW	0mW	12mW	4mW	36mW
39GHz Band Mode	17mW	0mW	11mW	4mW	32mW
47GHz Band Mode	35mW	0mW	12mW	4mW	51mW
60GHz Band Mode	50mW	0mW	21mW	4mW	75mW

TABLE III

MEASURED (a) OVERALL INTER-BAND BLOCKERS REJECTION AND (b) CONSTELLATIONS AND EVMS OF PROPOSED RECEIVER WITH 0-dBc BLOCKER SIGNAL

Case	Case 1	Case 2	Case 3	Case 4
Desired Signal Freq.	28GHz ($F_{LO}+F_{IF}$)	39GHz ($2\times F_{LO}-F_{IF}$)	47.2GHz ($2\times F_{LO}+F_{IF}$)	60.1GHz ($3\times F_{LO}-F_{IF}$)
Fundamental Blocker Rejection (dB) ($F_{LO}\pm F_{IF}$)	66@12GHz	58@15.5GHz 56@31.5GHz	68@11.5GHz 61@27.6GHz	64@14.7GHz 36@30.7GHz
2nd Harmonic Blocker Rejection (dB) ($2\times F_{LO}\pm F_{IF}$)	57@32GHz 58@48GHz	60@55GHz	59@31.2GHz	46@37.4GHz 43@53.4GHz
3rd Harmonic Blocker Rejection (dB) ($3\times F_{LO}\pm F_{IF}$)	63@52GHz NA*@68GHz	59@62.5GHz NA*@78.5GHz	50@50.8GHz 50@66.8GHz	NA*@76.1GHz
Blocker F_{IF} - Desired F_{IF}	0Hz	0Hz	0Hz	0Hz

*Limited by equipment operation range.

(a)

Case		Case 1	Case 2	Case 3	Case 4
Desired Signal Freq.		28GHz ($F_{LO}+F_{IF}$)	39GHz ($2\times F_{LO}-F_{IF}$)	47.2GHz ($2\times F_{LO}+F_{IF}$)	60.1GHz ($3\times F_{LO}-F_{IF}$)
Desired Signal Mod.*		256QAM (MCS27)	256QAM (MCS27)	256QAM (MCS27)	256QAM (MCS27)
Desired Signal BW_c		400MHz	400MHz	400MHz	400MHz
Desired Signal Power		-39.1dBm	-45.3dBm	-41.9dBm	-37.0dBm
Worst Case Blocker in EVM Measurement		32GHz ($2\times F_{LO}-F_{IF}$)	31.5GHz ($F_{LO}+F_{IF}$)	50.8GHz ($3\times F_{LO}-F_{IF}$)	30.7GHz ($F_{LO}+F_{IF}$)
Blocker Modulation*		16QAM (MCS10)	16QAM (MCS10)	16QAM (MCS10)	16QAM (MCS10)
Blocker BW_c		400MHz	400MHz	400MHz	400MHz
Blocker Power Level**		0dBc	0dBc	0dBc	0dBc
Without Blocker	Constellation				
	EVM (RMS)	-33.5dB (2.2%)	-31.1dB (2.8%)	-31.8dB (2.6%)	-29.3dB (3.4%)
With Blocker	Constellation				
	EVM (RMS)	-33.5dB (2.2%)	-31.1dB (2.8%)	-31.8dB (2.6%)	-29.3dB (3.4%)

*5G NR MCS index table 2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0).
**Measured EVMs are referred to the RMS magnitude.

(b)

tap is utilized at the output of the VGA for providing matching with an improved common-mode rejection ratio (CMRR). Fig. 17(b) demonstrates the measured normalized variable gain of the proposed receiver in four operating modes. The IF frequency is fixed at 8 GHz in measurement. During the measurement, the proposed VGA realized a 9-dB gain tuning range with 5G standard compatible bandwidth.

IV. MEASUREMENT RESULTS

The proposed two-channel multi-band phased-array receiver is fabricated with a 65-nm CMOS process. Fig. 18 shows the micrograph of the proposed chip. The chip size is 3.2 mm × 1.4 mm, including the two-channel receiver element. Each element occupies 1.2-mm^2 core area while covering almost 50-GHz bandwidth. The single-path receiver characteristic is first on-wafer measured. Fig. 19(b) demonstrates the overall CG of a single receiver path. The proposed phased-array receiver supports 24.25–71-GHz operation covering all allocated spectrums in 5G NR FR2 with the help of the proposed harmonic-selection technique. Regarding a fixed IF frequency of 8 GHz, the required LO coverage is only 16.25–26 GHz to cover 24.25–71-GHz operations. The measured CGs in four different operating modes are all around 15 dB. Flat response is maintained in each mode with less than 2-dB variation. The IRRs in all four operating modes are measured with two receiver paths and shown in Fig. 19(c). Owing to the Hartley receiver architecture and the bandpass filtering of LNA, the measured IRRs are always better than 52 dB within all operating modes. Fig. 19(d) presents the measured single-channel NF. The measured NFs are 3.6–8.0, 4.0–7.6, 5.3–6.8, and 4.9–6.7 dB within 24.25–35, 35–44, 44–57, and 57–67 GHz, respectively. To be a reference, the measured NFs of the stand-alone LNA at 28, 39, 47, and 60 GHz are 4.4, 4.7, 5.4, and 6 dB, respectively. The measured input P1dB is shown in Fig. 19(e). The achieved IP1dBs are −17.6 dBm at 28 GHz, −20.1 dBm at 39 GHz, −26.6 dBm at 48 GHz, and −31.8 dBm at 61 GHz.

The proposed receiver is then evaluated with 5G standard-compliant OFDMA-mode modulated signals. The OFDMA-mode modulated signals are generated by a

TABLE IV
PERFORMANCE COMPARISON OF MULTI-BAND PHASED-ARRAY RECEIVER

	This work				UCSD [20]		Georgia Tech [18]		CMU [17]		UCSD [22]
Process	65nm CMOS Bulk				22nm CMOS, FD-SOI		22nm CMOS, PD-SOI		65nm CMOS Bulk		0.18μm SiGe BiCMOS
Integration	LNA, Harmonic-Selection Mixer, LOPS, IF, LO				LNA, Mixer, IF, LO		LNA, Mixer, IF, LO		LNA, VSPS, Mixer, BB, LO		LNA, RFPS
Frequency	24.25 ~ 71GHz				20 ~ 44GHz		24.5 ~ 43.5GHz		27 ~ 38.75GHz		15 ~ 57GHz
Noise Figure (dB)	24.25 ~ 35GHz	35 ~ 44GHz	44 ~ 57GHz	57 ~ 71GHz**	20 ~ 44GHz		24.5 ~ 43.5GHz		27 ~ 29.75GHz	35 ~ 38.75GHz	15 ~ 57GHz
	3.6~8.0	4.0~7.6	5.3~6.8	4.9~6.7**	3.3~5		3.2~6.1		5.7~8.0*	8.5~10*	5.1~7.4
IP1dB* (dBm)**	28GHz	39GHz	48GHz	61GHz	20GHz	40GHz	28GHz	39GHz	28GHz	37GHz	40GHz
	-17.6	-20.9	-26.6	-31.8	-25*	-29.5*	-25	-27	-30	-23	-30*
Inter-Band Rej. Architecture	Harmonic Selection, Hartley RX				N/A		Hartley RX		Hartley RX		N/A
Inter-Band Rejection	Rejection to All Other Bands				N/A		Dual-Band Rej. to 28/39GHz		Dual-Band Rej. to 28/39GHz		N/A
	28GHz	39GHz	47.2GHz	60.1GHz	N/A		28GHz		28GHz/37GHz		N/A
	>57dB	>56dB	>50dB	>36dB	N/A		56dB		>35dB		N/A
Modulation w. Inter-Band Blocker	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	256QAM MCS27 OFDMA	N/A		256QAM (SC mode only)		N/A		256QAM OFDMA
Blocker Level	0dBc	0dBc	0dBc	0dBc	N/A		0dBc		N/A		N/A
EVM w. Blocker	-33.3dB	-30.9dB	-31.6dB	-28.5dB	N/A		-29.2dB		N/A		N/A
P_{DC}/Path	36mW	32mW	51mW	75mW	70mW		60mW		77.5mW		180mW
Area/Path	1.2-mm^2				1.28-mm^2*		0.52-mm^2		0.55-mm^2		0.77-mm^2*

* Estimated from paper. ** Referred to peak constellation power. *** Measured without VGA.

Keysight VXG signal generator M9374B. For signals higher than 44 GHz, an extra up-conversion mixer is adopted. The LO signal is generated by the Keysight signal generator E8275D. The received signals are analyzed by the Keysight oscilloscope UXR1102A. The measured EVMs and constellations over 24.25–71 GHz with QPSK, 16QAM, 64QAM, and 256QAM modulations are listed in Table I. With the power consumption listed in Table II, this work achieves EVMs of −31.6 dB at 24.25 GHz, −33.4 dB at 28 GHz, −31.9 dB at 39 GHz, −32.5 dB at 47.2 GHz, −30.5 dB at 60.1 GHz, and −28.9 dB at 71 GHz with 64QAM modulation. In 256QAM modulation, the measured EVMs are −31.4 dB at 24.25 GHz. −33.5 dB at 28 GHz, −31.6 dB at 39 GHz, −32.4 dB at 47.2 GHz, −30.3 dB at 60.1 GHz, and −28.9 dB at 71 GHz.

As mentioned previously, the multi-band receiver suffers from inter-band blockers. This work utilizes the harmonic-selection technique, LNA bandpass filtering, and the Hartley receiver architecture to improve the rejections to inter-band blockers. In this work, the worst blocker case happens when the blocker frequencies locate at the harmonic or image frequencies of the desired signals. In these conditions, the down-converted IF will be at the exactly same frequency as the desired signal, which cannot be removed by the IF bandpass filtering. In this work, the inter-band blockers are analyzed with four cases, which are at 28, 39, 47.2, and 60.1 GHz. The rejections to harmonics and images in the abovementioned four cases are first measured and shown in Table III(a). This work achieves better than 36-dB rejections against the blockers located at the harmonic and image frequencies. The constellations and EVMs are also measured with inter-band blockers. The measurement setup for each operating mode is explained in Fig. 20. The Keysight VXG signal generator M9384B is utilized to generate the OFDMA-mode desired and blocker signals in 256QAM and 16QAM, respectively. For signals higher than 44 GHz, an additional mixer is employed.

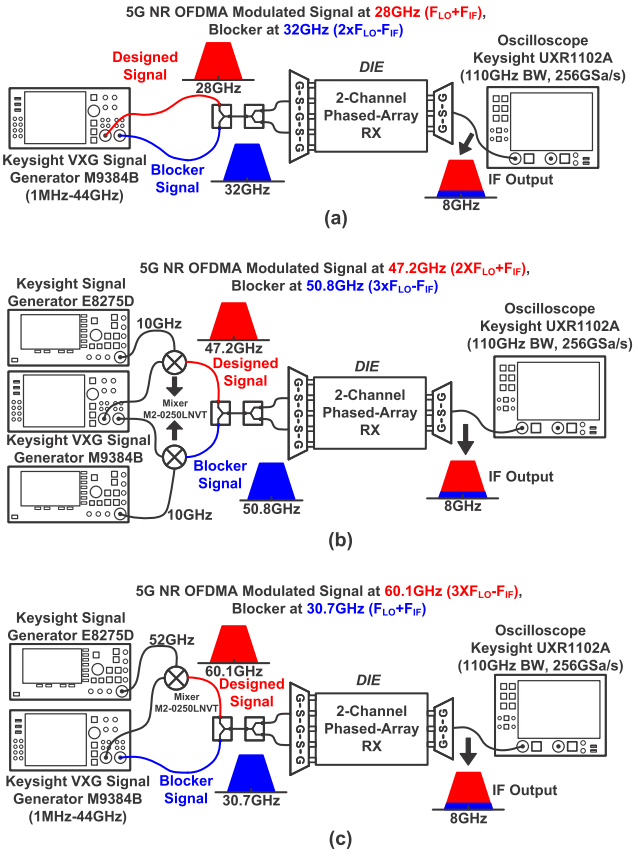


Fig. 20. Equipment setup for constellations and EVMs measurement with blockers for worst case on (a) 28-GHz mode, (b) 47-GHz mode, and (c) 60-GHz mode.

The worst case blocker frequency settings mentioned previously are applied in each case for convincing results. The measured EVMs and constellations are shown in Table III(b). Without the blockers, the proposed receiver demonstrates

EVMs of −33.5, −31.1, −31.8, and −29.3 dB at 28, 39, 47.2, and 60.1 GHz, respectively. With blockers on the same power level against desired signals, the measured EVMs are only slightly degraded to −33.3 dB at 28 GHz, −30.9 dB at 39 GHz, −31.6 dB at 47.2 GHz, and −28.5 dB at 60.1 GHz. The wideband modulated 256QAM signal is still supported with enough margin to meet the 5G NR standard.

Table IV compares this work with other state-of-the-art multi-band receivers designed for 5G NR FR2 [17], [18], [20], [22]. Thanks to the proposed harmonic-selection technique, this work supports the 24.25–71-GHz operation while maintaining over 36-dB inter-band blocker rejection. Each channel of the proposed receiver only consumes 36, 32, 51, and 75 mW when operating at 28, 39, 47.2, and 60.1 GHz, respectively. The proposed receiver can support ultra-wideband operation with minimized power consumption and improved inter-band blocker rejections.

V. Conclusion

In this work, a two-channel multi-band phased-array receiver with a proposed harmonic-selection technique is introduced. The frequency coverage of 24.25–71 GHz makes the receiver compatible with all existing 5G NR FR2 bands and the potential 60-GHz band. Cooperating with the dual-mode multi-band LNA and Hartley architecture, this work realizes rejections to inter-band blockers better than 57, 56, 50, and 36 dB at 28, 39, 47.2, and 60.1 GHz, respectively. As a result, the proposed receiver can support 400-MHz standard-compliant 5G NR modulated signals in 256QAM even regarding 0-dBc worst case inter-band blockers. The power consumptions per channel are only 36, 32, 51, and 75 mW at 28, 39, 47.2, and 60.1 GHz, respectively. The low-cost and energy-efficient multi-band phased-array receiver adapting to the evolving 5G NR standard with enhanced inter-band blocker rejections can be realized.

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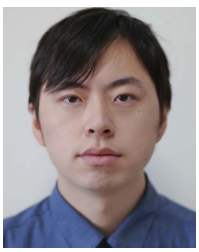

Yi Zhang (Graduate Student Member, IEEE) received the B.E. degree in microelectronic science and engineering from the Southern University of Science and Technology (SUSTech), Shenzhen, China, in 2018, and the M.E degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include both mixed-signal circuit design for millimeter-wave CMOS phased-array transceiver and power-efficiency receiver designs for fifth-generation (5G) and beyond-5G communication systems.

Jian Pang (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

From 2019 to 2020, he was a Post-Doctoral Researcher with the Tokyo Institute of Technology. From 2020 to 2022, he was a Special-Appointed Assistant Professor with the Tokyo Institute of Technology. He is currently a Special-Appointed Associated Professor with the Tokyo Institute of Technology, focusing on fifth-generation (5G) millimeter-wave systems. His current research interests include high-data-rate low-cost millimeter-wave transceivers, power-efficient power amplifiers for fifth-generation (5G) mobile systems, multiple-in multiple-out (MIMO), and mixed-signal calibration systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Pre-Doctoral Achievement Award for the term 2018–2019, the Seiichi Tejima Oversea Student Research Award in 2020, and the IEEE MTT-S Japan Young Engineer Award in 2021.

Zheng Li (Graduate Student Member, IEEE) received the B.E. and M.E. degrees in microelectronics and solid electronics from Xidian University, Xi'an, China, in 2014 and 2017, respectively. He is currently pursuing the Ph.D. degree in electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan, working on fifth-generation (5G) radio frequency (RF) front-end and system design.

His current research interests include millimeter-wave CMOS wireless transceivers and fifth-generation (5G) mobile systems.

Minzhe Tang (Student Member, IEEE) received the B.E. degree in microelectronic science and engineering from the Southern University of Science and Technology (SUSTech), Shenzhen, China, in 2020, and the M.E. degree in electrical and electronics engineering from the Tokyo Institute of Technology. Tokyo, Japan, in 2022, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include millimeter-wave CMOS wireless transceivers for fifth-generation (5G) mobile systems.

Yijing Liao received the B.E. degree from the Civil Aviation University of China, Tianjin, China, in 2020, and the M.E. degree in electrical and electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2022.

Her research interests include millimeter-wave CMOS wireless transceivers for fifth-generation (5G) mobile systems.

Ashbir Aviat Fadila (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Institut Teknologi Bandung, Bandung, Indonesia, in 2015, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

From 2015 to 2016, he was a Standard Cells Mask Layout Engineer with Marvell Technology Indonesia, Jakarta, Indonesia. From 2016 to 2017, he was a Research Assistant with the Institut Teknologi Bandung, researching system-on-chip (SoC) for IoT applications. His current research interests include analog-mixed signals, data converters, and synthesizable analog circuits.

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed an 802.11ax Wireless local area network (LAN) radio frequency (RF) transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motors with wireless communication. He is currently an Assistant Professor with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include RF CMOS transceivers for IoT, fifth generation (5G), and satellite communication.

Dr. Shirane is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science, Kyoto University. In 2003, he joined the Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor. He is currently a Professor of electrical and electronic engineering with the Tokyo Institute of Technology. He has authored or coauthored more than 400 journal articles and conference papers. His current research interests include millimeter-wave CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for fifth generation (5G), wireless gigabit alliance (WiGig), satellite and future wireless systems, digital phase-locked loop (PLL), synthesizable PLL, atomic clock, ultra-low-power wireless transceivers for Bluetooth low-energy, and sub-GHz applications.

Prof. Okada is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He is/was a member of the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC), the VLSI Circuits Symposium, the European Solid-State Circuits Conference (ESSCIRC), and the Radio Frequency Integrated Circuits Symposium (RFIC). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Awards in 2006 and 2011, the ASP-DAC Special Feature Award in 2011, the Best Design Awards in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, and more than 40 other international and domestic awards. He also is/was a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).