An Automatic Loop Gain Enhancement Technique in Magnetoimpedance-Based Magnetometer

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***Abstract*— A low-power, low-noise, and high-bandwidth magnetometer that utilizes the magnetoimpedance (MI) element as a sensor head is presented. The MI element has a high sensitivity, and it can be implemented in the mm-scale through the MEMS process. The analog front-end (AFE) circuit of the magnetometer includes a digital calibration scheme that automatically enhances the loop gain of the system, resulting in high bandwidth and low-noise characteristics. The AFE circuit is designed based on a switched-capacitor (SC) approach, and its dedicated switching scheme can suppress the folded noise of an amplifier. A single-coil magnetic negative feedback architecture with correlated double sampling (CDS) enables to achieve a high dynamic range (DR) and stable passband gain in addition to simplifying the structure of the MI element. The AFE chip of the magnetometer is implemented in a 0.18-μm CMOS process, and it achieves an 8-pT/$\sqrt{}$Hz noise floor within a 31-kHz bandwidth and the DR of 96 dB, where the power consumption is 1.97 mW.**

***Index Terms*— Analog front-end (AFE), biomagnetic, digital calibration, Internet of Things (IoT), magnetic feedback, magnetoimpedance (MI) element, magnetometer.**

I. Introduction

A BIOMAGNETIC sensing technique such as magnetomyography (MMG) or magnetoencephalography (MEG) is one solution for capturing biological information with a minimum invasive approach. Implantable MMG has the potential to acquire fast neuronal magnetic activity, which corresponds to the action potential of neurons close to skeletal muscle with high spatiotemporal resolution [1], [2], [3], as opposed to an approach with an optically pumped magnetometer that achieves low noise but a relatively large size because of the optical system [4]. Magnetometers for such applications require of low noise less than 100 pT/$\sqrt{}$Hz, high bandwidth over 10 kHz, low power, and small size because they are implanted. Furthermore, a wide input range over 100 μT is desired because there is a need to accept the geomagnetic field and artifact without saturating the signal. A magnetic negative feedback approach can be applied to realize a high dynamic-range (DR) magnetometer because it provides a wide linear input range and a stable passband gain.

For a low-noise solution, magnetometers based on fluxgate (FG) [5], [6], [7] and fundamental-mode orthogonal FG [8], [9], [10] have achieved few pT/$\sqrt{}$Hz-level noise floor for the applications of aerospace, geomagnetic observatories, and nondestructive testing. However, these magnetometers cannot be implanted because the size of the sensor head tends to be large. Magnetometers with integrated FG (IFG) have been developed for small-sized realizations [11], [12], [13], [14], where its noise floors are relatively high, around a few nT/$\sqrt{}$Hz. FG-based magnetometers require a larger excitation current for saturating magnetization of a core in the FG sensor heads. Approaches using magnetoresistance (MR) [15] such as giant MR (GMR) [16] and tunneling MR (TMR) [17], [18] can be implemented in few tens of micrometer scale, and they have been designed for sensing the magnetic nanoparticle and biomagnetic field. TMR-based magnetometers with high sensitivity have achieved few tens of pT/$\sqrt{}$Hz noise floor. Its available input range, however, is less than 10 nT, which leads to signal saturation because of geomagnetic and artifact [17]. Although a magnetometer using hybrid architecture containing hall and coil sensors has an extremely large input range over few mT with a MHz bandwidth [19], [20], a noise level over 100 nT/$\sqrt{}$Hz is large for biomagnetic applications. The use of the magnetoimpedance (MI) element as a sensor head is an attractive approach for realizing magnetometers with compact, high DR, low noise, and low power, because of the high sensitivity and low excitation current into the sensor head [21], [22]. The analog front-end (AFE) circuits for MI elements have been developed with discrete components, and they achieved a noise floor of few pT/$\sqrt{}$Hz using the millimeter-scale sensor heads [23], [24], [25], [26].

A low-power, low-noise MI-based magnetometer with high DR is presented in this article, and we introduce mainly three techniques: 1) digital calibration for enhancing loop gain in a magnetic negative feedback loop; 2) switching scheme for lowering noise; and 3) single-coil architecture with correlated double sampling (CDS) for both pickup and magnetic feedback. This article is the extended version of our previously published magnetometer [27], and the details of the theoretical analysis and simulation results are included. Furthermore, the prototype chip is refined in terms of digital and analog designs, and new measurement results are provided.

The rest of the article is organized as follows. Section II describes the proposed MI-based magnetometer by introducing

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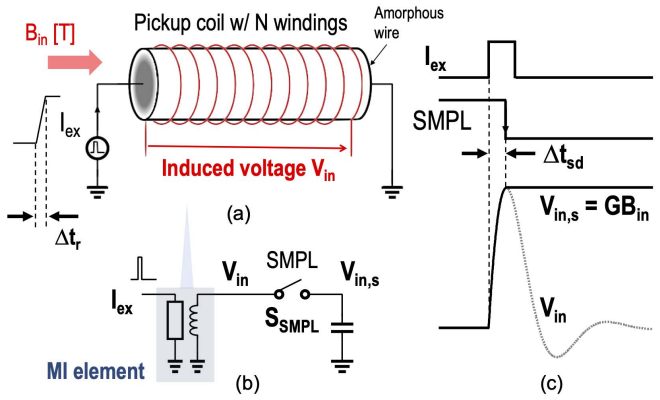

Fig. 1. MI-based magnetic sensing. (a) MI element, (b) sensing principle using peak sampling, and (c) its waveforms.

the fundamentals of the MI element and details of the technical features. The overall chip architecture and circuit details are presented in Section III. In Section IV, the measurement results of the prototype magnetometer and discussions are shown and compared with other state-of-the-art designs. Finally, Section V concludes the article.

II. MI-Based Magnetometer

A. Magnetic Field Sensing Using the MI Element

The MI element comprises an amorphous alloy wire with a diameter of few micrometers and a coil wounded around the wire as illustrated in Fig. 1(a) [22], [28], [29], [30]. If a current pulse I_{ex} with a fast transition time Δt_r is applied to the wire, the skin effect arises and the magnetization vector toward the surrounding direction of the wire surface rotates, which results in a magnetization change ΔM proportional to the external magnetic flux density B_{in}. The magnetic flux change $\Delta\phi$ on the surface is proportional to ΔM, and $\Delta\phi$ can be picked up by the coil as the induced voltage $V_{\text{in}} = N\Delta\phi/\Delta t_r$, where N represents the number of coil turns. Therefore, the peak voltage of the obtained V_{in} has a linear relation to B_{in}, and it can be captured using a simple sample and hold circuit as shown in Fig. 1(b), where B_{in} can be detected parallel to the wire. If the switch S_{SMPL} is driven by a clock SMPL with an appropriate sampling timing corresponding to the moment for the peak voltage of V_{in}, a sampled peak voltage $V_{\text{in},s}$ on the sampling capacitor is obtained as illustrated in Fig. 1(c), and can be expressed as

$$V_{\text{in},s} \approx G_0\left(\frac{G_1}{\sqrt{\Delta t_r}} - 1\right)B_{\text{in}} \tag{1}$$

where G_0 and G_1 represent parameters depending on the fabrication of the device and materials of the MI element [22]. The first and second factors of the right-hand side in (1) correspond to the intrinsic sensitivity of the MI-based magnetic sensor head; $G = G_0(G_1/\sqrt{\Delta t_r} - 1)$. As seen from (1), G can be increased by using the excitation current with a faster rising edge because G is inversely proportional to $\sqrt{\Delta t_r}$.

This approach that utilizes the current pulse and peak sampling shown in Fig. 1 allows saving the power consumption for the excitation of the sensor head because it dissipates a large current up to 50 mA only during a short period, less than few tens of nanoseconds, to have one sampled signal corresponding to the external magnetic field.

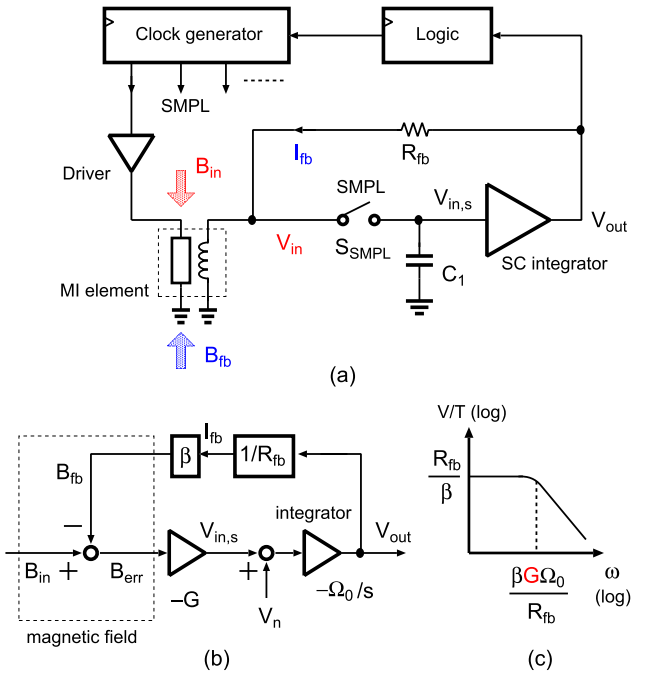

Fig. 2. MI-based magnetometer: (a) architecture, (b) simple linear model, and (c) frequency response with the bandwidth of $G\Omega_0$.

B. Architecture

Fig. 2(a) shows the basic architecture of the designed MI-based magnetometer that includes an MI element as a sensor head, a switched-capacitor (SC) integrator with a peak sampler, a clock generator to create clocks for the sampler, and the SC integrator, driver for the wire of the MI element, and logic circuit for a calibration described later. The peak sampling is done by the sampler as described in the previous subsection, and the obtained $V_{\text{in},s}$ proportional to B_{in} is integrated into a charge domain at the latter SC integrator.

The magnetometer adopts the magnetic negative feedback that the output voltage V_{out} is feedbacked as a current I_{fb} through a resistor R_{fb}. This I_{fb} flows into the coil and creates a magnetic flux density B_{fb}, the direction of which is opposite to B_{in}, where I_{fb} is linearly converted to B_{fb} with the coil based on the Ampere's Law. This can be expressed using a coefficient β; $B_{\text{fb}} = \beta I_{\text{fb}}$. A simple linear model of the magnetometer is shown in Fig. 2(b), where the transfer function of the SC integrator is expressed as a continuous-time model for simplicity; Ω_0/s. Therefore, the subtraction of B_{in} and B_{fb} is performed in a magnetic field domain, and its difference B_{err} will settle to zero with a large loop gain because this architecture forms the negative feedback. This implies the passband gain is almost determined by the parameters of components in the feedback path ideally, and the transfer function becomes

$$V_{\text{out}} = \frac{R_{\text{fb}}}{\beta}\cdot\frac{1}{\dfrac{R_{\text{fb}}}{\beta G\Omega_0}s + 1}\cdot B_{\text{in}} \tag{2}$$

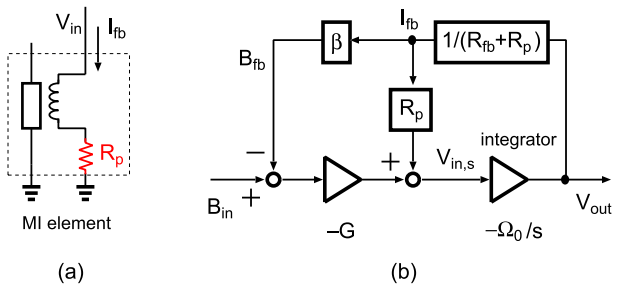

Fig. 3. Effect of parasitic resistor R_p in the coil: (a) equivalent circuit of the MI element and (b) linear model of the magnetometer with R_p.

where the intrinsic sensitivity of the MI element G, which tends to vary between devices, does not affect the passband gain directly. In addition, the nonlinearity of G is suppressed in the same manner as general negative feedback. The corresponding frequency response is shown in Fig. 2(c), and the bandwidth is $\beta G\Omega_0/(2\pi R_{\rm fb})$. In this design, the magnetic feedback is realized using only a single coil for both pickup and magnetic feedback, while two coils are generally used for each purpose. The single-coil approach has been utilized in some FG- and MI-based magnetometers for low-cost and small-size realizations [9], [11], [25].

There are several challenges when designing the MI-based magnetometer using the single-coil architecture shown in Fig. 2(a). As shown in Fig. 1(c), the intrinsic sensitivity G depends on a sampling timing for peak sampling, which is a time duration from the rising edge of $I_{\rm ex}$ to the falling edge of SMPL; it is defined as a sampling delay $\Delta t_{\rm sd}$. If $\Delta t_{\rm sd}$ is slightly changed from the moment of the peak of $V_{\rm in}$, $V_{{\rm in},s}$ is decreased and it indicates the degradation of G. This optimum timing for the peak sampling is changed between devices because of the variation of the resonance frequency at the coil terminals. Therefore, G represents a function of not only Δt_r, but $\Delta t_{\rm sd}$. Although the influence of the varied G in terms of the passband gain stability can be suppressed using magnetic negative feedback, G is directly involved with its bandwidth as shown in Fig. 2(c). In addition, since G is located before the integrator, the larger G plays a role in reducing the contribution of the integrator's noise at the output. If it is assumed that the input-referred noise power of the integrator is $\overline{V_n^2}$ as shown in Fig. 2(b), the input-referred noise power of the magnetometer, $\overline{B_{{\rm in},n}^2}$, in the passband can be expressed as

$$\overline{B_{{\rm in},n}^2} \approx \frac{1}{G^2}\overline{V_n^2}. \tag{3}$$

Therefore, it is important to keep G as large as possible, and it can be realized by finding the optimum $\Delta t_{\rm sd}$ that the sampler can capture the peak of $V_{\rm in}$. This can be achieved by a digital calibration scheme, which is described in Section II-C.

The single coil is used for both pickup and feedback to achieve low cost and compact realization. However, an intended drop voltage is sampled on a capacitor C_1 due to a parasitic resistor R_p of the coil and the feedback current $I_{\rm fb}$ as shown in Fig. 3(a), in addition to the desired signal component from the input magnetic field. In this situation, the magnetometer with the MI element including R_p is modeled

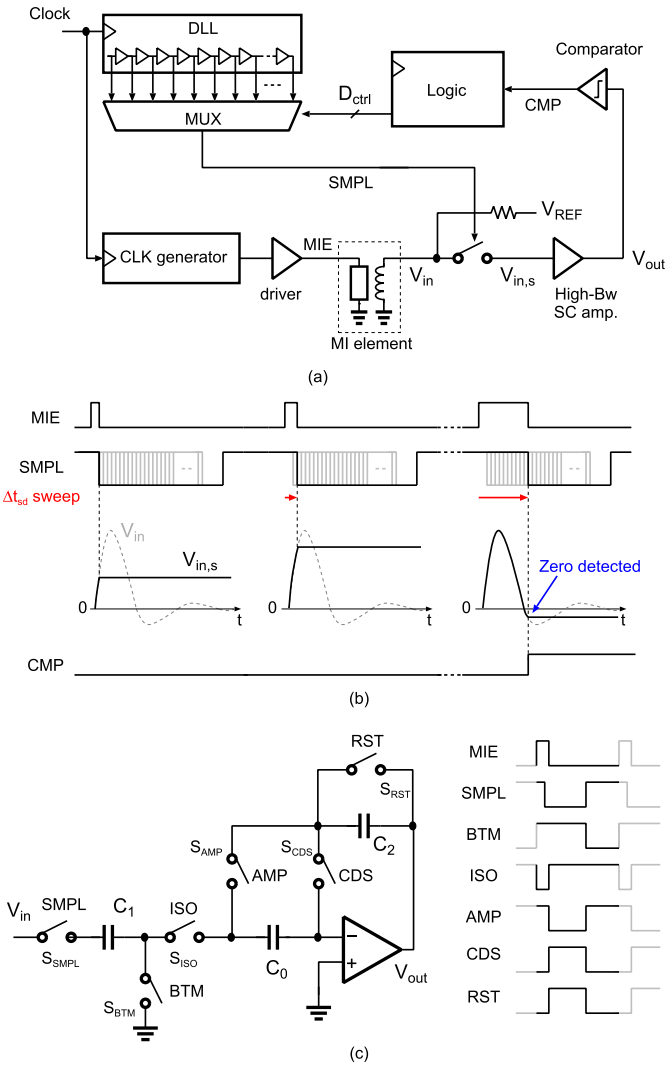

Fig. 4. Automatic digital calibration for finding the optimum sampling delay timing $\Delta t_{\rm sd}$: (a) circuit diagram in the calibration mode, (b) timing chart, and (c) SC amplifier circuitry for the zero-crossing detector.

as shown in Fig. 3(b); thus, the passband gain is derived as

$$\left|\frac{V_{\rm out}}{B_{\rm in}}\right|_{\omega=0} = \frac{G(R_{\rm fb}+R_p)}{G\beta+R_p} \tag{4}$$

where the variation of G affects the passband gain. This means that R_p deteriorates the effectiveness of the magnetic negative feedback, and a solution for this issue is provided using a CDS technique in Section II-D.

C. Automatic Digital Calibration Technique for Enhancing Loop Gain

A digital calibration scheme is proposed to search for the optimum $\Delta t_{\rm sd}$ automatically, as shown in Fig. 4. Fig. 4(a) illustrates the circuit diagram during the calibration where magnetic negative feedback is removed and a constant magnetic field is applied to the wire through a resistor and bias voltage, $V_{\rm REF}$. The SC integrator is reconfigured to be an SC amplifier with high gain and high bandwidth. This configuration shown in Fig. 4(a) measures the sensitivity G determined only by $\Delta t_{\rm sd}$ because the frontend circuit amplifies $V_{{\rm in},s}$ for a constant

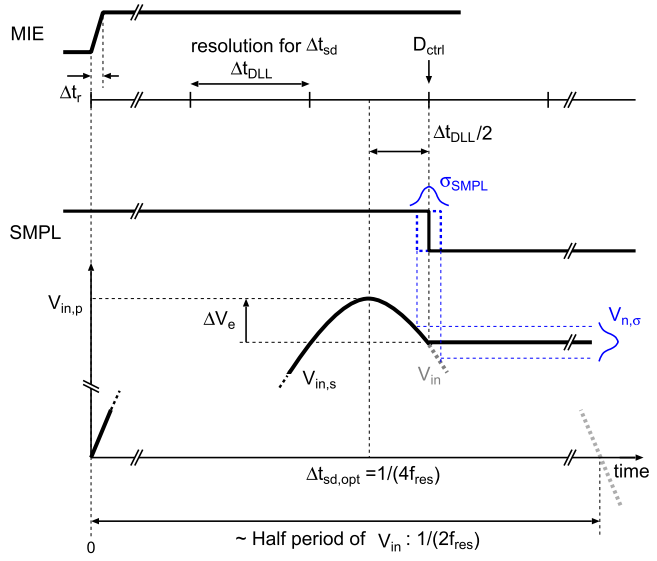

Fig. 5. Effects of the limited resolution of delay chain in DLL Δt_{DLL} and jitter for the sampling delay Δt_{sd}.

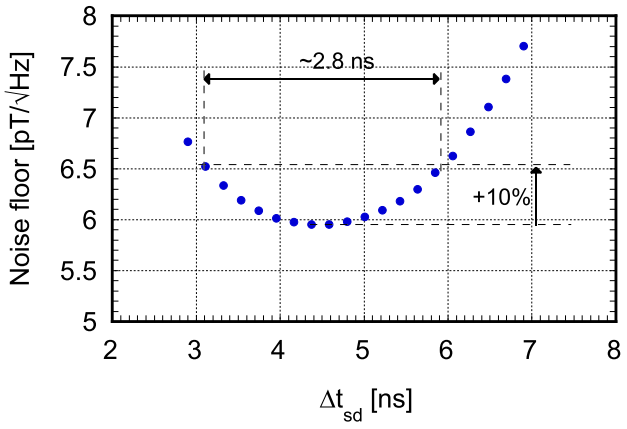

Fig. 6. Simulated relationship between noise floor and Δt_{sd} to estimate the required time resolution Δt_{DLL} in DLL.

magnetic field. The presented calibration is based on an automatic trimming approach; the adjustment of the sampling phase denoted by SMPL in Fig. 4(a) is accomplished using a delay-locked loop (DLL) circuit and multiplexer (MUX). The calibration procedure is explained as follows. In the calibration mode, after locking the DLL, the first sampling is performed by SMPL with the minimum Δt_{sd} set through MUX according to a digital code D_{ctrl} from the logic shown in Fig. 4(b). In the following steps, D_{ctrl} is swept sequentially, and the maximized sensitivity of the MI element is found by monitoring V_{out}. However, it is difficult to find the exact peak timing of V_{in} directly because the system assumes an analog output and does not have an ADC. Instead of using ADC to detect the peak, the presented calibration scheme utilizes an indirect approach that employs a comparator as a zero-crossing detector at the output, where the comparator detects a half period of the resonant frequency of the impedance between the coil terminals, which is almost constant for each sample. If the output of the comparator is activated, the logic stops the Δt_{sd} sweep and finishes the calibration. Thus, the optimum Δt_{sd} can be obtained as nearly half of the zero-crossed timing. Although the detection accuracy of the presented calibration scheme relies on that of the comparator, its requirements on noise and offset can be drastically relaxed because the SC amplifier, using CDS to eliminate the offset voltage and flicker noise as shown in Fig. 4(c) [31], acts as a preamplifier of the comparator [32], resulting in low power and simple realization.

The time duration for each delay element in the DLL is an important design parameter for determining the intrinsic sensitivity of the MI element. A jitter in Δt_{sd} for SMPL should also be considered. Fig. 5 shows a timing model that expresses the effects of the limited time resolution in the DLL, Δt_{DLL}, and the jitter effect on the sampled voltage $V_{\mathrm{in},s}$. In an ideal case, $V_{\mathrm{in},s}$ is acquired at the peak of V_{in}. If the expected resonance frequency of the induced voltage and amplitude of V_{in} are defined as f_{res} and $V_{\mathrm{in},p}$, respectively, the optimum sampling delay $\Delta t_{\mathrm{sd,opt}}$ becomes almost $1/(4f_{\mathrm{res}})$, where $V_{\mathrm{in},s} \approx V_{\mathrm{in},p}$. However, since this timing is quantized with Δt_{DLL}, this instance is slightly different, and the error voltage from the ideal peak ΔV_e can be obtained as

$$\Delta V_e = V_{\mathrm{in},p}\left[1 - \sin\left(\frac{\pi}{2} - \pi f_{\mathrm{res}} \Delta t_{\mathrm{DLL}}\right)\right] \tag{5}$$

where the worst-case timing for SMPL is assumed as $\Delta t_{\mathrm{sd}} = \Delta t_{\mathrm{sd,opt}} + \Delta t_{\mathrm{DLL}}/2$. Therefore, the intrinsic sensitivity G is decreased by the ratio of $\Delta V_e / V_{\mathrm{in},p}$ and it can be updated as G'

$$\begin{aligned} G' &= G(\Delta t_r)\left(1 - \frac{\Delta V_e}{V_{\mathrm{in},p}}\right) \\ &= G(\Delta t_r)\sin\left(\frac{\pi}{2} - \pi f_{\mathrm{res}} \Delta t_{\mathrm{DLL}}\right). \end{aligned} \tag{6}$$

In this design, the required Δt_{DLL} can be obtained by providing an acceptable change in G' from the highest sensitivity G. This sensitivity change is associated with the noise change from (3), and thus, if an acceptable noise change is provided as a specification, Δt_{DLL} can be specified. For example, a 10% increase in noise floor is allowed, G can be decreased by 1/1.1 through (6), and thus, a Δt_{DLL} of almost 2.74 ns is calculated, where the maximum f_{res} is assumed as 50 MHz. The simulated spot noise at 100 Hz for different Δt_{sd} is shown in Fig. 6, and a 10% noise degradation is confirmed within a 2.8-ns range, which is almost the same as the calculated value.

In addition to the above discussion about systematic error due to Δt_{DLL}, the effect of jitter at SMPL on the sampled voltage $V_{\mathrm{in},s}$ should be analyzed by using the same model. As the rising edge of the driving current into the wire denoted as MIE in Fig. 5 is synchronized with SMPL, a jitter of MIE can be merged with that of SMPL, and a random jitter with a standard deviation of σ_{SMPL} is assumed for SMPL in this analysis. The transfer gain G_σ from σ_{SMPL} to $V_{\mathrm{in},s}$ can be simply modeled as the slope at $t = \Delta t_{\mathrm{sd,opt}} + \Delta t_{\mathrm{DLL}}/2$, and thus it becomes

$$G_\sigma = 2\pi f_{\mathrm{res}} V_{\mathrm{in},p} \cos\left(\frac{\pi}{2} + \pi f_{\mathrm{ref}} \Delta t_{\mathrm{DLL}}\right). \tag{7}$$

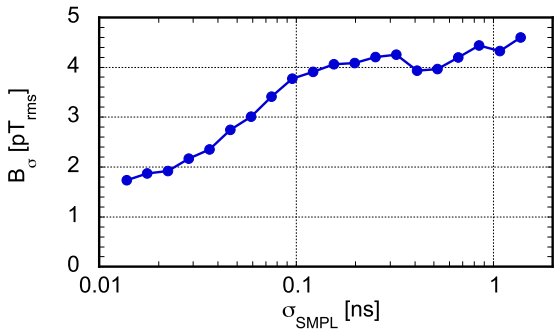

Fig. 7. Simulated random jitter contribution to the input-referred noise B_σ in rms.

If the input-referred noise power associated with σ_{SMPL} in the magnetometer is defined as $\overline{B_\sigma^2}$, it can be derived as

$$\overline{B_\sigma^2} = \left(\frac{G_\sigma}{G'}\right)^2 \sigma_{\mathrm{SMPL}}^2 = B_{\mathrm{err}}^2 \left[\frac{2\pi f_{\mathrm{res}}}{\tan\left(\frac{\pi}{2} - \pi f_{\mathrm{res}} \Delta t_{\mathrm{DLL}}\right)}\right]^2 \sigma_{\mathrm{SMPL}}^2 \tag{8}$$

where $B_{\mathrm{err}} = V_{\mathrm{in},p}/G$ is the magnetic flux density in the wire, and therefore, this jitter-related noise depends on the signal amplitude. Since B_{err} also corresponds to $B_{\mathrm{in}} - B_{\mathrm{fb}}$ in the magnetic negative feedback as shown in Fig. 2(b), it becomes almost zero if the loop gain is sufficiently large, which can be easily realized by a lossless SC integrator [33], [34]. Fig. 7 shows the simulated random jitter contribution to the input-referred noise, where B_σ is less than 5 pT$_{\mathrm{rms}}$ over σ_{SMPL} up to 1.4 ns. Since 5 pT$_{\mathrm{rms}}$ corresponds to 22.4 fT/$\sqrt{\mathrm{Hz}}$ floors if a 500-kHz bandwidth is assumed, the contribution of σ_{SMPL} is quite small compared with the overall noise floor of the magnetometer, which is a few pT/$\sqrt{\mathrm{Hz}}$, and therefore, it is negligible in this design. Hence, the magnetic negative feedback plays an important role in drastically reducing the requirement on the jitter of SMPL.

The accuracy of the zero-crossing detector determines the effectiveness of the proposed calibration, and it is characterized as the input-referred offset and rms noise voltages, which are represented in the form of standard deviation as $\Delta V_{z,n}$. Since the SC amplifier acts as a preamplifier of the comparator in the zero-crossing detector, $\Delta V_{z,n}$ corresponds to the input-referred noise or the offset voltage of this amplifier. Therefore, it is important to specify the required $\Delta V_{z,n}$ to achieve the desired accuracy of the calibration, and it can be used to design the SC amplifier and comparator. $\Delta V_{z,n}$ is associated with the provided f_{res} and Δt_{DLL}, and the same parameters are considered as an example. Fig. 8 shows the waveforms of $V_{\mathrm{in},p}$ and the relation to $\Delta V_{z,n}$ for $f_{\mathrm{res}} = 50$ MHz and $\Delta t_{\mathrm{DLL}} \approx 2.74$ ns. In this case, since the target D_{ctrl} should be 2, the zero-crossing detector should be activated at $D_{\mathrm{ctrl}} = 4$ or 5 in the calibration procedure, where it is assumed that the decimal point is suppressed upon determining the final D_{ctrl}. Therefore, activation at $D_{\mathrm{ctrl}} = 3$ and deactivation at $D_{\mathrm{ctrl}} = 6$ must be avoided for the success of the calibration, and these situations occur when the offset

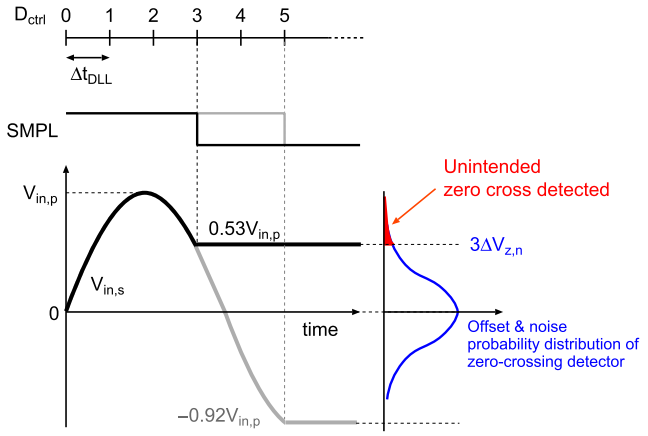

Fig. 8. Offset and noise model in the zero-crossing detector; in the case of f_{res} = 50 MHz and Δt_{DLL} = 2.74 ns.

and noise of the zero-crossing detector exceed the $V_{\mathrm{in},s}$'s. In particular, since $V_{\mathrm{in},s}$ at $D_{\mathrm{ctrl}} = 3$ is closer to zero, an unintended activation will occur with a certain probability defined by $\Delta V_{z,n}$. If it is assumed that the $|V_{\mathrm{in},s}|$ should be three times larger than the standard deviation of the offset and noise of the zero-crossing detector to prevent the error, the condition can be formulated as

$$3\Delta V_{z,n} < |\alpha_{\min} V_{\mathrm{in},p}| \tag{9}$$

where $\alpha_{\min} = 0.53$, which is determined by the combination of f_{res} and Δt_{DLL}. The above consideration in the worst case with f_{res} and Δt_{DLL} can provide the specification for the zero-crossing detector. Cases with different f_{res} and Δt_{DLL} need not be considered because a lower f_{res} or a finer Δt_{DLL} will relax $\Delta V_{z,n}$.

As the calibration for automatically finding the peak timing of the induced voltage is a type of foreground one, the timing and frequency to perform the calibration should be considered, which depends on the applications. Although f_{res} varies for different samples, it does not drift because f_{res} is determined by the impedance of the coil, which is almost independent of temperature and supply voltage. Therefore, it is considered that the calibration at power-on timing is appropriate for some applications, and the calibration rate can be defined by the user if needed.

D. SC-Based AFE Circuit for MI-Based Magnetometer

Fig. 9 shows the detailed AFE circuitry with its timing diagram. The AFE circuit operates with three phases: sampling, hold/CDS, and amplifying as shown in Fig. 10, and this includes two important features. One is to introduce the switch S_{ISO} for isolating the sampling part from the opamp side, resulting in a low-noise characteristic. Another is that an additional CDS technique is implemented during the amplifying phase to suppress an influence of a parasitic resistor R_p in the coil of the MI element. The detailed explanations and effects of these two features are provided in this section using each phase shown in Fig. 10.

In the sampling phase shown in Fig. 10(a), the feedback current I_{fb} flows in the coil to form negative feedback in the

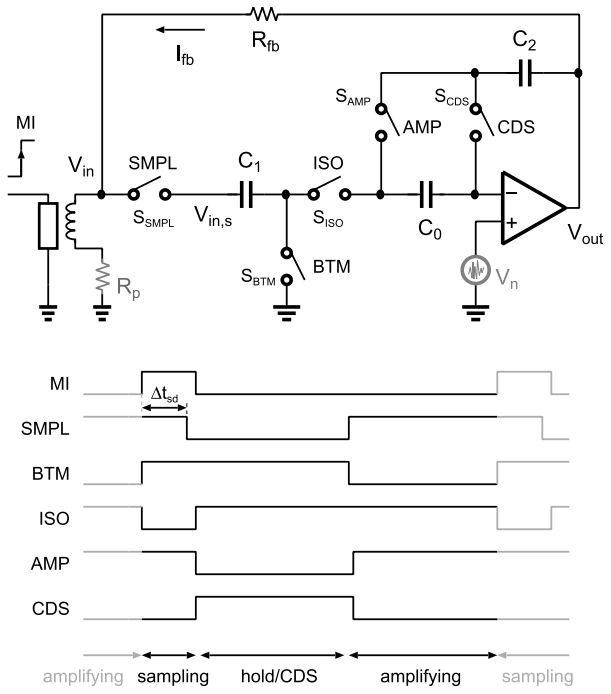

Fig. 9. AFE circuit of the MI-based magnetometer and its timing diagram.

magnetic field domain, whereas the peak of V_{in} is sampled at the instance of the negative edge of SMPL. Since I_{fb} is generated by V_{out} through R_{fb}, the noise of the opamp directly affects the signal quality of $V_{\text{in},s}$, in particular, the noise folding attributed to sampling by S_{SMPL}. Therefore, the noise spectrum around the sampling frequency f_s should be considered for low-noise design. As shown in the proposed AFE circuit in Fig. 9, the switch S_{ISO} plays an important role in minimizing the folding noise as well as in avoiding the influence of parasitic capacitance of C_1. During the sampling phase, C_2 holds a charge corresponding to the previously sampled signal. Furthermore, as shown in Fig. 10(a), if a parasitic capacitor C_p is assumed between node X and the ground, a noninverting amplifier is formed around the opamp. Hence, the output noise power spectrum density (PSD) $S_{\text{out},n}(f)$ at the moment of the peak sampling assuming the opamp noise V_n is dominant becomes

$$S_{\text{out},n}(f) \approx \frac{2\left(1+\frac{C_p}{C_2}\right)^2\left(1-\cos\pi\frac{f}{f_s}\right)}{\left(\frac{f}{f_0}\right)^2\left(1+\frac{C_p}{C_2}\right)^2+1}\cdot S_n(f) \quad (10)$$

where $S_n(f)$ represents the noise PSD of the opamp corresponding to V_n. In addition, the opamp is modeled as an integrator with the gain-bandwidth product (GBW) of f_0, and the spot noise at f_s, $\sqrt{S_{\text{out},n}(f_s)}$, can be calculated as 18 nV/$\sqrt{\text{Hz}}$, where each parameter is assumed as follows: f_0 is almost over 10 MHz, $C_p/C_2 = 0.1$, $f_s = 1.28$ MHz, and $\sqrt{S_n} = 8.1$ nV/$\sqrt{\text{Hz}}$. The spot noise at f_s can be used to estimate the folding noise during the sampling phase as shown in Fig. 10(a). The noise contribution from the series-connected feedback resistor R_{fb} between the coil and the opamp should also be considered in addition to (10) if it is not negligible.

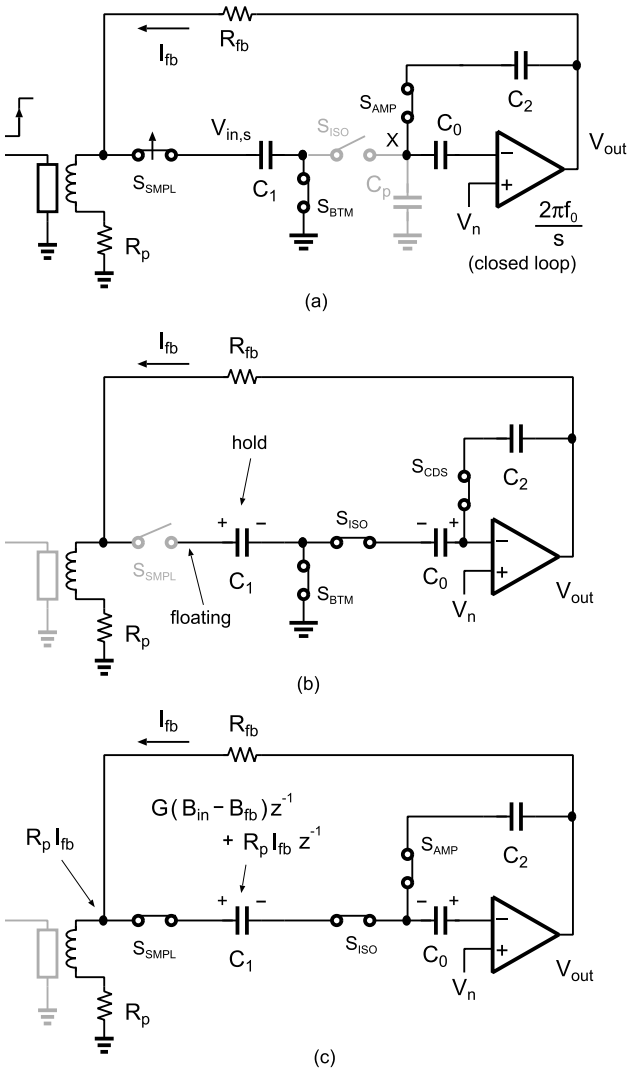

Fig. 10. AFE configuration for each phase: (a) sampling, (b) hold/CDS, and (c) amplifying phases.

The sampled voltage $V_{\text{in},s}$ is held during the hold/CDS phase because the left terminal of C_1 is floating as shown Fig. 10(b). At this time, the nonideal components are sampled on C_0 because a CDS technique is adopted around the opamp to eliminate its offset voltage and flicker noise in the passband [31]. Therefore, the noise of the opamp is high-pass-filtered by the CDS effect as shown in (10). The CDS technique also assists to realize the lossless SC integrator with the limited dc gain of the opamp [33], which can relax the jitter requirement on SMPL as discussed in Section II-C.

At the instance in the sampling phase defined as $n-1$ [see Fig. 10(a)], an unintended drop voltage due to R_p and I_{fb} deteriorates the effectiveness of the magnetic negative feedback as expressed in (4). In the designed magnetometer, an additional CDS technique is introduced for solving this issue, and it works in the amplifying phase shown in Fig. 10(c), and it eliminates the influence of the drop voltage. At the sampling instance, the sampled voltage $V_{\text{in},s}z^{-1}$ becomes $G(B_{\text{in}} - B_{\text{fb}})z^{-1} + R_p I_{\text{fb}} z^{-1}$; the first term is related to the intended signal components and the second one is the undesired drop voltage that depends on the signal because

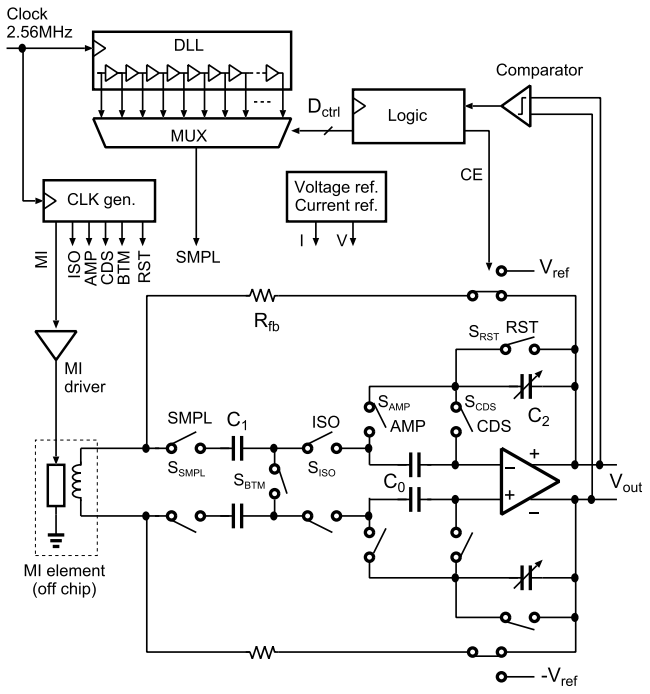

Fig. 11. Overall system diagram of MI-based magnetometer.

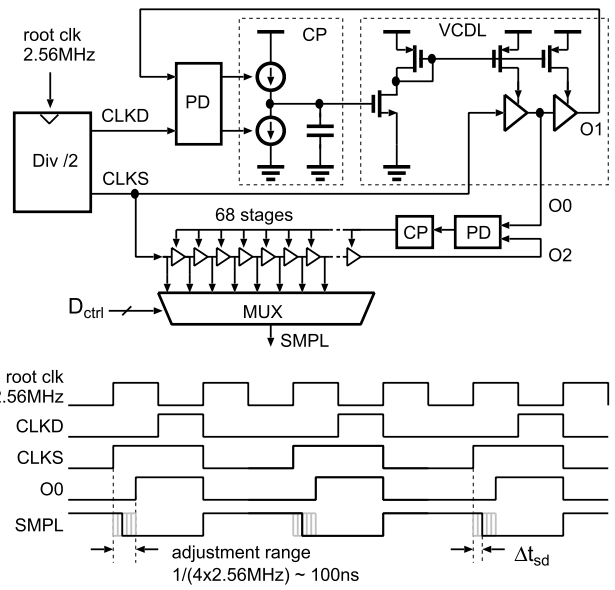

Fig. 12. DLL circuitry and timing diagram.

$I_{\rm fb}z^{-1} = V_{\rm out}z^{-1}/R_{\rm fb}$ as described in B. Then, the switch $S_{\rm SMPL}$ turns on again during the amplifying phase as shown in Fig. 10(c), and in this phase, because the wire of the MI element is not excited, $V_{\rm in}$ represents only a drop voltage $R_p I_{\rm fb}$. Therefore, the voltage across C_1 becomes $G(B_{\rm in} - B_{\rm fb})z^{-1} + R_p I_{\rm fb}(z^{-1} - 1)$, and therefore, the second nonideal term is suppressed within the signal bandwidth owing to high-pass filtering.Since this is equivalent to the effect of the CDS technique and the only desired charge on C_1 is transferred to C_2, the overall frequency response $|H(f)|$ can be derived by the transfer function $H(z) = V_{\rm out}(z)/B_{\rm in}(z)$ as

$$|H(f)| = \frac{R_{\rm eff}}{\beta} \cdot L(f, \gamma) \tag{11}$$

where $R_{\rm eff} = R_{\rm fb} + R_p$

$$L(f, \gamma) = \left[2\gamma(\gamma - 1)\left(1 - \cos 2\pi \frac{f}{f_s}\right) + 1\right]^{-\frac{1}{2}} \tag{12}$$

and

$$\gamma = \frac{R_{\rm eff}}{\beta G}\left(\frac{R_p}{R_{\rm eff}} + \frac{C_2}{C_1}\right). \tag{13}$$

The frequency-dependent factor expressed by (12) provides the characteristic of a low-pass filter with a gain of one. As seen from (11), the passband gain becomes $R_{\rm eff}/\beta$, which is independent of the intrinsic sensitivity G of the MI element, resulting in a stable passband gain.

III. Implementation

The overall system diagram of the MI-based magnetometer is shown in Fig. 11, and all components except for the MI element are integrated into a chip. The designed system includes a DLL/MUX, logic circuit, including serial peripheral interface (SPI), a comparator for the calibration, clock generator, voltage/current reference circuit, MI driver for the wire in the MI element, and SC-based AFE circuit.

The DLL for adjusting the SMPL to an appropriate sampling timing is composed of a phase detector (PD), a charge pump (CP), and a voltage-controlled delays line (VCDL). In this design, the required range of delay adjustment is assumed to be almost 100 ns because the expected resonant frequency of the induced voltage is larger than a few MHz. Therefore, the DLL is designed with a two-stage cascaded configuration for minimizing the number of delay cells as shown in Fig. 12. The DLL is driven by a clock CLKD with 25% duty and a 1.28-MHz frequency generated by a divider circuit, and the first DLL outputs a clock O0 with a delay that is one-fourth the period of the root clock, $1/(4 \times 2.56$ MHz), from the rising edge of a clock CLKS, which is divided by two from the root clock. The obtained O0 is used at the second DLL as a reference, and the rising edge of a delay chain output O2 is adjusted to that of O0, where the required resolution $\Delta t_{\rm DLL}$ is determined by the number of delay cells in this stage. As discussed in Section II-C, since $\Delta t_{\rm DLL}$ can be specified by the acceptable variation on the loop gain or noise floor of the magnetometer, the number of delay cells is determined as 68, where the same condition as discussed before (10% variation), is assumed, and the margin is almost double, resulting in $\Delta t_{\rm DLL} \approx 1.46$ ns.

The clocks for driving the analog part and others are created by the clock generator. The MI driver is implemented as an inverter with a large channel width to push a current up to 50 mA into the wire of the MI element. The analog part for acquiring the peak of the induced voltage from the MI element is designed as a fully-differential configuration and the magnetic negative feedback is realized through the feedback resistor $R_{\rm fb}$.

In the calibration mode, the control signal CE is activated to reconfigure the analog part for the calibration. As shown in Fig. 4(a), the feedback is removed and then $R_{\rm fb}$ is reused to

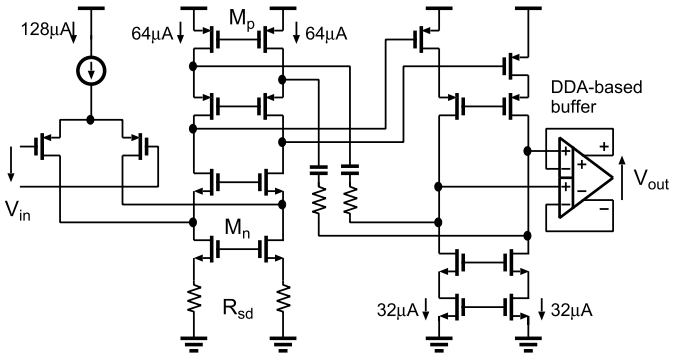

Fig. 13. Opamp circuitry for the SC integrator with DDA-based local negative feedback buffer.

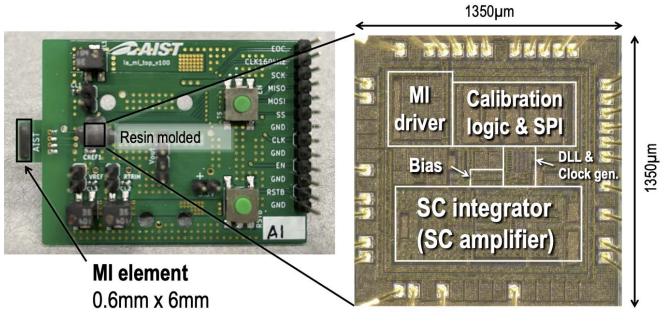

Fig. 14. Chip micrograph.

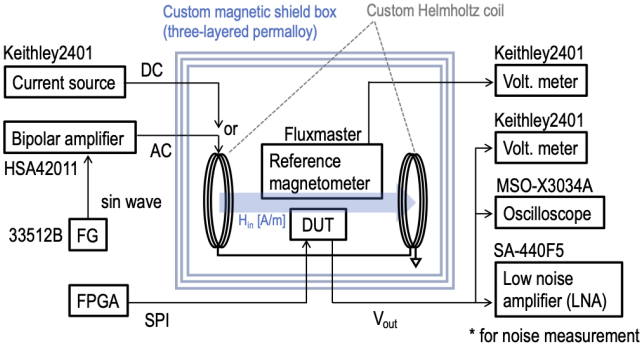

Fig. 15. Measurement setup.

generate a constant magnetic field in the MI element for the calibration through CE. The SC integrator is reconfigured as a high-bandwidth SC amplifier that gains the sampled induced voltage. This can be implemented by adding a reset switch S_{RST} driven by RST in parallel to the integration capacitor C_2; it works in the hold/CDS phase shown in Fig. 9. Therefore, RST is obtained by taking a logical product of CDS and CE. Meanwhile, the capacitance of C_2 is also changed by CE to adjust an appropriate gain and bandwidth. As discussed in Section II-C, the zero-crossing detector comprising the SC amplifier and comparator needs to satisfy (9). The detector is designed with 130-$\mu V_{\rm rms}$ input-referred noise and offset, which is considerably lower than the required $\Delta V_{z,n}$ defined in (9) when it is assumed that $V_{{\rm in},p}$ = 100 mV, $f_{\rm res}$ = 50 MHz, and $\Delta t_{\rm DLL}$ = 1.46 ns.

The opamp used in the SC integrator is based on a basic two-stage folded cascode topology with an output buffer, as shown in Fig. 13, where the bias and common-mode feedback circuits are omitted for simplicity. In the first stage, the bias current of the input differential pair is properly biased in the weak or moderate inversion region for a high transconductance/current efficiency [35] and for high transconductance, which is equivalent to low thermal noise. The source degeneration resistors, $R_{\rm sd}$'s, are utilized to reduce flicker noise contribution from the current source transistors, M_n's. The transconductance of the power-rail-sided transistors M_p's, which is another dominant noise contributor in the first stage, is reduced by letting its gate-overdrive voltage higher. The output stage is added to reduce its output impedance and have a driving capability because the amplifier requires to drive the feedback resistor $R_{\rm fb}$. This stage should be a wide-swing voltage buffer with a gain of one, and it is implemented by a differential-difference amplifier (DDA) [36] with a folded mesh class-AB output stage [37] where the DDA is configured as a voltage follower to reduce the output impedance with the open-loop gain of the DDA. In addition to this local negative feedback effect, since the opamp is used for the SC integrator, the output impedance can be further reduced. This closed-loop DDA is designed to have a higher bandwidth than the unity gain frequency of the first stage so that this stage does not affect the phase margin of the opamp. The designed opamp has approximately 10 MHz GBW for a proper setting in the 1.28-MHz clocked SC circuit.

IV. Measurement Results

The prototype AFE chip is fabricated in 0.18-μm CMOS technology. The chip area, which includes IOs and PADs, is 1.35 × 1.35 mm^2, as shown in Fig. 14, and the MI element chip occupies 0.6 × 6 mm^2 separately. Fig. 15 shows the measurement setup, where a magnetic field is generated by a custom Helmholtz coil with signal sources. A reference magnetometer is used to monitor the applied magnetic field in the device under test (DUT).

The measured dc curve and linearity error are shown in Fig. 16(a) and (b), respectively. The total sensitivity, or gain, from the input magnetic flux density $B_{\rm in}$ to the output voltage $V_{\rm out}$ is 9.0 mV/μT, and the linearity error within the input range of ±120 μT is +0.38/−0.29%. The worst-case error with the same input range for ten samples is +0.43/−0.98%. The linearity error is considered to be due to the switches in the feedback path shown in Fig. 11, which are required to change the mode between magnetic sensing and calibration.

The frequency response after the calibration is shown in Fig. 17 and the bandwidth is 31 kHz, where the passband gain is expressed in the decibel form calculated from $V_{\rm out}/B_{\rm in}$. The passband gain is determined by $R_{\rm eff}$ and β as described in (11), and the measured gain variation between ten samples is 0.5 dB in the passband. Fig. 18 shows the noise spectral density of the magnetometer where the in-band noise floor is input-referred with the gain. The low-frequency noise from the AFE circuit is suppressed by the CDS technique around opamp, and the in-band noise floor is 8.0 pT/$\sqrt{\rm Hz}$. Although in our previous design [27], there was a spur with the amplitude of almost 600 pT in the signal bandwidth, it is suppressed in this refined prototype. This in-band spur is attributed to the logic circuit,

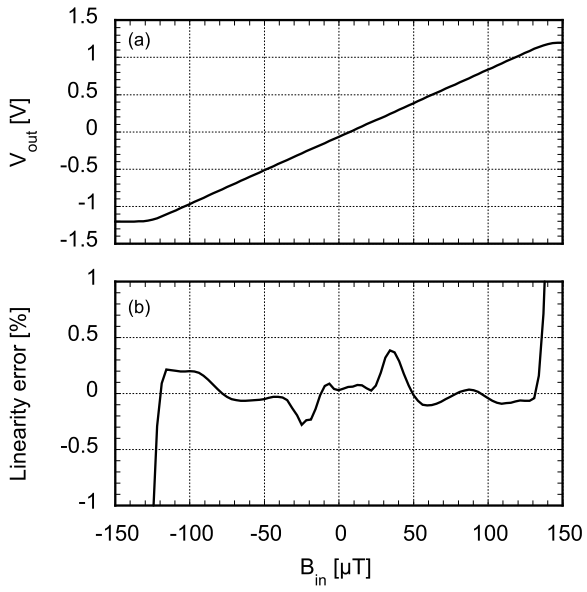

Fig. 16. Measured dc characteristics: (a) transfer curve and (b) linearity error.

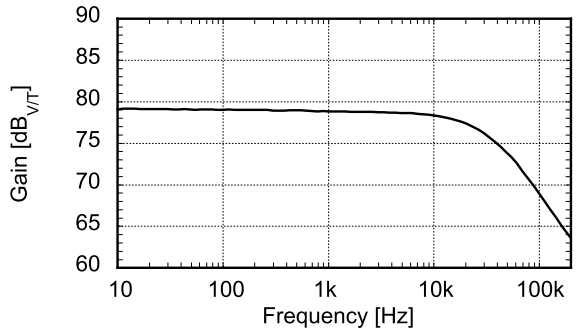

Fig. 17. Measured frequency response.

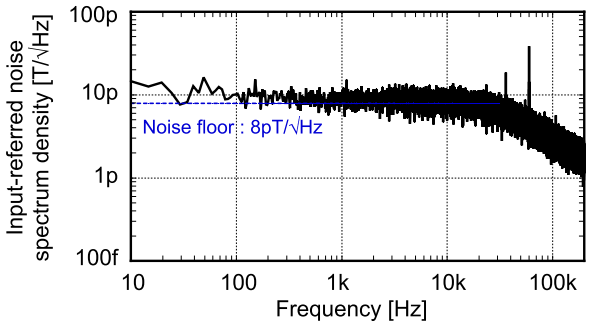

Fig. 18. Measured input-referred noise spectrum density.

and this expected cause can be avoided by optimization of the digital part and strengthening the isolation to the analog part in layout design. Fig. 19(a) and (b) shows transient responses for a 500-Hz sinusoidal input with magnitudes of 2 and 100 μT, respectively. The waveforms of the DUT for both small and large inputs are obtained without large noise or distortion compared with the current of the Helmholtz coil and the reference magnetometer output. The designed magnetometer utilizes a magnetic negative feedback architecture, and it requires a relatively large compensation current to make a magnetic field in the opposite direction to the input one; in this design, this current is generated by the

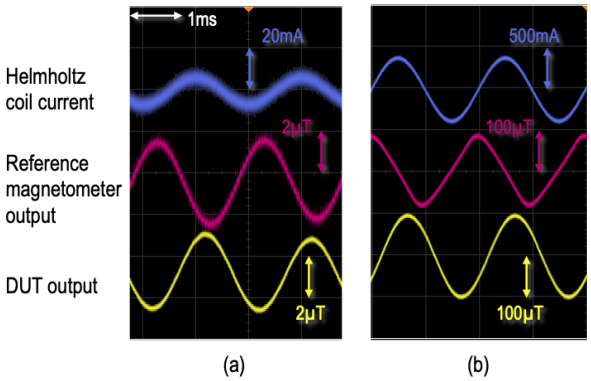

Fig. 19. Transient responses for (a) 2-μT and (b) 100-μT magnitude and 500-Hz sinusoidal input.

TABLE I
PERFORMANCE SUMMARY

Architecture	Magnetic negative feedback with single coil
Sensor head	Magnetoimpedance (MI) element
CMOS Technology	0.18 μm CMOS
Supply voltage	1.5 V
External clock	1.28 MHz
Power consumption	1.97 mW ($B_{in} = 0$ T)
Analog part	1.44 mW
MI driver	465 μW
Logic part	60 μW
Input range	$\pm$120 μT
Linearity error	$+0.38/-0.29$ %
Bandwidth (Bw)	31 kHz
Input-referred noise	8 pT/$\sqrt{}$Hz
Dynamic range (DR)	96 dB
Die size	1.82 mm^2
w/ MI element	5.42 mm^2

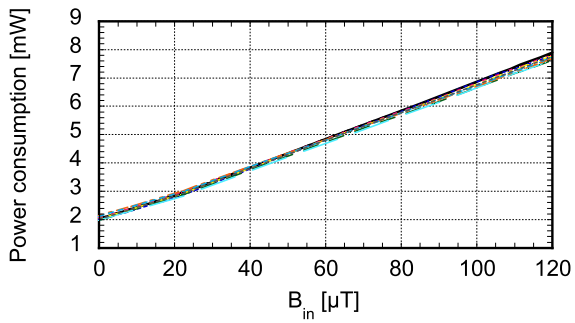

Fig. 20. Measured power consumption with operational point difference for ten samples.

feedback resistor R_{fb} and its applied voltage V_{out}. This current, or power consumption of the AFE circuit, is proportional to the signal magnitude or operating point at the output owing to a class-AB output stage in the amplifier. The dependency of the operating point, or the input B_{in}, on the power is illustrated in Fig. 20, where ten samples are measured.

The results indicate that the magnetometer consumes the power of almost 8.0 mW when $B_{in} = 120$ μT.

TABLE II
COMPARISON WITH STATE-OF-THE-ART MAGNETOMETERS

	Sensor head	CMOS Tech.	Output type	Input range	Bw	Non-linearity	Noise	DR	Power (B_{in} = 0 T)	Size
W. Magnes [5]	FG	0.35 μm	Digital	$\pm$2 μT	30 Hz	-	3.3 pT/$\sqrt{}$ Hz *1	98 dB	13 mW *2	20 mm^2
TFM100 [6]	FG	-	Analog	$\pm$100 μT	3.5 kHz	$\pm$0.0035 %	20 pT/$\sqrt{}$Hz	96 dB	700 mW	254 cm^2 *4
B. Yan [7]	FG	-	Analog	$\pm$100 μT	1 kHz	-	6 pT/$\sqrt{}$Hz	111 dB	120 mW	102 cm^3 *4
M. Kashmiri [12]	IFG	0.6 μm	Digital	$\pm$1.33 mT	75 kHz	$\pm$0.1 %	774 pT/$\sqrt{}$Hz	73 dB	280 mW	9.8 mm^2 *3
P. Garcha [14]	IFG	0.25 μm	Digital	$\pm$2.4 mT	125 kHz	$\pm$0.2 %	500 nT$_{\rm rms}$	71 dB	13 mW	7.6 mm^2 *3
J. Jiang [19]	Hall+Coil	0.18 μm	Analog	$\pm$7.8 mT	3 MHz	-	210 μT$_{\rm rms}$	28 dB	38.5 mW	8.75 mm^2 *3
CB-1DH [26]	MI	-	Analog	$\pm$2 μT	1 kHz	$\pm$2 %	200 pT$_{\rm rms}$	77 dB	75 mW	385 mm^2 *4
I. Akita [27]	MI	0.18 μm	Analog	$\pm$125 μT	33 kHz	$\pm$0.94 %	10 pT/$\sqrt{}$Hz	93 dB	2.6 mW	5.4 mm^2 *3
This work	MI	0.18 μm	Analog	$\pm$120 μT	31 kHz	$\pm$0.38 %	8 pT/$\sqrt{}$Hz	96 dB	1.97 mW	5.4 mm^2 *3

*1: Estimated from DR and input range.
*2: Excluding excitation power for FG (200mW).
*3: Die area including sensor head.
*4: Module size.

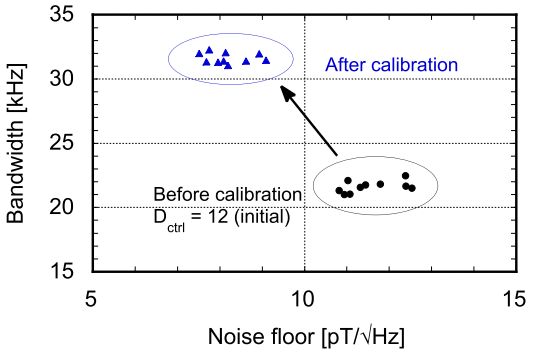

Fig. 21. Improvement of bandwidth and noise through the calibration for ten samples.

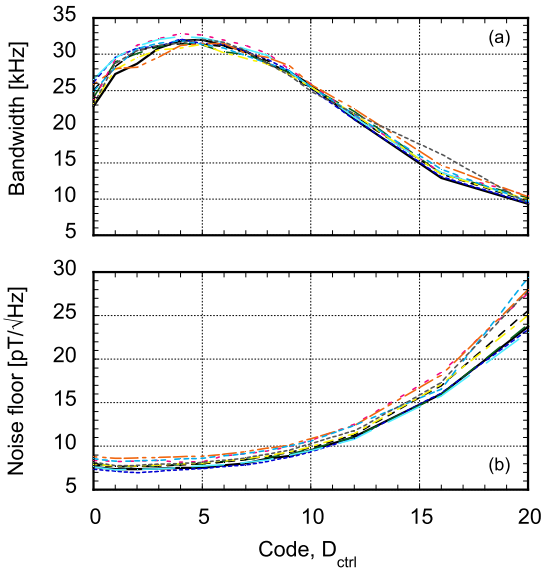

Fig. 22. Sampling delay $\Delta t_{\rm sd}$ dependency on (a) bandwidth and (b) noise floor for ten samples.

To confirm the effectiveness of the proposed calibration scheme, the bandwidth and noise floor relationships before and after calibration are plotted for ten samples in Fig. 21. The initial code $D_{\rm ctrl}$ before the calibration is 12, which corresponds to $\Delta t_{\rm sd}$ of almost 17.5 ns. After the calibration, the code for each sample settled to 4, 5, or 6. It is confirmed that both the bandwidth and noise floor are improved through the proposed calibration. There is variation even after the calibration because the intrinsic sensitivity in the loop gain varies between the devices. The bandwidth and noise floor are also measured for each sampling delay $\Delta t_{\rm sd}$, which can be set by the code $D_{\rm ctrl}$ into the MUX as shown in Fig. 4(a) and be swept manually through the SPI command. The $\Delta t_{\rm sd}$ dependency on the bandwidth and noise floor are illustrated in Fig. 22(a) and (b), respectively, and the results for ten samples are obtained. The inappropriate $\Delta t_{\rm sd}$ reduces the loop gain and loop bandwidth, and it directly degrades the signal bandwidth and the noise characteristic. These measurement results show there is the optimum $\Delta t_{\rm sd}$, which corresponds to around the code of 4, and it can be found automatically by using the proposed calibration scheme.

The typical characteristics of a prototype chip are summarized in Table I. The MI driver, SC-based AFE circuit logic circuit, and clock generator are driven by a 1.28-MHz clock, which is generated by an external 2.56-MHz clock. Since the input range is $\pm$120 μT, the DR becomes 96 dB for the in-band integrated noise. Conversely, if the noise with an out-of-band up to 200 kHz is integrated, it was 1.8 nT$_{\rm rms}$, corresponding to a DR of 93 dB.

A comparison to prior works is summarized in Table II. The FG magnetometers [5], [6] achieve the lower noise floor of a few tens of pT/$\sqrt{}$Hz. However, their consumed power is relatively high because their excitation current tends to be large for saturating magnetization of a core in the FG sensor. The MI-based magnetometer is driven by a short time pulse, and therefore, the excitation current can be saved compared with the FG-based ones. Although magnetometers based on IFG [12], [14] can provide a chip-scaled implementation and achieve a larger input range, they still have a higher level of noise and power consumption.

V. CONCLUSION

An automatic digital calibration technique for enhancing the loop gain in an MI-based magnetometer has been presented.

The designed magnetometer achieves low-noise and high-bandwidth characteristics. A dedicated switching scheme can avoid the open-loop state in the SC circuit and reduces the folded noise influence of opamp. In addition, by adopting the CDS technique, a nonideality related to the parasitic resistor of the coil in the MI element is suppressed, recovering the effectiveness of the magnetic negative feedback. A prototype chip fabricated in a 0.18-μm CMOS process achieved a noise floor of less than 10 pT/$\sqrt{}$Hz and 96-dB DR at a power consumption of 2 mW. A comparison with other state-of-the-art magnetometers shows that the presented chip achieves higher efficiency in terms of power, noise, DR, and bandwidth.

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