A 110/230 V AC and 15–400 V DC 0.3 W Power-Supply IC With Integrated Active Zero-Crossing Buffer

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***Abstract*— This work presents an offline power supply with fully integrated power stage in 0.18 μm high-voltage (HV) CMOS silicon on insulator (SOI). It supports both ac–dc and dc–dc conversion from 15–400 V input down to 3.3–10 V output and is optimized for applications below 300 mW such as the Internet of Things (IoT), smart home, and e-mobility. An active zero-crossing buffer enables on-chip integration of the HV buffer capacitor. Below 150 V, constant ON-time control is based on voltage intervals, sensed by ten HV threshold-detection circuits. Above 150 V, the converter operates in the resonant mode. It achieves a superior power density of 458 mW/cm^3 and 84% peak efficiency.**

***Index Terms*— ac–dc converter, dc–dc converter, high voltage (HV), light-load efficient, power density, silicon on insulator (SOI).**

I. Introduction

THE on-going decentralization and the increasing functionality of electronic devices leads to a growing demand for efficient and compact IC-level power converters supplied from the grid and from high-voltage (HV) dc supplies of up to 400 V down to below 5 V (see Fig. 1). The field of applications ranges from the Internet of Things (IoT) and smart home up to control circuits and other periphery in electrical vehicles and industrial applications with a power consumption in the milliwatt range. Fig. 2 shows the peak efficiency at ac input versus the power density of the state-of-the-art publications [1], [2], [3], [4], [5] and commercially available power modules [6], [7], [8] in comparison to the converter presented in this work. Prior art publications suffer from a poor power density <50 mW/cm^3 or a low efficiency ≤30%. They use capacitive [1], [2], [3], resistive [4], or direct coupling [5] in the ac interface.

The capacitive coupling at 50/60 Hz gives either very little power (below 20 μW) in case of fully integrated capacitors [1], [2], [9] or requires very large discrete capacitors [3], [9]. It is further limited to ac input voltages, which significantly reduces its range of applications.

Resistive coupling achieves milliwatt output power [4]; however, it still requires a large buffer capacitor during the zero-crossing of the ac mains and its efficiency (5% for the converter in [4]) is limited by the required HV LDO and the maximum input voltage of the subsequent dc–dc converter.

Direct coupling also allows for an output power in the milliwatt range, but its buffering time of up to 50% of the ac mains period leads to an even larger external buffer capacitor and conversion efficiencies have not shown to exceed 30%.

Commercially available power modules [6], [7], [8] commonly operate at low switching frequencies to keep the switching losses of the typically used hard-switched flyback topology small and, thus, achieve an overall peak efficiency of up to 74%. But the low switching frequency leads to a large transformer with up to several millihenry of inductance and large output capacitors. In addition, their passive buffer approach and their low dc input voltage range end up in large external capacitors to buffer the zero-crossing of the ac mains. Hence, the power density of commercially available power modules is below 160 mW/cm^3. Moreover, their operation in the continuous-conduction mode and their large control losses often lead to a poor light-load efficiency [10], [11].

Fig. 1. Increasing demand for smaller, cheaper, and efficient ac–dc and dc–dc converter ICs for smart home, IoT, e-mobility, and industry.

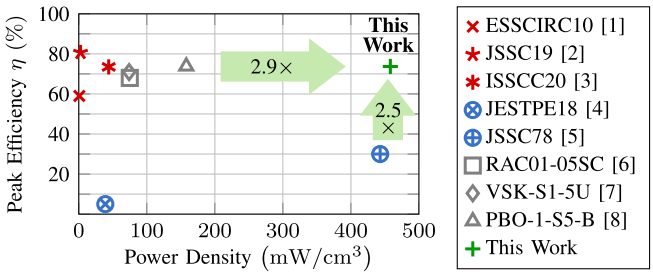

Fig. 2. Peak efficiency at ac input versus power density of published and commercially available ac–dc converters in the power range <1 W.

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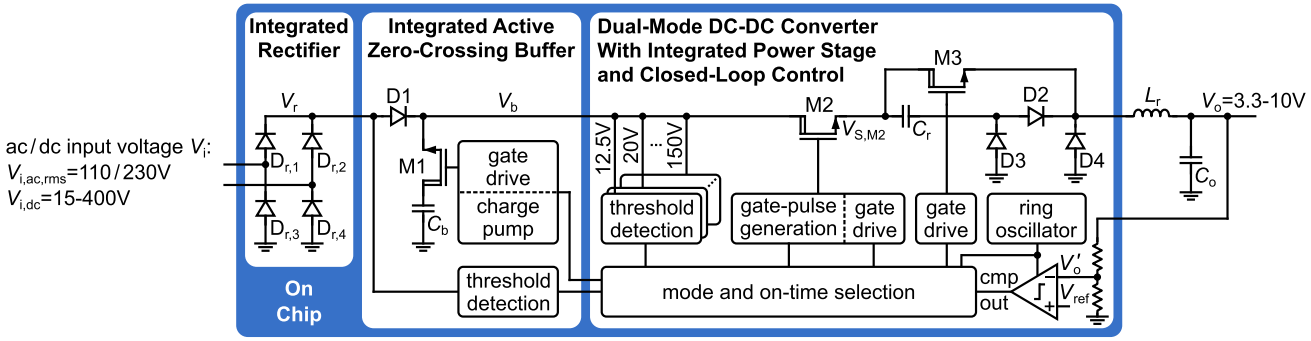


Fig. 3. Offline chip-scale converter topology with active zero-crossing buffer and voltage-interval-based dual-mode dc–dc converter.

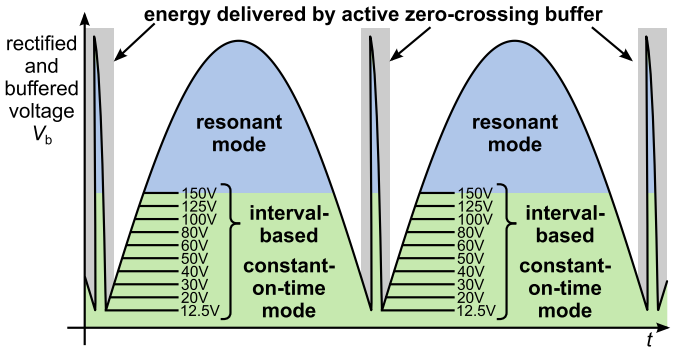


Fig. 4. Modes of operation depending on the full-wave rectified voltage V_b.

The large size at sufficient high output power and the low efficiency make the state-of-the-art approaches not well suitable for the targeted decentralized low-power applications.

This article presents an efficient and compact offline chip-scale power supply with a more than 2.9× higher power density compared with capacitive coupled converters and commercially available power modules as well as a more than 2.5× higher efficiency compared with resistive and direct coupled converters (see Fig. 2). It is optimized to efficiently supply low-power applications such as IoT nodes, sensors, RF transceivers, and LED strings, from the 120/230 V ac mains or from dc supplies within an input voltage range of 15 V $\leq V_{i,\mathrm{dc}} \leq$ 400 V, such as HV batteries or the dc link in industrial applications.

The high power density and high conversion efficiency are achieved by two topology-based innovations: a voltage-interval-based dual-mode dc–dc conversion and an active zero-crossing buffer in the ac interface, which significantly reduces the size of the HV buffer capacitor C_b and enables on-chip integration. They are described in detail in Section II. Due to the relatively low required output power, steady-state losses need to be reduced to its minimum, which is achieved by a pulse-based control approach and low-power block-level circuits, which are described in Section III. They include an innovative HV threshold-detection circuit for a high-speed low-power sensing of the converter input voltage and a binary-coded cycle-by-cycle-programmed gate-pulse generation at the high side for a high common-mode transient immunity (CMTI) and a reliable ON-time generation. The measurement results of the implemented converter are discussed in Section IV.

II. Offline Converter Architecture

This section presents a one-step offline buck topology with integrated rectifier and on-chip active zero-crossing buffer (see Fig. 3) [12], which is optimized for light-load conditions and a wide ac and dc input voltage range.

It comprises a fully integrated power stage with three HV transistors ($M1$–$M3$, rated to V_i) and eight HV diodes (D_{r1}–D_{r4} and D_1–D_4, rated to V_i) as well as external passives $L_r = 15\ \mu$H and $C_o = 4.7\ \mu$F. The design uses design techniques for loss reduction in silicon on insulator (SOI) like a fully depleted p-n-junction below the buried oxide as described in [10] and conducting trenches to increase CMTI as suggested in [13]. The non-isolated topology targets applications such as IoT nodes with stand-alone operation that do not need an electrical connection to the environment. For applications that require an isolation, the dc–dc converter block can be replaced by an active-clamp flyback as presented in [11], but with the drawback of a lower power density and a lower input voltage range, due to the high voltage stress of the power switches.

A. High-Voltage dc–dc Converter

The converter has two modes of operation depending on the rectified and buffered voltage V_b as shown in Fig. 4. The converter operates in constant ON-time mode for $V_b < 150$ V and goes in the resonant mode above 150 V. The active zero-crossing buffer kicks in for $V_b \leq 12.5$ V resulting in a voltage peak at V_b.

In constant ON-time mode ($V_b < 150$ V), $M3$ is permanently turned on, resulting in the buck topology shown on the top left in Fig. 5. Turning on $M2$ with zero-current switching (ZCS) starts the energy transfer to the output and results in a rising inductor current I_{Lr}. After turning $M2$ back off, the current through $M2$ commutates to $D4$ and the energy stored in L_r is transferred to the output until the inductor current returns to zero.

The energy transferred to the output in each switching cycle equals the energy that is transferred to L_r during the ON-time t_{ON} of $M2$ and, thus, depends on t_{ON}, L_r, V_b, and V_o. Hence, the output power scales with the switching frequency f_{sw} (frequency of the comparator output signal "cmp out," see Fig. 3) as approximated by (1) and so do the switching losses. The switching frequency reaches $f_{\mathrm{sw}} \sim 2$ MHz at the maximum power and goes down to ∼1 kHz at light load

$$P_o = \frac{1}{2} \cdot L_r \cdot I_{Lr,\mathrm{peak}}^2 \cdot f_{\mathrm{sw}} = \frac{t_{\mathrm{ON}}^2 \cdot (V_b(t) - V_o)^2}{2 \cdot L_r} \cdot f_{\mathrm{sw}}. \quad (1)$$

Defining the load resistance as $R_{\mathrm{load}} = V_o^2/P_o$, the load-dependent voltage conversion ratio can be derived

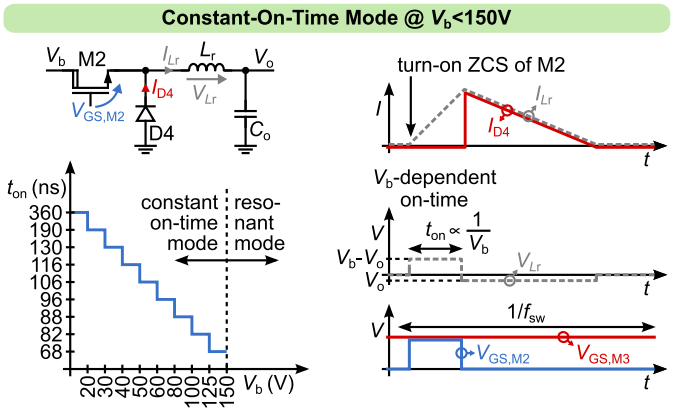


Fig. 5. Operating principle of the implemented offline converter in voltage-interval-based constant ON-time mode (V_b < 150 V).

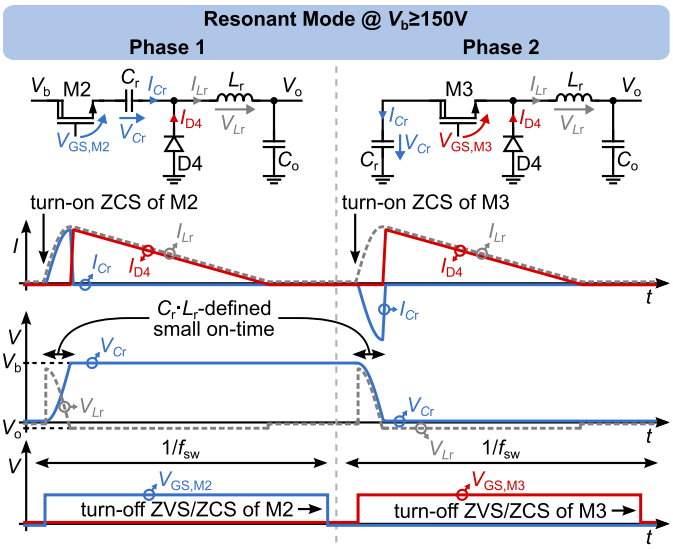


Fig. 6. Operating principle of the implemented offline converter in the resonant mode ($V_b \geq 150$ V).

from (1) by substituting P_o into V_o^2/R_{load}

$$\frac{V_o}{V_b(t)} = \frac{\sqrt{R_{\text{load}} \cdot f_{\text{sw}}} \cdot t_{\text{ON}}}{\sqrt{2 \cdot L_r} + \sqrt{R_{\text{load}} \cdot f_{\text{sw}}} \cdot t_{\text{ON}}}. \tag{2}$$

Equation (2) simplifies to (3) if V_b is much larger than V_o ($\sqrt{2 \cdot L_r} \gg \sqrt{R_{\text{load}} \cdot f_{\text{sw}}} \cdot t_{\text{ON}}$), which shows the linear scaling of the conversion ratio with t_{ON} and with the root of f_{sw} at high input voltages. If V_b approaches V_o ($\sqrt{2 \cdot L_r} \ll \sqrt{R_{\text{load}} \cdot f_{\text{sw}}} \cdot t_{\text{ON}}$), (2) simplifies to unity, which is the maximum conversion ratio of a buck converter.

$$\frac{V_o}{V_b(t)} \approx \sqrt{\frac{R_{\text{load}} \cdot f_{\text{sw}}}{2 \cdot L_r}} \cdot t_{\text{ON}}. \tag{3}$$

A challenge of this constant ON-time control is the dependency of the output power and, thus, the voltage conversion ratio, on V_b; see (1) and (2). Due to the large targeted input voltage range of the dc–dc converter in constant ON-time mode of 12.5 V $\leq V_b <$ 150 V, this dependency would require a wide range of f_{sw} to compensate for both the varying P_o and the varying V_b. To reduce the range of the switching frequency, a scaling of t_{ON} with $\sim 1/V_b$ is implemented to compensate for the varying V_b. Instead of a continuous adjustment of t_{ON}, which would require a lossy continuous input voltage sensing, a voltage-interval-based ON-time selection is implemented, which allows to use a low-power high-speed HV threshold-detection block (see Section III-C) to determine V_b. For each voltage interval within V_b as defined in Fig. 4, the ON-time of $M2$ (lower left of Fig. 5) is not only chosen to compensate for the varying V_b but also to achieve the best trade-off between capacitive losses and conduction losses. The scaling of the inductor current with the ON-time increases the energy transferred per switching cycle at larger t_{ON} and, thus, decreases the switching frequency and its related capacitive losses. The maximum value of the ON-time $t_{\text{on,max}}$ depends on the allowed peak current $I_{Lr,\text{max}}$ of the inductor L_r and can be estimated by (4). The number of V_b intervals (lower left of Fig. 5) is chosen to keep the deviation from the efficiency optimum low at reasonable circuit complexity

$$t_{\text{ON,max}} = \frac{I_{Lr,\text{max}} \cdot L_r}{V_{b,\text{max}} - V_o}. \tag{4}$$

For $V_b \geq 150$ V, parasitics and disturbances during switching impact the reliable generation of short ON-times. Therefore, the converter enters the resonant mode with zero-voltage switching (ZVS) and ZCS based on [14], which supports ON-times < 50 ns to maintain an efficient one-step conversion at high switching frequencies. In the resonant mode, the converter operates in two phases (see Fig. 6). At the beginning of phase 1, $M3$ is turned off (ZVS and ZCS), resulting in the equivalent circuit shown in the left of Fig. 6. $M2$ turns on with ZCS and increases the voltage across L_r (V_{Lr}) initially up to ($V_b - V_o$). The inductor current I_{Lr} rises sinusoidally, due to the resonant behavior. While the voltage across C_r (V_{Cr}) increases, $D3$ and $D4$ block any current to ground. I_{Lr} commutates to $D4$ and transfers the energy from L_r to C_o. When the converter enters phase 2, $M2$ turns off with ZVS and ZCS (equivalent circuit in Fig. 6 right). Similar to phase 1, the energy stored in C_r transfers to the output via L_r and thereby helps increasing the efficiency by up to 2×.

C_r causes a self-timed ON-time, which relaxes the turn-off timing of $M2$ and $M3$. The energy transferred to L_r in each switching cycle within the resonant mode is mainly defined by C_r (20 pF) and V_b. Hence, the output power scales with the switching frequency f_{sw} as approximated by the following equation:

$$P_o = 0.5 \cdot C_r \cdot V_b^2(t) \cdot f_{\text{sw}}. \tag{5}$$

Substituting P_o into V_o^2/R_{load}, the load-dependent voltage conversion ratio in the resonant mode can be derived from (5)

$$\frac{V_o}{V_b(t)} = \sqrt{0.5 \cdot C_r \cdot R_{\text{load}} \cdot f_{\text{sw}}}. \tag{6}$$

A detailed analysis of the resonant mode can be found in [10].

B. Active Zero-Crossing Buffer

During zero-crossing of the sinusoidal ac mains voltage, the converter requires a buffer capacitor C_b to deliver energy to the output. Depending on the required buffering time t_{buf}, the output power P_o, the efficiency of the dc–dc converter $\eta_{\text{dc–dc}}$, the peak value of the input voltage $V_{i,\text{peak}}$, and the minimum allowed input voltage of the dc–dc converter $V_{b,\text{min}}$, the required capacitance value of C_b can be estimated by the following equation:

$$C_b = \frac{2 \cdot P_o \cdot t_{\text{buf}}}{(V_{i,\text{peak}}^2 - V_{b,\text{min}}^2) \cdot \eta_{\text{dc–dc}}}. \tag{7}$$

Conventionally, C_b is directly connected to V_b and starts to deliver energy when V_r passes the peak of the ac input voltage. Depending on the minimum input voltage of the subsequent dc–dc converter, this conventional buffering approach results in a large capacitance value of up to several microfarad, due to the long buffering time of up to 50% of the period. The wide input voltage range of the implemented dc–dc converter already allows to reduce the buffering time to about ∼25% of the period, resulting in a ∼10× smaller capacitance value.

To further reduce the required capacitance, this design introduces an active zero-crossing buffer (see Fig. 3), similar to HV energy storing as implemented for gate drivers in [15]. C_b is charged up to the peak of V_i through the body diode of $M1$. If V_b drops below the minimum input voltage of 12.5 V, $M1$ is turned on and releases the energy stored on C_b. Due to the wide input voltage range of the dc–dc converter and the on-demand supply of C_b, the buffering time reduces to ∼0.25 ms. Hence, the value of C_b reduces by ∼400× compared with the conventional buffer approach to 0.65 nF, which allows for an on-chip integration up to $P_o = 50$ mW. For an output power up to 300 mW, an external SMD capacitor (0805) $C_b = 12/47$ nF is used at $V_{i,\text{ac,rms}} = 230/110$ V, respectively. $M1$ turns off at $V_r = 150$ V, controlled by the 150 V threshold-detection block that is connected to V_r.

III. Block-Level Circuits

Low-loss subcircuits are required to achieve a high light-load efficiency. In addition, measured slew rates as high as 50 V/ns demand for a high CMTI. This section describes the implementation of robust low-power subcircuits, required for proper operation of the presented topology in an HV environment.

A. Control

Fig. 7 shows the closed-loop-control block of the converter and the 2 MHz current-starved ring oscillator (see Section III-B). A new switching cycle is initiated by the rising edge of the clock frequency "clk," which triggers the threshold-detection circuits (see Section III-C) connected to V_b and V_r as well as the clocked comparator that determines whether the scaled output voltage V_o' has dropped below the reference voltage V_{ref}. In that case, the comparator initiates

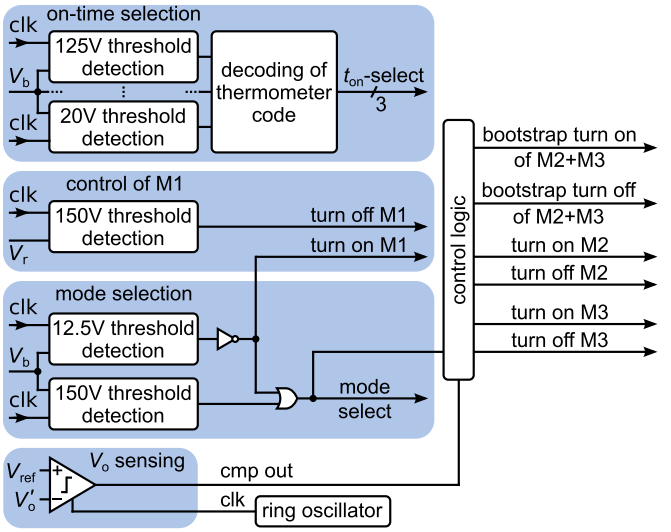


Fig. 7. Closed-loop control block diagram.

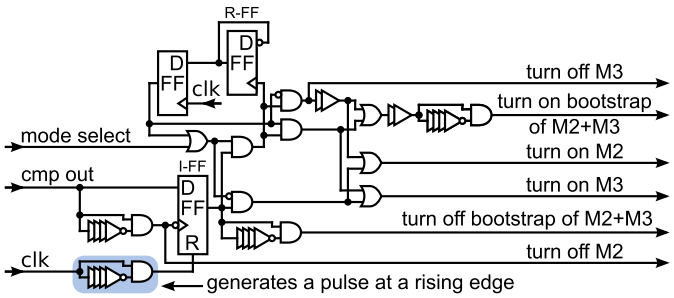


Fig. 8. Control logic block.

the next energy transfer to the output. If $V_b < 12.5$ V, the active zero-crossing buffer ($M1$) is turned on and "mode select" is set to the resonant mode. Between 12.5 V $\leq V_b <$ 150 V, "mode select" is set to the constant ON-time mode and the selected ON-time ("t_{ON}-select") is forwarded to the ON-time programming of transistor $M2$ (see Section III-D). For $V_b \geq 150$ V, "mode select" is set to the resonant mode. Finally, the control logic deactivates the bootstrapping of $M2/M3$ and activates the switches $M2/M3$ according to the selected mode and current phase within the resonant mode.

The detailed implementation of the control logic block is shown in Fig. 8. At each rising edge of the clock frequency "clk," the flip-flop I-FF is reset and a turn-off signal is sent to $M2$. A new switching cycle is initialized only at a rising edge of the comparator output signal "cmp out," which turns the output of I-FF into high. The subsequent logic then deactivates $M3$ (only in phase 1 of the resonant mode) and the bootstrapping of $M2/M3$, activates $M2$ or $M3$, depending on the selected mode (signal "mode select") and the current phase (stored in flip-flop R-FF), and turns the bootstrapping back on after the occurred rising transient at the source of $M2/M3$.

The comparator in Fig. 7 is implemented as clocked comparator [see Fig. 9(a)] to reduce steady-state losses.

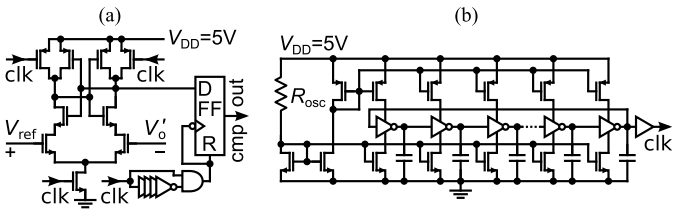


Fig. 9. (a) Clocked comparator and (b) 2-MHz current-starved ring oscillator.

B. Oscillator

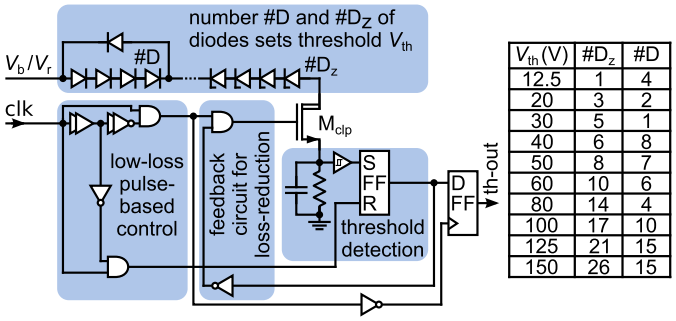
A low-power nine-stage current-starved ring oscillator [see Fig. 9(b)] is implemented to generate the 2 MHz clock frequency, with nine stages being the best trade-off between power consumption and layout area. Due to the insensitivity of the control toward a varying oscillator frequency, the reference current is generated by $R_{osc} = 1$ MΩ from $V_{DD} = 5$ V.

C. High-Voltage Threshold Detection

A well-known challenge in HV low-power designs is the detection of high voltages. Resistive voltage dividers consume excessive power, whereas additional sampling suffers from limited speed and parasitic leakage currents. The presented design implements a threshold-detection circuit (see Fig. 10) that provides both low losses and high-speed detection in the range of ∼10 ns using a stack of diodes and Zener diodes ($V_z = 5.3$ V) to define the threshold voltage. Their temperature coefficients partially compensate the temperature drift. Ten dedicated threshold-detection blocks are implemented with their threshold voltage set by a predefined combination of multiple diodes according to the table in the right of Fig. 10. During constant ON-time mode ($V_b < 150$ V), the output signals "th-out" of the threshold-detection circuits for 20 V up to 125 V are evaluated to select the predefined ON-time t_{ON}. The current flow through the diodes increases exponentially as soon as their threshold voltage is exceeded such that the connected Schmitt trigger reacts quickly. Pulse-based control turns on M_{clp} and the detection circuit only when required to reduce losses. M_{clp} also protects the subsequent low-voltage circuits against HV. Its turn-on signal and the reset of the state-saving flip-flop (SR-FF) are generated by a pulse-based control, which is triggered at a rising edge of the clock signal "clk." To limit the losses at input voltages beyond the threshold voltage, a feedback signal turns off M_{clp} as soon as the threshold signal is stored in the state-saving flip-flop. Below the threshold voltage, the diode current is negligible, which is another advantage versus a purely resistive detection circuit. All these loss reduction mechanisms lead to a > 1000× lower power loss compared with a simple resistive voltage divider.

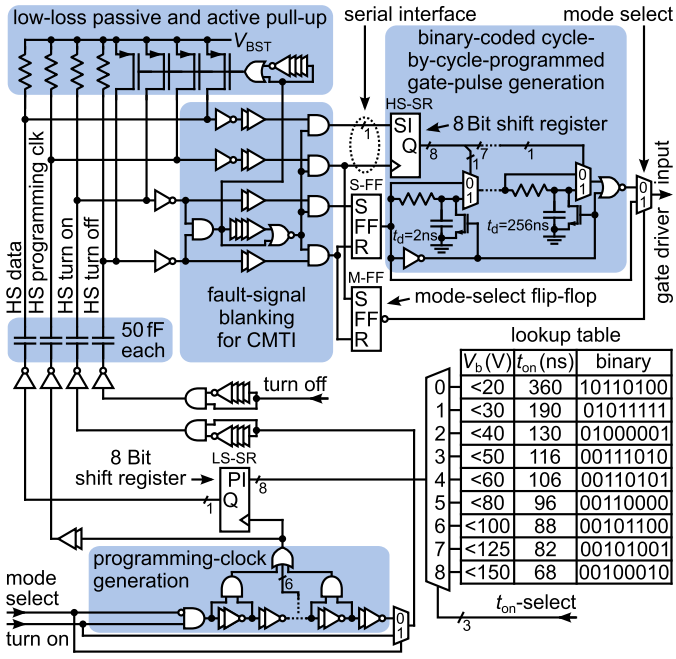
D. Level Shifter and High-Side ON-Time Generation

The capacitive coupled signal transmission of the HV level shifter (see Fig. 11, based on [10] and [16]), reduces steady-state losses. Because the gate control pulses are generated on the high side, reliable ON-times down to 68 ns are achieved even at measured transients of up to 50 V/ns. CMTI is ensured



V_{th} (V)	#D_z	#D
12.5	1	4
20	3	2
30	5	1
40	6	8
50	8	7
60	10	6
80	14	4
100	17	10
125	21	15
150	26	15

Fig. 10. High-speed low-power HV threshold detection.



	V_b (V)	t_{on} (ns)	binary
0	<20	360	10110100
1	<30	190	01011111
2	<40	130	01000001
3	<50	116	00111010
4	<60	106	00110101
5	<80	96	00110000
6	<100	88	00101100
7	<125	82	00101001
8	<150	68	00100010

Fig. 11. Binary-coded cycle-by-cycle programmed high-side gate-pulse generation and HV low-loss capacitive level shifter with a high CMTI.

by the fault-signal blanking circuit. It deactivates the inputs at the high side in case of an occurring common-mode transient, which is detected via a simultaneous pull-down of both the "HS turn on" and "HS turn off" signal during transients. The combination of high-resistive passive and low-resistive active pull-up allows for small coupling capacitors (50 fF each) and low capacitive losses. The active pull-up is activated only for a short time period (10 ns) after a common-mode transient. It charges the coupling capacitors fast, to prepare the level shifter for the next signal transmission.

In the constant ON-time mode, the gate-pulse generation is realized by eight binary coded *RC* delay gates (2–256 ns) corresponding to the ON-times that are selected from the lookup table by the signal "t_{ON}-select" (from threshold detection, see Fig. 7) and shifted to the high-side shift register HS-SR prior to the turn-on of the transistor. To minimize the amount of signal coupling paths to the high side and related losses, the 8-bit shift register (HS-SR) is programmed via a serial interface. This is initiated by the programming clock generation at the low side, which gets triggered at a rising edge of the "turn on"

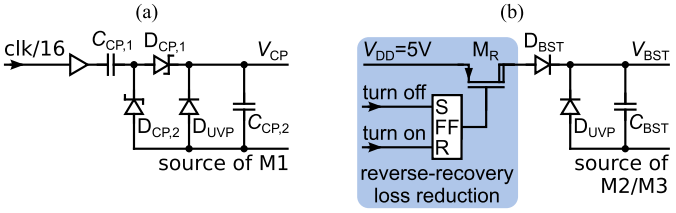


Fig. 12. Implemented high-side supply: (a) charge-pump gate supply for $M1$ and (b) bootstrapping of $M2$ and $M3$ with reverse recovery loss reduction.

signal when "mode select" is set to the constant ON-time mode. The generated pulses shift the binary coded ON-time to the shift register HS-SR. After programming, the signal "turn on" is forwarded to the state-save flip-flop (S-FF) to initiate the gate-pulse generation. In resonant mode, the programming clock generation is deactivated and the "turn on" signal is directly transferred to the state-save flip-flop. Therefore, "mode select" does not need to be transferred but can be extracted from the "HS programming clock" signal. Without clock signal, the mode select flip-flop (M-FF) remains in the resonant mode. Both the flip-flops, S-FF and M-FF, are cleared by the signal "turn off" prior to a new switching cycle. The level shifter is not only implemented for $M2$ but also for $M1$ and $M3$, but without ON-time programming and high-side pulse generation.

E. Gate Drivers and High-Side Supply

The gate drivers for $M1$–$M3$ are implemented as cascaded inverter stages. They should be fast, to achieve ZCS at turn-on. At turn-off, a fast driver for $M2$ is also beneficial to reduce switching losses in the constant ON-time mode, whereas the driver strength does not affect ZVS/ZCS at turn-off in the resonant mode. The ZVS/ZCS of $M1$ and $M3$ at turn-off is not affected by the driver strength in any mode of operation.

The charge pump in Fig. 12(a) supplies $M1$ with its source voltage being > 0 at all time. It operates at a clock frequency of 125 kHz (generated from the clock signal "clk" of the ring oscillator; see Section III-B) and uses an on-chip HV coupling capacitor $C_{\mathrm{CP},1}$ of 15 pF. Isolated low-voltage Schottky diodes ($D_{\mathrm{CP},1}$ and $D_{\mathrm{CP},2}$) are used to reduce the power loss and to maximize the voltage at the high side. D_{UVP} acts as under-voltage protection during rising transients.

Fig. 12(b) shows the bootstrapping circuit of $M2$ and $M3$ in which M_r gets deactivated prior to transients to reduce reverse recovery losses in D_{BST}, similar to [10]. D_{UVP} acts as under-voltage protection during rising transients.

IV. Experimental Results

The converter has been implemented in a 0.18 μm HV CMOS partial-SOI technology [17], [18]. It uses a reverse-biased junction depleting the handle wafer under the HV devices to achieve both high breakdown voltages and small devices at the same time [19]. Fig. 13 shows the chip micrograph and Fig. 14 the PCB implementation with a size comparison to a 1-cent coin. The IC has an active area of 12 mm^2 without the optional internal buffer capacitor C_b and 16 mm^2 with internal C_b. C_r and the integrated C_b are both sandwich capacitors [metal-oxide-metal (MOM)] within the available metal layers. Super-junction MOSFETs are used for the implementation of $M1$–$M3$, due to their low area-specific ON-resistance. If available, a further size reduction of $M2$ and $M3$ could be achieved with super-junction IGBTs as suggested in [20].

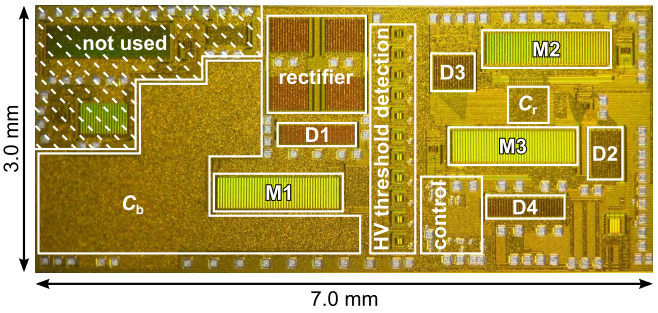


Fig. 13. Die micrograph of the implemented converter with an active area of 12 mm^2 without integrated C_b and 16 mm^2 with integrated C_b.

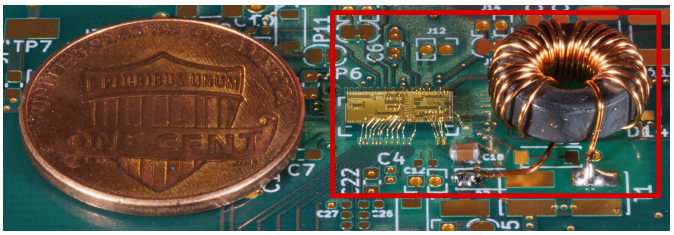


Fig. 14. PCB implementation of the presented converter with size comparison to a 1-cent coin, achieving a power density of 458 mW/cm^3.

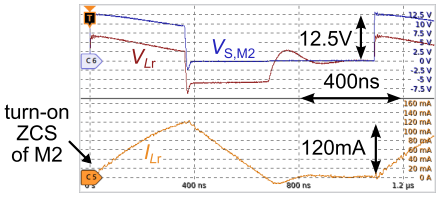


Fig. 15. Measured dc–dc converter transients in constant-ON-time mode at $V_{\mathrm{b,min}} = 12.5$ V, $V_o = 5$ V, and $f_{\mathrm{sw}} = 900$ kHz.

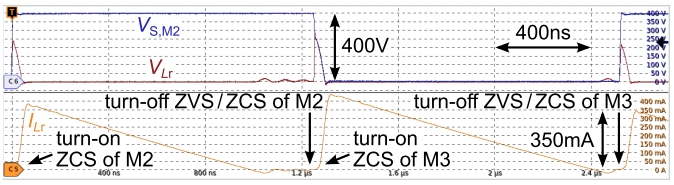


Fig. 16. Measured dc–dc converter transients in the resonant mode at $V_{\mathrm{b,max}} = 400$ V, $V_o = 5$ V, and $f_{\mathrm{sw}} = 800$ kHz.

The measured dc–dc converter transients in Figs. 15 and 16 confirm the expected switching behavior within one switching cycle in the constant ON-time mode ($V_{b,\mathrm{min}} = 12.5$ V, Fig. 15) and resonant mode ($V_{b,\mathrm{max}} = 400$ V, Fig. 16). In both modes of operation, the measured inductor current I_{Lr} is zero at the turn-on of $M2/M3$, which indicates the targeted ZCS of both the transistors and, thus, reduced switching losses at turn-on. The measured transients in the resonant mode (see Fig. 16) further show no current through L_r and no change in the

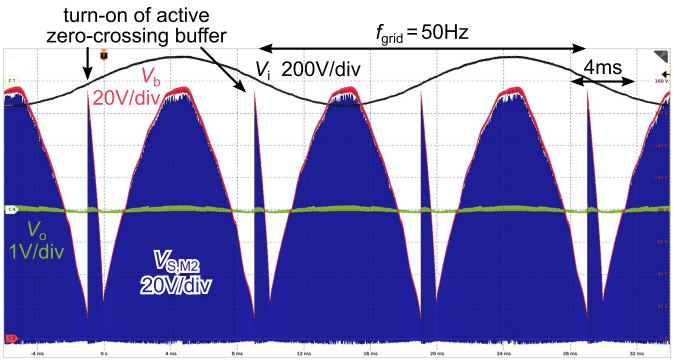


Fig. 17. Measured ac–dc converter transients with external C_b at $V_{i,\mathrm{ac,rms}} = 110$ V, $V_o = 5$ V, and $P_o = 300$ mW.

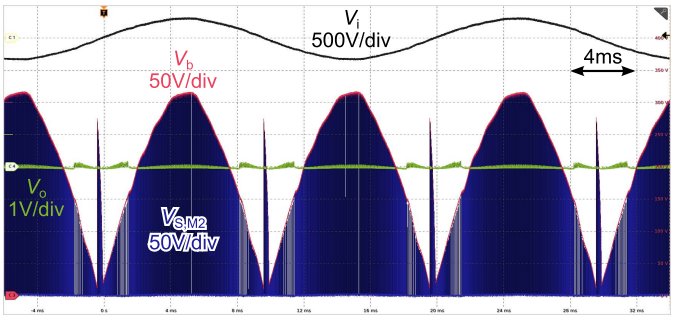


Fig. 18. Measured ac–dc converter transients with integrated C_b at $V_{i,\mathrm{ac,rms}} = 230$ V, $V_o = 5$ V, and $P_o = 50$ mW.

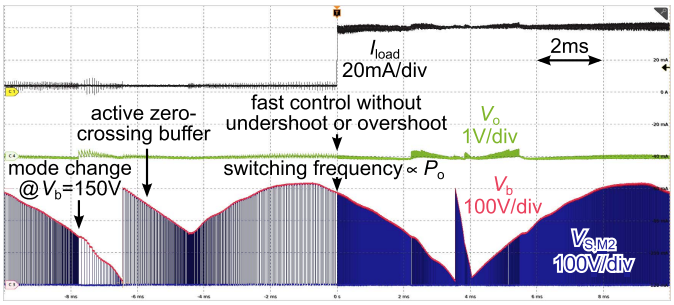


Fig. 19. Measured ac–dc converter transient with external C_b at a load step from 4 to 40 mA, $V_{i,\mathrm{ac,rms}} = 230$ V, and $V_o = 5$ V.

voltage across the transistors at turn-off, which proofs the intended ZVS/ZCS of $M2/M3$ at turn-off (see Section II-A).

Figs. 17 and 18 show the measured ac–dc converter transient voltages V_i, V_b, V_o, and $V_{S,M2}$ for $V_{i,\mathrm{ac,rms}} = 110$ V (integrated C_b) and $V_{i,\mathrm{ac,rms}} = 230$ V (external C_b), respectively. The rectified and buffered input voltage V_b confirms the correct operation of the on-chip rectifier and the intended activation of the active zero-crossing buffer at $V_b < 12.5$ V. The regulated output voltage V_o verifies the accurate control of the dc–dc converter.

The measured load step transients in Figs. 19 and 20 confirm the fast control response without over-/under-shoot due to hysteretic control and the expected linear scaling of the switching frequency with the output power. They also confirm the mode change at 150 V (indicated by the abrupt change in the switching frequency) and the typical varying slope of the voltage across C_b with the output power.

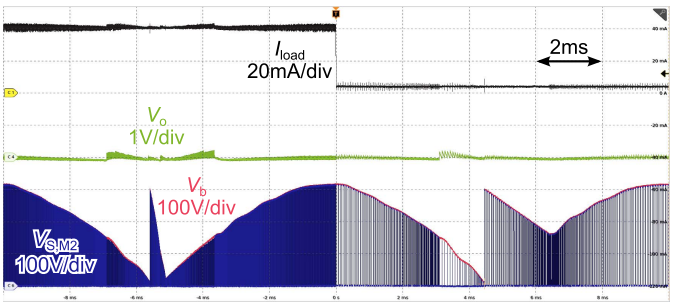


Fig. 20. Measured ac–dc converter transient with external C_b at a load step from 40 to 4 mA, $V_{i,\mathrm{ac,rms}} = 230$ V, and $V_o = 5$ V.

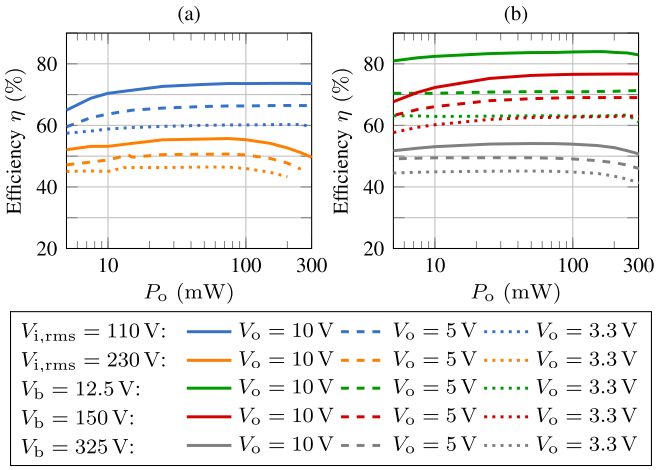


Fig. 21. Measured efficiencies of (a) ac–dc and (b) dc–dc converter.

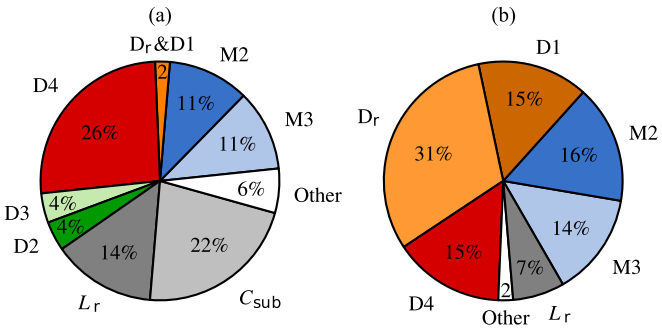


Fig. 22. Simulated loss breakdown at $V_o = 5$ V, $P_o = 50$ mW, and (a) $V_{i,\mathrm{dc}} = 325$ V and (b) $V_{i,\mathrm{dc}} = 15$ V.

The measured ac–dc converter efficiency for 3.3 V, 5 V, and 10 V output at $V_{i,\mathrm{ac,rms}} = 110/230$ V [see Fig. 21(a)] shows a relatively flat run with an overall peak efficiency of 73.7%. The efficiencies include the losses of the power stage and all the block-level circuits. Fig. 21(b) depicts the measured dc–dc converter efficiency for 3.3 V, 5 V, and 10 V output. Due to the pulse-based control, presented in Section II, the efficiency curves show a flat run over a wide output power range with an overall peak efficiency of 84%.

The loss breakdown of the implemented converter at high dc input voltages ($V_{i,\mathrm{dc}} = 325$ V) is shown in Fig. 22(a) and at low dc input voltages ($V_{i,\mathrm{dc}} = 15$ V) in Fig. 22(b). At $V_{i,\mathrm{dc}} = 325$ V, the converter operates in the resonant mode, where the main losses are contributed by the output

TABLE I
COMPARISON TO THE STATE-OF-THE-ART PUBLICATIONS AND COMMERCIAL PRODUCTS

	ESSCIRC10 [1]	JSSC19 [2]	JSSC78 [5]	ISSCC20 [3]	JSSC13 [9]	JESTPE18 [4]	RAC01-05SC [6]	PBO-1-S5-B [8]	**This work**
Technology	0.13 µm	0.35 µm	n.r.	n.r.	0.35 µm	0.35 µm	n.r.	n.r.	**0.18 µm**
Grid voltage (V)	120	120	120	120	120 / 230	120 / 230	120 / 230	120 / 230	**120 / 230**
DC input: $V_{\mathrm{i,dc}}$ (V)	n.a.	n.a.	24-28[a]	n.a.	n.a.	15.3-325	115-370	70-430	**15-400**
V_{o} (V)	3.5-4	11[b]	10[b]	1.25-5	3.3	3.3	5	5	**3.3-10**
$P_{\mathrm{o,max}}$ (W)	$1.5 \cdot 10^{-6}$	$15.16 \cdot 10^{-6}$	0.1	0.6	$125 \cdot 10^{-6}$	$3 \cdot 10^{-3}$	1	1	**0.3**
f_{osc} (kHz)	n.a.	20	n.a.	200	n.a.	900-1400	30	100	**1-2000**
External components	no	no	C=15 µF	R=n.r. Σ C=195.2 µF	Σ C=2 nF	C=10 µF	L=3000 µH[c] Σ C=334.4 µF	L=1500 µH[c] Σ C=172.7 µF	**L=10 µH Σ C=4.7 µF**
Measured ac peak efficiency $\eta_{\mathrm{p,ac}}$	59 %	80.7 %	30 %	73.5 %[d]	n.r.	5 %	68 %[d]	73.7 %[d]	**73.7 %**[e] **72.1 %**[f]
Measured dc peak efficiency $\eta_{\mathrm{p,dc}}$	n.a.	n.a.	n.r.	n.a.	n.a.	n.r.	78.6 %	74.2 %	**84 %**
Power density [BOM] (mW/cm^3)	0.8[a]	2.6[a]	443[a]	44[a]	1.7[a]	39[a]	75	158	**458**

n.r. = not reported n.a. = not applicable [a]estimated [b]unregulated [c]measured [d]extracted from diagram [e]external C_{b} [f]internal C_{b}

freewheeling diode $D4$ (26%), the power transistors $M2$ and $M3$ (22% in total), the power inductor L_r (14%), and capacitive losses caused by parasitic capacitances toward substrate C_{sub} (22%). The much higher conduction losses of $D4$ compared with all other diodes and transistors can be explained by the $>10\times$ longer conduction time of $D4$. The losses in $M2$ and $M3$ are mainly capacitive losses, which are caused by their drain–source and drain–gate capacitance at turn-on. Together with the losses caused by C_{sub}, capacitive losses represent ∼44% of the total losses at high input voltages. Without the implemented capacitive loss reduction mechanisms as suggested in [10], capacitive losses would even dominate the losses at high voltages.

At $V_{i,\mathrm{dc}} = 15$ V, the converter operates in the constant ON-time mode, where the main losses are contributed almost equally by the rectifier (15.5% by each of the rectifier diodes), $D1$ (15%), $D4$ (15%), $M2$ and $M3$ (16% and 14%, respectively), and L_r (7%). Due to the low voltage swing across parasitic capacitances, capacitive losses are negligible at low voltages. Hence, conduction losses dominate at low input voltages.

Table I shows the comparison to the state-of-the-art publications [1], [2], [3], [4], [5], [9] and commercially available power modules [6], [8]. Only the presented converter supports all the common grid voltages and a wide range of dc voltages at the input and the output. It shows a more than $3\times$ higher output power compared with other publications listed in Table I, except for [3], which requires six large external capacitors and one external resistor and, thus, shows a $10\times$ lower power density. The higher output power of the listed commercial power modules comes along with $>3\times$ lower power density and $>4\times$ higher minimal dc input voltage. The peak efficiency of the presented design is more than $2\times$ higher compared with the resistive coupled converters in [5] and [4] and similar to the capacitive coupled converters in [1], [2], [3], and [9], which have much lower output power, show a poor power density, and are not suitable for dc input voltages. The commercial power modules listed in Table I show a similar ac and dc efficiency as the presented design, but have a more than $3\times$ lower power density. With 458 mW/cm^3, the presented converter achieves the highest power density of all the publications and power modules listed in Table I at superior peak efficiency of 73.7% for ac input and 84% for dc input (see also Fig. 2).

V. CONCLUSION

Decentralization, miniaturization, and the increasing functionality of electronic devices lead to a growing demand for compact and efficient HV power conversion on IC level. Required are converters with an output power between a few milliwatt up to 300 mW supplied from the 120/230 V ac mains or from battery and dc-link voltages in the range of several tens of volt up to 400 V converted down to a 3.3–10 V output. The state-of-the-art approaches with capacitive, resistive, or direct coupling in the ac interface suffer from a limited power density or a poor conversion efficiency. One of the main limiting aspects of all the state-of-the-art converters is the large buffer capacitor, which is required to deliver energy during the zero-crossing of the ac mains.

This work presents an offline power supply with fully integrated power stage, implemented in a 0.18 μm HV CMOS SOI technology. It supports both ac–dc and dc–dc conversion from 15–400 V input down to 3.3–10 V output for applications below 300 mW. A voltage-interval-based dual-mode control is implemented, to achieve a high conversion efficiency over a wide input voltage range. Below 150 V, the converter operates in the interval-based constant-ON-time mode. The voltage intervals are sensed by ten HV threshold-detection blocks, which reduce HV sensing losses by more than $1000\times$ compared with a resistive voltage divider. Above 150 V, the converter operates in the resonant mode, to achieve reliable small ON-times <50 ns and low switching losses. An active zero-crossing buffer replaces the state-of-the-art passive buffer approach. It allows to reduce the required buffer capacitor by ∼$400\times$ and, thus, enables on-chip integration of the HV buffer capacitor up to 50 mW.

Compared with the state-of-the-art publications and commercially available power modules, the implemented converter

achieves both a superior power density of 458 mW/cm^3 and a high overall ac and dc peak efficiency of 73.7%/84%, respectively. This makes the converter well suitable for IoT, smart home, e-mobility, and many industrial applications.

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