A 76-Gbit/s 265-GHz CMOS Receiver With WR-3.4 Waveguide Interface

Shinsuke Hara, *Member, IEEE*, Ruibing Dong, Sangyeop Lee, *Member, IEEE*, Kyoya Takano, *Member, IEEE*, Naoya Toshida, Akifumi Kasamatsu, Kunio Sakakibara, *Senior Member, IEEE*, Takeshi Yoshida, *Member, IEEE*, Shuhei Amakawa, *Member, IEEE*, and Minoru Fujishima, *Senior Member, IEEE*

***Abstract*— A 76-Gbit/s 265-GHz CMOS receiver (RX) modularized with a WR-3.4 waveguide interface is presented. It is a mixer-first RX fabricated using a 40-nm CMOS technology. The primary design focus is simplicity and the resulting low noise and loss and high conversion gain (CG). To allow for both on-wafer and packaged measurements, ON-chip transmission lines are designed such that their characteristics are relatively insensitive to the presence or absence of adhesive covering the chip. The RX chip is flip-chip-mounted on a multilayer printed circuit board (PCB). Built into the PCB is a waveguide transition using double-resonant stacked patches for wideband operation. The CMOS RX module achieves the highest wireless data rate of 76 Gbit/s with 16 QAM, which is comparable to 80 Gbit/s reported previously for a CMOS RX with on-wafer probing measurement.**

***Index Terms*— 6G, beyond 5G, low-noise design, near-f_{max} circuits, terahertz wireless communication, waveguide transition.**

I. Introduction

ATMOSPHERIC propagation losses of radio waves tend to increase with frequency as shown in Fig. 1. The losses in the lower terahertz (THz) frequency band between 250 and 320 GHz are manageably low, and this "300-GHz band" is considered a promising platform for ultrahigh-speed broadband wireless communications beyond 5G [1]–[3]. Possible applications include real-time uncompressed transfer of high-definition video, ultrahigh-data-rate wireless access, and kiosk downloading (Fig. 1). World Radiocommunication Conference 2019 (WRC-19) identified 275–296 GHz for use for land mobile and fixed services [4], [5] [Fig. 2(a)]. This band could be used together with 252–275 GHz, already allocated for land mobile and fixed services [5]. IEEE Std 802.15.3d, established earlier in 2017, also concerns the use of the 300-GHz band [6] [Fig. 2(b)]. Research and development of the 300-GHz-band transmitter (TX) and receiver (RX) circuits have been very active in recent years [7]–[28].

In this article, we report on a 300-GHz-band RX chip fabricated using a 40-nm CMOS technology [29]. The center frequency of operation is 265 GHz. The RX chip is flip-chip-mounted on a printed circuit board (PCB) and modularized with a WR-3.4 waveguide interface. A standard waveguide interface offers flexibility in the choice of components, including off-the-shelf ones, to be used together, such as antennas and preamplifiers. This is an advantage over another popular approach of bonding a silicon lens on the backside of the die [30]–[33]. A price of flexibility is the comparative difficulty of implementing beam steering, but it is certainly doable [34]–[36]. Our The RX module achieves a wireless data rate of 76 Gbit/s. This is comparable to the wireless data rate of 80 Gbit/s reported in [23] for a CMOS transceiver (TRX), achieved by on-wafer probing.

The biggest challenge in this work was to make the RX as low noise and high gain as possible. Both these involve making losses as low as possible. The unity power gain frequency, f_{max}, of the technology used was about 280 GHz and was not high enough for implementing amplifiers. A low-noise amplifier (LNA)-less, mixer-first architecture, as shown in Fig. 3, therefore was adopted. The mixer noise figure, NF_1, and the conversion loss, $1/G_1$, should be made as low as possible, but subsequent stages must also be designed carefully to make the RX low-noise. Somewhat disappointingly, attempts at being clever do not always pay in sub-THz CMOS design due to the limited gain of MOSFETs and high losses of passive components. Of course, low-loss design of PCB, including a waveguide transition, is also important.

In Section II, we will further discuss the design of the CMOS RX chip itself and also the design of PCB that includes a waveguide transition. Section III presents the measured performance of RX chip and module, includ-

Manuscript received 20 January 2022; revised 11 April 2022; accepted 20 May 2022. Date of publication 19 July 2022; date of current version 26 September 2022. This article was approved by Associate Editor Woogeun Rhee. This work was supported by the Ministry of Internal Affairs and Communications of Japan under Grant JPJ000254. *(Corresponding author: Shinsuke Hara.)*

Shinsuke Hara, Ruibing Dong, and Akifumi Kasamatsu are with the National Institute of Information and Communications Technology, Koganei 184-8795, Japan (e-mail: s-hara@nict.go.jp).

Sangyeop Lee is with the Tokyo Institute of Technology, Yokohama 226-8503, Japan.

Kyoya Takano is with the Department of Electrical Engineering, Faculty of Science and Technology, Tokyo University of Science, Noda 278-8510, Japan.

Naoya Toshida and Kunio Sakakibara are with the Nagoya Institute of Technology, Nagoya 466-8555, Japan.

Takeshi Yoshida, Shuhei Amakawa, and Minoru Fujishima are with the Graduate School of Advanced Science and Engineering, Hiroshima University, Higashihiroshima 739-8530, Japan.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3179560.

Digital Object Identifier 10.1109/JSSC.2022.3179560

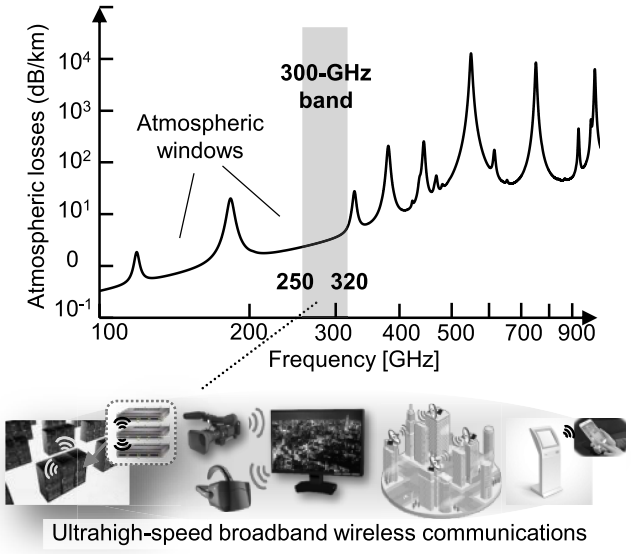


Fig. 1. Atmospheric propagation losses of radio waves between 100 GHz and 1 THz according to [3] and possible applications of 300-GHz band wireless communications.

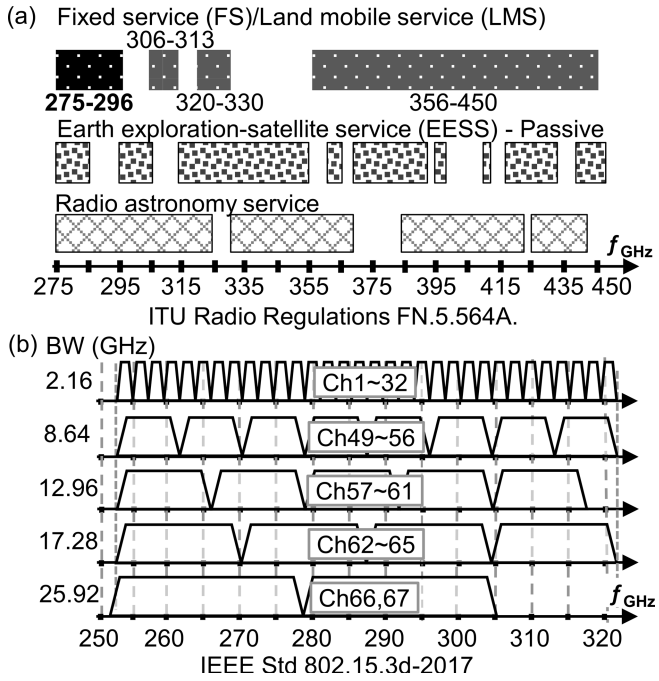


Fig. 2. (a) THz bands identified by WRC-19 [4], [5]. (b) Channels defined by IEEE Std 802.15.3d [6].

ing wireless reception of digitally modulated signals over some channels of 802.15.3d. Finally, Section IV draws conclusions.

II. Design

A. CMOS Receiver

The block diagram of the RX chip is shown in Fig. 4. The RX consists of a down-conversion mixer, a buffer amplifier, an intermediate-frequency (IF) amplifier, and a local oscillator (LO) signal multiplier chain. An LO signal at

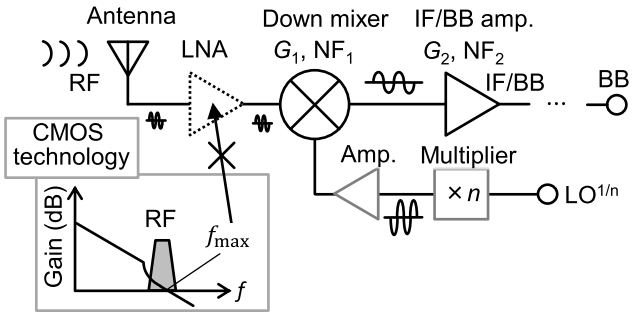


Fig. 3. LNA-less, mixer-first receiver architecture is adopted due to low f_{max}. G_i and NF_i are the gain and the noise figure of the ith stage, respectively.

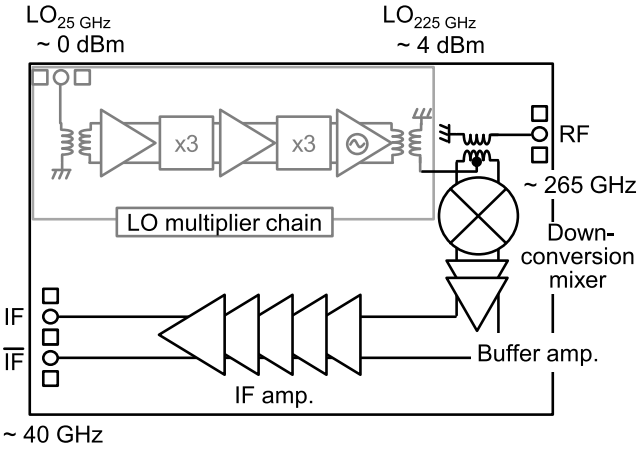


Fig. 4. Block diagram of the receiver. Details of the LO multiplier chain can be found in [37].

around 25 GHz (LO_{25} GHz) with 0-dBm power is supplied from an OFF-chip signal source and is multiplied by 9 to about 225 GHz (LO_{225} GHz). Details of the LO multiplier chain were presented in [37], and therefore will not be repeated in this article. The LO output power is about 4 dBm. A radio frequency (RF) signal at a frequency of around 265 GHz and the LO signal are superposed and fed to the down-conversion mixer. The down-converted differential signal at about 40 GHz goes through the buffer amplifier and the IF amplifier.

Since low noise is the most important design goal, the field-effect transistor (FET) resistive mixer [38], [39] is a mixer configuration that springs to mind. Since the drain-to-source bias is zero and FETs operate as (nearly) linear time-varying resistors in this configuration, the noise generated by FETs is primarily thermal noise, and flicker and shot noise components are very low [39], [40]. The single-sideband (SSB) noise figure (NF), therefore, is very nearly equal to the conversion loss. FET resistive mixers were adopted, for example, in [11], [16], and [24]. We have indeed confirmed by simulation using *lossless* passive components that conversion loss and SSB NF as low as about 6 dB are possible as anticipated. Nevertheless, our experience so far has been that when *lossy* components are used for matching and interconnection, the noise performance of the RX quickly deteriorates and becomes often worse than that achievable using transconductance mixers. On the other

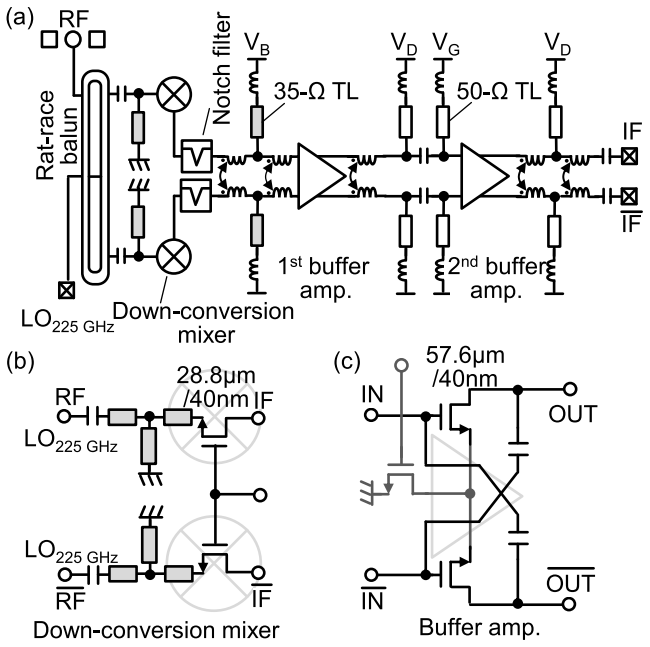


Fig. 5. (a) Schematic of the down-conversion circuit. (b) Details of the down-conversion mixer and of (c) buffer amplifier.

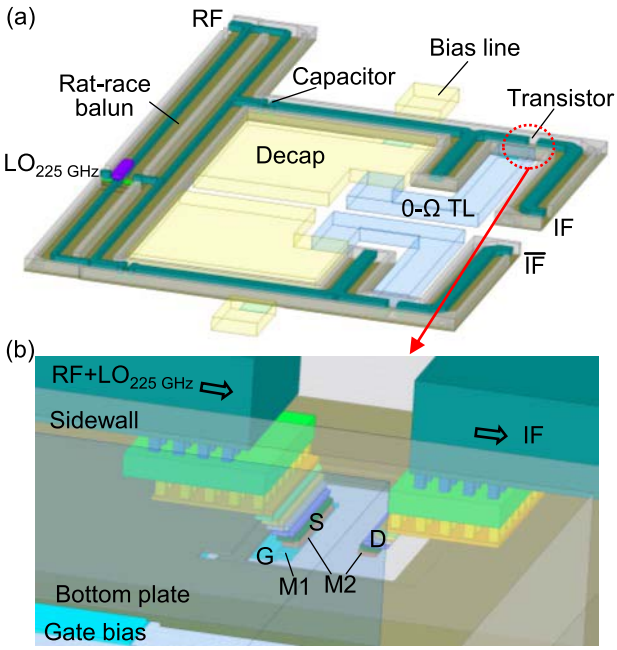
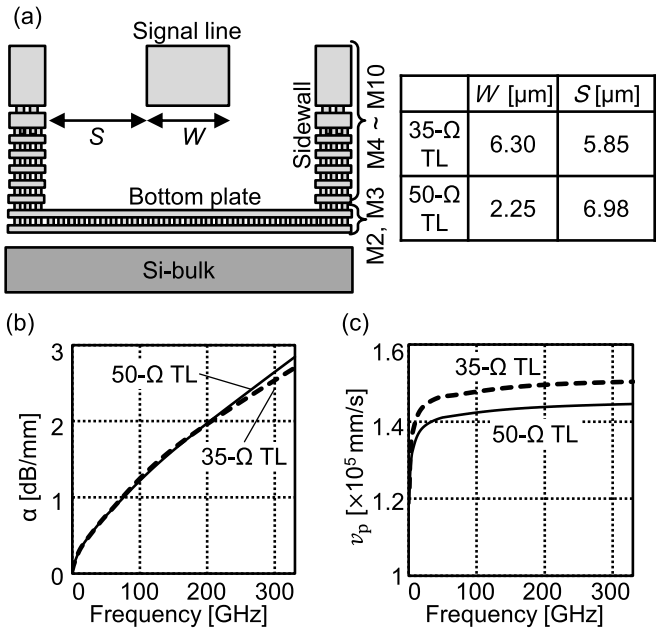


Fig. 6. (a) Layout of the 300-GHz band part. The bias line is for biasing the gate of the MOSFET. Its far end is connected to a dc pad, and the near end is connected to a decoupling capacitor and a 0-Ω transmission line (TL) [41], [42]. The latter feeds the gate. (b) Detailed metal routing for the common-gate mixing stage. The source and the drain are connected to TLs [Fig. 7(a)]. M1 layer is used to connect the 0-Ω TL and the gate.

hand, transconductance mixers offer higher gain (or lower losses) due to a nonzero drain-to-source bias but are noisier [39]. In the down-conversion circuit of our RX, we adopted a source-pumped transconductance mixer. Double-balanced mixer, adopted in our previous designs [17], was avoided due to higher layout complexity and resulting higher losses. Comparison of FET resistive mixers and transconductance mixers from a different perspective (power consumption) can be found in [25].

A schematic of the down-conversion circuit of the RX is shown in Fig. 5(a). LO and RF signals, superposed in a rat race balun, are input to the mixer. A simple low-loss L-section gives near-optimum power matching between the rat race and the mixer [29]. An open-stub notch filter is placed at the output of the mixer to suppress LO leakage. The rat race balun has a simple layout as shown in Fig. 6(a). Layout folding, often done at lower frequencies, is avoided because bends would introduce losses. On-chip dc bias lines use "0-Ω transmission lines (TLs)," having extremely small characteristic impedance [41], [42]. They closely approximate voltage biasing, and how the dc bias is supplied to dc pads (via bond wires or stud bumps) will not affect the operation of the RX. In the layout shown in Fig. 6(a), additional decoupling capacitors (decaps) further enhance decoupling capability at lower frequencies. Fig. 6(b) shows detailed metal routing for the common-gate MOSFET. To obey the design rules, connection to the gate must be via narrow strips (or fingers) of M1 metal, regardless of the choice of common terminal. In the case of a common-source stage, the same layout (narrow strips) must be replicated typically up to the M4 layer, in which they can finally form a comb. Such narrow metal strips connected vertically through vias have high parasitic resistance. We chose a common-gate stage to avoid letting a faint RF signal go through such lossy metal strips. In Fig. 6(b), the RF signal travels down to the source terminal through much larger pieces of metal. The common-gate mixer, therefore, gives somewhat better performance than the common-source mixer we adopted previously [23]. The gate feed in Fig. 6(b) is via an M1 comb and is shielded from the source feed by the bottom metal plate (actually, mesh) of the TL.

Two types of TLs, having different widths, are used in the down-conversion circuit. The cross-sectional structure of TLs is shown in Fig. 7(a). The TLs could be regarded as shielded microstrips in the sense that the center conductor couples more strongly with the metallic plate at the bottom than with the sidewalls. The characteristic impedances of the wide and narrow TLs are approximately 35 and 50 Ω, respectively. Attenuation constants and phase velocities are shown in Fig. 7(b) and (c), respectively. The 35-Ω TL occupies a larger area but has somewhat lower losses especially in the 300-GHz band. Therefore, it is used up to the input of the first buffer amplifier (except the rat race balun, which is built of 50-Ω TL) as shown in Fig. 5(a). The 50-Ω TL is used from the output of the first buffer amplifier onward. These TLs are actually considerably lossier than the lowest loss TL used in [23] and described in detail in [43]. Such an adverse design decision was made in favor of reduced sensitivity of the TL characteristics to the adhesive that may or may not cover the chip depending on whether it is flip-chip-bonded. The adhesive and the PCB are about 2 and 20 μm above the top surface of the M10 copper layer [Fig. 7(a)], respectively. The top aluminum layer is not used for the same reason. The



	W [μm]	S [μm]
35-Ω TL	6.30	5.85
50-Ω TL	2.25	6.98

Fig. 7. (a) Cross-sectional structure of the ON-chip transmission line (not to scale). (b) Electromagnetically (EM) simulated attenuation constant α versus frequency. (c) EM-simulated phase velocity $v_p = \omega/\beta$ versus frequency, where ω is the angular frequency and β is the phase constant.

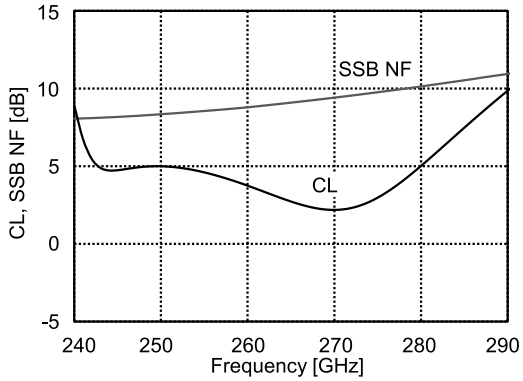


Fig. 8. Simulated frequency dependence of the transducer CL and SSB NF of the mixer in Fig. 5(b), obtained using ideal lossless passive components for matching. Input LO power is 0 dBm. The mixer was simulated by sweeping the RF frequency with a fixed LO frequency.

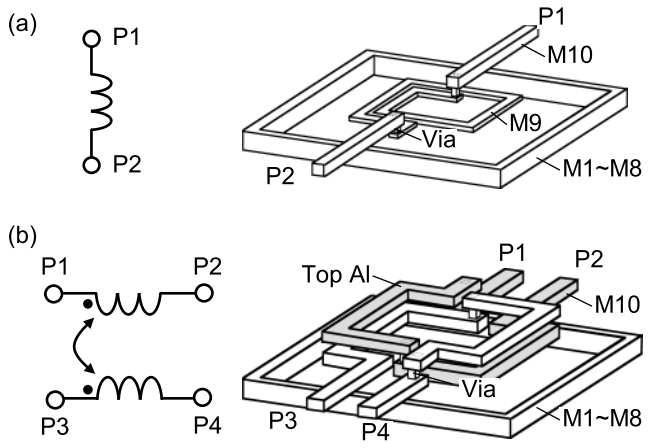


Fig. 9. (a) Parametrized 1.5-turn low-Q inductor layout. (b) Parametrized low-loss transformer layout.

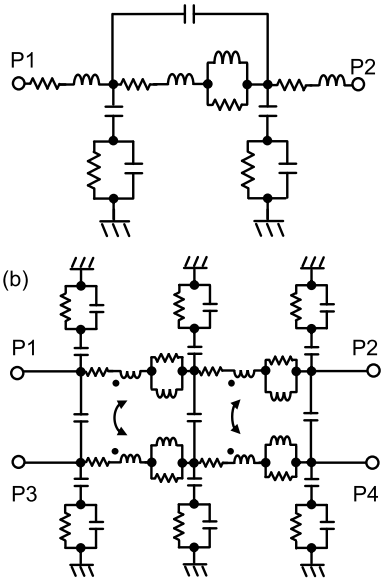


Fig. 10. (a) Circuit model of the inductor in Fig. 9(a). (b) Circuit model of the transformer in Fig. 9(b).

EM-simulated difference in phase velocities with and without adhesive and PCB is about 1% and is sufficiently small.

Detailed schematic diagrams of the down-conversion mixer and the buffer amplifier are shown in Fig. 5(b) and (c), respectively. The mixer adopts a common-gate stage. Fig. 8 shows that the minimum simulated transducer conversion loss (CL) is less than 3 dB and is smaller than that of an FET resistive mixer (about 6 dB). The transducer CL exhibits larger variations than those of SSB NF, also shown in Fig. 8, because only the former is affected by the mismatch at the output port. The differential buffer amplifier, as shown in Fig. 5(c), adopts common-source stages with cross-coupled capacitors. To obtain high gain over a wide bandwidth, large (57.6-μm-wide) transistors are used.

To achieve wide bandwidth, the matching network (MN) adopts shunt and series inductors [Fig. 5(a)]. The shunt inductors are 1.5-turn inductors with shielding rings as shown in Fig. 9(a). With hindsight, the rings could have been taller. The inductor is implemented as a parametrized cell (pcell). It is smaller in area than those available in the process design kit (PDK) offered by the manufacturer and also covers smaller inductance values. The copper layer just below the ultrathick copper layer [M10 in Fig. 7(a)] is used to make the inductor somewhat low-Q for wideband matching. The series inductors [Fig. 5(a)] are actually transformers that introduce coupling with the opposite-phase branch. The layout of the transformer is shown in Fig. 9(b). The top aluminum and the ultrathick copper layers are used to reduce losses. The transformer is also implemented as a pcell. The associated circuit models of the inductor and the transformer are shown in Fig. 10. The circuit element values are given by polynomial functions of the inner radius of the loop. The functions were determined using EM simulation data. Fig. 11 shows that the S-parameters

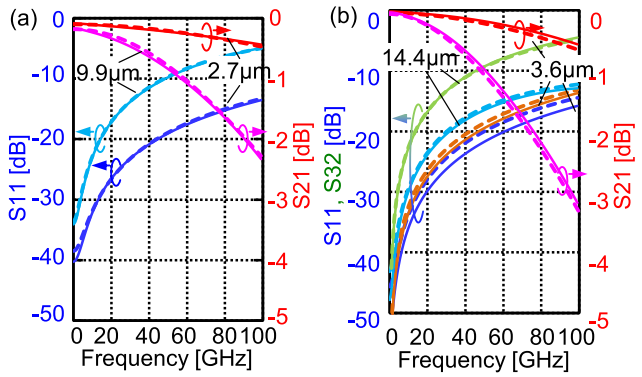


Fig. 11. S-parameters up to 100 GHz from EM simulation (solid) and from pcell models (dashed) of (a) inductors [Fig. 9(a)] of radii 2.7 and 9.9 μm, and of (b) transformers [Fig. 9(b)] of radii 3.6 and 14.4 μm.

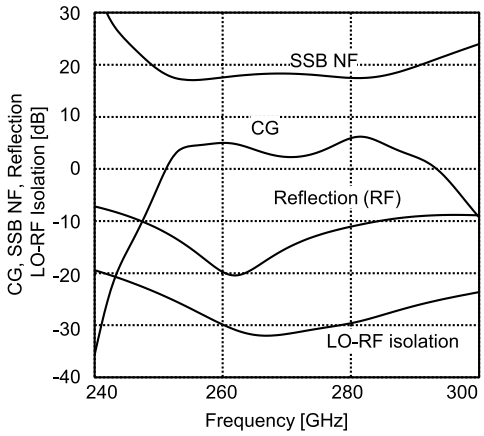


Fig. 12. Simulated transducer CG, SSB NF, RF port reflection, and LO-to-RF isolation of the down-conversion circuit in Fig. 5(a).

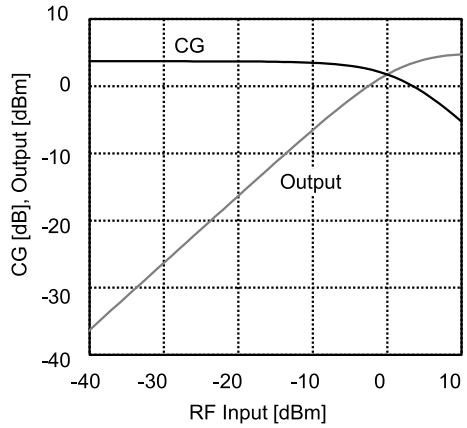


Fig. 13. Simulated output power and CG versus RF input power of the down-conversion circuit in Fig. 5(a). LO input power is 0 dBm.

from the models in Fig. 10 agree well with those from EM simulation.

The simulated transducer conversion gain (CG) and SSB NF of the down-conversion circuit [Fig. 5(a)] are shown in Fig. 12. The peak transducer CG is 6.2 dB, the minimum

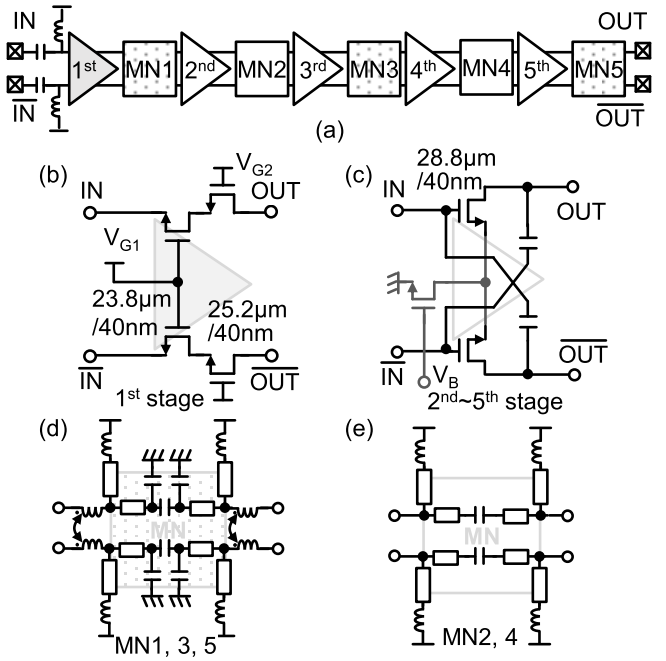


Fig. 14. (a) Block diagram of the IF amplifier. (b) Schematic of the first stage. (c) Second to fifth stages. (d) Matching networks 1, 3, and 5. (e) Matching networks 2 and 4.

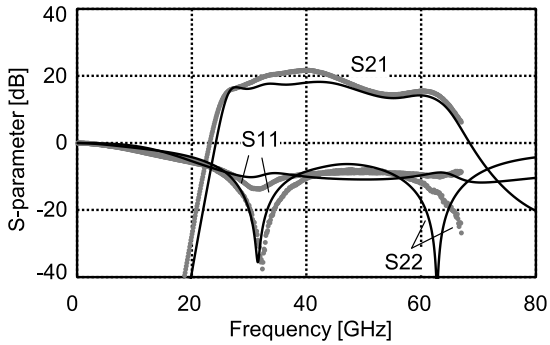


Fig. 15. Measured (gray dots) and simulated (solid) S-parameters of stand-alone IF amplifier. Presented data include characteristics of pads and access lines.

SSB NF is 17.0 dB, and the RF input reflection magnitude is below −10 dB between 247 and 283 GHz. Fig. 13 shows that the input 1-dB compression point, IP_{1dB}, at the RF frequency of 265 GHz is −4 dBm.

The IF amplifier is required to have an extremely wide fractional bandwidth (∼100%) and high gain (>20 dB). The requirement for the bandwidth makes the distributed amplifier a candidate, but it is essentially a transmission line periodically loaded with single-stage amplifiers. To meet the gain requirement, we chose an ordinary multistage amplifier. The schematic diagrams of the IF amplifier and its components are shown in Fig. 14. It consists of five differential amplifier stages. The first stage is a common-gate amplifier, which facilitates wideband impedance matching. Common-source stages with cross-coupled capacitors are used in subsequent stages to obtain high gain. Transistors are 28.8 μm in width. The schematics of MNs are shown in Fig. 14(d) and (e).

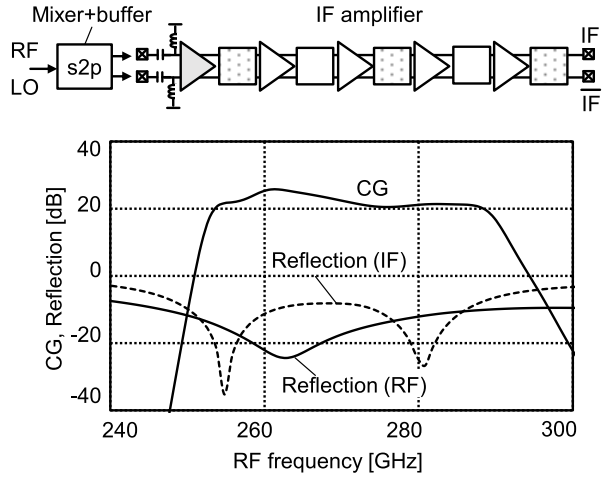


Fig. 16. Simulated RX CG, input (RF) reflection, and output (IF) reflection.

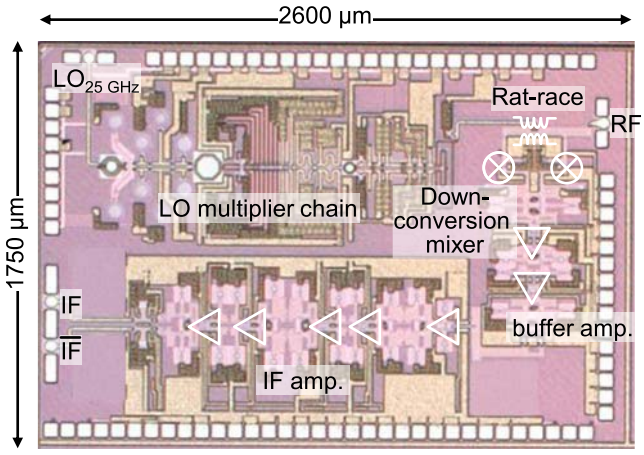


Fig. 17. Die micrograph of the 300-GHz-band CMOS receiver (cf. Fig. 4).

The simulated and measured S-parameters of a stand-alone IF amplifier are shown in Fig. 15.

The simulated CG and input (RF) and output (IF) reflection magnitudes of the RX are shown in Fig. 16. In the simulation, use was made of cross-frequency S-parameters of the mixer stage. The peak CG is 25.7 dB. A micrograph of the RX chip is shown in Fig. 17. The chip measures 2.60 × 1.75 mm^2.

B. PCB Including Waveguide Transition

Two PCBs were designed, one for probing measurements and the other for waveguide measurements. The PCB for probing measurements is basically for supplying dc power through bond wires, and therefore the RX chip is mounted on it face-up.

The other PCB, as shown in Fig. 18(a) and (b), adopts flip-chip bonding and has a WR-3.4 waveguide transition built into it. It allows wireless link measurements with an antenna having a WR-3.4 interface. The RX chip was mounted on one side of the PCB and a WR-3.4 waveguide flange was attached to the opposite side [Fig. 18(a)]. LO and IF signals, respectively, arrive and leave via coaxial connectors. The signal paths

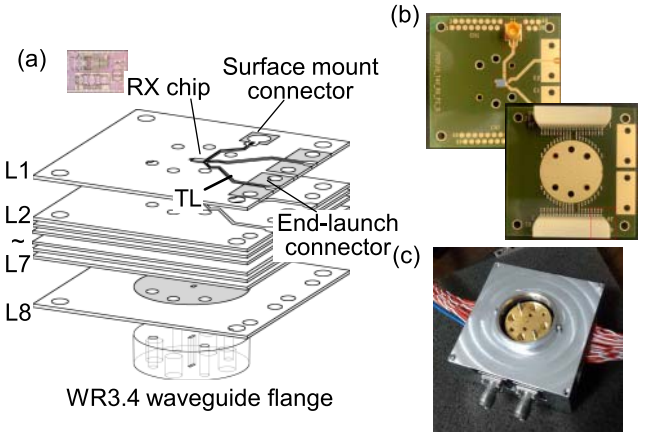


Fig. 18. (a) Design of multilayer PCB for flip-chip bonding of the RX chip and waveguide connection. (b) Photographs of the PCB. (c) Encased RX module.

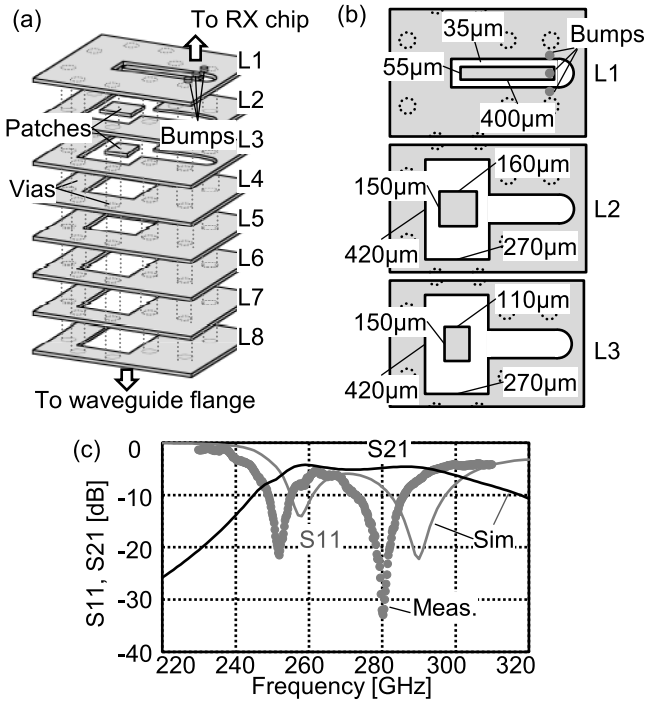


Fig. 19. (a) Waveguide transition built into the PCB. The metal layers are shown in gray and substrate dielectrics are not shown. The spacing between metal layers is not to scale. (b) Details of the metal layers L1–L3. These layers are nominally 15-μm thick, and the spacing between L1 and L2 (and L2 and L3) is 30 μm. (c) S-parameters of the transition. Port 1 (wave port) is at the bottom of the waveguide flange. Port 2 (wave port) is on the ON-chip 35-Ω TL connected to GSG pads. S_{11} was measured with a flip-chip-mounted RX chip.

between the coaxial connectors and stud bumps connected to the RX chip are on-PCB TLs.

The structure of the waveguide transition, located at the center of the PCB, is shown in Fig. 19(a). A vertical quasi-waveguide is formed in the PCB by arranging rectangular apertures in L2–L8 metal layers with the vias surrounding the apertures. The stacked rectangular metal patches with different sizes [Fig. 19(b)] located at the centers of the apertures in

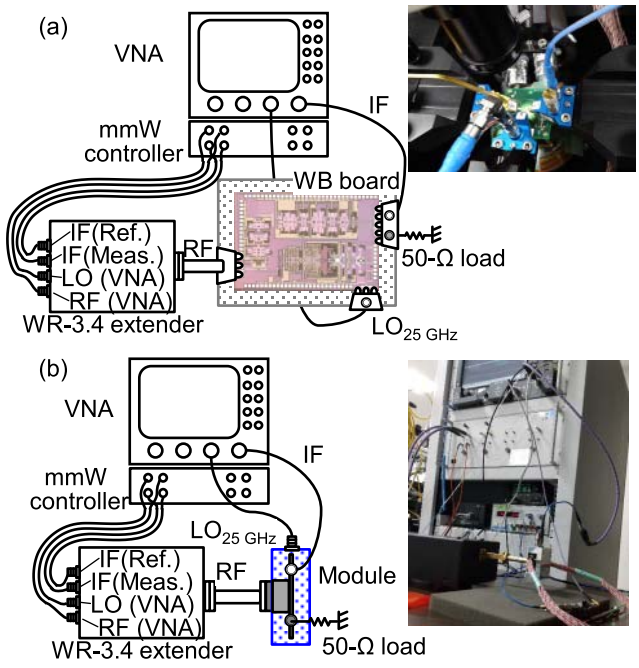


Fig. 20. (a) Probing measurement setup. (b) Module measurement setup.

TABLE I
PACKAGING LOSS BUDGET

Item	Loss estimate
From GSG pads to WR-3.4 interface @RF	~ 6 dB
From GSGSG pads to PCB TLs @IF	~ 5.5 dB
End-launch coax connectors @IF	~ 1.5 dB

the L2 and L3 layers create double resonance for broadband operation. The upper patch (in L2) is electrically coupled (without any vias) to an open end of a coplanar waveguide in the L1 layer. The other end of the coplanar waveguide is terminated with GSG stud bumps, to which the RX chip is flip-chip-connected.

The S-parameters of the waveguide transition are shown in Fig. 19(c). In the EM simulation, port 1 reference plane is at the bottom of the WR-3.4 waveguide flange [Fig. 18(a)], and port 2 reference plane is on the the ON-chip 35-Ω TL connected to GSG pads. The reference impedances of the ports are the complex natural reference impedances [44] of the respective waveguides (not 50 Ω). The adhesive that covers the upper surface of PCB was taken into consideration. The simulated peak $|S_{21}|$ was -4 dB. The loss is comparable to that of the chip-to-waveguide coupler presented in [45].

The PCB with an RX chip, complete with a waveguide flange and coaxial connectors, was put in an aluminum case, as shown in Fig. 18(c).

III. MEASUREMENT

The performance of the chip was measured first by on-wafer probing. The measurement setup is shown in Fig. 20(a). High-frequency signals were supplied via RF probes. $LO_2$5GHz and RF signal (before up-conversion) were both generated by a

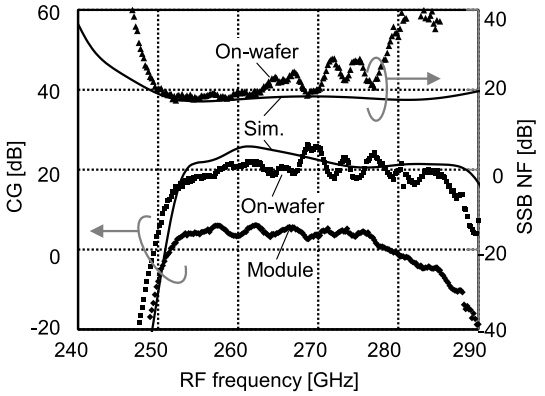


Fig. 21. Measured and simulated CG and SSB NF of the RX. CG was measured on-wafer [Fig. 20(a)] and via waveguide transition [Fig. 20(b)].

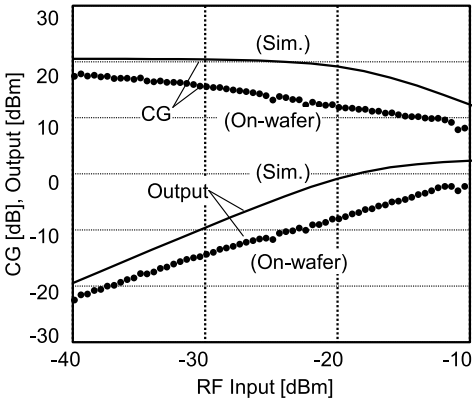


Fig. 22. Measured and simulated output power and CG of the RX versus input power. RF frequency is 265 GHz.

vector network analyzer (VNA) Keysight PNA-X N5247A. The RF signal underwent up-conversion by a WR-3.4-band (220–325-GHz) frequency extender from VDI. The down-converted signal was measured with VNA. One of the differential IF outputs (Fig. 4) was terminated with a 50-Ω load, screwed onto a GSGSG probe. A cold-source method was used to measure the NF.

The measured CG and SSB NF are shown in Fig. 21 together with the simulation results corresponding to on-wafer measurement setup. The frequency responses of the on-wafer and module CG are roughly consistent. The peak on-wafer CG is 26 dB, the peak module CG is 6 dB, and the minimum SSB NF is 17.4 dB. The measured frequency responses are bumpier than the simulation results. The reason for the discrepancies between measurement and simulation is presumably due to cumulative inaccuracies in models used in simulation. The CG of the RX module is roughly 15 dB lower than that from on-wafer measurement. The packaging loss budget is presented in Table I. The estimated loss associated with the waveguide transition is somewhat higher than the simulated value in Fig. 19(c) because surface roughness of the inner surface of the waveguide flange and possible misalignment between the flange and the PCB are not taken into account in

TABLE II
PERFORMANCE COMPARISON OF SOLID-STATE-INTEGRATED CIRCUIT-BASED SUB-THz RECEIVERS

Ref.	[11]	[16]	[17]	[19]	[23]	[24]	[30]	[46]	This work
Technology	35-nm GaAs mHEMT	80-nm InP HEMT	40-nm CMOS	40-nm CMOS	40-nm CMOS	65-nm CMOS	130-nm SiGe HBT	65-nm CMOS	40-nm CMOS
Circuit type	TX, RX	TX, RX	RX	RX	TRX	TRX	TX, RX	TRX	RX
RX 1st stage	LNA	LNA	Mixer	Mixer	Mixer	Mixer	Mixer	Mixer	Mixer
Frequency (GHz)	300	290	304	291	265.68	256	230	270	265.68
Peak Conversion gain (dB)	−19 (module)	-	−18 (on-wafer)	−23.7 (module)	9.5 (on-wafer)	7*	8 (module)	22 (module)	26 (on-wafer)
SSB NF (dB)	-	-	25.5 (min) (on-wafer)	33 (min) (module)	20.9 (min) (on-wafer)	-	14	22.2 (min) (module)	17.4 (min) (on-wafer)
P_{dc} (W)	-	4.5 (RX)	0.42	0.65	0.89 (RX)	0.75 (RX)	4.5 (RX)	0.84 (TRX)	0.47
Chip size (mm^2)	2.43	1.00 (mixer)	2.29	3.15	11.07	4.16	1.52	5	4.55
Modulation	QPSK	16QAM	16QAM	16QAM	16QAM	16QAM	16QAM	FMCW	16QAM
Data rate (Gbit/s)	64	120	32	20	80	36	80	-	76
Distance (cm)	100	980	5	10	3	2.5	100	200	6
Wireless experiment	Module	Module	On-wafer	Module	On-wafer	On-PCB antenna	Module	SIW antenna + lens	Module

*Read off from a graph.

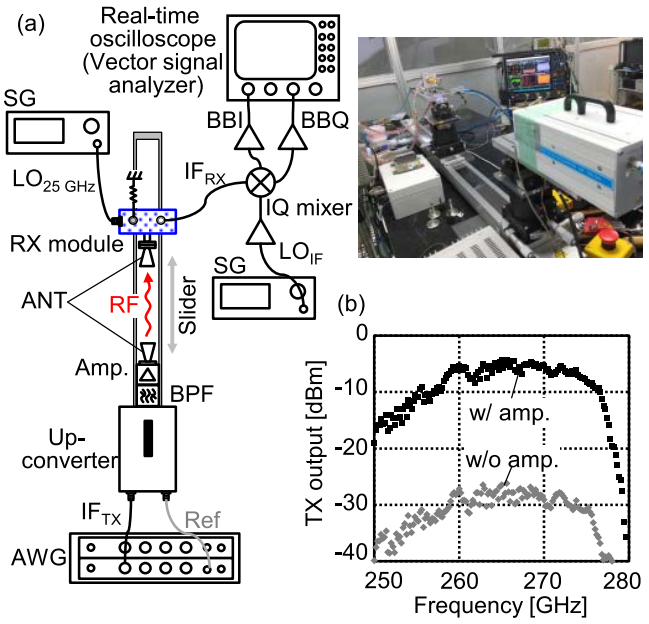


Fig. 23. (a) Over-the-air measurement setup. (b) Transmitter output power with and without a commercial off-the-shelf WR-3.4 amplifier.

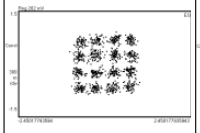
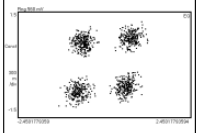
Constellation		
Modulation	16QAM	QPSK
Distance [cm]	6	100
EVM [%rms]	13.04	25.93
BER	2.27×10^{-4}	5.75×10^{-5}
Center frequency [GHz]	265.68	266.76
Symbol rate [Gbaud]	19	2.16
Data rate [Gbit/s]	76	4.32

Fig. 24. Measurement results at the highest data rate of 76 Gbit/s (left) and over the longest distance of 100 cm (right, limited by the measurement setup). The center frequencies for 16 QAM and QPSK are the same as those of channels 66 and 7, respectively, of 802.15.3d [6]. EVM: Error vector magnitude. BER: Bit error rate.

the simulation. The remaining entries in Table I are estimated from EM simulation and a data sheet from the manufacturer. The estimated losses do not quite add up to 15 dB, and measurement-based loss budgeting would be necessary to fully account for the losses. The power consumption is 467 mW. The output RF power and CG are shown in Fig. 22 as functions of the input RF power. The input RF power was swept by changing the VNA output power fed to the frequency extender. The output power of the extender was calibrated using a VDI PM-5 power meter. The measured $IP_{1\,dB}$ is −34 dBm. Significant soft compression is observed and the cause is under investigation.

Wireless link measurements were performed using the RX module and the setup shown in Fig. 23(a). The TX consists of an arbitrary waveform generator (AWG) (Keysight M8195A), an up-converter (Farran FBUC-03-300), a bandpass filter, and an amplifier. The TX performance is shown in Fig. 23(b). The 26-dBi horn antennas were used both on the transmitting and receiving sides. The down-converted IF signal from the RX module was led to an external IQ mixer, and the baseband signals were generated by mixing it with an LO (LO_{IF}) signal. The amplified baseband IQ signals were analyzed using a real-time oscilloscope (Keysight UXR1104A), capable of vector signal demodulation and channel equalization. The RX module was mounted on a movable slider stage.

Fig. 24 shows the results of wireless link measurements. The CMOS RX module achieves the highest data rate of 76 Gbit/s with 16 QAM over a distance of 6 cm. At a distance of 1 m, a data rate of 4.32 Gbit/s is achieved with QPSK. Note that the longest distance of 1 m is limited by the measurement setup [Fig. 23(a)]. Fig. 25 shows wireless measurement results with

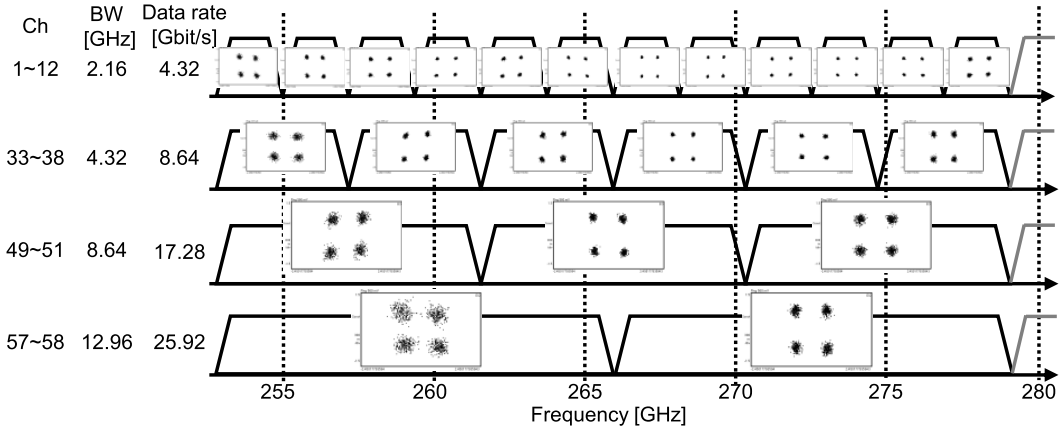


Fig. 25. QPSK signal constellations measured on 802.15.3d channels [Fig. 2(b)] below 280 GHz over a 12-cm distance.

QPSK over altogether 23 IEEE Std 802.15.3d channels that are below 280 GHz [Fig. 2(b)]. Bit error rates (BERs) are all well below 10^{-3}.

Performance of recently reported sub-THz RXs is compared in Table II. Our RX achieved a competitive data rate, given the facts that the technology adopted is 40-nm bulk CMOS and that the measurement was made via the WR-3.4 waveguide interface. Note also that the distance depends very much on the antennas used.

IV. Conclusion

We presented a mixer-first CMOS RX operating at 265 GHz. The RX chip was modularized with a WR-3.4 waveguide interface, enabling wireless link experiments using waveguide components including antennas. The waveguide transition was built into a multilayer PCB. Wireless data reception with QPSK was demonstrated over 23 (out of 65) channels defined in IEEE Std 802.15.3d (Fig. 25). The RX module achieved the highest data rate of 76 Gbit/s with 16 QAM over a distance of 6 cm, whereas the data rate was 4.32 Gbit/s with QPSK over 1 m (Fig. 24). The distance of 6 cm may not be exactly great. However, there clearly is room for improvement, and the results presented herein by no means represent what can be achieved by CMOS technology and WR-3.4 interface. The distance could possibly be made longer even with the present RX using the Cassegrain antennas used in [28].

We made efforts to make the RX low-noise and high-conversion-gain, resulting in a rather simple design. We had to make a tough decision about the design of ON-chip TLs so that the RX operates properly whether measured on-wafer or after flip-chip bonding. To further extend the communication distance while maintaining data rates, losses due to PCB at IF, in particular, must be reduced significantly (Table I). In wireless measurements, the signal-to-noise ratio (SNR) on the transmitting side also affects the outcomes and should be considered [47].

Acknowledgment

The authors thank Dr. Diawuo Henry Abu of the Nagoya Institute of Technology and all other collaborators for their help.

References

[1] G. Ducournau *et al.*, "THz communications using photonics and electronic devices: The race to data-rate," *J. Infr., Millim., THz Waves*, vol. 36, no. 2, pp. 198–220, Feb. 2015, doi: 10.1007/s10762-014-0112-x

[2] H.-J. Song and T. Nagatsuma, *Handbook of Terahertz Technologies: Devices and Applications*. Redwood City, CA, USA: Pan Stanford Publishing, 2015.

[3] *AMATERASU*. Accessed: Jul. 12, 2022. [Online]. Available: https://smiles-p6.nict.go.jp/thz/jp/decay.html

[4] *Final Acts WRC-19*. Accessed: Jul. 12, 2022. [Online]. Available: http://handle.itu.int/11.1002/pub/813b5921-en

[5] T. Kürner and A. Hirata, "On the impact of the results of WRC 2019 on THz communications," in *Proc. Int. Workshop Mobile THz Syst. (IWMTS)*, Jul. 2020, pp. 1–3, doi: 10.24355/dbbs.084-202008031403-0.

[6] *IEEE Standard for High Data Rate Wireless Multi-Media Networks–Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer*, IEEE Standard 802.15.3d-2017, 2017.

[7] J.-D. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2012, pp. 48–49, doi: 10.1109/VLSIC.2012.6243783.

[8] H.-J. Song, J.-Y. Kim, K. Ajito, N. Kukutsu, and M. Yaita, "50-Gb/s direct conversion QPSK modulator and demodulator MMICs for terahertz communications at 300 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 3, pp. 600–609, Mar. 2014, doi: 10.1109/TMTT.2014.2300844.

[9] S. Zeinolabedinzadeh *et al.*, "A 314 GHz, fully-integrated SiGe transmitter and receiver with integrated antenna," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 361–364, doi: 10.1109/RFIC.2014.6851742.

[10] S. Kim *et al.*, "300 GHz integrated heterodyne receiver and transmitter with on-chip fundamental local oscillator and mixers," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 1, pp. 92–101, Jan. 2015, doi: 10.1109/TTHZ.2014.2364454.

[11] I. Kallfass *et al.*, "Towards MMIC-based 300 GHz indoor wireless communication systems," *IEICE Trans. Electron.*, vol. E98-C, no. 12, pp. 1081–1090, Dec. 2015, doi: 10.1587/transele.E98.C.1081.

[12] K. Katayama *et al.*, "A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3037–3048, Dec. 2016, doi: 10.1109/JSSC.2016.2602223.

[13] K. Katayama, K. Takano, S. Amakawa, S. Hara, T. Yoshida, and M. Fujishima, "CMOS 300-GHz 64-QAM transmitter," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540218.

[14] K. Takano, K. Katayama, S. Amakawa, T. Yoshida, and M. Fujishima, "Wireless digital data transmission from a 300 GHz CMOS transmitter," *Electron. Lett.*, vol. 52, no. 15, pp. 1353–1355, Jul. 2016, doi: 10.1049/EL.2016.1148.

[15] K. Takano *et al.*, "A 105 Gb/s 300 GHz CMOS transmitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 308–309, doi: 10.1109/ISSCC.2017.7870384.

[16] H. Hamada *et al.*, "300-GHz-band 120-Gb/s wireless front-end based on InP-HEMT PAs and mixers," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2316–2335, Sep. 2020, doi: 10.1109/JSSC.2020.3005818.
[17] S. Hara *et al.*, "32-Gbit/s CMOS receivers in 300-GHz band," *IEICE Trans. Electron.*, vol. E101-C, no. 7, pp. 464–471, Jul. 2018, doi: 10.1587/transele.E101.C.464.
[18] K. Takano *et al.*, "300-GHz CMOS transmitter module with built-in waveguide transition on a multilayered glass epoxy PCB," in *Proc. IEEE Radio Wireless Symp.*, Jan. 2018, pp. 154–156, doi: 10.1109/RWS.2018.8304972.
[19] S. Hara *et al.*, "300-GHz CMOS receiver module with WR-3.4 waveguide interface," in *Proc. Eur. Microw. Conf.*, Sep. 2018, pp. 396–399, doi: 10.23919/EuMC.2018.8541693.
[20] S. Lee *et al.*, "A 6-mW-DC-power 300-GHz CMOS receiver for near-field wireless communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 504–507, doi: 10.1109/MWSYM.2019.8700961.
[21] M. Fujishima and S. Amakawa, *Design of Terahertz CMOS Integrated Circuits for High-Speed Wireless Communication*. Edison, NJ, USA: IET, 2019, doi: 10.1049/PBCS035E.
[22] S. Kim, D. Yoon, and J.-S. Rieh, "A 270-GHz CMOS triple-push ring oscillator with a coupled-line matching network," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 5, pp. 449–462, Sep. 2019, doi: 10.1109/TTHZ.2019.2923556.
[23] S. Lee *et al.*, "An 80-Gb/s 300-GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019, doi: 10.1109/JSSC.2019.2944855.
[24] I. Abdo *et al.*, "A 300 GHz-band phased-array transceiver using bi-directional outphasing and Hartley architecture in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 316–317, doi: 10.1109/ISSCC42613.2021.9365968.
[25] C. M. Grotsch, I. Dan, L. John, S. Wagner, and I. Kallfass, "A compact 281–319 GHz low-power downconverter MMIC for superheterodyne communication receivers," *IEEE Trans. THz Sci. Technol.*, vol. 11, no. 2, pp. 231–239, Mar. 2021, doi: 10.1109/TTHZ.2020.3038043.
[26] T. Hagiwara *et al.*, "A 258-GHz CMOS transmitter with phase-shifting architecture for phased-array systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 705–708, doi: 10.1109/IMS19712.2021.9574976.
[27] S. Lee *et al.*, "A 272-GHz CMOS analog BPSK/QPSK demodulator for IEEE 802.15.3d," in *Proc. IEEE 47th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2021, pp. 415–418, doi: 10.1109/ESSCIRC53450.2021.9567798.
[28] Y. Morishita *et al.*, "300-GHz-band OFDM video transmission with CMOS TX/RX modules and 40 dBi Cassegrain antenna toward 6G," *IEICE Trans. Electron.*, vol. E104.C, no. 10, pp. 576–586, Oct. 2021, doi: 10.1587/transele.2021MMP0005.
[29] S. Hara *et al.*, "A 76-Gbit/s 265-GHz CMOS receiver," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2021, pp. 1–3, doi: 10.1109/A-SSCC53895.2021.9634780.
[30] P. Rodríguez-Vázquez, J. Grzyb, and U. R. Pfeiffer, "RF front-end impairments for ultra-broadband wireless communication above 200 GHz," in *Proc. 16th Int. Symp. Wireless Commun. Syst. (ISWCS)*, Aug. 2019, pp. 335–339, doi: 10.1109/ISWCS.2019.8877308.
[31] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-GHz circularly polarized FMCW radar with a single-lens-coupled SiGe HBT chip," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 6, pp. 771–783, Nov. 2016, doi: 10.1109/TTHZ.2016.2602539.
[32] H. Jalili and O. Momeni, "A 436-to-467 GHz lens-integrated reconfigurable radiating source with continuous 2D steering and multi-beam operations in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 326–327, doi: 10.1109/ISSCC42613.2021.9365987.
[33] X. Yi *et al.*, "Emerging terahertz integrated systems in silicon," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 9, pp. 3537–3550, Sep. 2021, doi: 10.1109/TCSI.2021.3087604.
[34] S. Rey, D. Ulm, T. Kleine-Ostmann, and T. Kiirner, "Performance evaluation of a first phased array operating at 300 GHz with horn elements," in *Proc. 11th Eur. Conf. Antennas Propag. (EUCAP)*, Mar. 2017, pp. 1629–1633, doi: 10.23919/EuCAP.2017.7928868.
[35] T. Merkle *et al.*, "Testbed for phased array communications from 275 to 325 GHz," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2017, pp. 1–4, doi: 10.1109/CSICS.2017.8240474.
[36] G. D. Ntouni *et al.*, "Real-time experimental wireless testbed with digital beamforming at 300 GHz," in *Proc. Eur. Conf. Netw. Commun. (EuCNC)*, Jun. 2020, pp. 271–275, doi: 10.1109/EuCNC48522.2020.9200948.
[37] R. Dong, S. Hara, I. Watanabe, S. Tanoi, T. Hagino, and A. Kasamatsu, "A 213–233 GHz ×9 frequency multiplier chain with 4.1 dBm output power in 40 nm bulk CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 458–461, doi: 10.1109/IMS19712.2021.9574846.
[38] S. A. Maas, "A GaAs MESFET mixer with very low intermodulation," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-35, no. 4, pp. 425–429, Apr. 1987, doi: 10.1109/TMTT.1987.1133665.
[39] S. A. Maas, *The RF and Microwave Circuit Design Cookbook*. Norwood, MA, USA: Artech House, 1998.
[40] K. Ohmori and S. Amakawa, "Direct white noise characterization of short-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1478–1482, Apr. 2021, doi: 10.1109/TED.2021.3059720.
[41] S. Amakawa, R. Goda, K. Katayama, K. Takano, T. Yoshida, and M. Fujishima, "Wideband CMOS decoupling power line for millimeter-wave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4, doi: 10.1109/MWSYM.2015.7167043.
[42] S. Amakawa and M. Fujishima, "Wideband power-line decoupling technique for millimeter-wave CMOS integrated circuits," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2019, pp. 1–4, doi: 10.1109/ISCAS.2019.8702640.
[43] S. Amakawa *et al.*, "Causal characteristic impedance determination using calibration comparison and propagation constant," in *Proc. 92nd ARFTG Microw. Meas. Conf.*, Jan. 2019, pp. 1–6, doi: 10.1109/ARFTG.2019.8637225.
[44] S. Amakawa, "Scattered reflections on scattering parameters—Demystifying complex-referenced S parameters—," *IEICE Trans. Electron.*, vol. E99-C, no. 10, pp. 1100–1112, Oct. 2016, doi: 10.1587/transele.E99.C.1100.
[45] C. Wang, X. Yi, M. Kim, Q. B. Yang, and R. Han, "A terahertz molecular clock on CMOS using high-harmonic-order interrogation of rotational transition for medium-/long-term stability enhancement," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 566–580, Feb. 2021, doi: 10.1109/JSSC.2020.3021335.
[46] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220-to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, Feb. 2021, doi: 10.1109/JSSC.2020.3020291.
[47] S. Lee *et al.*, "300-GHz wireless data transmission system with low-SNR CMOS RF front end," in *Proc. 12th Global Symp. Millim. Waves (GSMM)*, May 2019, pp. 32–34, doi: 10.1109/GSMM.2019.8797671.

Shinsuke Hara (Member, IEEE) received the B.E., M.E., and Ph.D. degrees in physics from the Tokyo University of Science, Tokyo, Japan, in 2000, 2002, and 2005, respectively.

In 2013, he joined the National Institute of Information and Communication Technology (NICT), Koganei, Japan, as a Researcher. His research interests are millimeter-wave CMOS circuits' design and nano-scale semiconductor devices.

Ruibing Dong received the B.E. degree from Hunan University, Changsha, China, in 2004, the M.E. degree from the South China University of Technology, Guangzhou, China, in 2008, and the Ph.D. degree from Kyushu University, Fukuoka, Japan, in 2011.

In 2015, he joined the National Institute of Information and Communication Technology (NICT), Koganei, Japan, as a Researcher. His research interests are millimeter-wave and low-power CMOS circuits.

Sangyeop Lee (Member, IEEE) received the B.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2009, and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Yokohama, Japan, in 2010 and 2013, respectively.

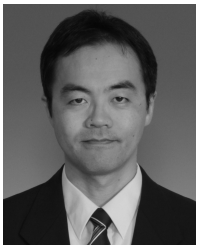
After working for a Korean research institute, Agency for Defense Development (ADD), Daejeon, South Korea, he joined Hiroshima University, Higashihiroshima, Japan, as a Researcher and an Assistant Professor, from 2017 to 2020. In 2020, he joined the Tokyo Institute of Technology, where he is currently an Assistant Professor. His current research interests include design of millimeter-wave/terahertz CMOS circuits and IoT sensors.

Kyoya Takano (Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 2006, 2008, and 2012, respectively.

From 2012 to 2018, he was a Project Assistant Professor with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Higashihiroshima, Japan. In 2018, he joined the Tokyo University of Science, Tokyo, as an Assistant Professor. He has been a Junior Associate Professor since 2021 and has been an Associate Professor with the Department of Electrical Engineering since 2022. His current research interests include design of millimeter-wave and terahertz integrated circuits.

Naoya Toshida received the B.E. degree in electrical and electronic engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 2020, where he is currently pursuing the M.E. degree in electrical and mechanical engineering.

His main interest is planar-line-to-waveguide transition in millimeter-waveband and above.



Akifumi Kasamatsu received the B.E., M.E., and Ph.D. degrees in electronics engineering from Sophia University, Tokyo, Japan, in 1991, 1993, and 1997, respectively.

From 1997 to 1999, he was a Research Assistant with Sophia University. From 1999 to 2002, he was with Fujitsu Laboratories Ltd., Atsugi, Japan. Since 2002, he has been with the National Institute of Information and Communications Technology (NICT), Koganei, Japan, where he is currently working as an Executive Researcher and a Principal Investigator of the terahertz wave electronics project. His current research interests are in wireless communication technology such as wireless transceivers and nano-scale semiconductor devices for millimeter-wave and terahertz-wave communications.

Kunio Sakakibara (Senior Member, IEEE) received the B.E. degree in electrical and computer engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1991, and the M.E. and D.E. degrees in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1993 and 1996, respectively.

From 1996 to 2002, he was with Toyota Central Research and Development Laboratories, Inc., Nagakute, Japan, where he was involved in the development of antennas for automotive millimeter-wave radar systems. From 2000 to 2001, he was a Guest Researcher with the Department of Microwave Techniques, University of Ulm, Ulm, Germany. In 2002, he joined the Nagoya Institute of Technology, as a Lecturer. Since 2004, he has been an Associate Professor, and he became a Professor with the Nagoya Institute of Technology in 2012. His current research interests include millimeter-wave and terahertz-wave antennas and feeding circuits.

Takeshi Yoshida (Member, IEEE) received the B.E., M.E., and D.E. degrees in electronics engineering from Hiroshima University, Higashihiroshima, Japan, in 1994, 1996, and 2004, respectively.

From 1996 to 2001, he was with the System Electronics Laboratories, Nippon Telegraph and Telephone Corporation, Atsugi, Japan. He is currently an Associate Professor with the Graduate School of Advanced Science and Engineering, Hiroshima University.

Dr. Yoshida is a member of the Institute of Electronics, Information and Communication Engineers.

Shuhei Amakawa (Member, IEEE) received the B.Eng., M.Eng., and Ph.D. degrees in engineering from the University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2001, respectively, and the M.Phil. degree in physics from the University of Cambridge, Cambridge, U.K., in 2000.

He was a Research Fellow with the Cavendish Laboratory, University of Cambridge, from 2001 to 2004. After working for a couple of electronic design automation (EDA) companies, he joined the Tokyo Institute of Technology, Tokyo, in 2006. Since 2010, he has been with Hiroshima University, Higashihiroshima, Japan, where he is currently an Associate Professor. His research interests include modeling and simulation of nanoelectronic devices and systems, design of RF circuits and interconnects, and microwave theory and measurement.

Dr. Amakawa currently serves as a Committee Member for the International Solid-State Circuits Conference and the International Microwave Symposium.

Minoru Fujishima (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1988, 1990, and 1993, respectively.

He joined the faculty with the University of Tokyo in 1988 as a Research Associate. He has been an Associate Professor with the School of Frontier Sciences, University of Tokyo, since 1999. He was a Visiting Professor with the ESAT-MICAS Laboratory, Katholieke Universiteit Leuven, Leuven, Belgium, from 1998 to 2000. Since 2009, he has been a Professor with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Higashihiroshima, Japan. He studied design and modeling of CMOS and BiCMOS circuits, nonlinear circuits, single-electron circuits, and quantum-computing circuits. He coauthored more than 40 journal articles and 100 conference papers, and a book titled *Design and Modeling of Millimeter-Wave CMOS Circuits for Wireless Transceivers: Era of Sub-100nm Technology* (Springer, 2008). His current research interests are in the designs of low-power millimeter- and short-millimeter-wave wireless CMOS circuits.

Dr. Fujishima is currently serving as a Technical Committee Member for several international conferences. He is a member of Institute of Electronics, Information and Communication Engineers (IEICE) and Japan Society of Applied Physics (JSAP). He was a Distinguished Lecturer of Solid-State Circuits Society (SSCS) from 2011 to 2012. He was the Chair of the IEEE SSCS Kansai Chapter from 2013 to 2014.