A Fractional-N Synthesizable PLL Using DTC-Based Multistage Injection With Dithering-Assisted Local Skew Calibration

Zule Xu, *Member, IEEE*

Abstract—A standard-cell-based fractional-N synthesizable phase-locked loop (PLL) [or multiplying-delay-locked loop (MDLL)] is proposed, where the multiple phases of the three-stage ring digitally controlled oscillator (DCO) are utilized for injection. The required digital-to-time converter (DTC) range is reduced to one third of the DCO's period, resulting in higher linearity, less jitter, lower power consumption, and smaller area. The issue of the mismatches among DCO's stages is solved by the proposed dithering-assisted local skew calibration, which removes the skews in the injection path and smears out the periodic pattern at the PLL side to reduce spurs. Most of the dithering noise is suppressed by the injection locking and the phase tracking loop. Measured at 1.0095-GHz output frequency with 24-MHz reference frequency, with the proposed solution, the integrated root-mean-square (rms) jitter can be reduced from 6.40 to 2.55 ps, and the power consumption is 3.36 mW. This translates to -226.6-dB figure of merit (FoM) and -232.8-dB FoM$_{ref}$. The measured fundamental fractional spurs range from -56 to -45 dBc.

Index Terms—Dithering, fractional-N phase-locked loop (PLL), injection locking, multiplying-delay-locked loop (MDLL), synthesizable.

I. INTRODUCTION

PHASE-LOCKED loops (PLLs) are imperative building blocks in wireless system-on-chips (SoCs) for modulation/demodulation and clock generation. Their designs often take long time, especially when multiple PLLs are needed in a large-scale SoC. Moreover, once the specification or the process technology is changed, almost the same redesign time can be required. Such an issue increases the development cost for a team with a small number of circuit designers. To reduce the development cost, standard-cell-based synthesizable PLLs have been proposed. Their digital architectures enable all the circuits to be described in register-transfer-level (RTL) codes

and to be placed and routed automatically through a common digital implementation flow. In this way, the design/redesign time can be drastically reduced, and the RTL and place-and-route (P&R) codes are friendly to be ported to another design with a different specification or process technology. Recently, this type of PLLs has been successfully incorporated into a larger synthesizable system such as processors [1], [2] and a wireless transceiver [3].

Early synthesizable PLLs are based on time-to-digital converters (TDCs) that suffer from large quantization noise [4]–[7]. Although fine resolution and more linear TDCs were proposed in [8]–[10], the performance improvement is still limited. To further reduce phase noise, integer-N synthesizable PLLs using injection locking and multiplying-delay-locked loops (MDLLs) were proposed [11]–[14]. This type of technique is useful not only to avoid the noise from a TDC but also to suppress the one from a digitally controlled oscillator (DCO), which is typically implemented in a synthesizable PLL. Nevertheless, similar to those custom-designed injection-lock PLLs and MDLLs, high-performance fractional-N operation is challenging to realize. In [15], multistage soft injection was proposed, but the frequency resolution is limited. A more effective way can be using a digital-to-time converter (DTC) to align the phase of the injecting reference clock [16]–[20]. Although a DTC basically features finer resolution than a TDC, the automatic P&R introduces unpredictable parasitic elements that worsen the jitter and linearity compared with a custom-designed one. Still, the phase noise and spurs of the PLL can be degraded.

To tackle this issue, recently, the essential idea is to reduce the range of the variable-slope DTC in a fractional-N PLL. In [16], [18], and [20], a segmented coarse-to-fine DTC was proposed, where the 8-bit variable-slope fine DTC is relatively linear. Its smaller area results in less parasitic elements as well. To cover the required one period of the DCO's output for fractional-N operation, a 6-bit coarse DTC is incorporated. In this way, the gain matching between the coarse and fine DTCs is so critical that complicated calibrations are necessary. In [17] and [19], the coarse DTC is a DCO replica, and the fine one is an interpolator. This combination relaxes the gain calibration but is still susceptible to the mismatches not only in the replica and but also in the interpolator. Thus, fractional and reference spurs can be undermined. The power consumption

Fig. 1. Concept of multistage injection and required DTC range.

Fig. 2. Timing diagram without and with DCO's stage mismatches.

is also a concern in the case when a wider interpolation range is required.

In this work, a DTC-based multistage injection architecture is proposed and demonstrated with a three-stage-injection fractional-N synthesizable PLL [21]. Instead of coarse-to-fine segmentation, only a fine DTC is needed and the multiphase information of the DCO is extensively utilized for phase tracking, window generation, and injection. Directly injecting at DCO's multiple stages leads to more compact architecture and more straightforward matching requirement. With a first-order $\Delta\Sigma$ modulator and three-stage injection, the required DTC range is only 1/3 period of the DCO's output. Thus, higher linearity, lower jitter, lower power consumption, and smaller area are expected, compared with a full range one. Also, since there is no coarse segmentation, no jitter is accumulated through that path. Nevertheless, the mismatches among DCO stages ought to be calibrated, similar to those custom-designed DTC-range-reduced PLLs where mismatched duty cycles are addressed [22]–[25]. In this work, the issue is solved with the proposed dithering-assisted local skew calibration.

II. PROPOSED SOLUTION

A. DTC-Based Multistage Injection

The concept of the proposed synthesizable PLL is shown in Fig. 1. In this work, a three-stage DCO is implemented as illustrated. A window signal win[n] enables the injection to a certain stage. The PLL for phase tracking harnesses a first-order $\Delta\Sigma$ modulator for fractional-N operation. Thus, conventionally, the required DTC range should be one period (T_v) of the DCO's output. Besides injection, if three phases of the DCO are utilized for fractional-N operation, the DTC only needs to cover $T_v/3$ due to the phase folding back shown in Fig. 1. Hence, the performance of the single DTC can be improved, as compared in Section III-B. The type-II digital PLL, comparing the phase difference directly between DTC's output (F_{dtc}) and a DCO stage signal ($F_v[n]$), removes the phase difference to ideally realize zero-offset injection. Increasing the number of stages further reduces the required DTC range but increases the power consumption of the DCO as well for the same output frequency. The mismatches among stages need to be calibrated as well, which will be described in Section II-B. Thus, the number of stages should be determined considering the process technology and the specifications of output frequency and DTC resolution. With 65-nm CMOS technology in this work, for about 1-GHz output frequency and sub-ps DTC resolution, the number of stages of this work is decided to be three.
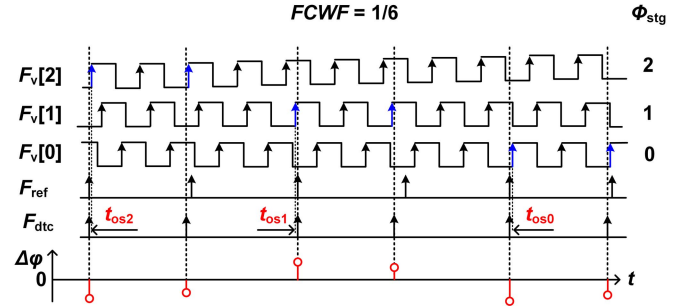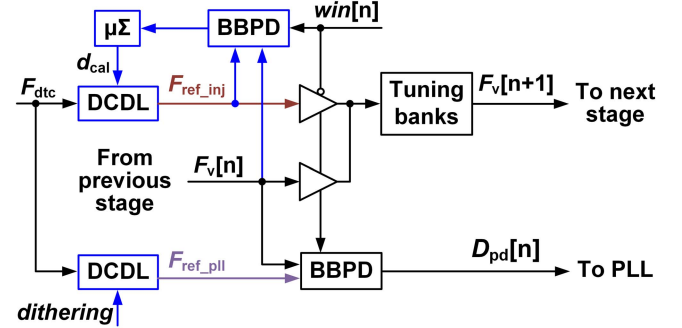

Fig. 3. Proposed dithering-assisted local skew calibration at each DCO stage.

The timing diagram of the fractional-N operation is shown in Fig. 2, where the fractional frequency control word (FCWF) is 1/6. When the loop is locked, the phase difference between the reference clocks (F_{ref}) and $F_v[n]$ increments cyclically, whereas the DTC correspondingly aligns F_{dtc} to the currently focused $F_v[n]$, canceling out the phase difference. The rotating phase signal (Φ_{stg}) indicates (or switches) the currently focused stage for phase comparison and injection. Hence, the loop can be operated in this way as a fractional-N PLL or $F_v[n]$ can be replaced by F_{dtc} periodically in the injection mode for lower phase noise. However, the circuit nonidealities, dominated by the mismatches among the DCO's stages, introduce skews between F_{dtc} and $F_v[n]$. As shown in the figure, large phase errors occur when the focused stage is switched to the next one. Then, the PLL tries to eliminate the phase errors, leading to more periodic patterns, which further causes high spurs.

B. Dithering-Assisted Local Skew Calibration

The skews due to DCO's stage mismatches necessitate calibration. Since the loop finally operates in the injection mode, the skew at the injection path in each stage is calibrated locally, as shown in Fig. 3. Once a stage is focused, win[n] enables the bang-bang phase detector (BBPD) to compare the timing offset. The result is integrated by the digital accumulator tuning the digitally controlled delay line (DCDL) to remove the skew. The DCDL has fine resolution and low jitter, and the BBPD is designed with large logic gates for small transistor mismatches. The details are described in Section III-D.

For the PLL side, the same DCDL and BBPD are added in each stage for similar time offset and phase comparison, respectively, as shown in Fig. 3. The loop first operates in the PLL mode to align $F_v[n]$ to F_{ref_pll}. Then, the skew calibration

Fig. 4. Proposed architecture.

removes the phase offsets between F_{ref_inj} and $F_v[n]$. During the calibration, $F_v[n]$ is still locked to F_{ref_pll} by the PLL. It should be noted that one BBPD in each stage for both skew calibration and phase tracking is also a possible option. In this case, the BBPD should be multiplexed in the time domain to avoid the conflict between the calibration loop and phase tracking loop (PLL side). This leads to lower effective reference frequency and longer skew calibration time. It should also be noted that one BBPD for all three stages is also a possible option. However, the resulting longer routes and the multiplexer before the BBPD tend to worsen the mismatch issue. Hence, in this work, two BBPDs in each stage are employed, resulting in more regular design hierarchy for implementation as well.

The paths among the three stages in the PLL side, however, still suffer from mismatches due to automatic P&R and transistor nonidealities. Consequently, periodic patterns are generated at the PLL side, and the spurs are degraded. Moreover, the calibrations of DTC gain and injection skew can be undermined due to non-white phase difference seen before the BBPDs.

To solve this issue, the DCDL is uniformly dithered, as shown in Fig. 3. The dithering power depends on the full-scale range of the DCDL. Since the dithered DCDL is as same as the calibrating one to keep a similar time offset, its range is determined by the requirement of covering the DCO stage mismatches (that will be shown later in Fig. 9). Compared with the effort of one more delicate calibration, randomization is a simpler way of reducing spurs caused by the PLL side. Thankfully, most dithering noise can be suppressed by the injection locking and the PLL, which is explained in Section II-C. Since the calibration loop is basically an integrator, if its input $F_v[n]$ contains periodic patterns, the calibration output can slowly fluctuate depending on the periodicity and power. Thus, by "whitening" $F_v[n]$, the dithering also helps the settling of the calibration.

C. Proposed Architecture and Noise Analysis

The proposed architecture of the fractional-N synthesizable PLL is shown in Fig. 4. The BBPDs for the PLL are

Fig. 5. Phase noise analysis model.

activated in turn by win[n], which is generated by the window generation logic. The activated one sends the result to the counter-based digital PLL for phase tracking. The digital loop filter contains proportional and integral paths in the PLL mode, while only the integral path is enabled in the injection mode. Three DCDLs before the BBPDs in the PLL are dithered by a uniform pseudo random number generator (PRNG) [26]. As previously mentioned, since three phases of the DCO are used for fractional-N operation, an 8-bit DTC is sufficient to cover $T_v/3$. The loop first operates in the coarse and fine tune modes for frequency acquisition and phase alignment, followed by the settling of the local skew calibration and the least-mean-square-based (LMS-based) DTC gain calibration. The two calibrations benefit from the dithering by seeing less periodic jitter at $F_v[n]$ for steady convergence. In the injection mode, the local skew calibration is turned off because the slowly changed calibration data can result in increased low-frequency phase noise, while the dithering is still activated to reduce the spurs from the PLL side.

As previously mentioned, the dithering signal does contribute quantization noise to the loop, but the effect is negligible due to the phase refreshing by injection locking. The noise model following [14] of the synthesizable PLL is shown in Fig. 5, where θ_{n_in}, θ_{n_dit}, and θ_{n_dco} represent the total noise of the reference clock, DTC, and DCDL; the quantization noise of the dithering; and the total noise of quantization and phase of the DCO, respectively. All the signals in this model are normalized to the phase of the DCO, i.e. $2\pi/T_v$. Thus, gain N is placed right after the input reference phase (Φ_{ref}), and the feedback gain from DCO to the input is 1. The transfer
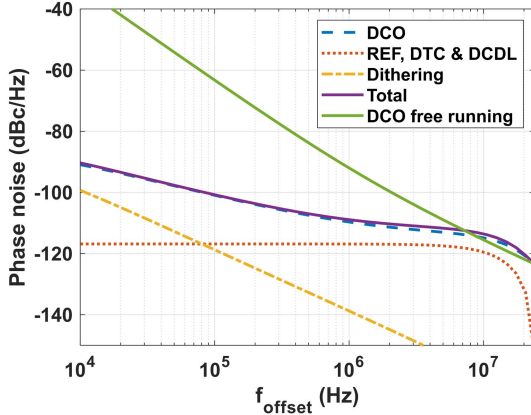
Fig. 6.   Phase noise analysis result.

function

$$H_{rp}(s) = 1 - e^{-s/(2f_{ref})} \cdot \text{sinc}(\pi f/f_{ref}) \qquad (1)$$

represents the injection effect of phase replacement. Intuitively, the differentiation-like transfer function filters out most noise from the DCO and results in a narrow bandwidth together with the feedback to suppress the dithering noise. The transfer function

$$H_{inj}(s) = e^{-s/(2f_{ref})} \cdot \text{sinc}(\pi f/f_{ref}) \qquad (2)$$

models the noise from the injection path to the output, where gain N is not placed due to the normalization to the DCO's phase. Since the DCO's gain (K_{dco}) can be normalized in the digital domain by f_{ref}/K_{dco}, it is not shown in the model but is counted in for the quantization noise in θ_{n_dco}. Since the uniform dithering of the BBPD implies a well-defined gain (K_{pd}) that can be normalized as well, K_{pd} in this model is $1/2\pi$ for simplicity. β is the gain of the digital integral path. The uniform dithering noise is modeled as

$$\theta_{n_{dit}} = \frac{2\pi}{T_v} \cdot \sqrt{\frac{T_{dit_{fs}}^2}{12}} \qquad (3)$$

where T_{dit_fs} is the full scale of the DCDL.

For calculation, 24-MHz reference frequency and 1.04-GHz output frequency are assumed. β is chosen as 2^{-9}. The DCDL is with 6 bits and 56-ps full-scale range obtained from the post-layout simulation. The values are designed to cover the stage mismatches of the DCO (shown later in Fig. 11) while keeping sufficiently high calibration resolution. The noise data are obtained from the post-layout simulation as well. The calculated phase noise and the noise contributions are shown in Fig. 6. It can be seen from the figure that the dithering noise contribution is largely suppressed due to the injection locking and small β. Another way of further reducing the dithering noise is digital or time-domain cancellation [27]–[31]. These approaches, requiring either a wide-range higher resolution TDC or an auxiliary DTC, may not suit this synthesizable implementation. The integrated root-mean-square (rms) jitter from 10 kHz to 10 MHz is 1.1 ps, which is an optimistic estimation because spur effect, coupled power supply noise, and flicker noises of the reference clock and DTC are not involved.
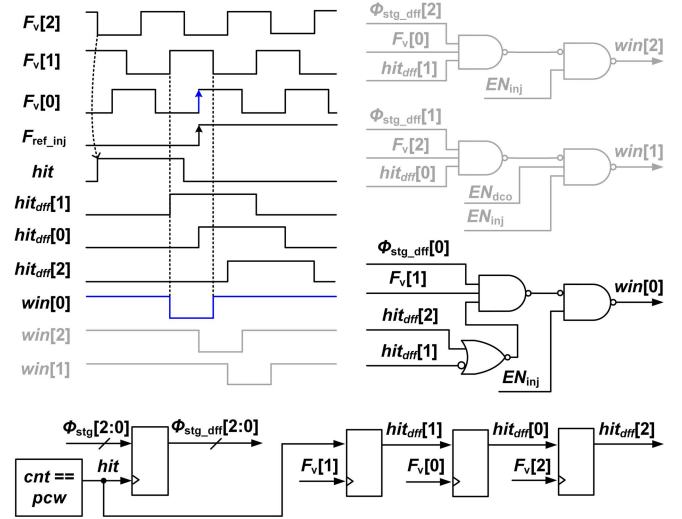
Fig. 7.   Synchronous window generation utilizing DCO's multiple phases.
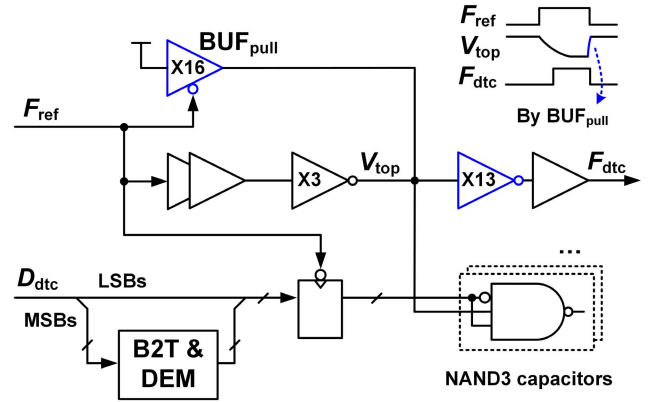
Fig. 8.   Circuit topology of DTC.

III. CIRCUIT DESIGN

A. Window Generation

A synchronous approach for window generation utilizing DCO's multiple phases is proposed, as shown in Fig. 7, where the logic and timing for win[0] generation are highlighted. When the counter's output equals the expected digital phase (pcw), a signal (hit) is generated and re-latched (hit_{dff}) by F_v. Then, Φ_{stg_dff} (latched from Φ_{stg}), F_v, and hit_{dff} are utilized to generate the injection windows through combinational logic. As shown in the timing diagram, the start of win[n] is synchronized, and its pulsewidth is guaranteed by the PLL. Compared with the conventional methods using process–voltage–temperature (PVT) sensitive delay-cell-based gating or asynchronously reset D flip-flops (DFFs) [32], the proposed approach can be more suitable to synthesizable implementation.

B. Digital-to-Time Converter

The single-stage 8-bit variable-slope DTC is shown in Fig. 8, where the variable capacitors are realized using NAND3 gates [12]. For better matching and less voltage ripple when switching MSBs, the capacitor array is implemented
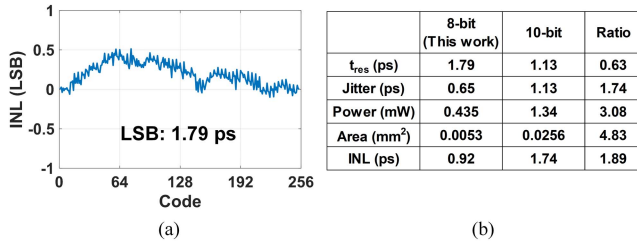
Fig. 9. Post-layout simulation results. (a) INL of 8-bit DTC. (b) Normalized performance comparison between 8- and 10-bit DTCs.

with 63-bit thermometer MSBs connected with dynamic element matching (DEM) and 2-bit binary LSBs. The falling of V_{top} is typically slow due to the parasitic capacitance, as expected, but its rising becomes slow as well. This issue limits possible operation frequency and can lead to uncertain initial voltage of V_{top} before the next falling. While in a custom design, it is simply overcome by enlarging the PMOS transistors, for this all-standard-cell solution, a tri-state pull-up buffer (BUF$_{pull}$) is added for the fast rising of V_{top}. A relatively large size of BUF$_{pull}$ is chosen not only to accelerate the rising but also to provide a low-impedance path to suppress the potential voltage ripple when switching large capacitance.

The inverter following V_{top} is also relatively sized large to reduce the jitter caused by the slow falling of V_{top}. The simulated rms jitter of the 8-bit full range with layout parasitic extraction (LPE) is about 0.66 ps. During its automatic P&R, V_{top} is routed in the top metal layer as much as possible, which is handled by the script. This layer, featuring small resistance, is dedicated for V_{top} routing. Thus, the parasitic resistance in between NAND3 capacitors and V_{top} can be reduced. Fig. 9(a) shows the simulated INL of the DTC with LPE. The nominal resolution (LSB) is 1.79 ps, and the INL is about 0.5 LSB. The rms jitter of full range is 0.66 ps. The performance is compared with a 10-bit one, as shown in Fig. 9(b). Except for the time resolution and range, the 8-bit DTC suggests better performance because the resulting smaller area contributes less parasitic elements, which is consistent with the motivation of this work. Thanks to the automatic P&R, the porting to the 10-bit one takes only about 1.5 h.

C. Tuning Bank of DCO

The topology of one stage of the DCO is shown in Fig. 3. In this section, the circuits of the tuning banks are described, as shown in Fig. 10(a). The tuning banks contain a 6-bit coarse-tune bank (D_{coarse}), an 8-bit fine-tune bank (D_{fine}), and 6-bit $\Delta\Sigma$-modulated resolution enhancing bank (D_{dsm}).

Although NAND3 capacitors are also employed in the DCO, the upper node is always connected to the ground, differently from the DTC and the DCDL. As shown in Fig. 11(b), the conventional connection has an issue of switching current (Δi) and one more variable capacitor (C_p). During the switching, Δi leads to not only short-circuit current but also unwanted charges through C_p to $F_v[n]$, potentially leading to more disturbance at $F_v[n]$. Also, the existence of C_p slightly increases the range of the variable capacitance, limiting
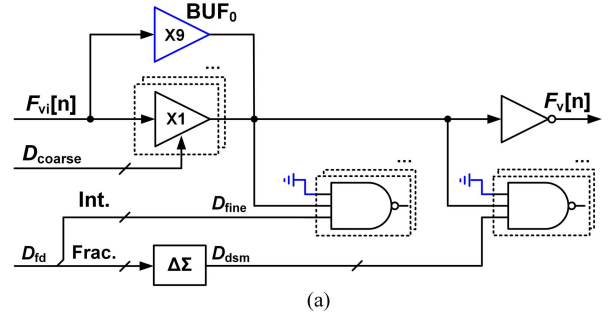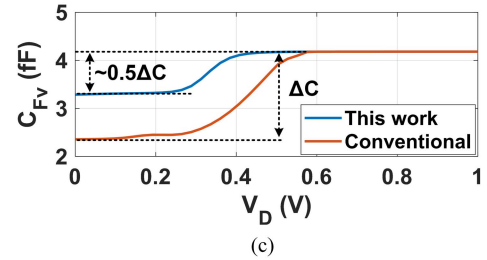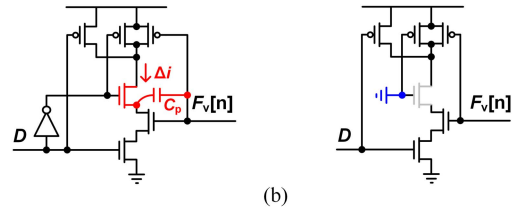

Fig. 10. (a) Circuit topology of DCO tuning banks. (b) Comparison between NAND3 capacitors of DTC/DCDL and DCO. (c) Improvement of variable capacitance in DCO.
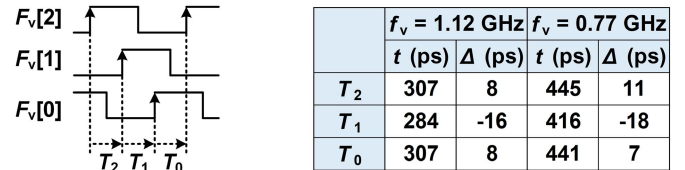

Fig. 11. Simulated DCO's stage mismatches with LPE in terms of lag time.

the frequency resolution. An alternative connection is found in [12] where the lower transistor is cut off to avoid switching current, but variable C_p and charge injection still exist. In this work, the upper NMOS is always cut off, resulting in no Δi or variable C_p. Fig. 11(c) shows the simulated capacitances of the two cases, suggesting about twice improvement of the minimum variable capacitance. Since the finer resolution can reduce the fine-tune range, adjacent fine-tune curves may not well overlap with each other. An overriding buffer (BUF$_0$) can alleviate this issue with a proper gate size at the cost of reduced coarse-tune range.

The DCO is automatically placed and routed without specific position or wiring controls, which means that each stage can have randomly different delays. Fig. 11 shows the simulated stage mismatches in terms of lag time because this information is more meaningful to the skew calibration. According to the results, the difference from the mean value
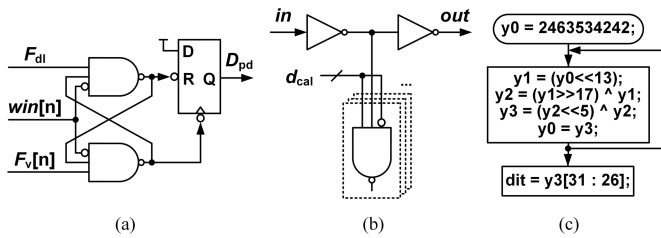
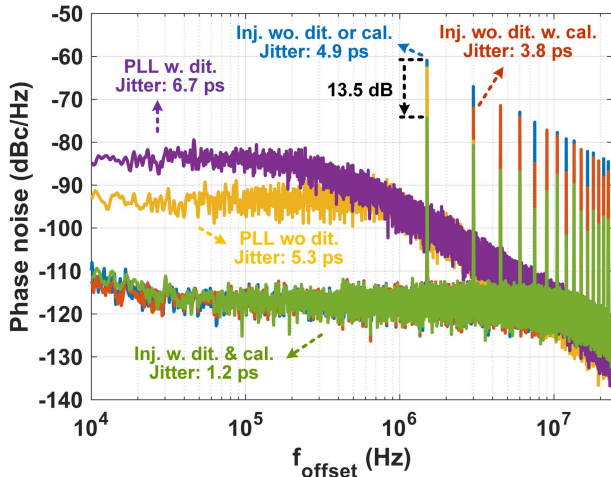Fig. 12. Circuit topology of (a) BBPD and (b) DCDL. (c) Algorithm of uniform dithering.

Fig. 13. Behaviorally simulated phase noises.

of T_0, T_1, and T_2 can be as large as -18 ps. Thus, the range of the DCDL should cover this value.

D. Other Building Blocks

A zero-offset aperture BBPD is implemented, as shown in Fig. 12(a). A slight difference from [33] and [34] is that win[n] is connected to the RS latch for phase selection. Large NAND3 gates are chosen for smaller transistor mismatch. The Monte Carlo simulation result suggests about 0.6-ps mismatch (1σ), which is negligible, compared with the skews introduced by P&R. The DCDL topology with 6 bits is shown in Fig. 12(b). The LPE simulation result in about ± 28-ps variable range and 0.13-ps rms jitter. The range is sufficient to cover the aforementioned stage mismatches of the DCO, and the introduced jitter is less dominant. The algorithm of the uniform PRNG is shown in Fig. 12(c) [26]. Six MSBs of the 32-bit output are extracted as the dithering signal.

E. Behavioral Simulation Results

A behavioral model of the proposed PLL was created using VerilogHDL, where the jitters and mismatches are obtained from the DTC's and DCO's LPE simulation results and described using real numbers available in VerilogHDL.

Fig. 13 shows behaviorally simulated phase noises. In the PLL mode without dithering, high phase noise and high spurs can be observed, while with dithering, the phase noise

becomes even higher, but the spur level decreases due to narrower loop bandwidth and the dithering. The integrated rms jitters from 10 kHz to 10 MHz in the two cases are 5.3 and 6.7 ps. In the injection mode without calibration or dithering, the highest spurs are observed although the noise floor is significantly reduced. Applying the calibration but without dithering, the spur reduction effect is limited. With the calibration and dithering, the lowest spurs can be achieved without contaminating the noise floor, suggesting the effectiveness of the proposed solution. The integrated rms jitters are 4.9, 3.8, and 1.2 ps. The behavioral simulation suggests a 13.5-dB improvement of the fundamental spur (-35.1 to -48.6 dBc). It should be noted that no $1/f$ or $1/f^3$ noises are involved in this time-domain behavioral model because the main purpose of the simulation is to check the spur reduction effect. Thus, the noise floor at lower frequencies is flat, and the integrated rms jitters are optimistic estimations. Nevertheless, the PLL locks to the frequency close to the one used in the noise analysis, and at this frequency, the free-running DCO's phase noise at 1-MHz offset is made equal to the LPE simulated result. Hence, from Fig. 13, it is observed that the noise floor level between 1 and 10 MHz is close to that of the analysis result shown in Fig. 6.

Fig. 14 shows a behavioral simulation result of startup sequence. The settling time of LMS gain calibration and skew calibration is about 280 and 660 μs, respectively. The settling time of calibration is determined by the reference frequency and attenuation factor (μ in Fig. 3) in the loop.

IV. EXPERIMENTAL RESULTS

The prototype chips are fabricated in 65-nm CMOS. Fig. 15 shows the chip micrograph and the power breakdown. The core area is 0.075 mm². With 0.85-V power supply for the DCO and 1.0 V for the rest, the total power consumption is 3.36 mW at 1.0095-GHz output frequency and 24-MHz reference frequency. The measured tunable output frequency ranges from 0.79 to 1.16 GHz.

Fig. 16 shows the measured phase noises in the fractional-N mode (FCWF $= 2^{-4}$) with and without the dithering-assisted local skew calibration. As shown in Fig. 16(a), without the proposed solution, high spurs at higher frequencies are observed, and the integrated rms jitter from 10 kHz to 10 MHz is 6.40 ps, which are mainly due to the spurs at higher frequencies. The in-band phase noise at 100 kHz is -103 dBc/Hz. In contrast, as shown in Fig. 16(b), with the proposed solution, the measured integrated rms jitter is reduced to 2.55 ps, and most spurs diminish, at a slight but acceptable cost of the increased in-band phase noise by 1 dB.

Fig. 17 shows the measured fractional and reference spur reduction effects. The result suggests a 15-dB decrease of fundamental fractional spur when applying the proposed solution, as shown in Fig. 17(a). The reference spur improved from -39 to -42 dBc, as shown in Fig. 17(b). In this design, the reference spur is also related to the DCO's fine-tune frequency resolution that is 117 kHz. Although quantization noise is suppressed by the DSM bank, the fine bank is still updated at 24 MHz, which theoretically leads to a reference spur of
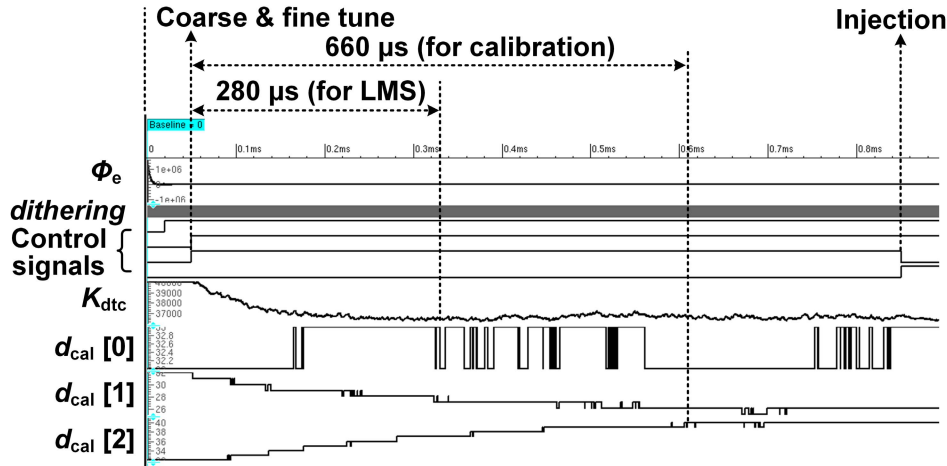
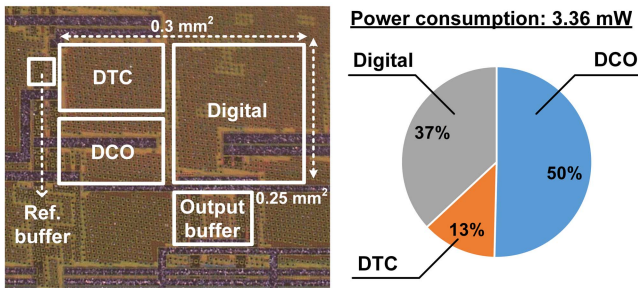Fig. 14. Behavioral simulation result of startup sequence.

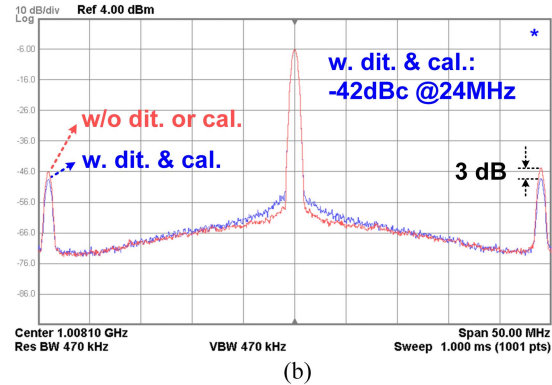Fig. 15. Chip micrograph and power breakdown.

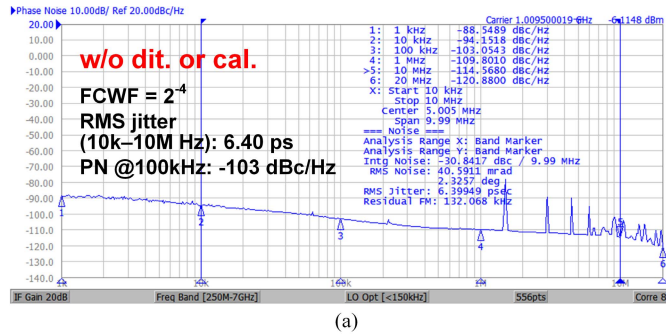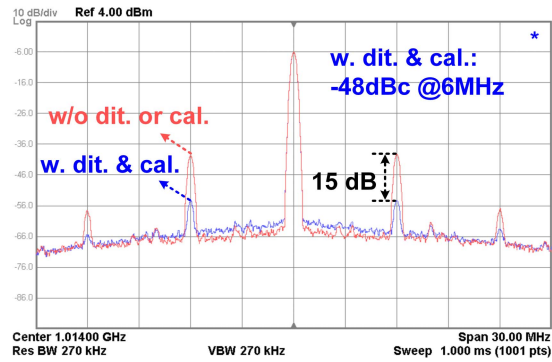Fig. 16. Measured phase noises (a) without dithering or calibration and (b) with dithering and calibration.

Fig. 17. Measured improvements of (a) fractional spurs (when FCWF = 2^{-2}) and (b) reference spurs (when FCWF = 2^{-8}).

Fig. 18. Measured fundamental fractional spurs and rms jitters with different FCWFs.

−46 dBc calculated with $20\log_{10}(K_{\mathrm{dco}}T_{\mathrm{ref}})$ [19], consistent with the measurement result. In contrast, considering 0.9-ps DCDL's resolution, the theoretical resulting reference spur is −61 dBc, calculated with $20\log_{10}(t_{\mathrm{cal,res}}T_{\mathrm{ref}}N)$ [19]. A reason
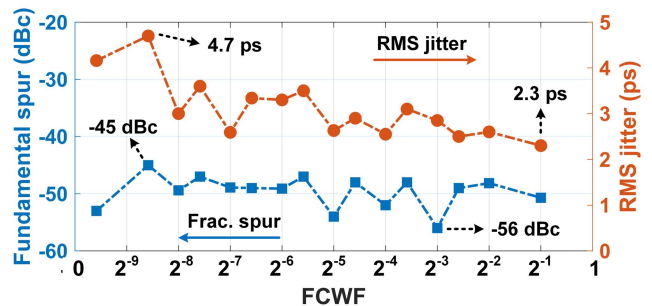
TABLE I

PERFORMANCE COMPARISON WITH STATE OF THE ARTS OF SYNTHESIZABLE AND POTENTIALLY SYNTHESIZABLE FRACTIONAL-N PLLS

	This Work	Lee JSSC'19 [10]	Kundu JSSC'21 [19]	Liu TCAS-I'21 [20]	Zhang JSSC'22 [31]	Deng ISSCC'15 [15]	Liu SSC-L'20 [17]	Kundu ISSCC'16 [33]
CMOS (nm)	65	28	22	65	65	65	5	65
Synthesizable	Yes	Partially	Yes (w. custom-layout cells)	Yes	No	Yes	Yes	No
Architecture	DTC + MDLL w. multi-stage inj.	Speculative- TDC + PLL	DCO-replica- DTC + MDLL	Segmented- DTC + MDLL	DTC + MDLL	Soft inj. PLL	DTC + MDLL	MDLL w. multi-stage inj.
Required DTC range (T_{dco})	1/3	NA	1	1	1	NA	1	NA
f_{out} (GHz)	1.0095	2.056	3.6175	1.0008	1.5008	1.5222	1.0	1.4175
RMS jitter (ps) Int. range (Hz)	2.55 10k - 10M	2.13 10k - 100M	2.74 10k - 100M	0.64**** 10k - 40M	1.69 10k - 10M	3.6 1k - 100M	1.90 10k - 10M	2.80 10k - 10M
Reference spur (dBc)	-42	-52	-60	-64.5	-43	NA	-30.9	-47
Worst frac. spur (dBc)	-45	-24****	-47	-59.6	-52	NA	-44.3	-45
Power (mW)	3.36	6.95	3.19	1.85	11.95	3.00	0.95	8.00
Area (mm^2)	0.075	0.0043	0.0052	0.126	0.18	0.048	0.0036	0.054
f_{ref} (MHz)	24	80	80	100	50	380	100	87.5
Freq. resolution (kHz)*	31.25	2500	125	6.10	781.3	NA	6.10	17500
FoM (dB)**	-226.6	-225.0	-226.3	-241.2	-224.8	-224.2	-234.7	-222.0
FoM$_{ref}$ (dB)***	-232.8	-226.0	-227.3	-241.2	-227.8	-218.4	-234.7	-222.6

* Frequency resolution = f_{ref} / (equivalent DTC/TDC total steps)
** FoM = $10 \times \log_{10}[(\text{jitter/1s})^2 \times (\text{power/1mW})]$ *** FoM$_{ref}$ = FoM + $10\log_{10}(f_{ref}/100\text{MHz})$
**** Read from the corresponding figure

for the less fine frequency resolution is due to the non-minimum size of the selected cells to cover the required tuning range of the fine bank. Although it is less flexible to tweak variable capacitance with limited choices of standard cells, the frequency resolution can still be improved by selecting smaller size gates and adding one more medium bank as done in [20]. Also, the noise coupled from power supply is susceptible to the reference spur as well because no low dropout regulators are employed for this work. The increase of noise floor shown in the figure may also be due to the coupling from the power supply because the dithered DCDLs share the same power supply with the DCO. When dithering is operating, the DCO's phase noise can be degraded. Fig. 18 shows the measured fractional spurs and integrated rms jitters with different FCWFs. The fundamental fractional spurs range from −56 to −45 dBc, while the integrated rms jitters range from 2.3 to 4.7 ps.

Table I shows a performance comparison with the state-of-the-art synthesizable or custom-designed injection-lock PLLs/MDLLs. Unlike other works, this work needs only a fine DTC that covers $T_v/3$. Compared with the two 65-nm DTC-based PLLs [20], [31], the core area of this work is smaller. Work [20] is a remarkable work featuring the lowest jitter and spur and best figure of merit (FoM). Compared with [20], this work provides another perspective that only a short-range fine DTC is possible for the fractional-N operation without complex calibrations. Also, for the applications where multiple phases of the oscillator are needed, the proposed techniques in this work can be utilized, while the DCO in [20] is understood as "one stage." Finally, with the lowest reference frequency, this work still achieves comparable rms jitter and competitive frequency resolution. After normalizing the reference frequencies to 100 MHz [35], the resulting −232.8-dB FoM$_{ref}$ of this work is also competitive.

V. CONCLUSION

A DTC is one of the most critical building blocks in a fractional-N synthesizable injection-lock PLL/MDLL. In this work, multistage injection with dithering-assisted local skew calibration is proposed to reduce the required DTC range for improved performance and to solve the issues of the mismatches in the DCO and the PLL, with most of the dithering noise being suppressed. Measured at 1.0095 GHz with 24-MHz reference frequency, a prototype chip has suggested an rms jitter improvement from 6.40 to 2.55 ps and a fractional spur improvement by about 15 dB. With 3.36-mW power consumption, the translated FoM and FoM$_{ref}$ are −226.6 and −232.8 dB, respectively.

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Zule Xu (Member, IEEE) received the B.E. degree in electrical engineering from the Dalian University of Technology, Dalian, China, in 2006, the M.E. degree in electrical communication engineering from Tohoku University, Sendai, Japan, in 2011, and the Ph.D. degree in physical electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2015.

From 2015 to 2016, he was a Researcher with the Tokyo Institute of Technology. From 2016 to 2018, he was with the Tokyo University of Science, Tokyo, as an Assistant Professor. From 2018 to 2022, he was with The University of Tokyo, Tokyo, as an Assistant Professor/Research-Intensive Lecturer. Since 2022, he has been with IMEC, Eindhoven, The Netherlands, as a Researcher. His research interests include data converters, phase-locked loops (PLLs), oscillators, and their design automation.

Dr. Xu is a member of the Institute of Electronics, Information and Communication Engineers (IEICE). He is also serving as a Technical Program Committee Member of IEEE A-SSCC and an Associate Editor of *IEICE Transactions*. He was a recipient of the NEWCAS Best Student Paper Award in 2013, the CICC Student Scholarship Award in 2013, and the Yasujiro Niwa Outstanding Paper Award in 2017.