An Ultrasound ASIC With Universal Energy Recycling for >7-m All-Weather Metamorphic Robotic Vision

Han Wu, *Student Member, IEEE*, Miaolin Zhang, *Student Member, IEEE*, Zhichun Shao, Jiaqi Guo, *Student Member, IEEE*, Kian Ann Ng, *Senior Member, IEEE*, Liwei Lin, *Member, IEEE*, and Jerald Yoo, *Senior Member, IEEE*

***Abstract*— An ultrasound ASIC that enables compact, 3-D nonvisual robotic navigation for >7-m is presented. The proposed ultrasound ASIC mitigates the limitations of camera vision navigation systems in all-weather, low-power, low-cost aspects. The ASIC integrates TX and RX paths for 64 channels, enabling four-directional navigation using 4 × 4 ultrasound arrays. The proposed universal energy recycling transmitter (UERTX) driver circuit, which can drive both single-ended and differential transducers, reduces energy consumption by 44% compared with non-overlap switching-assisted conventional class-D ultrasonic drivers, addressing large TX power consumption. In addition, the on-chip programmable power management unit (PMU) eliminates off-chip supplies and reduces off-chip passive components for compact system miniaturization. Furthermore, PMU enables the tuning of TX driving amplitude for the range of 6–14 V_{pp} allowing wide detection range adaptability. Fabricated in 0.18 μm 1P6M standard CMOS, the ASIC system measures 25 mm^2 and has >7-m obstacle detection capability while consuming 4.3 mW/channel. The proposed ultrasound ASIC system is demonstrated with a four fps, 3-D navigating metamorphic robot, which consumes 0.28 W, occupies 125 cm^3, and weighs ≤100 g.**

***Index Terms*— All-weather, energy recycling, low-power, machine vision, real-time, small form factor, ultrasound.**

I. Introduction

METAMORPHIC robot is a new type of small form factor robot that can change its shape to execute particular tasks, such as pipeline inspection, cave rescue, geological surveys, and building inspections. As its moving speed is slow, a high frame rate is unnecessary, but as it operates in a challenging environment, it must be robust against low-light conditions. For example, a commercial metamorphic robot (Daran Robotics, MW-74Pi) weighs 2 kg with a maximum load capacity of 2 kg, and the form factor is 37 × 25 × 8 cm^3. Therefore, the 3-D vision system mounting on the metamorphic robot should be low power (<1 W), small form factor (∼cm^3), and lightweight (∼0.1 kg). Machine vision is commonly realized using optical means [1], IR, radar, or LIDAR. The visual and IR cameras have high image resolution but require high compute capability and high power consumption to process massive raw image data (>1 GB/s [2]) [3]. Most importantly, visual camera systems cannot work under low-light situations and lack object depth information. IR cameras can work in low-light conditions, but their resolution is dependent on object temperature variations. Radar [4] and LIDAR [5] have a long detection range; however, they consume several watts of power, making them unsuitable for power-constrained applications. In contrast, ultrasound does not suffer from the aforementioned constraints, making it an ideal fit for power-constrained all-weather 3-D vision applications. Therefore, this article presents an ultrasound ASIC system for the all-weather metamorphic robotic 3-D vision that fulfills low power (sub-watt), low cost, small form factor (∼cm^3), and lightweight (≤100 g) (see Fig. 1). Four arrays facing each direction are connected with the ASIC and mounted on the metamorphic robot. For each direction, the ASIC produces bursts of pulses via the center four transducers,

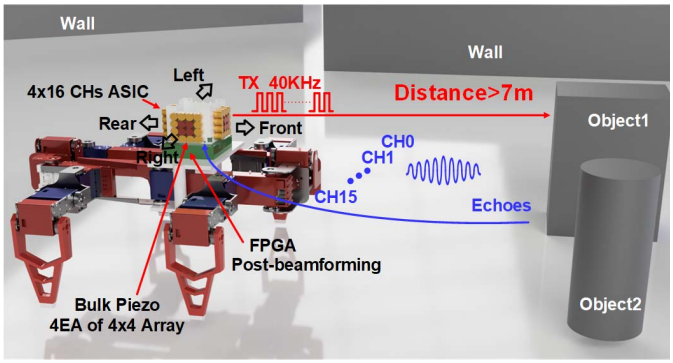


Fig. 1. Ultrasound ASIC for metamorphic robotic vision.

Manuscript received 17 January 2022; revised 19 March 2022 and 7 May 2022; accepted 28 May 2022. Date of publication 4 July 2022; date of current version 26 September 2022. This article was approved by Associate Editor Woogeun Rhee. This work was supported in part by the A*STAR AME Nanosystems through the Edge Program under Grant A18A4b0055 and in part by A*STAR AME Wavefront Computing Program under Grant A18A4b0055. *(Corresponding author: Jerald Yoo.)*

Han Wu and Jiaqi Guo are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117583.

Miaolin Zhang was with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117583. He is now with Huawei Technologies, Chengdu 611730, China.

Zhichun Shao and Liwei Lin are with the Department of Mechanical Engineering, University of California at Berkeley, Berkeley, CA 94720 USA.

Kian Ann Ng is with the Digipen Institute of Technology, Singapore 139660.

Jerald Yoo is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117583, and also with the N.1 Institute for Health, Singapore 117456 (e-mail: jyoo@nus.edu.sg).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3182102.

Digital Object Identifier 10.1109/JSSC.2022.3182102

and then all 16 channels receive the echoes, which the on-chip ADC then digitizes. The raw data are processed by the post-beamforming algorithm [6], [7] implemented on FPGA to generate 3-D visual images.

There are several ultrasound ASICs that target biomedical diagnosis applications [8]–[10], but 3-D space perception has not gained much research attention. The one-channel ultrasound ASIC [11] pioneered range finder application, but its detection is limited to one object in a 1-D space. Nine channels (two TX + seven RX) were developed, which achieved gesture recognition within a range of 1-m [12]. In [13], the 4 × 4 piezoelectric micromachined ultrasonic transducers, namely, PMUT, were used for a 1.5-m range 3-D space perception. The array has a small factor of only 6 × 6 mm^2, but the measurement was tethered to an oscilloscope for channel data acquisition and is therefore not portable. Moreover, the data are post-processed offline on a PC for image reconstruction and cannot accomplish real-time data acquisition and processing.

To address all issues mentioned above, the proposed ASIC accomplishes a 3-D space perception with object detection >7-m. The 64-channel ASIC integrates an energy-efficient ultrasound interface with a high-voltage (HV) transmitter, an on-chip power management unit (PMU), and receiver chains [14]. Using the ultrasound ASIC system for 3-D vision has a drawback: the spatial resolution is not as good as the camera sensor. It cannot reconstruct the object's contours because the sound wavefront usually is not perpendicular to the objects' edges. The spatial resolution depends on the ultrasound array size, pitch size of the transducers, and resonant frequency of the transducer. The beam pattern equation from the ultrasound theory derives the spatial resolution [15]. For the 4 × 4 transducer array (pitch size 1 cm with 40-kHz resonant frequency) at a 1-m distance, the spatial resolution is around 20 cm. If it detects objects located at a longer distance, the spatial resolution will worsen. However, as a typical metamorphic robot moves slowly (∼0.1 m/s), it does not require high-quality spatial resolution for its navigation. Rough objects' 3-D space location can help it plan the route for navigation. As it is highly power-constraint, a low-power (<1 W) 3-D vision system is much needed; therefore, the proposed ASIC trades off the low power and low cost with the spatial resolution. In addition, the pulse-to-echo scheme is a single, broad-beam transmission using the four central elements, followed by parallel receivers on all the elements, on which parallel RX beamforming is applied.

The rest of this article is organized as follows. Section II introduces the proposed ultrasound ASIC 3-D vision system architecture, transducer characterization, and design considerations. Section III describes the building blocks for ASIC. Section IV discusses the measurement results, and Section V concludes the work.

II. Machine Vision Ultrasound ASIC System Overview

A. System Architecture

Fig. 2 shows our proposed ultrasound ASIC-based system architecture for 3-D machine vision. It consists of the proposed ASIC, 64-channel bulk piezo transducers, FPGA, and mobile phone for real-time 3-D image display. Fog, snow, and rain do not affect sound waves significantly, giving ultrasound-based navigation an attractive means to address different weather conditions [16]. Although this comes at a lower spatial resolution compared with camera vision, this is not a big issue for metamorphic robot navigation purposes. The 64-channel interface (TX and RX) provides a low-cost solution to cater to a wide range of commercial ultrasound transducers. The proposed universal energy recycling transmitter (UERTX) significantly reduces the driving power needed for a >7-m detection range at 14 V_{pp} and can drive single-ended and differential transducers. Below the 7-m detection range, the on-chip PMU can be programmed to provide a lower driving voltage to reduce system power. The integrated PMU eliminates the need for bulky off-chip supplies and reduces off-chip passive components. In addition, the programmable pulse frequency can cope with small-pitch size transducers for applications requiring a small form factor. The FPGA is primarily used for buffering and processing the data for displaying the user interface (UI) over WiFi transmission; this UI is not required for robot's navigation purposes; hence, FPGA power can be reduced. We still implemented UI with FPGA in the system for comparison with camera vision.

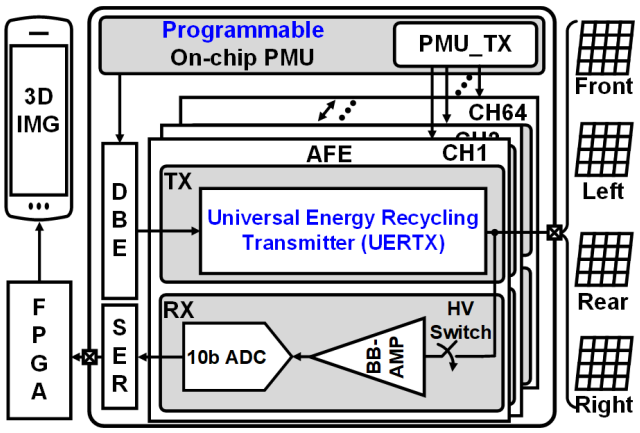


Fig. 2. Architecture of the 3-D ultrasound ASIC system.

B. Energy-Efficient TX Requirement

Bulk piezo transducers are preferred for air-coupled applications because of their high output sonic pressure [17]. However, TX power consumption is a significant concern, especially in battery-constrained metamorphic robotic machine vision. The theoretical average dynamic power consumption of the transmitter when driven by a conventional class-D driver [18], [19] is

$$P_{TX} = \alpha f C_{FT} V_{TX}^2 \quad (1)$$

where α is the duty cycle of TX duration of each frame, f is the driving frequency, C_{FT} is the feedthrough capacitance, and V_{TX} is the amplitude of the driving voltage. The bulk piezo transducer used in the article has a 40-kHz center frequency with a 1.9-nF feedthrough capacitance. For our metamorphic

TABLE I
COMPARISON OF EXISTING ENERGY-EFFICIENT TX FOR ULTRASOUND ASIC

Technique Paths	Stepwise Charging [21]	Charge Redistribution [22]	Energy Replenishing [23]	Universal Energy Recycling TX
Energy Saving Ratio	38%	42.6%	73.1%	44%
Transducer Load (pF)	40	15.4	820	1900
Transducer Type	CMUT	PMUT	Bulk Piezo	Bulk Piezo
Operation Frequency (Hz)	2.5M	5M	1M	40k
Output Amplitude (V_{pp})	30	13.2	30	10
External Component/ Ch.	1 capacitor for 2 channels	0	1 inductor	1 capacitor for 16 channels
Process	0.18 μm HV CMOS	0.18 μm standard CMOS	0.18 μm BCD	0.18 μm standard CMOS
Power (mW)	39.4	9.26	1*	6.54

* The estimated power consumption extracted from graph.

robot application, we experimentally determined that bursts of 64 pulses are suitable for detecting an object at 7-m at a scan rate of 4 fps while the robot is moving at 0.1 m/s.

From the above specifications, the average TX dynamic power calculated by equation (1) is 95 μW. More importantly, the average power per channel of a conventional class-D during the TX turn-on period is 15 mW. The power for driving four channels is 60 mW, much higher than RX power; therefore, a low-power TX is necessary. Moreover, a robust on-chip PMU is required to supply high peak power output. Integrating the energy-efficient and area-effective TX on a single chip is also mandatory to cope with large transducer array ($\geq 4 \times 4$).

In addition to adjusting V_{TX} for different detection ranges to conserve power, there is a need to reduce the power overhead when driving C_{FT}. Conventionally, there are three main methods to reduce the power overhead associated with driving C_{FT} to improve energy efficiency, as summarized in Table I.

The first method proposed by Chen *et al.* [21] is the multi-level driving scheme inspired by stepwise charging [24]. While it is suitable for driving CMUT transducers with single-ended termination, this method needs two off-chip capacitors for four channels [21] or feedback control [25], increasing circuit complexity and system form factor. In the second method, the charge redistribution technique is proposed [22], [26] to reduce TX's power consumption of PMUT. This method is confined to driving PMUT transducers with three electrodes, as it relies on PMUT's structural strength to return the electrodes to their original position. Recently, the energy replenishing technique was proposed [23] to reuse the electrical charge usage during transmission with the help of an off-chip inductor. This method successfully reduces energy consumption with adiabatic switching [27], but it is limited to driving single-ended bulk piezoelectric transducers similar to the multi-level driving scheme. Moreover, this method needs an off-chip inductor for each channel. Therefore, a high-efficiency ultrasound TX driver that can be easily integrated on-chip and drive both the single-ended and differential transducers is highly desirable.

We adopt the charge recycling (CR) concept [24] to form a multi-channel UERTX to overcome these limitations while improving the energy efficiency of the TX with a minimal area overhead. The achieved energy-saving ratio when UERTX is enabled is 44%. It also requires fewer off-chip components (one capacitor for 16 channels) than the previous method and can drive various ultrasonic transducers.

C. Transducer Characterization and PMU Requirements

The ultrasound transducer is responsible for transmitting the diverging wave and receiving echo signals from the reflectors. Its sonic output pressure and received echo sensitivity determine the detection range. For 3-D object detection, the detection range can be dramatically different for various use cases. For example, in-door applications only require a 3-m detection range. In contrast, outdoor applications need a detection range of 7-m for providing sufficient collision margin, while the onboard navigation system calculates an effective route. Therefore, a PMU that provides programmable TX driving voltages for different detection ranges is necessary for high system power efficiency.

This work uses the commercial bulk piezo transducer to experimentally obtain the driving voltage for various detection ranges (Prowave, 400ST/R100). As the reflector's geometric size, material, and surface directivity affect the echo signal strength, we used the carbon boxes to represent all the objects. We placed the test carbon box perpendicular to the wavefront during characterization. A test object of size 0.5 m $\times$ 0.5 m carbon box is placed from 1 to 7 m away from the transducer, and the TX driving strength is set at 6, 10, and 14 V_{pp}, respectively. The echo signal strength is then measured, as shown in Fig. 3. The resulting received echo signal amplitude shows a 20-dB change when the object is moved from 1 to 5 m. Zooming in the 5–7-m range, when the driving voltage is raised from 6 to 14 V_{pp}, the received echo signal amplitude at 7 m is tripled. At 6 V_{pp} driving strength, the echo signal amplitude is close to the noise floor of 100 μV and has a low signal-to-noise ratio (SNR) of 3.5 dB. Therefore, a driving voltage of at least 10 V_{pp} is required to ensure a high SNR of 6 dB at 7-m.

The tests show that sufficiently high SNR is maintained even for lower driving voltages for distances <7-m while the transducer is driven at voltages <14 V_{pp}. This brings a significant reduction in power for shorter distances (<7-m), as described in equation (1). On the other hand, a higher driving voltage is necessary to maintain a sufficiently high SNR for detection beyond 7-m. Therefore, the PMU that provides programmable TX driving voltage helps maintain high system power efficiency for various detection ranges. The PMU also powers the rest of the chip without any

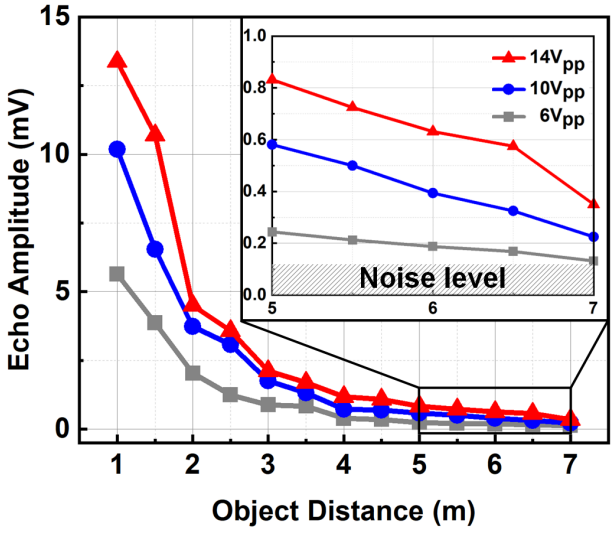


Fig. 3. Echo amplitude versus object distance for different driving voltages.

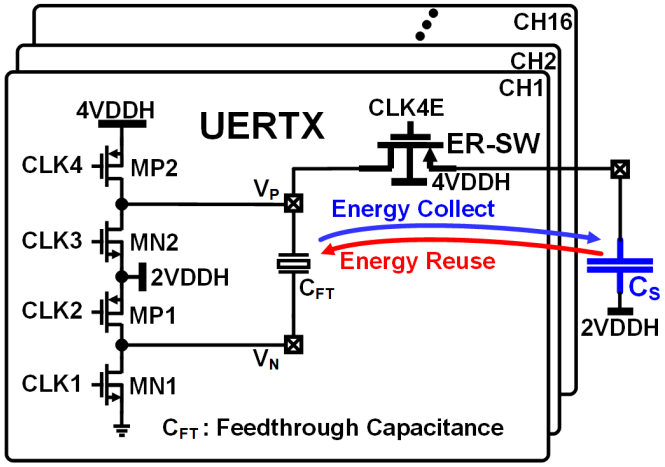


Fig. 4. Schematic of UERTX.

off-chip regulators, lowering the system's cost and form factor.

III. Chip Implementation

A. Universal Energy Recycling TX

Based on the CR circuit proposed in [20] and [26], we propose a UERTX, which can efficiently drive transducers having either two (single-ended) or three electrodes (differential), as shown in Fig. 4. In the schematic, a PMOS switch (ER-SW) connects the transducer's C_{FT} top (V_P) with the off-chip storage capacitor (C_S)'s top (V_{CS}). The sources of transistors MN2 and MP1 are tied together to 2VDDH. V_P swings between 2VDDH and 4VDDH, while V_N swings between 2VDDH and 0. They are connected to the two terminals of the bulk piezo transducer or can be connected to the outer and inner electrodes of the PMUT transducer. In the triple-terminal PMUT transducer, the top and bottom electrodes are tied to the 2VDDH generated by the on-chip PMU.

Assuming that R_{ON} of ER-SW is zero and applying the charge conservation law, the dynamic energy reduction

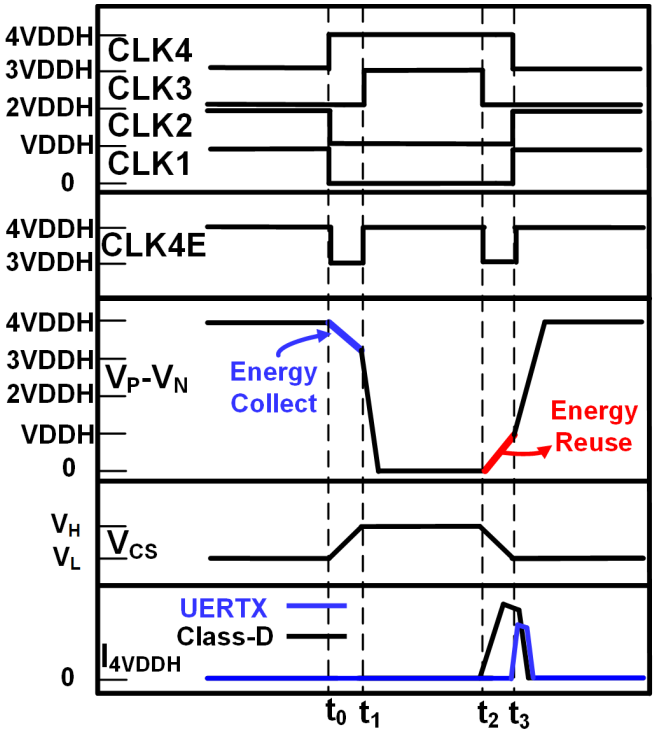


Fig. 5. Working principle of UERTX.

ratio (ERR) of UERTX driver compared with class-D driver [19] is derived as

$$\mathrm{ERR}_{\mathrm{UERTX}} = \frac{C_S + C_{FT}}{2C_S + C_{FT}}. \tag{2}$$

Equation (2) shows that the dynamic ERR can approach 50% as long as C_S is much greater than C_{FT}. As illustrated in Fig. 5, during the energy collect period ($t0 \rightarrow t1$), CLK2 and CLK4E turn on MP1 and ER-SW. Before charging up the bottom plate of C_{FT}, C_S collects the charges to make up for the energy loss in the energy reuse period. During the energy reuse period ($t2 \rightarrow t3$), CLK2 and CLK4E turn on MP1 and ER-SW again to generate the energy flow loop. C_{FT} is charged up first by C_S, then by 4VDDH supply. This significantly halves the transient peak current. In practical cases, R_{ON} is non-zero, and therefore the ERR will be lower than 50%.

Due to the in-phase transmission TXs, 16 TX drivers share a single off-chip capacitor, C_S, minimizing off-chip component count. The simulation in Fig. 6 illustrates that at the same driving strength (10 V_{pp}), frequency of 40 kHz, and a capacitive load of 1.9 nF per channel, the UERTX consumes 44% less energy than the class-D driver, which uses the non-overlap switching method in [19]. While the UERTX requires fewer off-chip components, the current ASIC does not support out-of-phase driving. Nevertheless, the UERTX scheme can still be applied to out-of-phase driving (for TX beamforming) and is left for our future implementation.

B. On-Chip Programmable PMU

The on-chip programmable PMU reduces the system form factor, increases the power efficiency, and makes the

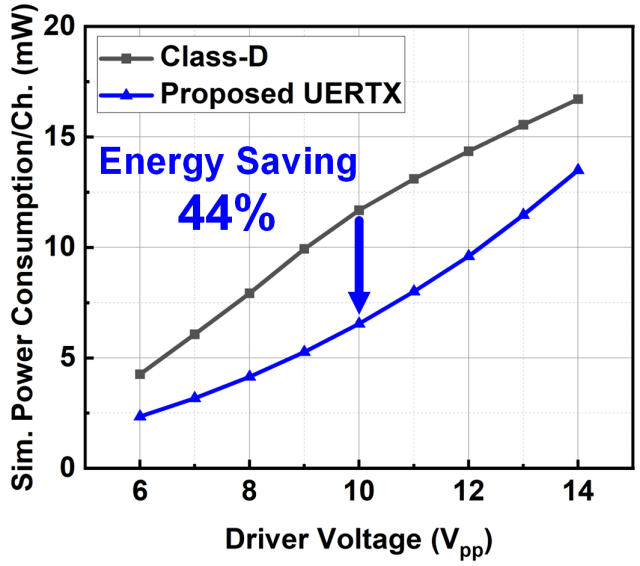


Fig. 6. Simulated power consumption comparison of the proposed UERTX and non-overlap switching-assisted class-D [19].

ultrasound ASIC system more cost-effective. The PMU diagram consists of a bandgap (BG), low-dropout regulators (LDO), and an LDO-charge pump cascade, as shown in Fig. 7(a).

The single 5-V input supply allows for easy accessibility from a portable power bank. Each of the three HV domains (2VDDH, 3VDDH, and 4VDDH) has separate LDOs and charge pump paths because the charge pump's voltage doubling property is not maintained when the output is greater than the nominal voltage of the standard CMOS. The four voltage domains (VDDH, 2VDDH, 3VDDH, and 4VDDH) for UERTX are tunable by their corresponding select signals (VSEL [3:0]). These DC supplies' stability is essential for the normal function of MOS transistors in the UERTX driver. Two large 10-pF on-chip capacitors are implemented for each voltage doubler, and nine charge pumps are connected in parallel to provide sufficient large load current capability. In the layout, they are placed on top of the large conducting transistors for area-saving. In the output of each charge pump, there is an off-chip capacitor (47 μF) to stabilize the outputs further. The FPGA provides the clock input to the charge pump. It determines the final driving capability of 4VDDH, which provides the majority of the power to UERTX. The load capacity is set as the target for sizing the LDO and charge pump transistors during the design stage. At the clock speed of 25 MHz, 4VDDH can generate up to 14 V_{pp} and supply a maximum transient load current of 160 mA required by 16 bulk piezo transducers with $C_{FT} = 1.9$ nF. The on-chip PMU also provides the VDDQ for the 16 digital IOs, 2.5 V compatible with the MAX10 FPGA IOs. It also outputs VDDD 1.8 V for the digital backend (DBE) and serializer (SER) modules. In addition, it provides VDDA (1.5 V) for the analog front-end (AFE) circuits.

The programmability of PMU makes the driving voltage of TX tunable based on the object distance, as shown in Fig. 7(b). For objects under the 7-m range, the driving voltage is below

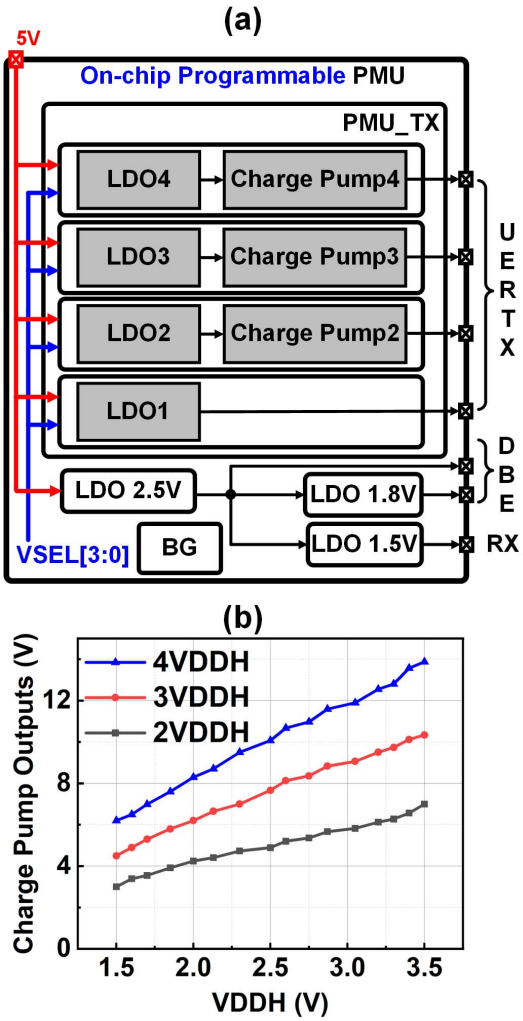


Fig. 7. (a) Diagram of the on-chip programmable PMU and (b) measured programmability of PMU.

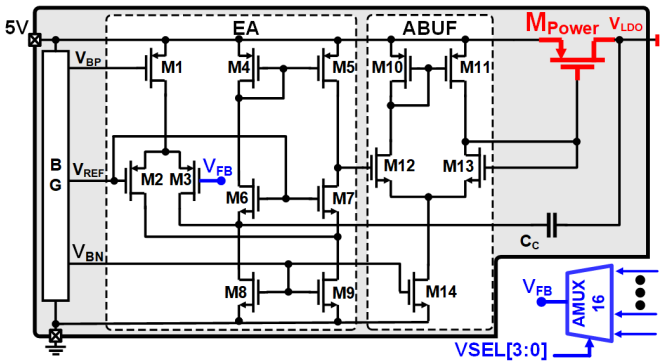


Fig. 8. Schematic of LDO.

10 V_{pp} to save power while maintaining a high SNR. However, for object detection beyond 7-m, the driving voltage can be set above 10 V_{pp}. This feature significantly improves the overall energy efficiency for a wide detection range.

The LDO circuit is shown in Fig. 8. It consists of BG, error amplifier (EA), analog buffer (ABUF), and power transistor

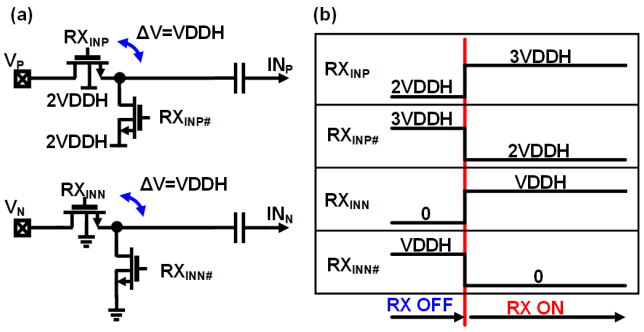


Fig. 9. (a) Schematic and (b) timing diagram of HV switch.

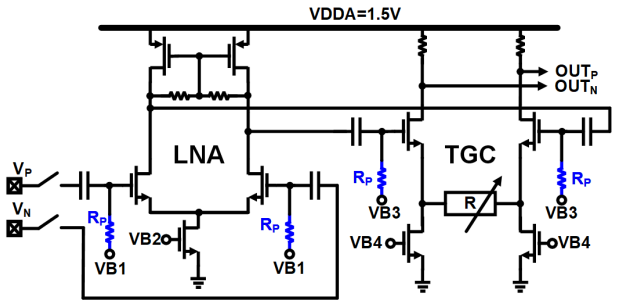


Fig. 10. Schematic of RX amplifiers.

(M_{Power}). The BG provides the bias voltage V_{BP}, V_{BN}, and reference voltage V_{REF}. The feedback voltage (V_{FB}) is sampled from the resistor ladder and multiplexed by the analog multiplexer. All the LDOs leverage the same schematic and layout, except for the different feedback voltage. It helps alleviate the efforts for design and minimizes intra-chip variations among all the LDOs.

C. Receiver (RX) Chain

The ultrasound ASIC's RX path consists of the HV switch, broadband amplifier, and a coarse-fine shared ADC. The HV switch isolates the TX output high swings from 0 to 14 V_{pp} from the RX path. The HV switch comprises four deep n-well transistors, as shown in Fig. 9(a). The gate-to-source voltages of the switches are confined to one VDDH in the RX ON state, preventing the breakdown of the transistors, as shown in Fig. 9(b). The reset transistors are turned on by $\text{RX}_{\text{INP\#}}$ and $\text{RX}_{\text{INN\#}}$ signals during the RX OFF state to eliminate the differential input noise. The ASIC uses the mixed-signal 1P6M process with deep n-well support. The HV T/R switch is constructed using the thick oxide deep n-well NMOS. All the MOS device gate-to-source tolerance voltage is 1VDDH. The reverse-biased breakdown of P+/NW, N+/PSUB, NW/PSUB, and DNW/PSUB is >10 V, >10 V, >14 V, and >14 V, respectively. The maximum drive voltage is 14 V_{pp}, within the maximum reverse-biased diode breakdown voltage of NW/PSUB and DNW/PSUB. Also, the drain-to-source 7 V_{pp} voltage difference is under the tolerance of the process rated voltage.

As discussed in Fig. 3, the echo signal dynamic change is around 20 dB from the 1 to 5 m. Therefore, the low-noise

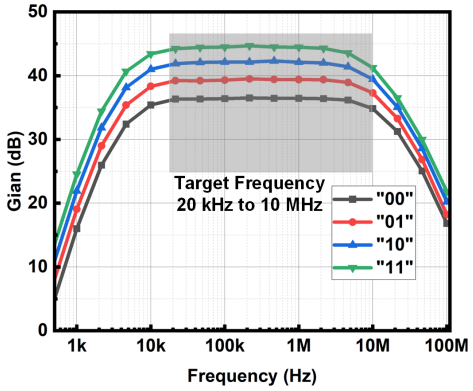


Fig. 11. Measured frequency response of RX amplifier.

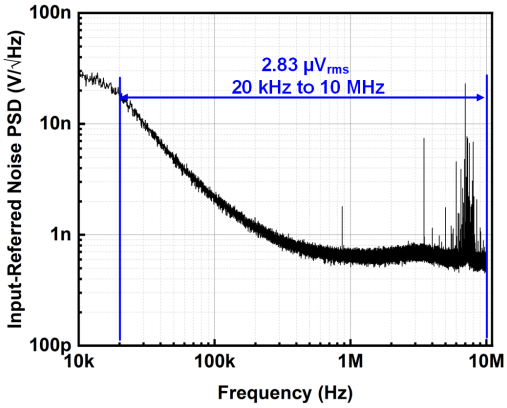


Fig. 12. Measured input-referred noise of LNA + TGC.

amplifier (LNA) is designed with a target gain of 20 dB. The echo signal has additional attenuation beyond 7-m, so LNA is cascaded by a time-compensation gain (TGC) amplifier. The overall RX front-end schematic is shown in Fig. 10. The on-chip bias circuit generates the bias voltages to eliminate off-chip components. The bandpass filter is integrated into the amplifiers to reduce the input noise. The high-pass corner of the bandpass filter is composed of an input capacitor and pseudo-resistor, R_{P}. The pseudo resistor R_{P} requires a much smaller area than using on-chip resistors. The input capacitor isolates the dc signal from the TX and helps eliminate the offset for both LNA and TGC. The TGC tunable gain compensates for the echo signal dynamics for distances above 7-m.

The cascaded amplifier is 2-bit tunable from 37 to 45.2 dB. Fig. 11 shows the measured frequency response of the broadband amplifier covering 20 kHz–10 MHz which can correspond to various transducers. This performance achievement is promising for future transducer arrays with smaller pitches and lower costs. The measured input-referred noise is shown in Fig. 12. The noise over the bandwidth of 20 kHz–10 MHz is 2.83 μV_{rms}, which is around two orders of magnitude lower than the echo signal strength at the amplifier's input (225 μV) from an object 7-m away under 10 V_{pp} driving.

The adjacent four channels of the ultrasound transducer array receive a similar echo signal, especially in the 8 × 8 array scenario. Hence, the ADC coarse bits

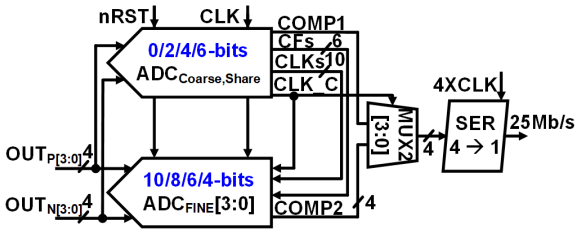


Fig. 13. ADC block diagram of four channels.

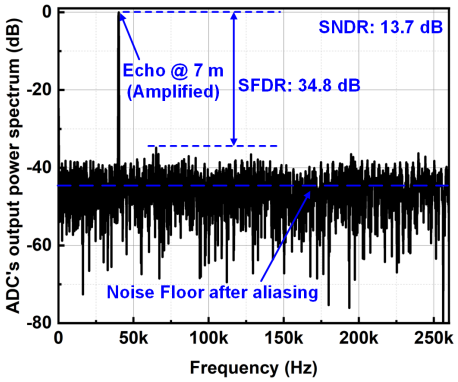


Fig. 14. ADC output power spectrum with echo at 7-m.

can be shared among four adjacent channels, significantly reducing the ADC's switching power per channel. Therefore, ADCs adopt the dynamic-bit-shared (DBS) successive-approximation-register (SAR) logic [22]. The coarse-fine shared ADCs are arranged in four channels per group, as shown in Fig. 13. Under the maximum bits sharing (6 bits), the ADC power has a 1.5× reduction, which boosts the energy efficiency for the ultrasound ASIC system with smaller pitch-size transducer arrays. In addition, the SER is implemented to reduce the PAD, which further reduces the area. The ADC sampling rate is programmable between 0.2 and 20 MS/s by the DBE module to support various transducers. For example, the sampling rate can be programmed to 10 MS/s and 520.8 kS/s for the 1-MHz and 40-kHz transducers, respectively. For the 40-kHz transducer's case, as the bandwidth of the amplifier is much greater than the ADC's sampling rate, noise aliasing is inevitable; however, as shown in the measured ADC's output power spectrum (see Fig. 14), even with the smallest echo from 7-m (under 10 V_{pp} driving), the measured SNDR and SFDR are 13.7 and 34.8 dB, respectively, showing the echo is still recoverable from noise.

D. DBE Processing

The ASIC requires a DBE to provide control signals to the on-chip circuits. The DBE is programmable via FPGA. In addition, DBE is also responsible for controlling the raw data flow between FPGA and ultrasound ASIC. The block diagram of the proposed ultrasound ASIC's DBE is shown in Fig. 15.

The DBE contains four main blocks, parameter block, clock block, pulse generator, and SER. The parameter block stores parameters that control all the other digital blocks and AFE

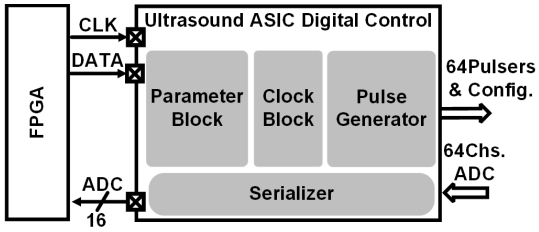


Fig. 15. DBE diagram.

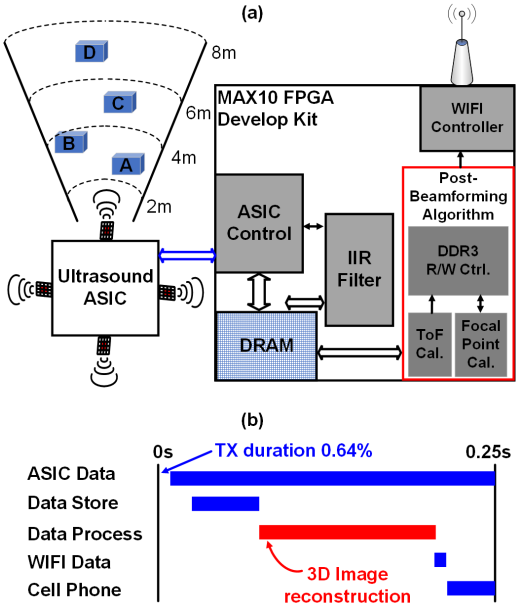


Fig. 16. (a) Diagram of the ultrasound ASIC 3-D vision system and (b) pipeline of ultrasound ASIC system data processing.

modules. The pulse generator block has enabled the programmability of the ultrasound ASIC to make the AFE capable of driving transducers with various pulses and frequencies. The clock block configures the ADC clock to adjust the sampling rate. The 64-channel ADC outputs pass through SER and are then streamed out through 16 pads.

E. 3-D Vision System Construction

As illustrated in Fig. 16(a), the serial data output from ASIC are fed to FPGA at 25 Mb/s using 16 pads. The FPGA deserializes the data and concatenates 10-bit data into one sample for each channel. The received data are stored in DRAM through a ping-pong SRAM buffer. After an entire frame is stored in the DRAM through the customized DRAM read and write (RW) controller, the 64-channel data are reread and fed into the IIR filter (sixth order with 35–45 kHz passband) sequentially. Finally, the filtered data are written back to the DRAM again. Then post beamforming algorithm starts calculating ToF and fetching data from DRAM for 3-D image reconstruction. After the focal point calculation of the entire volume within the 8-m range, the reconstructed image data are transmitted to cell phone application through the WiFi module to display at four frames per second (fps). The data processing pipeline

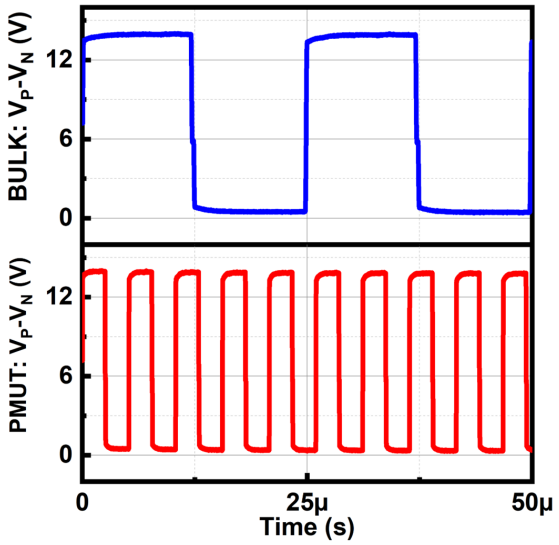


Fig. 17. Measured UERTX waveform of the bulk piezo transducer and PMUT at 14 V_{pp}.

is illustrated in Fig. 16(b). There is a gap in the ultrasound ASIC data processing pipeline at the beginning of ASIC data input. This is because TX transmission occupies approximately 0.64% of the frame. Therefore, the TX transmission portion can be reduced for energy-saving or increased for longer range object detection. Currently, the FPGA resource limits the four frames/sample. Hence, the data stored on FPGA stop at 50 ms of each frame. The data beyond the 8-m range are not stored on FPGA.

IV. Measurement Results

A. TX Measurement

To verify that the proposed UERTX can save energy for both two-terminal and three-terminal transducers, the UERTX is measured by driving the bulk piezo and PMUT to fit different machine vision applications. The measured UERTX driver waveform at 14 V_{pp} of a 40-kHz bulk piezo transducer with 1.9-nF C_{FT} and the 192-kHz PMUT with 0.4-nF C_{FT} are shown in Fig. 17. Fig. 18 shows the zoomed-in view of the UERTX waveform, including the energy collect and energy reuse periods.

The measured energy recycling switch (ER-SW) turn-on time is 45 ns, which corroborates the simulated turn-on time of 50 ns. Furthermore, the voltage variations of VP-VN in both the periods are 6 V_{pp}, approaching 2VDDH. This measurement proves that UERTX is universal for different transducers under a broad spectrum of resonant frequencies and has a simple control logic with negligible power overhead.

The power consumption of TX versus VDDH is shown in Fig. 19. The power consumption of TX, including PMU_TX and UERTX, is measured under 16 channels driving 64 pulses at the 4 fps of the ASIC system. As the output voltage increases from 6 to 14 V_{pp}, the TX power increases by 6.4×. The curve shows that reducing the drive voltage is preferred as long as the application requirement (enough sonic pressure for object detection) is achieved. The TX driving voltage used

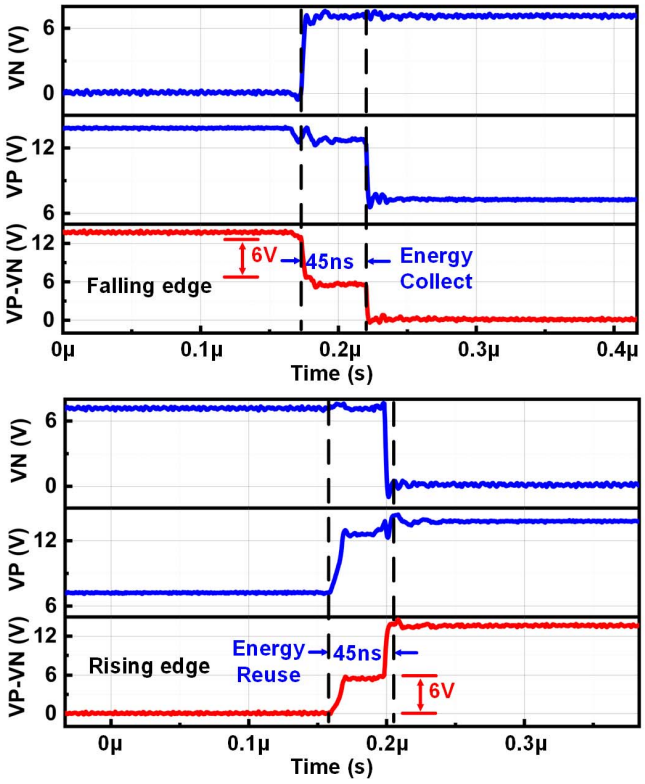


Fig. 18. Zoom-in measurement waveform of the UERTX driver including energy collect (falling edge) and energy reuse (rising edge) periods.

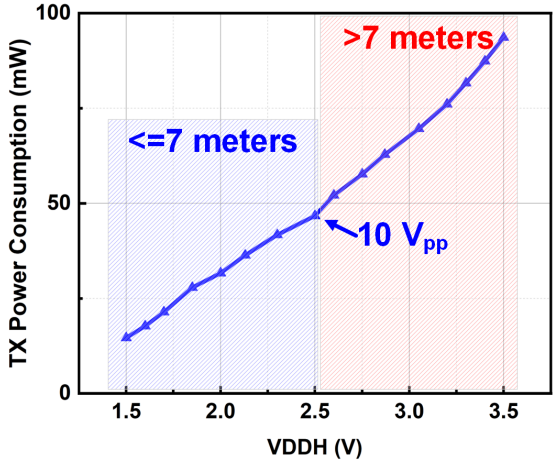


Fig. 19. Power consumption of TX versus VDDH.

in the final ultrasound ASIC system for image reconstruction is 10 V_{pp}. For the 7-m object measurement, the driver voltage of TX is programmed to 10 V_{pp} to ensure that the echo signal strength has a minimum SNR. To detect distances greater than 7-m, ASIC can program the TX driving voltage to be higher than 10 V_{pp}, which consumes more power. The TX driving voltage can also be set to <10 V_{pp} for short-distance detection (<7-m) to save power.

B. ASIC Power Breakdown

The ultrasound ASIC chip is fabricated in 0.18 μm 1P6M standard CMOS, as shown in Fig. 20(a). The whole chip area

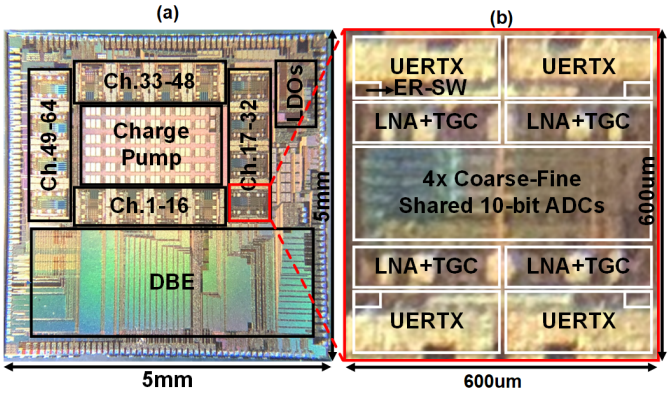


Fig. 20. (a) Chip photograph of the proposed ultrasound ASIC system and (b) micrograph of four channels.

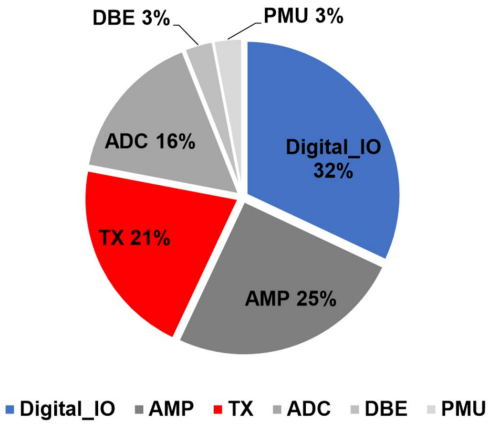


Fig. 21. Power breakdown of ultrasound ASIC.

is 5 × 5 mm^2. The integrated 64 channels are separated into four groups, and each group has 16 channels. Under the 16 channels, there are four subgroups. Fig. 20(b) shows that each subgroup has four channels. Each channel consists of ER-SW, UERTX, LNA, TGC, and dedicated coarse-fine shared ADC. The area overhead of ER-SW is merely 1.1%, which is negligible considering the significant 44% energy-saving of the UERTX compared with the class-D driver, which uses a non-overlap switching method [19].

Functioning as the metamorphic robot's 3-D vision sensors, the four sets of bulk piezo 4 × 4 arrays with 1-cm pitch are connected to ASIC's respective channels, one for each direction. Each side drives four center channels (out of 16) at four fps for its TX at 0.64% duty cycle during each frame to enhance sound pressure. The TX power consumption at 10 V_{pp} accounts for only 21% of the entire system, as shown in Fig. 21. The TX power per channel is 0.9 mW. The complete ASIC consumes 0.28 W, benefiting the metamorphic robot's power-constrained application. The digital IOs have become the dominant power-consuming block due to 64-channel data being continuously streamed out during each frame. The digital IO can be applied with the CR technique using an adequate on-chip storage capacitor for further energy-saving. The system-on-chip can further reduce data processing and

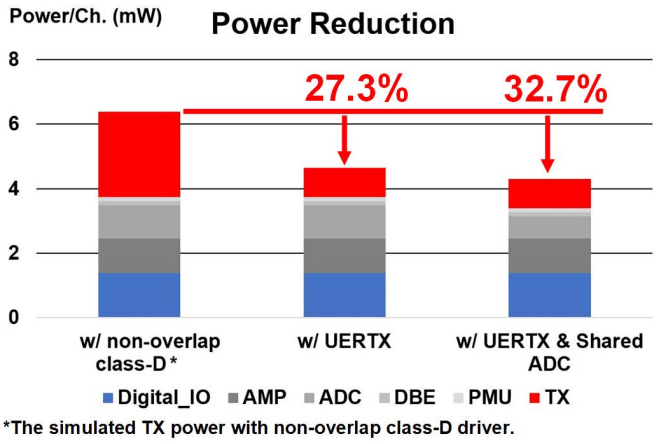


Fig. 22. Power per channel of the proposed ASIC for three different scenarios.

moving for energy-saving. Reducing the supply for RX chain will contribute significantly to power reduction. In addition, the ADC can be waked up by echoes rather than sampling the entire RX duration to improve its energy efficiency significantly.

Fig. 22 shows the measured power breakdown per channel for three different configurations, e.g., with non-overlap class-D, with UERTX only, and with UERTX and coarse-fine shared (6-bit sharing) ADC under the working load of driving 16 transducers at 10 V_{pp}, four fps, and 0.64% duty cycle. The power consumption of TX with non-overlap class-D is the simulation value, and all the others are measured values. The UERTX reduces the total power consumption of ASIC by 27.3%, while the coarse-fine shared ADC contributes an additional 5.4% power reduction.

C. Real-Time 3-D Vision

The ASIC board, connected with an FPGA, is mounted on the robot [see Fig. 23(a)]. The ADC data are streamed out from the chip and processed by FPGA. For a performance comparison with the proposed system, a visible light camera is mounted on the robot close to the ultrasound ASIC to capture the night view [see Fig. 23(b)]. Objects A, B, C, and D are placed from the robot at 1.7−, 3.6−, 5.4−, and 7.2-m distances. The temperature is 27 °C, the humidity is 75%, and the light is 5 lx. The B-mode is used for image reconstruction. Center 4 transducers of each array excite 64 pulses every 250 ms. The driving voltage is 10 V_{pp}. Then all parallel RXs receive and digitize the echo; meanwhile, the FPGA stores the entire frame data for focal point calculation. The 3-D space focal points are predefined in the latitude, longitude, and radius directions with 52 steps, 52 steps, and 77 steps. After the entire 208 208 focal points' calculation, the threshold is chosen to be ten times the minimum value. After filtering the value below the threshold, the calculated focal points are transmitted to the mobile phone through the WiFi module to display at 4 fps.

The top view [see Fig. 23(c)] and the 3-D view [see Fig. 23(d)] of the real-time reconstructed image shows that the proposed system successfully generates the image at

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED ULTRASOUND ASIC WITH RECENT WORKS

Metrics	This Paper	JSSC'21 [22]	ISSCC'18 [28]	ISSCC'16 [29]	JSSC'15 [12]	JSSC'13 [30]	ISSCC'21 [23]
Application	**Machine Vision**	Medical Diagnosis	Medical Diagnosis	Fingerprint Reading	Gesture Recognition	Medical Diagnosis	Medical Diagnosis
TX Energy Saving	**44%**	42.6%	N.A.	N.A.	N.A.	38%	73.1%
Depth Information	**Yes (3D)**	Limited*	Limited*	Limited**	Yes (3D)	Limited*	Limited*
Supply/ Driver Voltage	**Fully On-Chip/ Tunable 6-14 V_{pp}**	Partial On-Chip/ 13.2 V_{pp}	Off-chip/ 60 V_{pp}	Off-chip/ 24 V_{pp}	Off-chip/ 30 V_{pp}	Off-chip/ 30 V_{pp}	Off-chip/ 30 V_{pp}
Compatible Transducer	**PMUT/ Bulk Piezo**	PMUT	PZT/ CMUT	PMUT	PMUT	CMUT	Bulk Piezo
f_c coverage	**40 kHz of TRX 192 kHz of TX**	1/ 2/ 5/ 10 MHz	7 MHz	14 MHz	217 kHz	3.3 MHz	1 MHz of TX
Power/Ch (mW)	**4.3 @ 10 V_{pp}**	5.37 @ 5 V_{pp}	6.26	-	-	66.7@ 30V_{pp}	N.A.
TRX + ADC	**Yes**	Yes	External ADC	External ADC	Yes	External ADC	TX only
Ch. #	**64**	36	64	6160	10	4	1
System Form Factor	**5×5×5 cm^3, ⩽ 100 g**	Bulky External Supply	Bulky External Supply	Bulky External Supply	Bulky External Supply	Bulky External Supply	Bulky External Supply
Technology	**0.18 µm Standard CMOS**	0.18 µm Standard CMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.18 µm BCD

*[22], [23], [28], and [30] need to rotate the probe to get the 3D information.
** The 3D information of [29] is confined by the transducer array area.

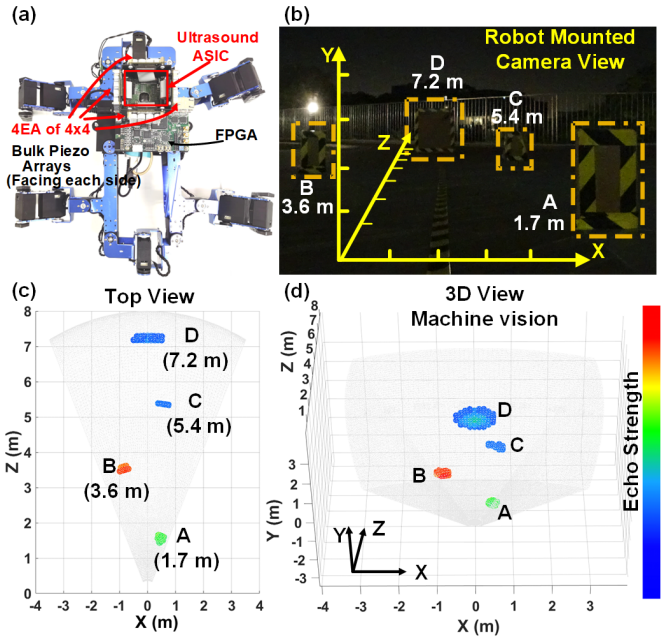


Fig. 23. (a) Photograph of the proposed ultrasound ASIC system mounted on the metamorphic robot (top view), (b) measurement setup (at 00:30 AM), (c) corresponding reconstructed image (at 4 fps) top view (*XZ* plane), and (d) 3-D view for robotic vision.

four fps with crucial depth information for metamorphic robots' 3-D vision (moving at 0.1 m/s). Current visible light camera implementations cannot achieve this under low-light conditions. Object D has large dispersion because its geometry is nine times larger than object A. Objects A, B, and C are in the same geometry, 15 cm × 20 cm. A's reflecting surface is not perpendicular to the wavefront to emulate the real navigation scenario. Therefore, its echo strength is weaker than object B though its distance is nearer than B's; such cases are common while robots negotiate obstacles. The cone shape in Fig. 23(c) indicates that the field of view is confined to 52° due to the transducer array's grating lobe effect, which can be improved by replacing more miniature transducers with smaller pitches. The bit-sharing technique is not applied to this image because the bulk piezo transducer array's pitch size (1 cm) is close to the wavelength (8.6 mm); however, for 100-kHz PMUT with 1-mm pitch, it can benefit from ADC's bit-sharing.

To verify the proposed ultrasound ASIC system operation under various weather conditions, additional experiments were done under different temperatures (20 °C–35 °C), relative humidity (50%–89%), indoor and outdoor scenarios, and dry/rainy situations (including a heavy thunderstorm). ASIC is able to reconstruct the image with negligible effect under different challenging conditions.

Table II summarizes the performance of the proposed ASIC along with state-of-the-art works. The proposed ultrasound ASIC system achieves a >7-m detection range in the air channel. The proposed ultrasound ASIC power consumption is also competitively low at only 4.3 mW/channel when the TX driving is 10 V_{pp}. In contrast, the design of [22] consumes 5.37 mW/channel when driving at 5 V_{pp}. In addition, this

ultrasound ASIC system is the first to integrate an on-chip programmable PMU, thereby eliminating bulky, off-chip power supply. Finally, UERTX has been verified to drive PMUT and bulk piezo transducers.

V. Conclusion

This article presents an air-coupled ultrasound ASIC system with a >7-m long detection range and consumes 0.28 W. The 64-channel ASIC system weighing only 100 g mitigates the limitation of the camera vision system under low-light conditions or bad weather such as the rainy environment by successfully reconstructing multiple objects with different depth information, all on a metamorphic robot.

Acknowledgment

The authors would like to thank Yang Luo, Yue Zhuang, Zhuoyue Li, and Rucheng Jiang from the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, for the 3-D vision system build-up. The authors also would like to thank Dr. Chunsong Zhang from Daran Robotics, China, for providing the metamorphic robot and its 3D model.

References

[1] O. Elkhalili, O. M. Schrey, P. Mengel, M. Petermann, W. Brockherde, and B. J. Hosticka, "A 4 × 64 pixel CMOS image sensor for 3-D measurement applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1208–1212, Jul. 2004.

[2] L. Lindgren, J. Melander, R. Johansson, and B. Möller, "A multiresolution 100-GOPS 4-Gpixels/s programmable smart vision sensor for multisense imaging," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1350–1359, Jun. 2005.

[3] J. Lu, S. Young, I. Arel, and J. Holleman, "A 1 TOPS/W analog deep machine-learning engine with floating-gate storage in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 270–281, Jan. 2015.

[4] K. Dandu *et al.*, "2.2 High-performance and small form-factor mm-wave CMOS radars for automotive and industrial sensing in 76-to-81 GHz and 57-to-64 GHz bands," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 40–41.

[5] O. Kumagai *et al.*, "7.3 A 189×600 back-illuminated stacked SPAD direct time-of-flight depth sensor for automotive LiDAR systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 110–111.

[6] A. Ibrahim *et al.*, "Efficient sample delay calculation for 2-D and 3-D ultrasound imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 815–831, Aug. 2017.

[7] Z. Shao, Y. Peng, S. Pala, Y. Liang, and L. Lin, "3D ultrasonic object detections with >1 meter range," in *Proc. IEEE 34th Int. Conf. Micro Electro Mech. Syst. (MEMS)*, Jan. 2021, pp. 386–389.

[8] J. Tillak and J. Yoo, "A 23 μW digitally controlled pMUT interface circuit for Doppler ultrasound imaging," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 1618–1621.

[9] C. Chen and M. A. P. Pertijs, "Integrated transceivers for emerging medical ultrasound imaging devices: A review," *IEEE Open J. Solid-State Circuits Soc.*, vol. 1, pp. 104–114, 2021.

[10] Y. Zhang and A. Demosthenous, "Integrated circuits for medical ultrasound applications: Imaging and beyond," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 5, pp. 838–858, Oct. 2021.

[11] C. Kuratli and Q. Huang, "A CMOS ultrasound range-finder microsystem," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 2005–2017, Dec. 2000.

[12] R. J. Przybyla, H.-Y. Tang, A. Guedes, S. E. Shelton, D. A. Horsley, and B. E. Boser, "3D ultrasonic rangefinder on a chip," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 320–334, Jan. 2015.

[13] Z. Shao, S. Pala, Y. Peng, and L. Lin, "Bimorph pinned piezoelectric micromachined ultrasonic transducers for space imaging applications," *J. Microelectromech. Syst.*, vol. 30, no. 4, pp. 650–658, Aug. 2021.

[14] H. Wu *et al.*, "A 7m-range, 4.3 mW/Ch. Ultrasound ASIC with universal energy recycling TX for all-weather metamorphic robotic 3D vision system," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2021, pp. 1–3, doi: 10.1109/A-SSCC53895.2021.9634764.

[15] B. E. Eovino, Y. Liang, S. Akhbari, and L. Lin, "A single-chip flow sensor based on bimorph PMUTS with differential readout capabilities," in *Proc. IEEE 31st Int. Conf. Micro. Electro. Mech. Syst. (MEMS)*, Jan. 2018, pp. 1084–1087.

[16] A. S. Mohammed, A. Amamou, F. K. Ayevide, S. Kelouwani, K. Agbossou, and N. Zioui, "The perception system of intelligent ground vehicles in all weather conditions: A systematic literature review," *Sensors*, vol. 20, no. 22, p. 6532, Nov. 2020.

[17] Y. Kusano, I. Ishii, T. Kamiya, A. Teshigahara, G.-L. Luo, and D. A. Horsley, "High-SPL air-coupled piezoelectric micromachined ultrasonic transducers based on 36% ScAlN thin-film," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 66, no. 9, pp. 1488–1496, Sep. 2019.

[18] A. Banuaji and H.-K. Cha, "A 15-V bidirectional ultrasound interface analog front-end IC for medical imaging using standard CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 8, pp. 604–608, Aug. 2014.

[19] H.-Y. Tang, Y. Lu, S. Fung, D. A. Horsley, and B. E. Boser, "11.8 integrated ultrasonic system for measuring body-fat composition," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 210–211.

[20] J. Lee *et al.*, "11.1 A 5.37 mW/channel pitch-matched ultrasound ASIC with dynamic-bit-shared SAR ADC and 13.2 V charge-recycling TX in standard CMOS for intracardiac echocardiography," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 190–191.

[21] K. Chen, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic imaging front-end design for CMUT: A 3-level 30 Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver," in *Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC)*, Nov. 2012, pp. 173–176.

[22] J. Lee *et al.*, "A 36-channel auto-calibrated front-end ASIC for a pMUT-based miniaturized 3-D ultrasound system," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1910–1923, Jun. 2021.

[23] J. Choi *et al.*, "34.4 An energy-replenishing ultrasound pulser with $0.25CV^2f$ dynamic power consumption," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 486–487.

[24] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," in *Proc. IEEE Symp. Low Power Electron.*, Oct. 1994, pp. 100–101.

[25] N. Sanchez *et al.*, "34.1 An 8960-element ultrasound-on-chip for point-of-care ultrasound," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 480–481.

[26] J. Tillak, S. Akhbari, N. Shah, L. Radakovic, L. Lin, and J. Yoo, "A 2.34 μJ/scan acoustic power scalable charge-redistribution pMUT interface system with on-chip aberration compensation for portable ultrasonic applications," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 189–192.

[27] J. G. Koller and W. C. Athas, "Adiabatic switching, low energy computing, and the physics of storing and erasing information," in *Proc. Phys. Comput. Workshop*, Oct. 1992, pp. 267–270.

[28] G. Jung *et al.*, "10.6 Single-chip reduced-wire active catheter system with programmable transmit beamforming and receive time-division multiplexing for intracardiac echocardiography," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 188–189.

[29] H.-Y. Tang *et al.*, "11.2 3D ultrasonic fingerprint sensor-on-a-chip," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 202–203.

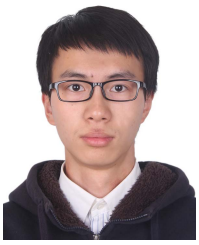
[30] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, Nov. 2013.

Han Wu (Student Member, IEEE) received the B.Eng. degree in electronic science and technology and the M.E. degree in microelectronics and solid-state electronics from the College of Optoelectronic Engineering, Chongqing University, Chongqing, China, in 2013 and 2016, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, in 2021.

He is currently a Research Fellow with the Department of Electrical and Computer Engineering, National University of Singapore. His research focuses on energy-efficient high-speed links, ultra-low-power system-on-chip design, and microelectromechanical system (MEMS) sensor interface circuit design.

Miaolin Zhang (Student Member, IEEE) received the B.Eng. degree in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2017, the distinguished graduate Diploma degree from the University of Strathclyde, Glasgow, U.K., in 2017, and the Ph.D. degree from the National University of Singapore, Singapore, in 2021.

He is currently working with Huawei Technologies, Chengdu. His research interests include machine learning algorithm developing for resource-constrained hardware, energy-efficient SoC design, and ASICs for high-performance Ethernet switch.



Zhichun Shao received the B.S. degree in engineering mechanics from Tsinghua University, Beijing, China, in 2017, and the M.S. and Ph.D. degrees in mechanical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 2019 and 2021, respectively.

He joined the Berkeley Sensor and Actuator Center (BSAC), University of California at Berkeley, in 2017. His research interest includes development of new architectures of microelectromechanical system (MEMS) ultrasonic transducers with enhanced output performance for sensing and actuation applications.

Jiaqi Guo (Student Member, IEEE) received the B.S. degree from Xidian University, Xi'an, China, in 2019, and the M.S. degree from the National University of Singapore (NUS), Singapore, in 2020, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

His current research interests include power management units and transmitter circuits and systems for an ultrasonic transmission imaging application.

Kian Ann Ng (Senior Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. degree in IC design from Nanyang Technological University, Singapore, in 2000 and 2005, respectively, and the Ph.D. degree from the National University of Singapore, Singapore, in 2015.

From 2000 to 2009, he has held senior technical positions with the following companies: STMicroelectronics, Singapore, Chartered Semiconductor Manufacturing, Singapore, and Oxford Semiconductors, Singapore He has designed EEG/ECG mixed-signal front ends, switched-capacitor circuits, RF identification circuits, image sensors, ESD/IO circuits, USB (1.0 to 3.0) SerDes, and Firewire SerDes, IEC60601-compliant devices. From 2010 to 2020, he was a Research Fellow with the National University of Singapore. He is currently an Assistant Professor with the Digipen Institute of Technology, Singapore. He has authored or coauthored more than 30 technical articles and holds five U.S. patents. His primary research focuses on analog IC and system design, implantable neural recording systems, and peripheral nerve prostheses.

Dr. Ng is an Active Committee Member of IEEE Solid-State Circuits Society (Singapore Chapter).

Liwei Lin (Member, IEEE) received the B.S. degree from the Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan, in 1986, and the M.S. and Ph.D. degrees from the Department of Mechanical Engineering, University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, in 1991 and 1993, respectively, all in mechanical engineering.

He is currently the James Marshall Wells Professor of the Department of Mechanical Engineering and the Co-Director of the Berkeley Sensor and Actuator Center, UC Berkeley. He has authored/coauthored more than 300 journal articles. His research interests include microelectromechanical systems (MEMS), nanoelectromechanical systems, nanotechnology, design and manufacturing of microsensors and microactuators, development of micromachining processes by silicon surface/bulk micromachining, micromolding process, and mechanical issues in MEMS such as heat transfer, solid/fluid mechanics, and dynamics.

Dr. Lin is a fellow of ASME and a Subject Editor of IEEE JOURNAL OF MICROELECTROMECHANICAL SYSTEMS.

Jerald Yoo (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2002, 2007, and 2010, respectively.

From 2010 to 2016, he was with the Department of Electrical Engineering and Computer Science, Masdar Institute, Abu Dhabi, United Arab Emirates, where he was an Associate Professor. From 2010 to 2011, he was also a Visiting Scholar with the Microsystems Technology Laboratories (MTL), Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. Since 2017, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he is currently an Associate Professor. He has pioneered research on low-energy body area network (BAN) for communication/powering and wearable body sensor networks using the planar-fashionable circuit board for a continuous health monitoring system. He has authored book chapters in *Bio-Medical CMOS ICs* (Springer, 2010), *Enabling the Internet of Things—From Circuits to Networks* (Springer, 2017), *The IoT Physical Layer* (Springer, 2019), and *Handbook of Biochips (Biphasic Current Stimulator for Retinal Prosthesis)* (Springer, 2021). His current research interests include low-energy circuit technology for wearable bio-signal sensors, flexible circuit board platform, BAN communication and powering, ASIC for piezoelectric micromachined ultrasonic transducers (PMUT), and system-on-chip (SoC) design to system realization for wearable healthcare applications.

Dr. Yoo has served as an IEEE Solid-State Circuits Society (SSCS) Distinguished Lecturer from 2017 to 2018 and an IEEE Circuits and Systems Society (CASS) Distinguished Lecturer from 2019 to 2021. He was a recipient or a co-recipient of several awards: the IEEE International Solid-State Circuits Conference (ISSCC) 2020 Demonstration Session Award (Certificate of Recognition), the IEEE International Symposium on Circuits and Systems (ISCAS) 2015 Best Paper Award (BioCAS Track), the ISCAS 2015 Runner-Up Best Student Paper Award, the Masdar Institute Best Research Award in 2015, and the IEEE Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Award in 2005. He was the Founding Vice-Chair of IEEE SSCS United Arab Emirates (UAE) Chapter, and is currently the Chair of the IEEE SSCS Singapore Chapter. He is serving/served as a Technical Program Committee Member for the IEEE International Solid-State Circuits Conference (ISSCC), the Co-Chair for ISSCC Student Research Preview, the Emerging Technologies and Applications Subcommittee Chair for IEEE Asian Solid-State Circuits Conference (A-SSCC), and IEEE Custom Integrated Circuits Conference (CICC). He is also an Analog Signal Processing Technical Committee Member of IEEE Circuits and Systems Society.