A Bi-Directional 300-GHz-Band Phased-Array Transceiver in 65-nm CMOS With Outphasing Transmitting Mode and LO Emission Cancellation

Ibrahim Abdo, *Member, IEEE*, Carrel da Gomez, Chun Wang, Kota Hatano, Qi Li, *Graduate Student Member, IEEE*, Chenxin Liu, Kiyoshi Yanagisawa, *Member, IEEE*, Ashbir Aviat Fadila, *Graduate Student Member, IEEE*, Takuya Fujimura, Tsuyoshi Miura, Korkut Kaan Tokgoz, *Member, IEEE*, Jian Pang, *Member, IEEE*, Hiroshi Hamada, *Member, IEEE*, Hideyuki Nosaka, *Senior Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Senior Member, IEEE*

***Abstract*— This article introduces a four-element 300-GHz-band bi-directional phased-array transceiver (TRX). The TRX utilizes the same antenna, signal path, and local oscillator (LO) circuitry to operate either in transmitter (TX) mode or receiver (RX) mode. The TX mode adopts the outphasing technique to increase the average output power for higher order modulation schemes by utilizing the two mixers that are connected directly to the antenna in a mixer-last fashion. The two signal paths also enable the canceling of the LO feed-through (LOFT). The RX mode also benefits from the LOFT cancellation technique to suppress the LO emission, which is a common issue of the mixer-first RXs. The RX has a separate Hartley operation mode to reject the image signal coming from the TX. The TRX chip was implemented using CMOS 65-nm process, and a four-element phased array was implemented by stacking liquid crystal polymer (LCP) flexible printed circuit boards (PCBs). The stacked structure provides the required narrow antenna pitch at the 300-GHz band. The measured beam angle range is from −18° to 18°. The single-element power consumption is 750 mW for both TX mode and RX mode.**

***Index Terms*— 300 GHz, beyond 5G, bi-directional transceiver (TRX), CMOS, frequency multiplier, outphasing, phased array, subharmonic mixer.**

Manuscript received 5 August 2021; revised 24 November 2021 and 27 April 2022; accepted 18 May 2022. Date of publication 8 June 2022; date of current version 25 July 2022. This article was approved by Associate Editor Patrick Reynaert. This work was supported in part by STAR and in part by VDEC in collaboration with Cadence Design Systems, Inc., Synopsys Inc., Mentor Graphics, Inc., and Keysight Technologies Japan, Ltd. *(Corresponding author: Ibrahim Abdo.)*

Ibrahim Abdo was with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan. He is now with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan (e-mail: ibrahim.abdo.nr@hco.ntt.co.jp).

Carrel da Gomez, Chun Wang, Kota Hatano, Qi Li, Chenxin Liu, Kiyoshi Yanagisawa, Ashbir Aviat Fadila, Takuya Fujimura, Tsuyoshi Miura, Jian Pang, Atsushi Shirane, and Kenichi Okada are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan.

Korkut Kaan Tokgoz was with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8550, Japan. He is now with the Faculty of Engineering and Natural Sciences, Sabanci University, 34956 Istanbul, Turkey.

Hiroshi Hamada was with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan. He is now with NTT DOCOMO, Inc., Yokosuka 239-8536, Japan.

Hideyuki Nosaka was with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan. He is now with the Department of Electrical and Electronic Engineering, Ritsumeikan University, Shiga 525-8577, Japan.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3179166.

Digital Object Identifier 10.1109/JSSC.2022.3179166

I. Introduction

FREQUENCIES above 200 GHz are among the strongest candidate bands to be utilized in beyond 5G wireless communication systems where very high data rates and low latency are required. Pushing the carrier frequencies higher makes it possible to increase the RF bandwidth and the communication speeds. In the recent years, many efforts have been made to standardize the 300-GHz band, including the amendment of IEEE 802.15.3d [1], [2].

The 300-GHz-band TRX systems using compound semiconductors and SiGe were demonstrated in several works with excellent performance due to the high maximum oscillation frequency ($f_{\max}$) as in [3]–[18]. However, implementing these systems using the CMOS process is considered more attractive due to the cheap cost and the ability to integrate large digital circuits. One large drawback of the CMOS process is its low $f_{\max}$, which does not normally exceed 300 GHz. As a result, the CMOS amplification is not normally used for systems that operate at frequencies above 170 GHz [19]–[22]. Although several 300-GHz-band CMOS amplifiers have been demonstrated lately [23]–[26], their characteristics are still not reliable for wideband 300-GHz-band wireless TRXs, causing the dominance of the mixer-last (or multiplier-last) transmitter (TX), mixer-first receiver (RX) architecture in the recent works [27]–[35]. This architecture suffers from the limited output power, high noise figure, and the LO feed-through (LOFT) radiation from both TX and RX. The output power issue was mainly faced by using frequency multipliers instead of mixers [27], [29], [30], [32], [35].

In most of the recent sub-terahertz (THz) CMOS transceiver (TRX) implementations, high-gain horn or parabolic antennas [36]–[39], lens antennas [40], and a combination of both horn and lens antennas [41] are used to overcome

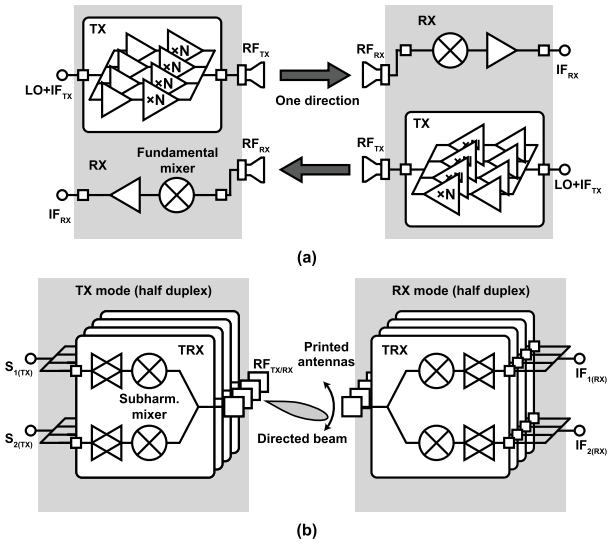


Fig. 1. (a) Conventional sub-THz TRX. (b) Proposed TRX with bi-directional phased-array architecture and beamforming.

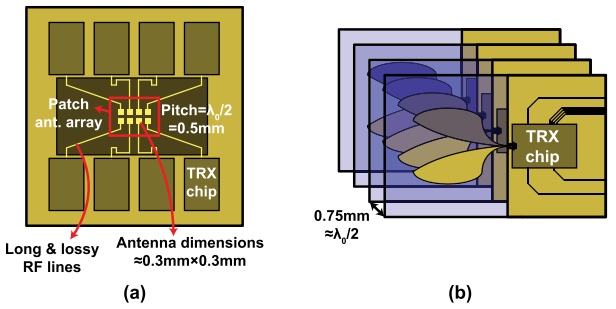


Fig. 2. (a) 300-GHz-band half-wavelength-pitched phased array using patch antennas. (b) Stacked antenna placement for short wavelength arrays.

the large path loss, but the radiation is only toward a single direction. The phased-array implementation commonly used in millimeter-wave systems is the most suitable solution to this issue as it enables beam steering and boosts the antenna gain. The lens antenna can be added to the array to increase the gain, but it causes a narrower steering angle range [41], [42]. To avoid a large and complicated array configuration, antenna sharing between the TX and the RX is essential. As can be observed in the latest 200–300-GHz CMOS TRXs [27]–[32], the TX and RX parts are designed separately mainly because the multiplier-based mixers are uni-directional and cannot be shared between TX and RX, as shown in Fig. 1(a). Hence, separate antennas are used for TX and RX to avoid the large losses of the antenna switches, which usually exceed 4 dB at the 300-GHz band as reported in [43] and [44]. In this work, we adopt a bi-directional mixer architecture that makes it possible to share all the circuit components and antennas, reducing by that the area on-chip and off-chip, as shown in Fig. 1(b).

In the conventional phased-array systems operating below 100 GHz, the antennas are aligned in 2-D arrays with a $\lambda_0/2$ pitch. The arrays are also implemented using broadside antennas, so the chips are placed on the same plane as the array. However, at the 300-GHz band, the wavelength and the antenna pitch are smaller than the chip itself. Thus, to implement a 2-D TRX array, the RF lines on the printed circuit boards (PCB) must be relatively long to face the short pitch issue, as shown in Fig. 2(a). The long RF PCB lines result in large losses at high frequencies. The measured 1-cm line loss of a 50-μm-thick liquid crystal polymer (LCP) PCB at 30 GHz is around 0.5 dB, so by simple extrapolation, the best case loss at 300 GHz can be estimated to be around 5 dB/cm. Such loss will directly affect the link quality since it degrades the TX output power and the RX noise figure. On-chip arrays are possible for continuous-wave radiators [42], [45]–[49], but they become less feasible for wideband TRX systems where many additional components and circuits, such as modulators, buffers, and wideband amplifiers, are required. It is also very challenging to achieve good radiation efficiency using silicon on-chip antennas [50], [51]. Knowing that the thickness of the CMOS chip with the PCB can be less than λ_0 even at the 300-GHz band, this work adopts a stacked endfire 1-D antenna alignment instead of the horizontally adjacent configuration. The array elements here are aligned in a plane perpendicular to the chip plane. The antenna pitch in the stack is around 0.7–0.8 mm, which is close to $\lambda_0/2$ around the target frequency. The stacked arrangement used in this work is shown in Fig. 2(b). The number of stacked elements in this configuration is limited by the maximum thickness decided by the form factor and the target application.

This article describes the design details and measurements of a phased-array bi-directional 300-GHz-band TRX that utilizes outphasing with LOFT cancellation as its transmitting mode and the local oscillator (LO) emission cancellation for its receiving mode [52]. The Hartley architecture is also applicable as a separate receiving mode for high-power received image situations.

In Section II, the TRX architecture is discussed. Section III explains the design details of the 300-GHz-band TRX CMOS circuits. Section IV presents the implementation and the measured performance. Finally, Section V concludes this article.

II. 300-GHz-Band Bi-Directional TRX Design

Fig. 3 shows the block diagram of the 300-GHz-band CMOS TRX system. It consists of two mixing paths with a bi-directional subharmonic mixer and a bi-directional IF distributed amplifier forming each path. The LO chain includes three phase shifters to control the beam direction and the operation mode. It also includes frequency doublers and LO buffers to generate the required LO frequency. All the circuit components are shared between the TX and the RX. LOFT cancellation can be performed in both TX and RX modes, and image cancellation is also possible in the RX mode by applying a 90° phase shift externally. The applied LO frequency is 30 GHz, and it becomes 240 GHz at the RF end after frequency multiplication and subharmonic mixing. The RF channel is selected by adjusting the IF center frequency. The antennas are printed on PCBs and the connection with CMOS is designed using the flip-chip process to implement a four-element phased array. The bi-directional subharmonic mixer design and the operation of the TX mode and the RX mode are explained in this section.

A. Bi-Directional Subharmonic Mixer

There are two main issues that make it difficult to use the conventional simple single-transistor mixer shown in

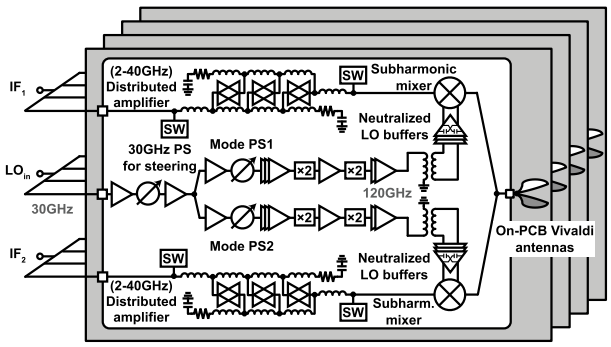


Fig. 3. Bi-directional 300-GHz-band phased-array TRX architecture.

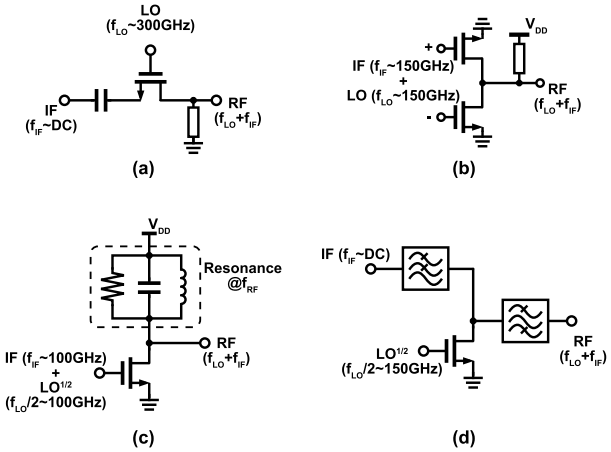


Fig. 4. Conventional 300=GHz-band CMOS mixers. (a) Single-transistor switching mixer, (b) square mixer, (c) transconductance mixer, and (d) resistive subharmonic mixer.

Fig. 4(a) or the double-balanced mixer at frequencies that exceed 200 GHz. The first issue is that getting good conversion gain and linearity requires high LO signal power to drive the mixer. However, the CMOS amplifiers cannot provide acceptable driving power at 300 GHz [28], [31]. The other issue is that the transistor parasitic capacitance results in small shunt impedance values at such high frequencies causing the conversion gain and the output power to degrade. These two issues were faced by introducing multiplier-based mixers where both the LO and the IF signals are applied to the same input port, as shown in Fig. 4(b) [30], [32]. The output power of these mixers is high enough to achieve reliable communication at the 300-GHz band, but the IF signal second harmonic appears in-band and the IF frequency is higher than 100 GHz. The operation of the mixer is uni-directional as well, so the circuit/antenna sharing between TX and RX is not possible.

To reduce both the IF and the LO frequencies, subharmonic mixing is a good choice. In this case, the LO frequency drops to half or lower depending on the harmonic used. As a result, frequencies around 100 GHz can be used while keeping the IF frequency at lower values [29], [33], [34]. Such a frequency plan is much more suitable for CMOS LO buffering. The transconductance mixer shown in Fig. 4(c) utilizes the third-order non-linearity of the transistor to extract the subharmonic

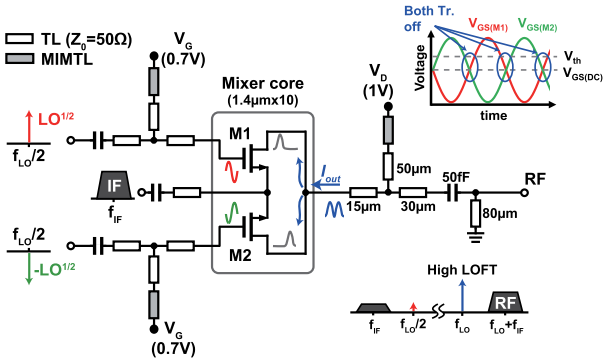


Fig. 5. Schematic and operation of the push–push subharmonic mixer.

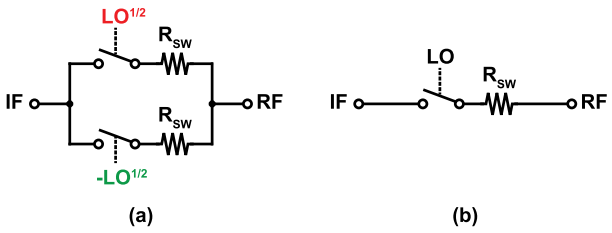


Fig. 6. (a) Switching operation of the proposed mixer and (b) equivalent circuit with second harmonic switching.

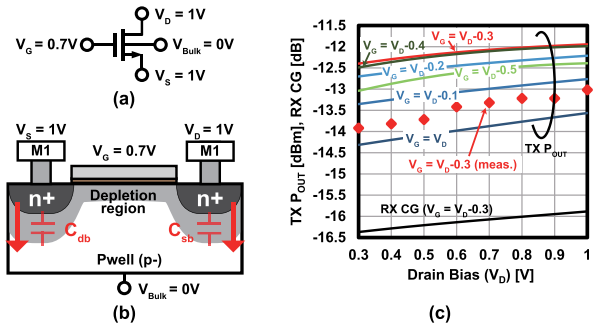


Fig. 7. (a) Proposed mixer biasing technique. (b) Transistor cross section and junction capacitance reduction. (c) Output power and conversion gain improvement due to the reduced junction capacitance.

mixing components at the output using matching or an *LC* tank. Both LO and IF are applied to the mixer gate, which means that the bi-directional operation is not possible. Many undesired harmonics also appear at the output affecting the linearity [29]. The resistive mixer shown in Fig. 4(d) can also be used for subharmonic mixing [53], but a wideband matching with high isolation is required to achieve the desired performance. The same issue can be found in the push–push doubler-based mixers introduced in [54] and [55].

In this work, we propose a switching subharmonic mixer to utilize a lower LO frequency while providing good conversion gain and output power. The design was briefly introduced in [33], and the same circuit is used here with some matching network optimization. In addition, the mixer supports a bi-directional operation in this work to enable antenna sharing. The proposed subharmonic mixer has the push–push frequency multiplier as a starting design point. The push–push doubler

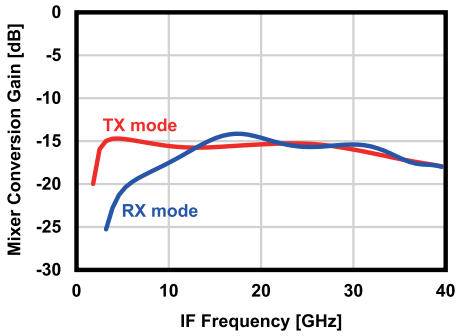


Fig. 8. Simulated mixer conversion gain against frequency.

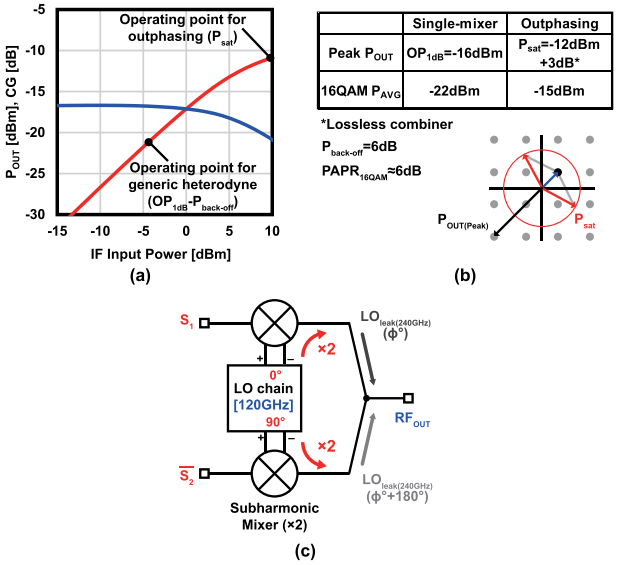


Fig. 9. (a) Mixer simulated linearity characteristics and operating point options (50-Ω input–output termination). (b) Improvement on average power by outphasing. (c) LOFT cancellation.

has two transistors with connected drains and sources, but the input is applied differentially to their gates similar to the circuit in Fig. 4(b). The output current of the push–push doubler has twice the frequency of the input signal. To provide a switching operation without cascoding transistors, a dc blocking capacitor is added to the source node and the IF signal is applied to the sources through that capacitor, as shown in Fig. 5. V_{GS} is set to a value that is smaller than the threshold voltage of the transistor. The source dc voltage is controlled by applying the desired voltage to the drain, as the high cycle of the LO signal passes the current that charges the dc blocking capacitor to the drain voltage level. The ac de-coupling is done by MIM transmission lines (MIMTLs) [56] to provide good RF–dc isolation while avoiding any undesired resonances. Having V_{GS} lower than the threshold will create some off periods in the current of the mixer [Fig. 6(a)], and this will result in a switching operation close to that of the fundamental mixer, but at twice the frequency of LO [Fig. 6(b)]. With a theoretical maximum conversion gain of $1/\pi^2$, higher conversion gain can be expected from this mixer compared to the resistive mixers [57], and the CMOS transconductance mixers depend on g_m of the transistor [58]. However, the usage of the source node limits the size of the transistors and the output power as a result. The outphasing technique explained in Section II-B is used to overcome this issue.

Another advantage of this design is that the IF and the LO ports in this mixer are separated, which means that the desired bi-directional operation is possible.

By increasing both the gate and the source voltage levels, the depletion region inside the CMOS transistor expands as the drain and the source voltage values are higher than the voltage of the grounded transistor body, as shown in Fig. 7(a) and (b). This will reduce the capacitance of the reverse-biased source–bulk and drain–bulk p/n junctions. As a result, the output power improves as shown by the simulation and measurement results at 256-GHz RF frequency in Fig. 7(c). Increasing the source–bulk voltage also affects the threshold voltage of the transistor due to the body effect. The simulated threshold voltage value is around 0.5 V when the source voltage is 1 V. The time interval in which the gate voltages of both transistors are equal is extremely short compared to the sinusoidal peak. Therefore, knowing that the LO voltage amplitude is around 1.2 V, the gates should be biased at around 0.7 V so that the threshold point ($V_G = 1.5$ V) is closer to the highest current point where one of the two transistors is fully ON ($v_g(t) = 1.9$ V and $v_{gs}(t) = 1.2$ V) than to the point when both transistors are OFF ($v_g(t) = 0.7$ V). The simulation results in Fig. 7(c) show that the best gate voltage is between 0.3 and 0.4 V below the drain voltage. The 1.5-V peak source–bulk voltage in this configuration is still far below the p-n junction breakdown voltage of the 65-nm CMOS process [59]. The simulated conversion gain of the mixer after matching is shown in Fig. 8. The gain difference at low frequencies is due to the slightly degraded matching at that band since the matching with the IF amplifier is also considered.

B. TX Mode Operation

The outphasing technique is usually applied to power amplifier systems to improve their efficiency by driving the amplifier at higher output power levels [60]–[62]. It was also used with frequency multipliers to provide higher efficiency as in [35]. In our design, we adopt the outphasing architecture using the passive subharmonic mixers to improve the average output power of the TX at the 300-GHz band. The outphasing technique is one of the most suitable options to leverage the mixer saturated power to the maximum, as applying the constant envelope signal to the mixer means that the mixer can be driven at its saturated output power. Doing that improves the average power of the TX by several decibels compared to the single mixer case, as shown in Fig. 9(a) and (b). The 6-dB back-off, or the PAPR of the modulation scheme in the outphasing case, is taken from the mixer saturated power instead of its 1-dB compression point. A T-junction is utilized in this work to combine the two outphasing signals so that the RF losses are reduced as much as possible.

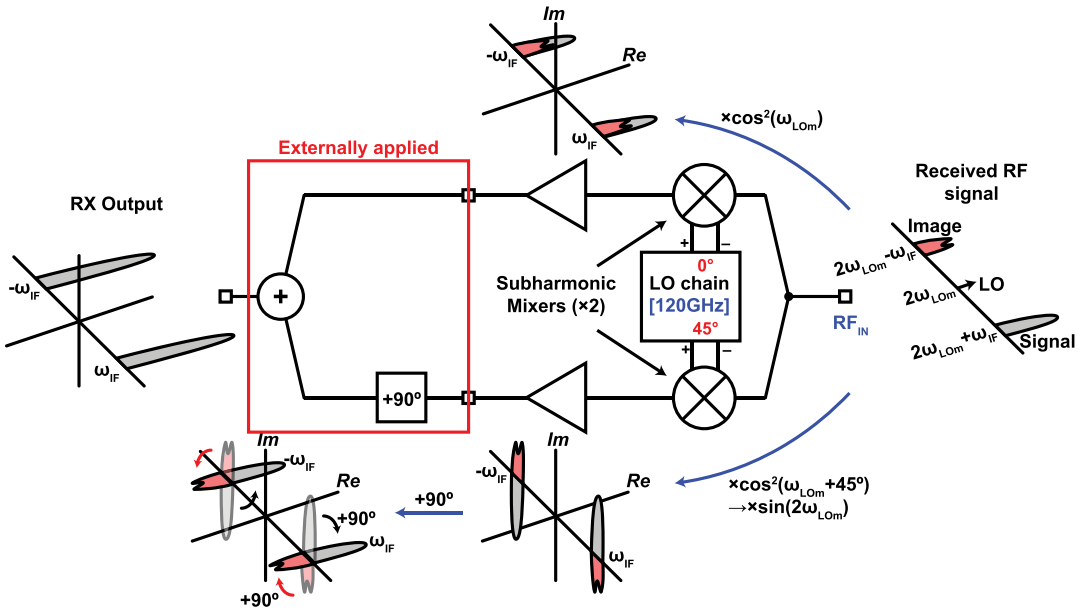


Fig. 10. Operation of the Hartley receiving mode.

The TX modeoperation is explained in Fig. 9(c). The input constant envelope signals can be expressed as follows [35], [60]:

$$S_1(t) = \frac{A_M}{2}\cos(\omega_{\rm IF}t + \theta + \phi) \tag{1}$$

$$S_2(t) = \frac{A_M}{2}\cos(\omega_{\rm IF}t + \theta - \phi) \tag{2}$$

where $S_1(t)$ and $S_2(t)$ are the input outphasing signals, $\omega_{\rm IF}$ is the IF angular frequency, θ is the modulated phase, and ϕ is the outphasing angle. Both of these signals are upconverted using the subharmonic mixers with a relatively high LOFT. The second-order non-linearity of the subharmonic mixers converts the applied LO signal with an angular frequency of $\omega_{{\rm LO}m}$ and two additional phase shifts (ζ for beamforming and ξ for mode selection) as follows:

$$\begin{aligned}{\rm LO}(t,\xi) &= \left(A_{{\rm LO}m}\cos(\omega_{{\rm LO}m}t + \zeta + \xi)\right)^2 \\ &= \frac{A_{{\rm LO}m}^2}{2}\left(1 - \cos\left(2\omega_{{\rm LO}m}t + 2\zeta + 2\xi\right)\right) \\ &= \frac{A_{{\rm LO}m}^2}{2}\left(1 - \cos\left(\omega_{\rm LO}t + 2\zeta + 2\xi\right)\right)\end{aligned} \tag{3}$$

and it can be observed that the system LO frequency becomes $\omega_{\rm LO} = 2\ \omega_{{\rm LO}m}$ as the dc component can be ignored due to the presence of the biasing signals. Also, the previously applied phase shifts double providing wider phase range. To cancel the LOFT at the TX mode, the phase ξ is set to 0° in one outphasing path and to 90° in the other path. The phase of the second outphasing input $S_2(t)$ is inverted to recover the phase of the desired signal. The resulting output at the combining node from the first path can be calculated as follows:

$$\begin{aligned}S_1(t){\rm LO}(t,0^\circ) = \frac{A_M}{2}&\cos(\omega_{\rm IF}t + \theta + \phi) \\ &\cdot\frac{A_{\rm LO}^2}{2}\cos(\omega_{\rm LO}t + 2\zeta)\end{aligned} \tag{4}$$

$$\overline{\rm LO_{Leak}}(t,0^\circ) = \frac{\alpha A_{\rm LO}^2}{2}\cos(\omega_{\rm LO}t + 2\zeta) \tag{5}$$

and the calculated output of the second path is

$$\begin{aligned}\overline{S_2(t)}{\rm LO}(t,90^\circ) = \frac{A_M}{2}&\cos(\omega_{\rm IF}t + \theta - \phi + 180^\circ) \\ &\cdot\frac{A_{\rm LO}^2}{2}\cos(\omega_{\rm LO}t + 2\zeta + 180^\circ)\end{aligned} \tag{6}$$

$$\overline{\rm LO_{Leak}}(t,90^\circ) = \frac{\alpha A_{\rm LO}^2}{2}\cos(\omega_{\rm LO}t + 2\zeta + 180^\circ). \tag{7}$$

The TX output is calculated by adding all the mixing and the leak components together

$$\begin{aligned}{\rm RF_{OUT}} = S_1(t){\rm LO}(t,0^\circ) + \overline{S_2(t)}{\rm LO}(t,90^\circ) \\ + \overline{\rm LO_{Leak}}(t,0^\circ) + \overline{\rm LO_{Leak}}(t,90^\circ).\end{aligned} \tag{8}$$

The leak components cancel each other out and the final output formula of the desired RF output signal (excluding the image components) is given as follows:

$$\begin{aligned}{\rm RF_{OUT}} = \frac{A_M A_{\rm LO}^2}{8}\Big(&\cos\left((\omega_{\rm LO} + \omega_{\rm IF})t + 2\zeta + \theta + \phi\right) \\ &+ \cos\left((\omega_{\rm LO} + \omega_{\rm IF})t + 2\zeta + \theta - \phi\right)\Big).\end{aligned} \tag{9}$$

The LOFT is completely canceled by applying a 90° phase difference between the LO signals of the two outphasing paths without affecting the desired RF signal by using the proposed technique. The phase of the output signal is twice that of the input LO signal reducing the phase range requirements of the phase shifters. The same operation is used at the RX mode by inverting one of the output IF signals before combining them.

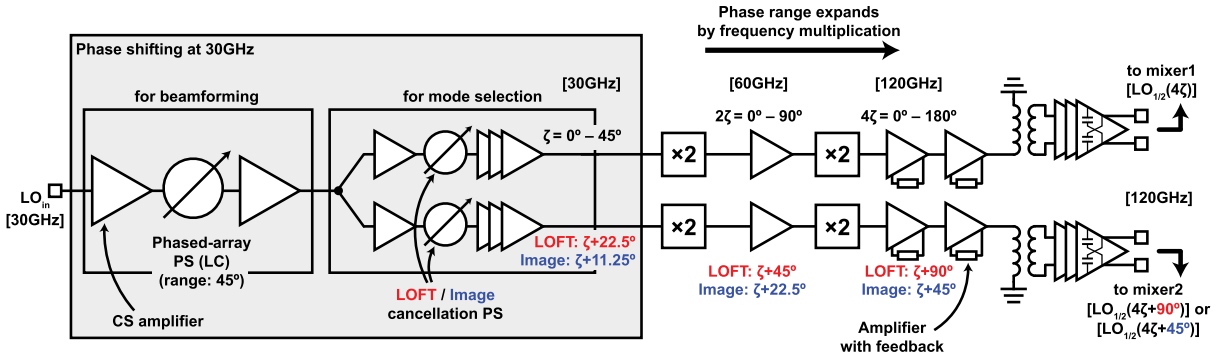


Fig. 11. LO chain block diagram.

C. RX Mode Operation

The RX can be operated at two different modes depending on the desired characteristics. First, the LO emission cancellation mode mentioned in Section II-B is used when the image signal is suppressed by the bandpass characteristics of the antenna. The other mode is for high received image power situation as the Hartley architecture can be applied. Fig. 10 shows the Hartley operation of the RX. A 45° phase difference is applied to the LO inputs of the two mixers and is translated to 90° between the IF outputs

$$\mathrm{RF}(t)\mathrm{LO}(t,45^\circ) = \frac{A_{\mathrm{RF}}}{2}\cos(\omega_{\mathrm{RF}}t) \cdot \frac{A_{\mathrm{LO}}^2}{2}\cos\left(\omega_{\mathrm{LO}}t + 2\zeta + 90^\circ\right). \quad (10)$$

An additional 90° phase shift is applied externally to completely cancel the image signal while combining the desired signal.

III. Circuit Implementation for IF and LO

After implementing the bi-directional sub-harmonic mixer circuit, the main focus of this work is on achieving bi-directional amplification using the IF amplifier and flexible phase generation for beamforming and LOFT cancellation. The detailed LO chain and IF amplifier circuit implementation of the proposed TRX chip will be introduced in the remaining part of this section.

A. LO Chain (Phase Shifters and LO Buffers)

Fig. 11 shows the LO chain design details. The phase shifting is done mainly at the input LO frequency at 30 GHz. One phase shifter is used for beamforming, and two more phase shifters are used for LOFT and image cancellation. The frequency multiplier chain up-converts the LO frequency to 120 GHz and quadruples the phase range. The outputs of the two phase shifting paths are applied to baluns to generate the differential LO inputs of the mixers. The required phase resolution at the output for an array factor degradation of around 0.05 dB is approximately 11.05° at the RF frequency [63], so a 1.38° maximum resolution is allowed at 30 GHz considering the multiplication factor of the LO chain and the subharmonic mixing.

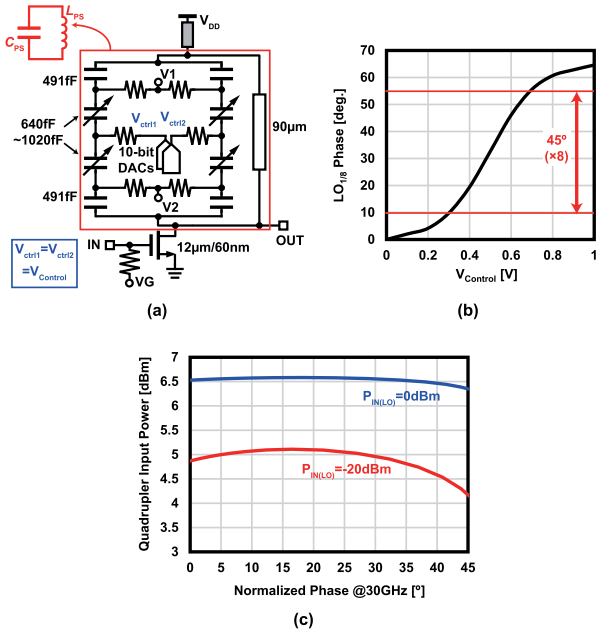


Fig. 12. Phase shifter core: (a) schematic and (b) measured phase range. (c) Simulated power variation against phase at the 30-GHz LO buffer output.

Fig. 12(a) shows the circuit schematic of the 30-GHz phase shifter. A varactor/transmission line combination is used as a load of a common-source stage to generate the required phase shift. Based on a small-signal analysis, the voltage gain of the phase shifter is

$$A_v = g_m \frac{j\omega_{\mathrm{LOin}}(1/C_{\mathrm{PS}})}{1/L_{\mathrm{PS}}C_{\mathrm{PS}} - \omega_{\mathrm{LOin}}^2 + j\omega_{\mathrm{LOin}}(1/r_0C_{\mathrm{PS}})} \quad (11)$$

where C_{PS} and L_{PS} are the capacitance and the inductance at the drain of the transistor, respectively. The phase shift is calculated as follows:

$$\phi = \tan^{-1}\left(\frac{r_0}{\omega_{\mathrm{LOin}}L_{\mathrm{PS}}} - \omega_{\mathrm{LOin}}C_{\mathrm{PS}}r_0\right). \quad (12)$$

Thus, the value of C_{PS}, which is directly related to the varactor capacitance value, controls the phase of the output signal. The varactor utilizes a parallel combination to extend the tuning range so that the required phase range is covered. In addition, the voltage values of $V1$ and $V2$ are optimized to achieve wide

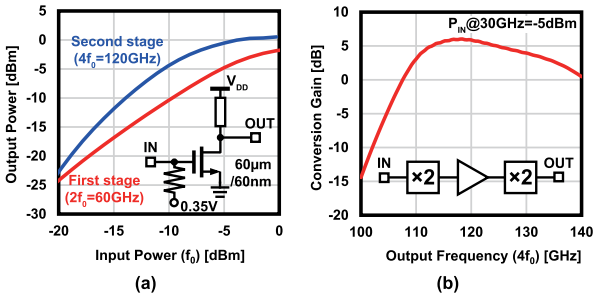


Fig. 13. (a) Frequency doubler schematic and simulated output power. (b) Simulated conversion gain of the quadrupler chain.

and the linear characteristics in the target range. The varactor control voltage is generated using a 10-bit digital-to-analog (DAC) as in [64]. Fig. 12(b) shows the measured phase range at 30 GHz by sweeping the control voltage. The required 45° is totally covered by around 400 DAC steps, so the estimated phase resolution is around 0.1125° (0.9° at 240 GHz). The maximum resolution in the middle of the curve is around 0.13° at 30 GHz (1.04° at 240 GHz). This resolution is much smaller than the required one for beamforming, and it is suitable for the fine-tuning of the LOFT cancellation signals. Hence, the same circuit is used to implement the three phase shifters of the LO chain.

Buffering stages are added after each phase shifter to reduce the output power variation caused by the phase change. The output stage buffers must be saturated so that input power changes caused by the phase shifting do not significantly affect the output power. Fig. 12(c) shows the power variation at the input of the quadrupler at two different LO input power values. It can be observed that the power variation is reduced when the last-stage buffer is saturated.

The frequency doublers are based on the CMOS device non-linearity by biasing it around its threshold voltage

$$i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + \ldots. \tag{13}$$

This circuit is quite simple and it has a good output power as shown by the simulation results in Fig. 13(a). Both the first stage (30–60 GHz) and the second stage (60–120 GHz) provide more than −5-dBm output power. The simulated conversion gain after adding a buffering stage between the two doublers is shown in Fig. 13(b). The doublers also multiply the phase of their input signals by two as the subharmonic mixer does in (3). The 45° coverage of the phase shifter at 30 GHz is translated to 360° at 240 GHz at the output after the frequency multipliers and the subharmonic mixer.

The 120-GHz LO buffers are divided into two parts: the single-ended stages and the differential stages. Amplification at 120 GHz using CMOS is not straightforward as that frequency is pretty close to $f_{max}/2$. The single-ended stages are designed to fulfill the conditions of the maximum achievable gain [23], [24], [65], [66], as shown in Fig. 14(a). The passive feedback is formed using transmission lines to increase the total gain. The target optimal voltage gain and phase of the transistor calculated using the transistor's Y-parameters to

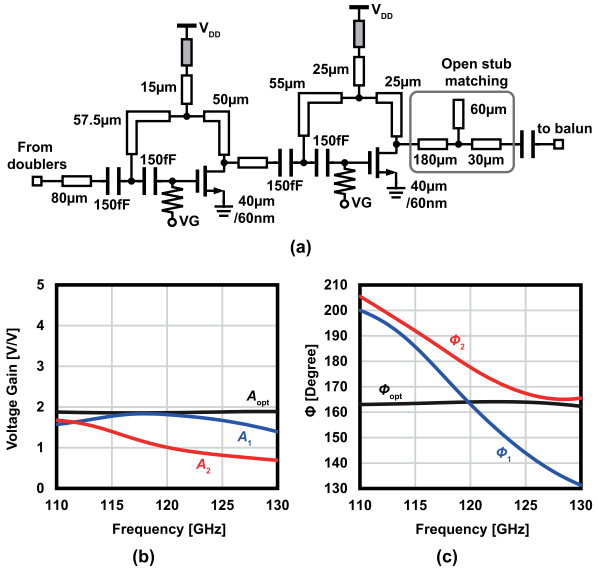


Fig. 14. (a) Schematic of the two-stage 120-GHz single-ended LO Buffer using the maximum achievable gain. (b) Simulated transistor gain compared to the optimal value (A_1: first-stage gain). (c) Simulated transistor phases.

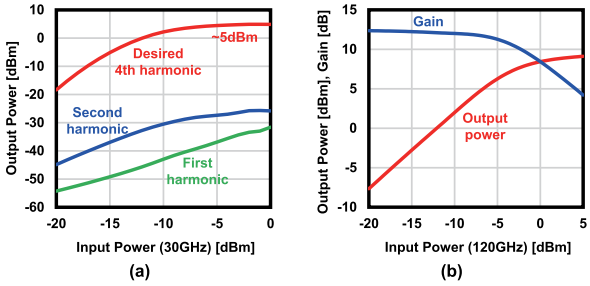


Fig. 15. (a) Simulated output power of the single-ended LO chain (balun input). (b) Differential neutralized LO buffer chain output power characteristics (mixer LO input power).

obtain the maximum achievable gain are [65]

$$A_{opt} = \frac{|Y_{12} + Y_{21}^*|}{2G_{22}} \tag{14}$$

$$\Phi_{opt} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^*). \tag{15}$$

The simulated transistor conditions for both single-ended stages are shown in Fig. 14(b) and (c). The simulated conditions are close enough to the optimal values. The slight difference between the optimal and the simulated results of the second stage is due to the consideration of other matching and stability requirements. The 150-fF capacitors are used to separate the dc gate bias voltage from the supply voltage, and their effect on the transistor gain and phase conditions is also considered. Transmission lines are used for inter-stage matching to save the area, and an open stub is used to match the inductive impedance of the balun at the output. Fig. 15(a) shows the simulated power provided by the single-ended doublers and the buffer chain to the balun input. Around 5-dBm LO signal power and more than 30-dB suppression of the other harmonics are achieved.

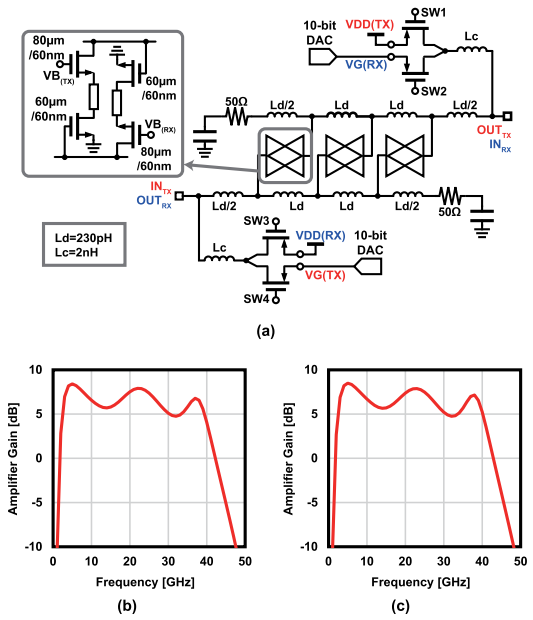


Fig. 16. (a) Bi-directional distributed variable-gain IF amplifier schematic. (b) TX mode gain. (c) RX mode gain.

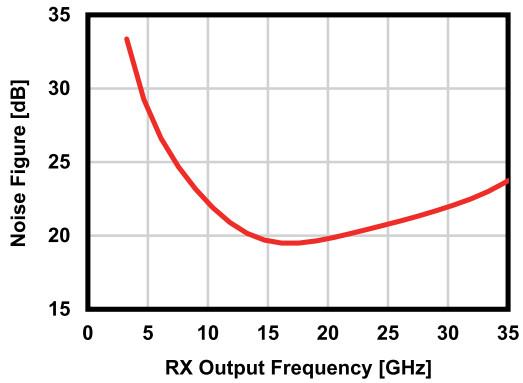


Fig. 17. RX mode simulated noise figure.

The differential part consists of neutralized common-source amplifiers. Cross-coupled capacitors are used for neutralization. The simulated input–output power characteristics of the differential amplifiers are shown in Fig. 15(b). The maximum achieved power is around 9 dBm, but since the highest balun output is around 2.5 dBm due to its 2.5-dB loss, the maximum simulated LO power is around 8.7 dBm and it is applied directly to the mixer.

B. IF Bi-Directional Distributed Amplifier

To achieve the full bi-directional operation, the IF amplifiers must also have a bi-directional structure. Knowing that the mixer bandwidth is very wide, the system bandwidth is decided by the bandwidth of the IF amplifiers. The amplifier is also supposed to have a controllable gain to provide the ability of mismatch compensation as the mismatch between the two outphasing paths in TX or the two Hartley paths in RX causes serious degradation on the error vector magnitude (EVM) of the system.

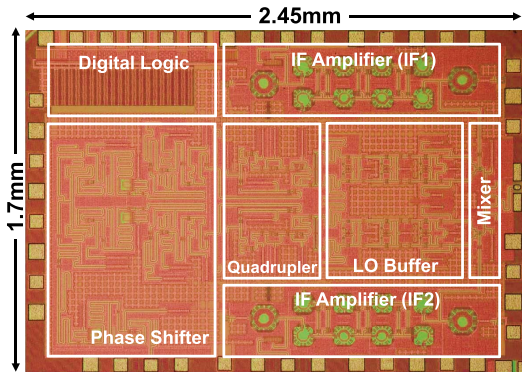


Fig. 18. Die micrograph.

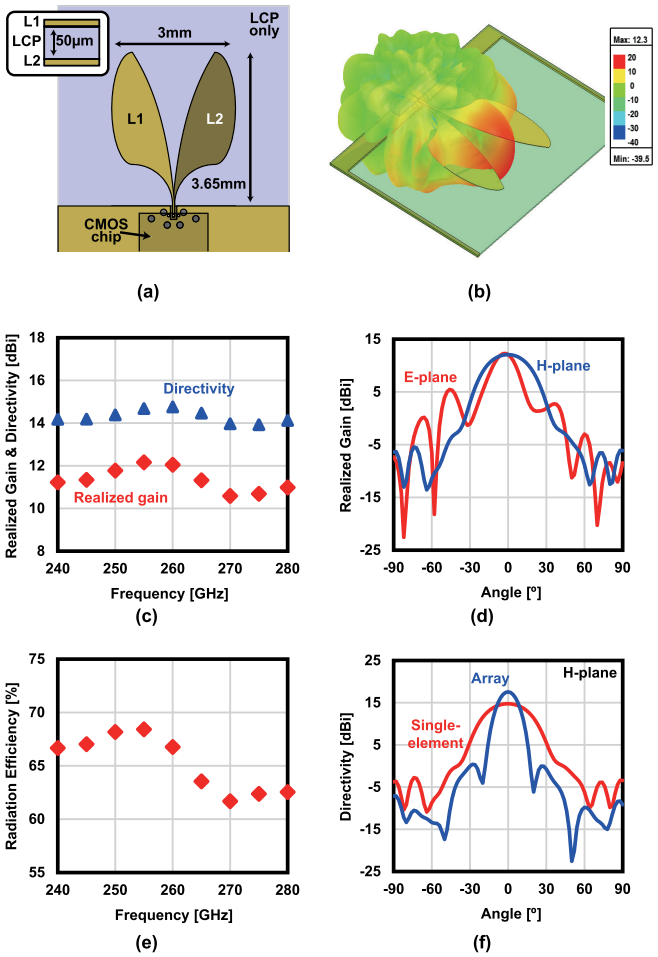


Fig. 19. Vivaldi antenna: (a) design, (b) simulated pattern, (c) simulated realized gain (including the connection to CMOS) and directivity, (d) simulated radiation pattern for *E*-plane and *H*-plane (260 GHz), (e) simulated efficiency, and (f) single-element versus array simulated directivity.

In this work, the distributed amplifier circuit is adopted to provide wide bandwidth operation at low frequencies. Three cascode stages are used with a bi-directional structure [67] to provide several decibels' gain to the TX and the RX paths. The operation mode (TX or RX) is selected by controlling the switches SW1–4 and the biases of the cascode transistors. The

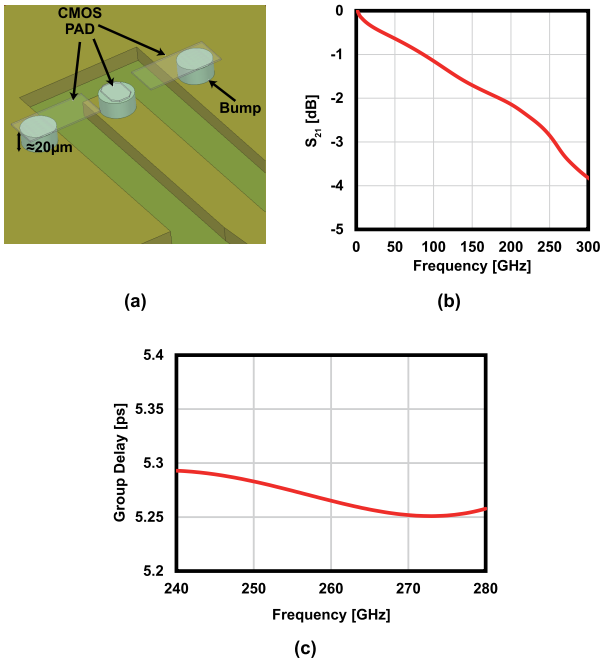


Fig. 20. Bump connection between the CMOS and the LCP PCB. (a) Model, (b) simulated loss, and (c) simulated group delay across the RF bandwidth.

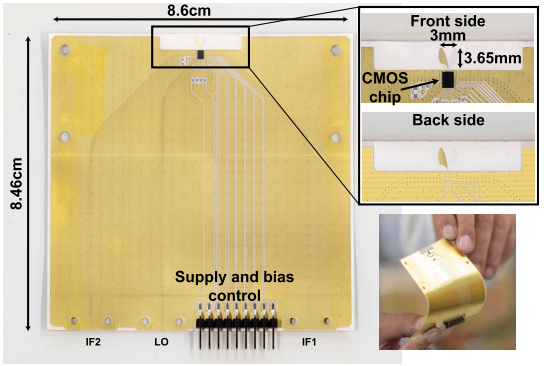


Fig. 21. Photographs of the PCBs used for phased-array implementation.

schematic of the bi-directional distributed amplifier is shown in Fig. 16(a). The simulated amplifier gain values at the TX mode and the RX mode are shown in Fig. 16(b) and (c). The gain of the amplifier can be controlled by adjusting the bias voltage of the transistors using DACs to make sure that the outphasing signals amplitudes are equal in the TX case and the image signal amplitudes are equal in the RX Hartley case.

The simulated overall RX noise figure including the distributed amplifiers is shown in Fig. 17. The noise figure is below 25 dB for most of the target band.

IV. PCB Implementation for Phased-Array

The proposed 300-GHz-band TRX chip is fabricated in a 65-nm CMOS process. Fig. 18 shows the chip micrograph. The chip size is 2.45 mm × 1.7 mm.

An on-PCB Vivaldi antenna is used to build the phased array. The designed Vivaldi antenna is shown in Fig. 19(a). The Vivaldi antenna was chosen due to its endfire radiation pattern

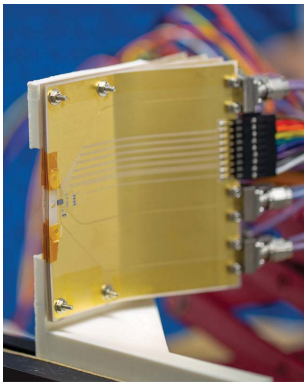


Fig. 22. Photograph of the implemented four-element phased array.

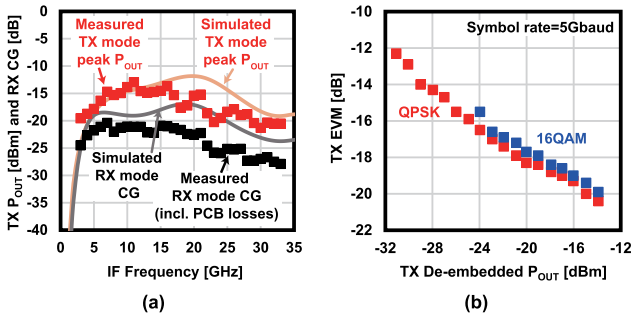


Fig. 23. (a) Measured TX mode output power and RX mode conversion gain. (b) Measured TX EVM.

and wide bandwidth characteristics. However, the material for the 300-GHz-band Vivaldi antenna must be carefully chosen to avoid the breaking up of the main beam, by fulfilling the optimal value of the effective substrate thickness normalized to the free-space wavelength that is between 0.005 and 0.03 [68] and defined by

$$\frac{t_{\text{eff}}}{\lambda_0} = \left(\sqrt{\varepsilon_r - 1}\right)\frac{t}{\lambda_0} \tag{16}$$

where t is the substrate thickness.

From (16), it can be observed that the thickness and permittivity requirements become more severe as the frequency increases. The LCP material is used to fabricate the PCB in this work to take advantage of its thin substrate (50 μm), low permittivity ($\varepsilon_r = 3$), and flexible characteristics as will be explained later in this section. The 3-D radiation pattern of the antenna is shown in Fig. 19(b). The bandwidth of the Vivaldi antenna covers the whole band with more than 10-dBi gain, as shown in Fig. 19(c). The simulated E-plane and H-plane radiation patterns are shown in Fig 19(d). Fig. 19(e) shows the simulated radiation efficiency, including the connection to the CMOS chip. The main limitation of the efficiency is the degraded matching due to the PCB design rules. The overall array directivity is simulated and compared to the single-element directivity in Fig. 19(f). The coupling between the adjacent elements causes a slight degradation in the gain of each element, and hence, the array gain is several decibels lower than the ideal theoretical value.

The CMOS-to-antenna flip-chip connection must also be designed very carefully to avoid large losses in the RF band. The CMOS signal pad size was chosen to be as small as possible. The dimensions are 25 μm $\times$ 35 μm. Such a small pad has less capacitance and less reflection as its impedance is close to 50 Ω. However, some difficulties may appear in the implementation as the pad is slightly smaller than the connecting bump. The bump position and PCB variations also cause phase offsets between the elements, so the output phase of each element must be adjusted manually. A calibration system can be considered as proposed by several works for lower frequency bands [69], [70], but it is beyond the scope of this work. The 3-D model of the CMOS pads and bumps is shown in Fig. 20(a). The simulated loss, including CMOS and PCB connecting transmission lines, is around 3 dB at the band of interest as shown in Fig. 20(b), and Fig. 20(c) shows the simulated group delay across the target RF bandwidth.

The detailed photographs of the flexible 50-μm LCP PCB are shown in Fig. 21. The implemented four-element phased-array photograph is shown in Fig. 22. In the part surrounding the antennas, 0.5-mm spacers are used to provide enough room for the 0.3-mm-thick CMOS chips. By adding the 0.25-mm PCB thickness, the total spacing between every two elements is around 0.75 mm. The spacing can be further reduced to reach $\lambda_0/2$ by thinning the CMOS chip and using shorter spacers.

The IF signals are applied through V-band connectors to each PCB using external dividers. The antenna pitch is much smaller than the V-band connector size, so a flexible part of the LCP PCB is slightly bent to fit the connectors. Such implementation could cause group delay variation across the IF bandwidth for wideband operation, but such variation can be compensated using equalization as in [71].

V. Measurement

The on-wafer characteristics are evaluated first by implementing a PCB with wire-bonding connections to the CMOS chip except for the RF port. The RF port is connected to the measurement equipment using a waveguide probe with known loss. Fig. 23 summarizes the measured characteristics of the TRX chip and compares it to the simulated results. An estimated bonding wire inductance of 1 nH is considered at the IF ports in the simulations. Fig. 23(a) shows the measured maximum output power of the TX mode over the whole frequency band. The TX output was down-converted by an external mixer, and the losses were de-embedded. The output power is not high compared to the other works due to the bi-directional design of the mixer, but using the outphasing means that the average power is closer to P_{sat}. The RX conversion gain is also shown in Fig. 23(a), including the bonding wires and the PCB losses at the IF side. Fig. 23(b) shows the TX EVM for different output power situations at a 5-GBd symbol rate. Due to the outphasing technique, the third-order intermodulation product (IM3) effect on the EVM is not observed as the EVM saturates with the output power.

The LOFT cancellation was also tested for both the TX mode and the RX mode (LO emission cancellation). Fig. 24(a)

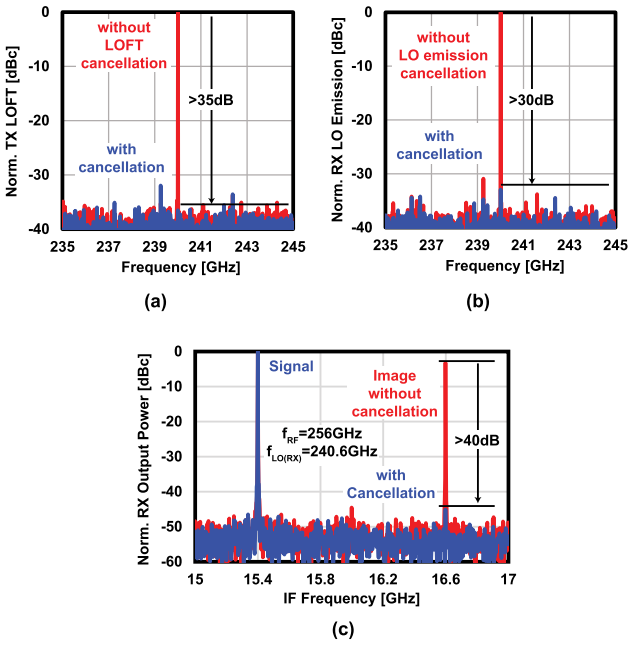


Fig. 24. Measured LOFT cancellation in (a) TX mode and (b) RX LO emission rejection mode. (c) Measured image rejection of RX Hartley mode.

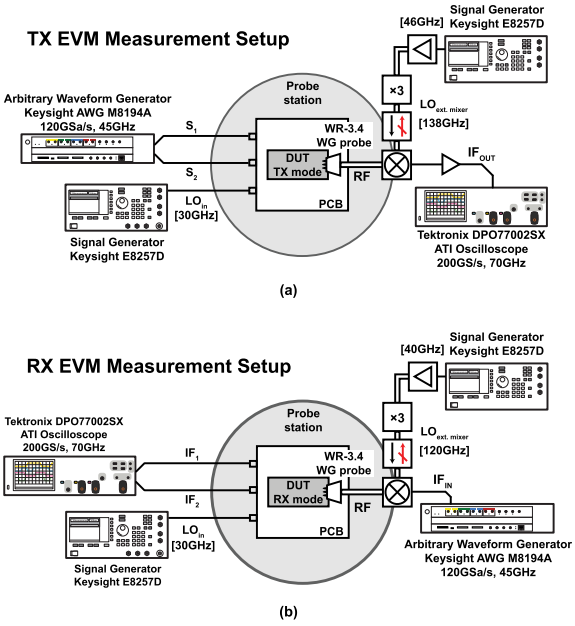
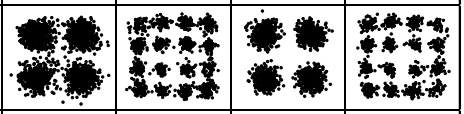
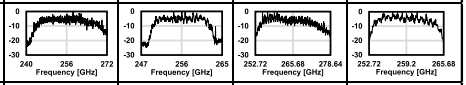
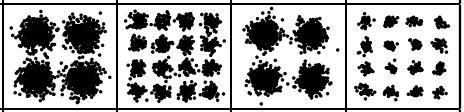


Fig. 25. Measurement setup for (a) TX mode and (b) RX mode EVM.

shows the TX mode LOFT cancellation. More than 35-dB cancellation is possible by using the proposed technique with the fine resolution of the phase shifter. The LO emission cancellation of the RX mode is shown in Fig. 24(b) with more than 30-dB suppression as well. The Hartley RX mode was tested by down-converting a double-sideband (DSB) signal provided by an external mixer using a slightly shifted LO frequency. The external mixer up-converts a 16-GHz signal using an LO frequency of 240 GHz to generate two sidebands at 224 and 256 GHz. The RX chip LO frequency is set to

TX mode				
	Maximum data rate conditions		IEEE802.15.3d channels	
Channel ID	N/A	N/A	Ch. 66	Ch. 57
Modulation	QPSK	16QAM	QPSK	16QAM
f_{center} [GHz]	256	256	265.68	259.2
Symbol rate [Gbaud]	26	12	21.12	10.56
Data rate [Gb/s]	52	48	42.24	42.24
TX down converted constellation				
TX spectrum				
TX EVM [dB]	-9.8	-16.6	-11.5	-16.8

(a)

RX mode				
	Maximum data rate conditions		IEEE802.15.3d channels	
Channel ID	N/A	N/A	Ch. 57	Ch. 2
Modulation	QPSK	16QAM	QPSK	16QAM
f_{center} [GHz]	256	256	259.2	255.96
Symbol rate [Gbaud]	18	3	10.56	1.76
Data rate [Gb/s]	36	12	21.12	7.04
RX down converted constellation				
RX EVM [dB]	-10.1	-16.8	-10.8	-17.1

(b)

Fig. 26. Measured EVM and constellations of (a) TX mode and (b) RX mode.

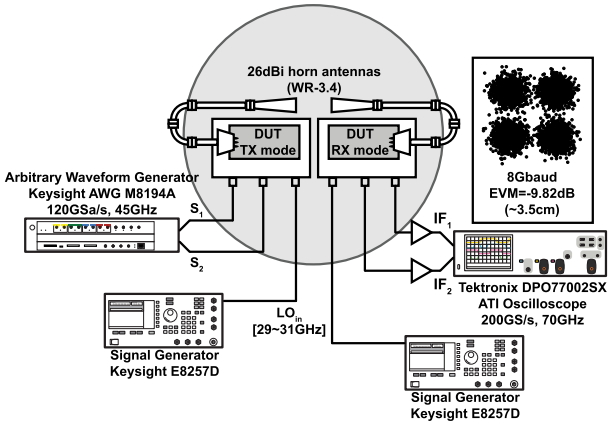
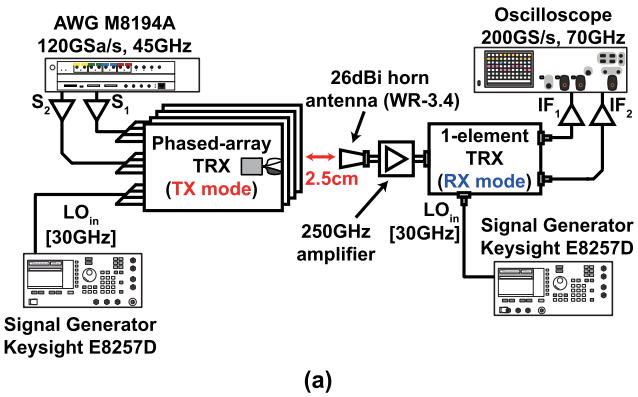
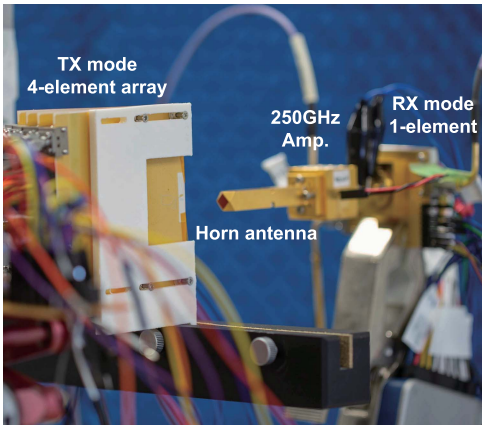


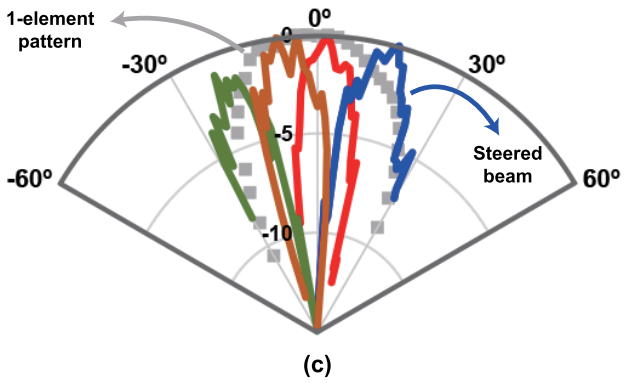
Fig. 27. Measurement setup of OTA measurement.



(a)



(b)



(c)

Fig. 28. Array pattern measurement setup: (a) block diagram and (b) photograph. (c) Measured steered beam pattern.

240.6 GHz to down-convert the desired signal and the image at two different frequencies (the desired signal at 15.4 GHz and the image at 16.6 GHz). Both IF output signals are applied to an oscilloscope. The 90° phase shift at the IF is applied using the oscilloscope as well in the digital domain. The image rejection measurement results are shown in Fig. 24(c). More than 40-dB image rejection is achieved at a single frequency for the worst case situation where the signal power is equal to the image power. The estimated RX input power after considering the probe loss is around −30 dBm, which is way lower than the 10-dBm simulated RX input 1-dB compression point. Such high compression point power value is caused by the power divider loss at the input. The amplitude and phase optimization in this measurement was performed using the on-chip phase shifters and the amplifier bias voltages.

Fig. 25 shows the setup used to evaluate the TX mode and the RX mode EVM separately while probing the RF signal. The PCB previously mentioned in this section was placed on a probe station with all the IF and LO connections provided using wire bonding. For the TX mode EVM measurement, the outphasing signals are generated using the Keysight arbitrary waveform generator (AWG) M8194A. The AWG generates the two single-sideband (SSB) IF signals while providing the required 180° phase shift between them. A roll-off factor of 0.25 is used in all the EVM measurements. The measurement

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART 300-GHz-BAND TRXs

	Process	**Freq. [GHz]**	**Structure**	**Antenna sharing**	**TX topology**	**Max. baud rate [Gbaud]**	P_{DC}**[W]**	**Area [mm^2]**
IMS '20 [16]	130nm SiGe	240	Single-element	No	Single-stream / power amplifier	25 (16QAM)	TX:1.24 RX:0.85	TX:7 RX:5.1
MWCL '19 [14]	130nm SiGe	230	Single-element	No	Single-stream / power amplifier	23.75 (16QAM)	TX:0.96 RX:0.45	TX:1.5 RX:1.25
JSSC '20 [3]	80nm InP-HEMT	290	Single-element	No	Single-stream / power amplifier	30 (16QAM)	TX:4.5* RX:4.5*	TX:2.44 RX:2.44
JSSC '15 [27], [28]	65nm CMOS	240	Single-element	No	Single-stream / tripler-last	TX:8 (QPSK) RX:8 (QPSK)	TX:0.22 RX:0.26	TX:2 RX:2
ISSCC '17 [30] & IMS '17 [31]	40nm CMOS	290	Single-element	No	Power combining	TX:21 (32QAM) RX:14 (QPSK)	TX:1.4 RX:0.65	TX:5.19 RX:3.15
JSSC '19 [32]	40nm CMOS	266	Single-element	No	Power combining	20 (16QAM) TX:28 (16QAM) RX:N/A	TX:0.89 RX:0.9	TRX:11
IMS '20 [33]	65nm CMOS	288	Single-element	No	Single-stream / mixer-last	17 (QPSK)	TX:0.27 RX:0.14	TX:1.9 RX:1.9
JSSC '14 [26]	32nm SOI CMOS	210	Combining-array	No	Single-stream / PA-last	Not measured#	TX:0.24 RX:0.07	TX:3.5% RX:1.1
This Work	65nm CMOS	256	**Phased-array$ / bi-directional**	**Yes**	Outphasing	8 (QPSK) TX:26 (QPSK)† RX:18 (QPSK)†	TX:0.75 RX:0.75	**TRX:4.17**

* Without LO multiplier. $ Only CW performance tested. † Direct connection to waveguide. # Only OOK. % Four elements total area.

channel is selected using the AWG by adjusting the center frequency of the IF signal while keeping the LO frequency fixed. The TX output signal is applied to an external subharmonic mixer through a waveguide probe. The LO of the external mixer is set at a higher frequency (138 GHz $\times 2 =$ 276 GHz) to avoid down-converting the image signal to the target IF frequency. The 138-GHz signal is generated using a signal generator and a tripler. The down-converted signal is amplified and observed using the Tektronix DPO77002SX oscilloscope. The TX mode setup is shown in Fig. 25(a).

The RX mode measurement setup is shown in Fig. 25(b). This time, the RF input signal is generated externally using the subharmonic external mixer with a 120 GHz $\times 2 =$ 240 GHz LO frequency. The image signal appears in-band in this measurement, so the image rejection can also be tested. The IF outputs are then observed using the oscilloscope. The 90° phase shift and signal combining are performed using the oscilloscope as well.

Fig. 26(a) summarizes the TX mode EVM performance for several situations. The maximum baud rate achieved is 26 GBd using QPSK with an EVM of about -9.8 dB. The center frequency of the IF, in this case, is 16 GHz since higher frequencies suffer from low IF amplifier gain and high bonding wire losses. The corresponding TX mode maximum data rate is 52 Gb/s. It can be observed from the TX spectrum that the low-frequency part of the data is suppressed by the TX bandwidth characteristics, causing a slight degradation of the EVM. The wide total bandwidth also causes some folding below 1 GHz, but the folded components are also suppressed by the TX characteristics. Since the peak output power conditions are considered here, the estimated average output power is around -16 dBm. Using the same IF center frequency and a narrower bandwidth, 16 QAM modulation scheme is also achieved. The maximum symbol rate that satisfies the 16 QAM required EVM is 12 GBd (48 Gb/s). The IEEE 802.15.3d channels were also evaluated and Fig. 26(a) shows the results of two channels. Ch. 66, which has a wide bandwidth of 25.92 GHz, can provide a symbol rate of 21.12 GBd considering the 0.25 roll-off factor. The EVM achieved using this channel is around -11.5 dB, which means that the QPSK modulation is usable with a 42.24-Gb/s data rate. Ch. 57 has a narrower bandwidth of 12.96 GHz, and the EVM achieved that there is -16.8 dB, so the 16 QAM is used to obtain a data rate of 42.24 Gb/s.

The RX mode EVM performance is summarized in Fig. 26(b). The maximum baud rate achieved is 18 GBd with a -10.1-dB EVM at an RF center frequency of 256 GHz. The maximum data rate achieved by the RX is 36 Gb/s. From the mentioned results, it can be observed that the RX performance is limited compared to the TX since the RX does not benefit from the outphasing technique. The Hartley mode narrow bandwidth and the limited output power of the external mixer also cause the RX measured performance to be lower than that of the TX. The 16 QAM modulation is also achieved at the same RF center frequency with a 3-GBd symbol rate (12 Gb/s). The results of IEEE 802.15.3d ch. 57 and ch. 2 are also shown; 21.12 Gb/s is achieved in ch. 57 using the QPSK modulation, and 7.04 Gb/s is achieved using the 16 QAM in ch. 2.

To evaluate the over-the-air (OTA) performance of a single-element-to-single-element case, two TRXs were placed on the probe station, as shown in Fig. 27. The outphasing signals with opposite phases are applied to the input of the first TRX, which operates at the TX mode. The 300-GHz-band signal is applied to the input of a 26-dBi horn antenna using

waveguide bends and a waveguide probe. The U-like shape makes it possible to align the antennas as the same connection is used for the second TRX, which operates at the RX mode. The output of the RX is observed by the oscilloscope where the 90° phase shift and the combining take place. Different signal generators are used for the TX and RX to calibrate the image cancellation by shifting the down-conversion frequency. The maximum data rate achieved over an estimated distance of 3.5 cm between the phase centers of the horn antennas is 16 Gb/s. The TX-to-RX performance is limited compared to that of separate TX and RX performance due to the better external mixer characteristics and the additional path loss in the TX-to-RX measurement.

The beam pattern of the four-element phased array was measured using the setup in Fig. 28(a) and (b). A simple chip-to-waveguide transition was attached to a single-element RX so that a receiving horn antenna can be connected, and the down-conversion of the radiated signal can be performed. However, the resulting high insertion loss of the transition causes a large drop in the received signal, so a compensating III–V semiconductor amplifier [72] was attached. The unknown transition loss, the large losses at the IF side caused by the external divider network and the long PCB lines, and the lack of a reliable 300-GHz source for calibration made it very difficult to perform an EIRP measurement with correct results, so the EIRP values are not presented in this article. The mentioned packaging and measurement limitations also resulted in omitting the throughput measurement results of the phased-array configuration. Considering the array dimensions, the 2.5-cm separating distance shown in Fig. 28(a) is larger than the 1.6-cm Fraunhofer distance. Hence, it is in the far field of the array. However, considering the 5.5-cm Fraunhofer distance of the horn antenna, the array is in the Fresnel region of the horn. Therefore, the horn antenna gain is several decibels lower than the far-field 26-dBi gain indicated in Fig. 28(a). The measured beam is shown in Fig. 28(c). The steering range in the H-plane of the Vivaldi antennas covers the angles from $-18°$ to 18°. The scanning angle range is limited by the narrow Vivaldi antenna pattern since the total array directivity is calculated by multiplying the element pattern by the array factor. Larger phase shifts between the adjacent elements will result in low radiated power values that cannot be properly measured for pattern evaluation. The LO phase shifter configuration required for a certain beam angle when the array operates at the RX mode is expected to slightly differ from the configuration used in the TX mode considering the different phase mismatch conditions. However, the scanning range does not change since it is dominated by the single-element antenna pattern.

In Table I, this work is compared with several state-of-the-art 300-GHz-band TRXs. The bi-directional architecture reduces the area considerably and the mixer-distributed-amplifier combination contributes to the very wide operating bandwidth.

VI. Conclusion

In this work, a 30-GHz-band CMOS bi-directional four-element phased-array TRX is introduced. The outphasing technique is used to overcome the low output power issue of the bi-directional subharmonic mixer in the TX mode. The flexible phase generation enables several additional features, including LOFT cancellation (TX and RX) and image rejection (RX). The TX and RX achieve 26- and 18-GBd symbol rates, respectively. The stacked Vivaldi antenna structure makes it possible to have a good beam steering range as the antenna pitch can be close to $\lambda_0/2$ at the RF band. The measured beam pattern demonstrates a coverage from $-18°$ to 18° in the H-plane of the stacked Vivaldi antennas.

References

[1] *IEEE Standard for High Data Rate Wireless Multi-Media Networks–Amendment 2, 100 Gb/s Wireless Switched Point-to-Point Physical Layer*, IEEE Standard 802.15.3d-2017, 2017.

[2] V. Petrov, T. Kurner, and I. Hosako, "IEEE 802.15.3d: First standardization efforts for sub-terahertz band communications toward 6G," *IEEE Commun. Mag.*, vol. 58, no. 11, pp. 28–33, Nov. 2020.

[3] H. Hamada *et al.*, "300-GHz-band 120-Gb/s wireless front-end based on InP-HEMT PAs and mixers," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2316–2335, Sep. 2020.

[4] H. Hamada *et al.*, "300-GHz, 100-Gb/s InP-HEMT wireless transceiver using a 300-GHz fundamental mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1480–1483.

[5] H. Hamada *et al.*, "300-GHz 120-Gb/s wireless transceiver with high-output-power and high-gain power amplifier based on 80-nm InP-HEMT technology," in *Proc. IEEE Compound Semicond. Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, pp. 1–4.

[6] H.-J. Song *et al.*, "Demonstration of 20-Gbps wireless data transmission at 300 GHz for KIOSK instant data downloading applications with InP MMICs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[7] I. Kallfass *et al.*, "All active MMIC-based wireless communication at 220 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 2, pp. 477–487, Nov. 2011.

[8] I. Kallfass *et al.*, "64 Gbit/s transmission over 850 m fixed wireless link at 240 GHz carrier frequency," *J. Infr., Millim., THz Waves*, vol. 36, no. 2, pp. 221–233, Feb. 2015.

[9] F. Boes *et al.*, "Ultra-broadband MMIC-based wireless link at 240 GHz enabled by 64GS/s DAC," in *Proc. 39th Int. Conf. Infr., Millim., THz Waves*, Sep. 2014, pp. 1–2.

[10] I. Kallfass *et al.*, "Towards MMIC-based 300 GHz indoor wireless communication systems," *IEICE Trans. Electron.*, vol. 98, no. 12, pp. 1081–1090, 2015.

[11] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Ferster, B. Heinemann, and U. R. Pfeiffer, "A wideband fully integrated SiGe chipset for high data rate communication at 240 GHz," in *Proc. 11th Eur. Microw. Integr. Circuits Conf.*, Oct. 2016, pp. 181–184.

[12] P. Rodriguez-Vazquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 65 Gbps QPSK one meter wireless link operating at a 225–255 GHz tunable carrier in a SiGe HBT technology," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2018, pp. 146–149.

[13] P. Rodríguez-Vázquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "Towards 100 Gbps: A fully electronic 90 Gbps one meter wireless link at 230 GHz," in *Proc. 48th Eur. Microw. Conf. (EuMC)*, Sep. 2018, pp. 1389–1392.

[14] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-M wireless link with an EVM of 17% at 230 GHz in an SiGe technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 4, pp. 297–299, Apr. 2019.

[15] M. H. Eissa *et al.*, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018.

[16] M. H. Eissa, N. Maletic, E. Grass, R. Kraemer, D. Kissinger, and A. Malignaggi, "100 Gbps 0.8-m wireless link based on fully integrated 240 GHz IQ transmitter and receiver," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Los Angeles, CA, USA, Jun. 2020, pp. 627–630.

[17] C. Jiang, A. Cathelin, and E. Afshari, "A high-speed efficient 220-GHz spatial-orthogonal ASK transmitter in 130-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2321–2334, Sep. 2017.

[18] X.-D. Deng *et al.*, "A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 6, pp. 930–940, Nov. 2015.

[19] K. K. Tokgoz *et al.*, "A 120 Gb/s 16 QAM CMOS millimeter-wave wireless transceiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 168–170.

[20] H. Wang, H. Mohammadnezhad, and P. Heydari, "Analysis and design of high-order QAM direct-modulation transmitter for high-speed point-to-point mm-wave wireless links," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3161–3179, Nov. 2019.

[21] H. Mohammadnezhad, H. Wang, A. Cathelin, and P. Heydari, "A 115–135-GHz 8PSK receiver using multi-phase RF-correlation-based direct-demodulation method," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2435–2448, Sep. 2019.

[22] P. Nazari, S. Jafarlou, and P. Heydari, "A CMOS two-element 170-GHz fundamental-frequency transmitter with direct RF-8PSK modulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 282–297, Feb. 2020.

[23] K. Tokgoz *et al.*, "A 273–301-GHz amplifier with 21-dB peak gain in 65-nm standard bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 5, pp. 342–344, Apr. 2019.

[24] O. Momeni, "A 260 GHz amplifier with 9.2 dB gain and −3.9dBm saturated power in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 140–141.

[25] D. W. Park *et al.*, "A 280-/300-GHz three-stage amplifiers in 65-nm CMOS with 12-/9-db gain and 1.6/1.4% PAE while dissipating 17.9 mW," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 1, pp. 79–81, Jan. 2018.

[26] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.

[27] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK transmitter in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Oct. 2015.

[28] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2268–2280, Oct. 2015.

[29] K. Katayama *et al.*, "A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3037–3048, Dec. 2016.

[30] K. Takano *et al.*, "A 105 Gb/s 300 GHz CMOS transmitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 308–309.

[31] S. Hara *et al.*, "A 32 Gbit/s 16 QAM CMOS receiver in 300 GHz band," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1703–1706.

[32] S. Lee *et al.*, "An 80-Gb/s 300-GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019.

[33] I. Abdo *et al.*, "A 300 GHz wireless transceiver in 65 nm CMOS for IEEE802.15.3d using push-push subharmonic mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 623–626.

[34] I. Abdo, T. Fujimura, T. Miura, K. K. Tokgoz, A. Shirane, and K. Okada, "A 0.41W 34 Gb/s 300 GHz CMOS wireless transceiver," in *Proc. 26th Asia South Pacific Des. Autom. Conf.*, Jan. 2021, pp. 3–4.

[35] A. Standaert and P. Reynaert, "A 390-GHz outphasing transmitter in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2703–2713, Oct. 2020.

[36] A. Standaert and P. Reynaert, "A 400-GHz 28-nm TX and RX with chip-to-waveguide transitions used in fully integrated lensless imaging system," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 4, pp. 373–382, Jul. 2019.

[37] K. Takano *et al.*, "300-GHz CMOS transmitter module with built-in waveguide transition on a multilayered glass epoxy PCB," in *Proc. IEEE Radio Wireless Symp. (RWS)*, Jan. 2018, pp. 154–156.

[38] S. Hara *et al.*, "300-GHz CMOS receiver module with WR-3.4 waveguide interface," in *Proc. 48th Eur. Microw. Conf. (EuMC)*, Sep. 2018, pp. 396–399.

[39] Y. Morishita *et al.*, "300-GHz-band OFDM video transmission with CMOS TX/RX modules and 40dBi Cassegrain antenna toward 6G," *IEICE Trans. Electron.*, vol. 104, no. 10, pp. 576–586, Oct. 2021.

[40] D. Simic, K. Guo, and P. Reynaert, "A 420-GHz sub-5-μm range resolution TX–RX phase imaging system in 40-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3827–3839, Dec. 2021.

[41] K. Guo and P. Reynaert, "29.2 A 0.59 THz beam-steerable coherent radiator array with 1 mW radiated power and 24.1 dBm EIRP in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 442–444.

[42] H. Jalili and O. Momeni, "A 436-to-467 GHz lens-integrated reconfigurable radiating source with continuous 2D steering and multi-beam operations in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 326–328.

[43] J. Kim, S. Kim, K. Song, and J.-S. Rieh, "A 300-GHz SPST switch with a new coupled-line topology in 65-nm CMOS technology," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 2, pp. 215–218, Mar. 2019.

[44] F. Meng, K. Ma, K. S. Yeo, C. C. Boon, W. M. Lim, and S. Xu, "A 220–285 GHz SPDT switch in 65-nm CMOS using switchable resonator concept," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 4, pp. 649–651, Jul. 2015.

[45] H. Saeidi, S. Venkatesh, C. R. Chappidi, T. Sharma, C. Zhu, and K. Sengupta, "A 4×4 distributed multi-layer oscillator network for harmonic injection and THz beamforming with 14 dBm EIRP at 416 GHz in a lensless 65 nm CMOS IC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 256–258.

[46] H. Jalili and O. Momeni, "A 318-to-370 GHz standing-wave 2D phased array in 0.13 μm BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 310–311.

[47] Y. Tousi and E. Afshari, "A scalable THz 2-D phased array with +17 dBm of EIRP at 338 GHz in 65 nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 258–259.

[48] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[49] K. Guo, Y. Zhang, and P. Reynaert, "A 0.53-THz subharmonic injection-locked phased array with 63-μ W radiated power in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 380–391, Feb. 2019.

[50] A. Babakhani, G. Xiang, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[51] A. Safaripour, B. Asghari, M. R. M. Hashemi, and A. Hajimiri, "Proximal-field sensing: *In situ* prediction of far-field radiation for integrated radiators," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3743–3756, Sep. 2019.

[52] I. Abdo *et al.*, "A 300 GHz-band phased-array transceiver using Bi-directional outphasing and Hartley architecture in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 316–318.

[53] S.-K. Lin, J.-L. Kuo, and H. Wang, "A 60 GHz sub-harmonic resistive FET mixer using 0.13μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 10, pp. 562–564, Oct. 2011.

[54] I. Momson, S. Lee, S. Dong, and K. O. Kenneth, "425-to-25-GHz CMOS-integrated downconverter," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 80–83, 2021.

[55] C. Wang and R. Han, "Rapid and energy-efficient molecular sensing using dual mm-wave combs in 65 nm CMOS: A 220-to-320 GHz spectrometer with 5.2 mW radiated power and 14.6-to-19.5dB noise figure," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 302–303.

[56] K. Okada *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[57] K. Yhland, "Simplified analysis of resistive mixers," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 604–606, Aug. 2007.

[58] Y. Yan, M. Bao, S. E. Gunnarsson, V. Vassilev, and H. Zirath, "A 110–170-GHz multi-mode transconductance mixer in 250-nm InP DHBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2897–2904, Sep. 2015.

[59] Y. Ismail, H. Lee, S. Pamarti, and C.-K. K. Yang, "A 36-V 49% efficient hybrid charge pump in nanometer-scale bulk CMOS technology," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 781–798, Mar. 2017.

[60] D. Zhao, S. Kulkarni, and P. Reynaert, "A 60-GHz outphasing transmitter in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3172–3183, Dec. 2012.

[61] S. Li, T. Chi, J.-S. Park, H. T. Nguyen, and H. Wang, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1243–1253, May 2019.

[62] S. Li, T. Chi, H. T. Nguyen, T.-Y. Huang, and H. Wang, "A 28 GHz packaged Chireix transmitter with direct on-antenna outphasing load modulation achieving 56%/38% PA efficiency at peak/6dB back-off output power," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 68–71.

[63] J. Pang, R. Kubozoe, Z. Li, M. Kawabuchi, A. Shirane, and K. Okada, "A 28-GHz CMOS vector-summing phase shifter featuring I/Q imbalance calibration supporting 11.2Gb/s in 256QAM for 5G new radio," *IEICE Trans. Electron.*, vol. 103, no. 2, pp. 39–47, Feb. 2020.
[64] J. Pang *et al.*, "A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, May 2019.
[65] O. Momeni and E. Afshari, "A high gain 107 GHz amplifier in 130 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2011, pp. 1–4.
[66] H. Bameri and O. Momeni, "A high-gain mm-wave amplifier design: An analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.
[67] M.-K. Cho, J. Kim, and D. Baek, "A switchless CMOS bi-directional distributed gain amplifier with multi-octave bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 611–613, Nov. 2013.
[68] K. S. Yngvesson, T. L. Korzeniowski, Y.-S. Kim, E. L. Kollberg, and J. F. Johansson, "The tapered slot antenna—A new integrated element for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 37, no. 2, pp. 365–374, Feb. 1989.
[69] Y. Wang *et al.*, "A 39-GHz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5G NR in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1249–1269, May 2020.
[70] J. Pang *et al.*, "A CMOS dual-polarized phased-array beamformer utilizing cross-polarization leakage cancellation for 5G MIMO systems," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1310–1326, Apr. 2021.
[71] Z. Zhang, Y. Yin, and G. M. Rebeiz, "Intersymbol interference and equalization for large 5G phased arrays with wide scan angles," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 3, pp. 1955–1964, Mar. 2021.
[72] H. Hamada *et al.*, "230–305 GHz, >10-dBm-output-power wideband power amplifier using low-Q neutralization technique in 60-nm InP-HEMT technology," in *Proc. IEEE BiCMOS Compound Semicond. Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4.

Ibrahim Abdo (Member, IEEE) received the B.Sc. degree in electronics engineering from Princess Sumaya University for Technology (PSUT), Amman, Jordan, in 2014, and the M.E. degree in physical electronics and the Ph.D. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2017 and 2021, respectively.

He is currently a Researcher with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Japan, where he is engaged in the research and development of monolithic microwave integrated circuits (MMICs) for ultra-high-speed wireless communications. His research interests include high-data-rate millimeter-wave/sub-terahertz wireless transceiver circuit design and phased-array implementation.

Dr. Abdo was a recipient of the Japanese Government (MEXT) Scholarship and the IEEE SSCS Predoctoral Achievement Award for the period 2021–2022. He serves as a Reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT).

Carrel da Gomez received the B.Sc. degree in electrical engineering from the Institut Teknologi Bandung, Bandung, Indonesia, in 2017, and the M.Eng. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His current research interests include CMOS millimeter-wave and sub-terahertz integrated circuits for wireless communication and radar.

Mr. da Gomez was a recipient of the Japanese Government (MEXT) Scholarship in 2018.

Chun Wang received the B.E degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2015, and the M.E. degree from Zhejiang University, Hangzhou, China, in 2018. He is currently pursuing the Ph.D. degree in electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan, with a focus on millimeter-wave front-end and system design.

His current research interests include *F*-band and 300-G transceivers for wireless communications.

Kota Hatano received the B.E. degree in electrical and electronic engineering from the Tokyo University of Science, Tokyo, Japan, in 2019, and the M.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, in 2021.

His current research interest includes 300-GHz CMOS integrated circuits for wireless communication.

Qi Li (Graduate Student Member, IEEE) received the M.E. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

His research topics are regarding electromagnetism, antenna design, coupler design, and multi-beam antenna feeding networks.

Chenxin Liu received the B.E. degree from the Nanjing University of Science and Technology, Nanjing, China, in 2019, and the M.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2021, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His current research is about millimeter-wave wireless communication system design.

Kiyoshi Yanagisawa (Member, IEEE) received the B.E. and M.E. degrees in information science from Tohoku University, Sendai, Japan, in 1998 and 2000, respectively.

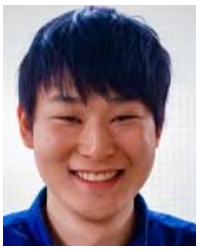
From 2013 to 2019, he was with Rohde & Schwarz, Tokyo, Japan, where he was engaged in the test and measurement of wireless systems. From 2019 to 2020, he was a Researcher with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo. His research interests include new technology in wireless systems and devices.

Mr. Yanagisawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE).

Ashbir Aviat Fadila (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Institut Teknologi Bandung, Bandung, Indonesia, in 2015, and the M.Eng. degree from the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

From 2015 to 2016, he was a Standard Cells Mask Layout Engineer with Marvell Technology Indonesia, Jakarta, Indonesia. From 2016 to 2017, he was a Research Assistant with the Institut Teknologi Bandung, where he researched system-on-chip (SoC) for the Internet of Things (IoT) applications. His current research interests include analog–mixed signals, data converters, and synthesizable analog circuits.

Takuya Fujimura received the B.E. degree in electrical and electronic engineering from the Tokyo University of Science, Tokyo, Japan, in 2016, and the M.S. degree in physical electronics from the Tokyo Institute of Technology, Tokyo, in 2018.



Tsuyoshi Miura received the B.E. degree in electrical engineering from the Tokyo University of Science, Tokyo, Japan, in 2017, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, in 2019.

Korkut Kaan Tokgoz (Member, IEEE) received the B.Sc. and M.Sc. degrees from the Department of Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey, in 2009 and 2012, respectively, and the M.Eng. and Ph.D. degrees from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2014 and 2018, respectively.

From 2018 to 2019, he worked as a Senior Researcher/Assistant Manager with NEC Corporation, Kawasaki, Japan, where he was involved in 5G systems and fixed point-to-point wireless links. From 2019 to 2022, he worked as an Assistant Professor with the Tokyo Institute of Technology. He is currently working as a Faculty Member with the Faculty of Engineering and Natural Sciences, Sabanci University, Istanbul, Turkey. He is also the Co-Founder and the CTO of Evrim Company Ltd., Yokohama, Japan. His research interests include analog/RF/millimeter-wave/sub-terahertz transceivers for wireless communications; low-power edge-artificial intelligence (AI) for monitoring systems; the Internet of Things (IoT), sensors and systems; de-embedding; device characterization; and high-power, high-efficiency power amplifiers (PAs) for wireless systems.

Dr. Tokgoz was a recipient of several awards and scholarships, including the SSCS Predoctoral Achievement Award in 2018, the IEEE MTT-S Graduate Student Fellowship in 2017, the IEICE Student Encouragement Prize in 2017, the Seiichi Tejima Overseas Student Research Award, and the IEEE/ACM ASP-DAC University LSI Design Contest 2017 Best Design Award.

Jian Pang (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

From 2019 to 2020, he was a Post-Doctoral Researcher with the Tokyo Institute of Technology. From 2020 to 2022, he was a Special-Appointed Assistant Professor with the Tokyo Institute of Technology. He is currently a Special-Appointed Associated Professor with the Tokyo Institute of Technology, focusing on 5G millimeter-wave systems. His current research interests include high-data-rate low-cost millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile systems, multiple-in–multiple-out (MIMO), and mixed-signal calibration systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Pre-Doctoral Achievement Award for the term 2018–2019, the Seiichi Tejima Oversea Student Research Award in 2020, and the IEEE MTT-S Japan Young Engineer Award in 2021.

Hiroshi Hamada (Member, IEEE) received the B.E. and M.E. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2009 and 2011, respectively.

He joined NTT Photonics Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Atsugi, Japan, in 2011, where he started the research and development of the millimeter-wave/terahertz (THz) monolithic microwave integrated circuits (MMICs) for wireless communications. He was engaged in research of InP-transistor-based THz MMICs and modules such as 300-GHz power amplifiers, mixers, transceivers, and 500-GHz amplifiers at NTT Photonics Labs and Device Technology Labs from 2011 to 2021. In 2021, he was transferred to NTT DOCOMO, Inc., Yokosuka, Japan, where he is currently working at the 6G-IOWN Promotion Department as a Manager.

Mr. Hamada is a member of the Institute of Electronics, Information and Communication Engineers (IEICE). He has been serving as a member for the IEEE Microwave Theory and Techniques Society (MTT-S) Technical Committee on Microwave and Millimeter-Wave Solid State Devices (TC-9). He was a recipient of the IEEE IMS Best Industry Paper Award in 2016, the URSI AP-RASC Young Scientist Award in 2016, the APMC Prize in 2018, the IEICE Young Researcher's Award in 2019, and the IEEJ Excellent Presentation Award in 2022.

Hideyuki Nosaka (Senior Member, IEEE) received the B.S. and M.S. degrees in physics from Keio University, Yokohama, Japan, in 1993 and 1995, respectively, and the Dr.Eng. degree in electronics and electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2003.

From 1995 to 2021, he was with NTT Corporation, Atsugi, Japan, where he has been involved in research and development of ultra-high-speed mixed-signal integrated circuits (ICs) for wireless and optical communications. He is currently a Professor with the Department of Electrical and Electronic Engineering, Ritsumeikan University, Shiga, Japan. He has authored or coauthored over 150 journal articles and conference papers and has over 150 patents issued. His current research interests include analog and mixed circuits for 6G, wireless power supply, the Internet of Things (IoT), and satellite wireless systems.

Dr. Nosaka is a member of the IEEE Microwave Theory and Techniques Society (MTT-S), the IEEE Solid-State Circuits Society (SSCS), and the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan. He served as a Technical Program Committee (TPC) Member for the European Microwave Conference (EuMC) in 2010, the IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS) from 2011 to 2013, the Asia-Pacific Microwave Conference (APMC) in 2014, and the IEEE International Solid-State Circuits Conference (ISSCC) from 2013 to 2017. He has been serving as a member for the IEEE MTT-S Technical Committee on MTT-15 RF/Mixed-Signal Integrated Circuits and Signal Processing since 2016. He was a recipient or co-recipient of the IEICE Young Engineer Award in 2001, the IEICE Best Paper Award in 2011, the URSI Young Scientist Award in 2016, and the APMC 2018 Prize.

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched on intelligent motor with wireless communication. He is currently an Associate Professor with the Laboratory for Future Interdisciplinary Research of Science and Technology, Institute of Innovative Research, Tokyo Institute of Technology. His current research interests include RF CMOS transceiver for the Internet of Things (IoT), 5G, and satellite communication and wireless power transfer.

Dr. Shirane is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science, Kyoto University. In 2003, he joined the Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering. He has authored or coauthored more than 500 journal articles and conference papers. His current research interests include millimeter-wave and terahertz CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for 5G, WiGig, satellite and future wireless system, digital phase-locked loop (PLL), synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low energy, and sub-gigahertz applications.

Dr. Okada is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC, Prolific Author Award in 2020, the Kenjiro Takayanagi Achievement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC, Best Paper Award in 2020, and more than 50 other international and domestic awards. He is/was a member of the Technical Program Committee of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), and Radio Frequency Integrated Circuits Symposium (RFIC). He is/was a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).