A Charge-Sharing IIR Filter With Linear Interpolation and High Stopband Rejection

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***Abstract*— This article introduces a new discrete-time (DT) charge-sharing (CS) low-pass filter (LPF) that achieves high-order filtering and improves its stopband rejection while maintaining a reasonable duty cycle of the main clock at 20%. It proposes two key innovations: 1) a linear interpolation of the sampling capacitor and 2) a charge re-circulation of the history capacitors for deep stopband rejection. Fabricated in 28-nm CMOS, the proposed IIR LPF demonstrates a 1–9.9-MHz bandwidth (BW) programmability and achieves a record-high 120-dB stopband rejection at 100 MHz while consuming merely 0.92 mW. The in/out-of-band IIP3 is +17.7 dBm/+26.6 dBm, and the input-referred noise is 3.5 nV/$\sqrt{\text{Hz}}$.**

***Index Terms*— Discrete-time (DT) filter, first-order hold (FOH), infinite-impulse response (IIR), linear interpolation, low-pass filter (LPF), switched capacitor, zero-order-hold (ZOH).**

I. Introduction

INTEGRATED low-pass filters (LPFs) with strong rejection of out-of-band frequency components are essential building blocks in various applications, such as wireless communications [1]–[5], magnetic recording [6], [7], and video [8], [9]. Attention is drawn toward low noise, small area, high in-/out-of-band linearity, and low-power consumption.

The three well-known conventional analog techniques, that is, g_m-C, active R-C, and active switch-capacitor filters [10]–[14], are not amenable to advanced technology nodes. The g_m-C filters suffer from poor bandwidth (BW) tunability since the BW is mainly defined based on g_m, capacitance, and resistance, and it is susceptible to process–voltage–temperature (PVT) variations. Consequently, they require calibration for accurate BW. Both the active R-C and active switch-C filters suffer from op-amp-related issues. First, using an active component, such as an op-amp, increases the power consumption. Moreover, it is difficult to design a high-gain and wide-BW op-amp, especially in finer CMOS nodes, because of the decrease in available headroom voltage for active components. Therefore, the process scalability is challenging for these structures [15], [16].

Recently, various new techniques have been introduced for high-performance LPFs targeting scaled CMOS. This includes charge-sharing (CS) infinite-impulse response (IIR) [15]–[18], analog finite-impulse response (AFIR) [19], filtering by aliasing [20], and flipped/coupled source followers (FSFs/CSFs) [21], [22]. Tohidian *et al.* [15] introduced a high-order (i.e., 7th) IIR LPF by means of adding more clock phases and history capacitors to the conventional first-order IIR filter. Unfortunately, that solution suffers from an inherently poor rejection of the roll-off part of the transfer function (TF) due to the fact that the passive CS filter's poles are limited to real values. A solution was offered via a digital post-emphasis (equalizer) filter to sharpen the transient region. Payandehnia *et al.* [16] used active negative feedback around their fourth-order IIR filter to generate complex conjugate poles, thus leading to an improvement in the filter's band-edge transition. However, such an installation of complex poles comes at the cost of extra active circuitry, which leads to more noise and losses as well as deterioration of linearity. Lulec *et al.* [17] introduced an idea to create two complex conjugate-pole pairs in a conventional IIR filter by means of a feedback path through a sampling capacitor (C_S). In [19], a low-power AFIR was introduced that contains a single inverter-based g_m-C integrator implemented as a digital-to-analog converter (DAC). A filtering-by-aliasing approach introduced in [20] is based on two integrate-and-dump circuits, each taking a benefit of a time-varying resistor [i.e., $R(t) = R(t + T_s)$] to make an equivalent FIR filter with the desired impulse response. Xu *et al.* [22] presented a compact CSF-based continuous-time (CT) LPF filter that requires no operational transconductance amplifiers (OTAs). It takes advantage of a third-order low-pass TF in a single stage with two CSFs and three capacitors.

As argued in [15] and [23], discrete-time (DT) CS filters are becoming increasingly important because they mainly rely on CMOS switches, inverters, and capacitors, which all offer high process scalability. They also provide a solution in addressing one of the key remaining issues in advanced communication

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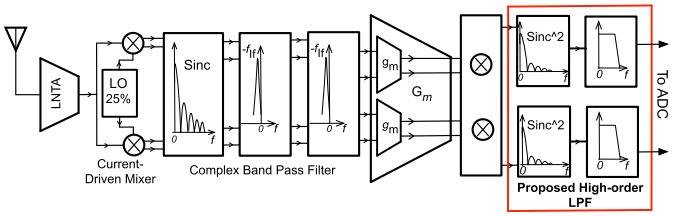

Fig. 1. Wireless discrete-time (DT) superheterodyne (i.e., high-IF) receiver as an example application of the proposed filter.

systems: the out-of-band rejection strength, which is highly desired, for example, for strong blocker rejection in 5G applications where a −15-dBm continuous-wave (CW) blocker can be located 85-MHz away from the desired channel. That brings strict linearity requirements on receivers, leading to a high demand for higher-order filtering [24]–[26].

An example of an application of such a DT CS filter is a wireless DT superheterodyne (i.e., high IF) receiver shown in Fig. 1. The DT receiver's front-end path generally starts with a CT low-noise transconductance amplifier (LNTA) [27] to amplify the antenna input and convert it to an RF current. It is followed by a multi-phase (i.e., quadrature or octal [5]) passive sampling mixer [28], [29] that preserves the DT nature of the signal. Thus, the generated intermediate frequency (IF) signal feeds a multistage IF DT filter [5], [23] to perform channel selection and reject the IF images. Afterward, the signal is downconverted to the baseband by another set of IF mixers and fed to the LPF [15], [18]. The proposed LPF offers an improved filtering characteristic by enhancing the stopband rejection. Hence, design constraints on the previous filtering stages can be relaxed while simultaneously keeping the sampling frequency (f_s) constant to prevent any aliasing issues in the following stages, especially in the analog-to-digital converter (ADC).

In the conventional CS IIR filtering (shown later in Figs. 3 and 4), the current is sampled over an integrating time window $T_i = 1/f_s$ (i.e., "integrate and sample"). The resulting integrated charge is interpreted as a DT "charge packet." The window integration acts like a zero-order hold (ZOH) on the integrated charge, which forms a CT anti-aliasing filter of the frequency response $\text{sinc}(\pi f/f_s)$ [3], [30]. The DT charge samples are then LPF by a passive switched-capacitor circuit. Through the sampling capacitor (C_S), the charge rotates between several history capacitors (C_H), as shown in Fig. 4, leading to high-order LPF. The order of filtering can be arbitrarily increased but at the cost of increasingly denser clock phases and more history capacitors [15].

Conceptually, if the ZOH is replaced with an FOH, whose frequency response is $\text{sinc}^2(\pi f/f_s)$, its stopband rejection would substantially improve (see Fig. 2). This would better attenuate unwanted signals that might fold from around the multiples of the sampling frequency, f_s, to the input BW. However, in practice, the realization of linear interpolation is very challenging. In [31], a rectangular boxcar was convolved with itself to make a triangular response with a TF of $\text{sinc}^2(\pi f/f_s)$. However, that technique requires another stage of a charge sampling filter whose transconductance g_m

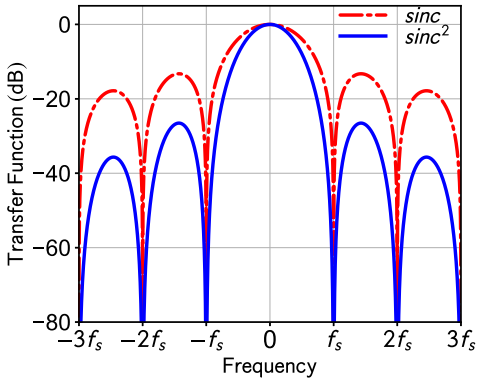

Fig. 2. TF comparison of $\text{sinc}(\pi f/f_s)$ and $\text{sinc}^2(\pi f/f_s)$.

converts the voltage output of the first stage to the current and then integrates it into another sampling capacitor (C_S) for providing the second boxcar. That, unfortunately, leads to higher complexity and power consumption. Moreover, since the number of sampling capacitors is doubled and a reset of both stages is required, charge losses increase, causing further deterioration of the signal-to-noise ratio (SNR).

This extended article of [18] proposes two techniques to improve the stopband rejection of the conventional DT IIR filter. We first introduce a new approach to implement the $\text{sinc}^2(\pi f/f_s)$ function by providing a pseudo-linear interpolation through an L-fold technique. Moreover, we propose to dynamically re-engage the history capacitor in each stage to provide higher-order filtering. The proposed techniques are applied to a fourth-order IIR LPF, demonstrating the highest out-of-band rejection among analog filters.

The rest of the article is organized as follows. Section II reviews the basic concept of CS IIR filter and the conventional approach to increasing the order of filtering. Two techniques to improve the stopband rejection are then proposed and are described in detail. Additionally, an extensive analysis of the filter's TF is provided. The last part of Section II applies the proposed techniques to a conventional fourth-order IIR filter to achieve the best stopband rejection reported in the literature. In Section III, the circuit implementation is provided. Finally, the measurement results are given in Section IV.

II. Low-Pass Filter Topology

A. Conventional First/Fourth-Order Charge-Sharing IIR LPF

Fig. 3 shows the conventional first-order CS IIR filter. It consists of the g_m-stage to convert the input voltage to a current, the history capacitor (C_H) to store the input charge (i.e., the integrated current), and the sampling capacitor (C_S) to perform charge sharing and to transfer (make available) its charge to the output stage. According to the timing diagram, at ϕ_1, the input charge is transferred to the output via C_S, and at ϕ_2 C_S is reset. The signal flow diagram of the IIR filter in Fig. 3(c) consists of the $\text{sinc}(\pi f/f_s)$ anti-aliasing filtering due to the time window integration over ϕ_1, and LPF due to its passive switched-capacitor circuitry [3]. Nonetheless, the conventional LPF does not provide a strong stopband rejection.

By adding more phases and history capacitors, the filter order can be increased [15]. Fig. 4(a) shows a conventional

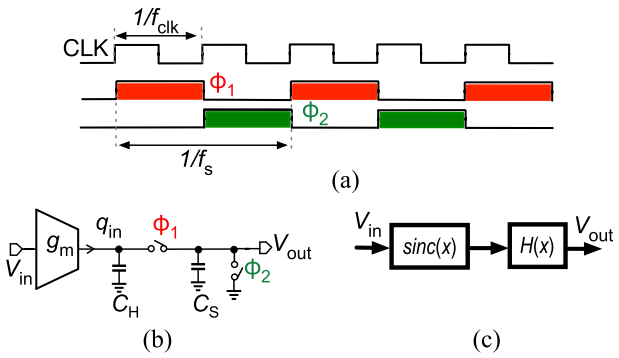

Fig. 3. First-order DT IIR filter: (a) timing diagram, (b) schematic, and (c) provided filtering. The input can be CT.

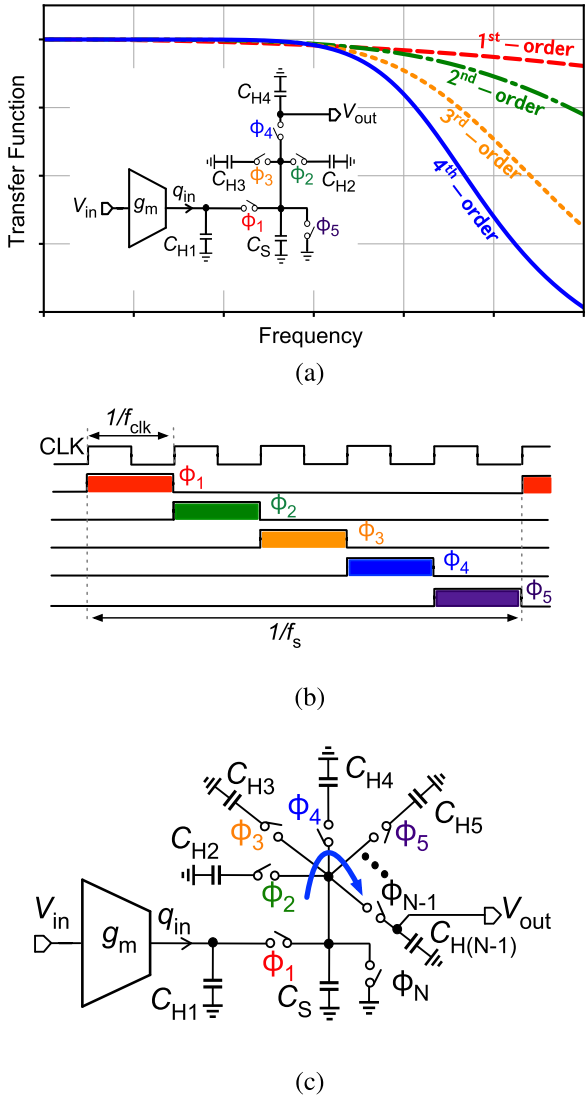

Fig. 4. (a) Prior-art fourth-order CS IIR filter with $N = 5$ phases and its conceptual TF plots at different stage outputs, yielding different orders of filtering. (b) Timing diagram of the fourth-order IIR filter. (c) Further extension to an $(N-1)$th-order filtering.

fourth-order IIR filter with $N = 5$ phases. The input charge is stored in the first history capacitor (C_{H1}). At ϕ_1, the input charge and the accumulated charge on C_{H1} from the previous

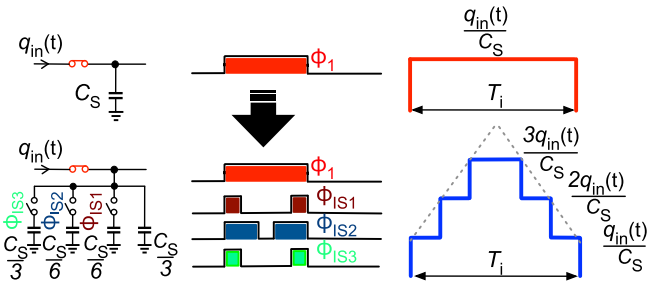

Fig. 5. Improvement #1: FOH and its timing diagram. The developed voltage is due to constant input $q_{in}(t)$.

cycle are shared with C_S. Then at ϕ_2, the remaining charge on C_S of the prior phase and the charge on C_{H2} from the last cycle are shared.

The same CS principle between C_S with C_{H3} and C_{H4} is applied during the remaining phases ϕ_3 and ϕ_4, respectively, until the charge is transferred to the primary output. Finally, at ϕ_5, C_S is reset. Following this approach, if the top plate of a farther history capacitor (i.e., C_{H1-4}) is taken as an output, an increased order of the DT IIR filtering can be achieved, as depicted in the conceptual TF plot of Fig. 4(a). This idea can be extended indefinitely to an $(N-1)$th-order of filtering, as shown in Fig. 4(c). However, a major bottleneck arises due to the N number of required clock phases to perform the charge sharing. Consequently, as illustrated in the timing diagram, to keep the pulsewidth constant, the sampling frequency f_s has to be decreased, possibly leading to aliasing issues. If one desires to keep f_s constant, then the required pulsewidth could become very narrow and thus difficult to implement for a high number of phases. Indeed, in the finer technologies, this is becoming less of an issue since the pulsewidth can be made very narrow due to the switches being very fast (e.g., 5–20-ps rise/fall time). However, after a certain (technology-dependent) pulsewidth duration is satisfied, what really matters is the overall number of clock edge transitions and the need to distribute clocks over larger distances (local is favored over global). Hence, we introduce in this work two key improvements: 1) a stronger $\text{sinc}^2(\pi f/f_s)$ anti-aliasing filtering instead of the conventional $\text{sinc}(\pi f/f_s)$, as shown in Fig. 2, and 2) improving the LPF via a new technique of a passive switched-capacitor circuitry to provide local filtering without sacrificing f_s.

B. Proposed Techniques to Improve IIR Filtering

1) Improvement #1: Pseudo-Triangular Time-Window Integration: A staircase approximation to the triangular response is shown in Fig. 5. Instead of the sampling capacitor C_S staying constant as in the conventional solutions, its capacitance steps down and up over time to approximate the triangular response. Enabling a different combination of the constituent sampling capacitors during each sampling sub-phase allows varying the effective sampling capacitance over the integrating window. Thus, it achieves the staircase approximation of the triangular sampling window integration [$\text{sinc}^2(\pi f/f_s)$ anti-alias filtering] instead of the box sampling window integration [$\text{sinc}(\pi f/f_s)$] when C_S is constant.

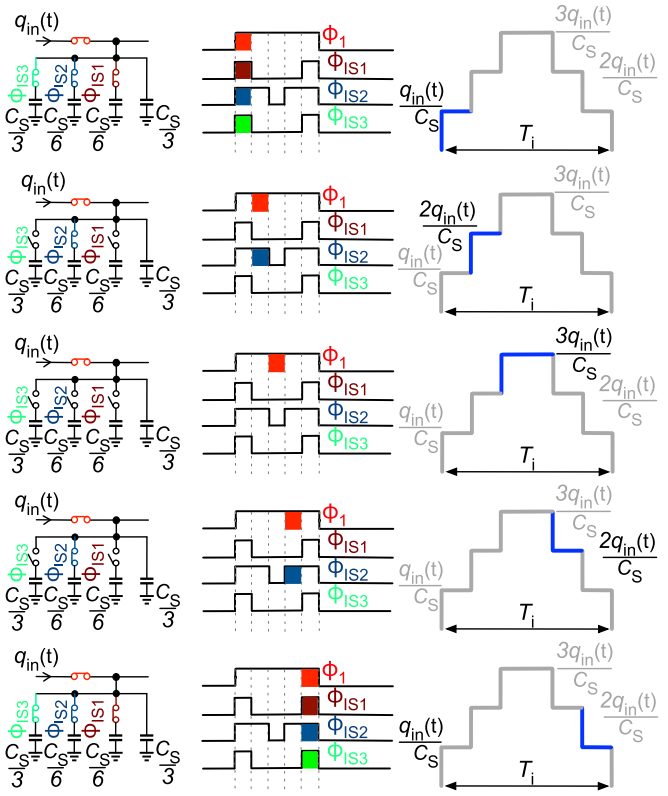

Fig. 6. Proposed scheme of the sampling capacitor to achieve pseudo-triangular time-window integration. The developed voltage is due to constant input $q_{\text{in}}(t)$.

Fig. 6 highlights the operation of the proposed technique. The integrating phase ϕ_1 is split into five equal sub-phases to generate the three sub-integrating control signals, ϕ_{IS1}, ϕ_{IS2}, and ϕ_{IS3}. The sampling capacitor C_S is split into four constituent capacitors, $C_S/3$, $C_S/6$, $C_S/6$, and $C_S/3$, the first three controlled, respectively, by $\phi_{\text{IS1}-3}$. At sub-phase #1 of ϕ_1, all sampling capacitors are engaged, resulting in the lowest voltage, q_{in}/C_S, due to the CT input charge packet $q_{\text{in}}(t)$. At sub-phase #2, the fixed sampling capacitor and one switchable by ϕ_{IS2} are connected, consequently leading to the increase in voltage. At sub-phase #3, all switches are OFF, and only the fixed capacitor is engaged. Hence, the top step of the proposed staircase is reached. Moving to sub-phase #4, ϕ_{IS2} is ON again, and the voltage moves down to the second level. Eventually, all capacitors are connected in the final step, pushing the voltage again all the way down to q_{in}/C_S. As a result, a staircase is approximated in the time domain, leading to an approximation of $\text{sinc}^2(\pi f/f_s)$ in the frequency domain.

Fig. 2 earlier illustrated that replacing $\text{sinc}(\pi f/f_s)$ with $\text{sinc}^2(\pi f/f_s)$ yields a sharper stopband rejection filtering at higher frequencies (>10 dB at around f_s and increasing beyond).

2) Improvement #2: Dynamically Re-Engaged History Capacitor: Using the dynamically re-engaged history capacitor C_H, an extra local LPF can be achieved, thus strengthening the overall filtering characteristics, as illustrated in Fig. 7. This is a similar concept as that proposed above for the time-varying sampling capacitor C_S, but the input charge q_{in} here

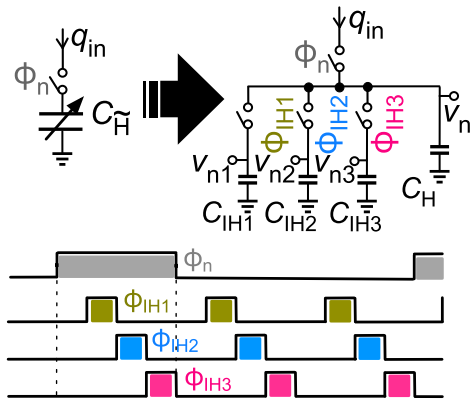

Fig. 7. Improvement #2: Local LPF (ϕ_{n}, $n = 1, 2, 3, \ldots, N$) due to the dynamically re-engaged history capacitor and its timing diagram.

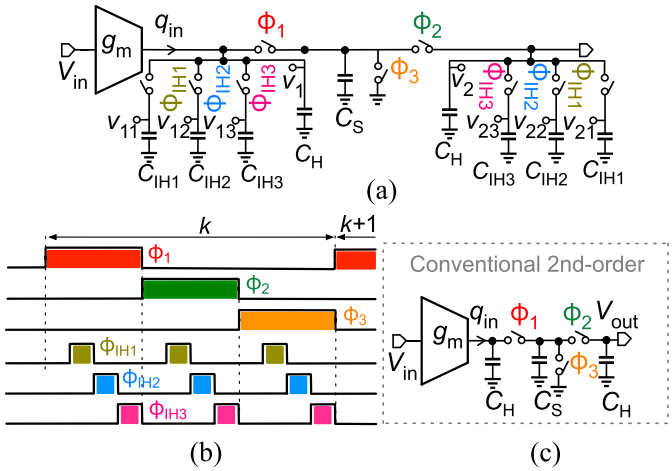

Fig. 8. Second-order IIR filter ($N = 3$): (a) with the proposed local LPF, (b) its timing diagram, and (c) conventional structure for reference.

is no longer assumed CT but can be a charge packet. Its constituent switchable capacitors are engaged according to the timing diagram. The main phase is divided into four equal sub-phases.[1] The rearrangement in capacitance C_H is carried out during the last three sub-phases, $\phi_{\text{IH}_{1-3}}$.

To examine the operation of the proposed technique, the dynamically re-engaged history capacitor scheme of Fig. 7 is applied to the conventional second-order CS IIR filter redrawn in Fig. 8(c). The resulting arrangement is depicted in Fig. 8(a) with the corresponding timing diagram in Fig. 8(b). For simplicity, the sharing capacitor C_S is kept constant. It is important to emphasize that the local (i.e., intra-$C_{\tilde{H}}$) filtering happens continuously and irrespective of the phase, that is, even if no new charge is allowed to enter the composite $C_{\tilde{H}}$. A detailed operation of this second-order IIR filter is presented in Fig. 9. During the first fourth sub-space of ϕ_1, the input charge q_{in} and any remaining charge on C_H from the previous cycle are shared with C_S. Moving to the second sub-phase of ϕ_1, the switch of the first sub-phase, ϕ_{IH1}, closes, and the first incremental history capacitor C_{IH1} is engaged in the

[1]Generally, this idea can be applied to any main phase which drives the history capacitor, ϕ_{n}, $n = 1, 2, 3, \ldots, N$.

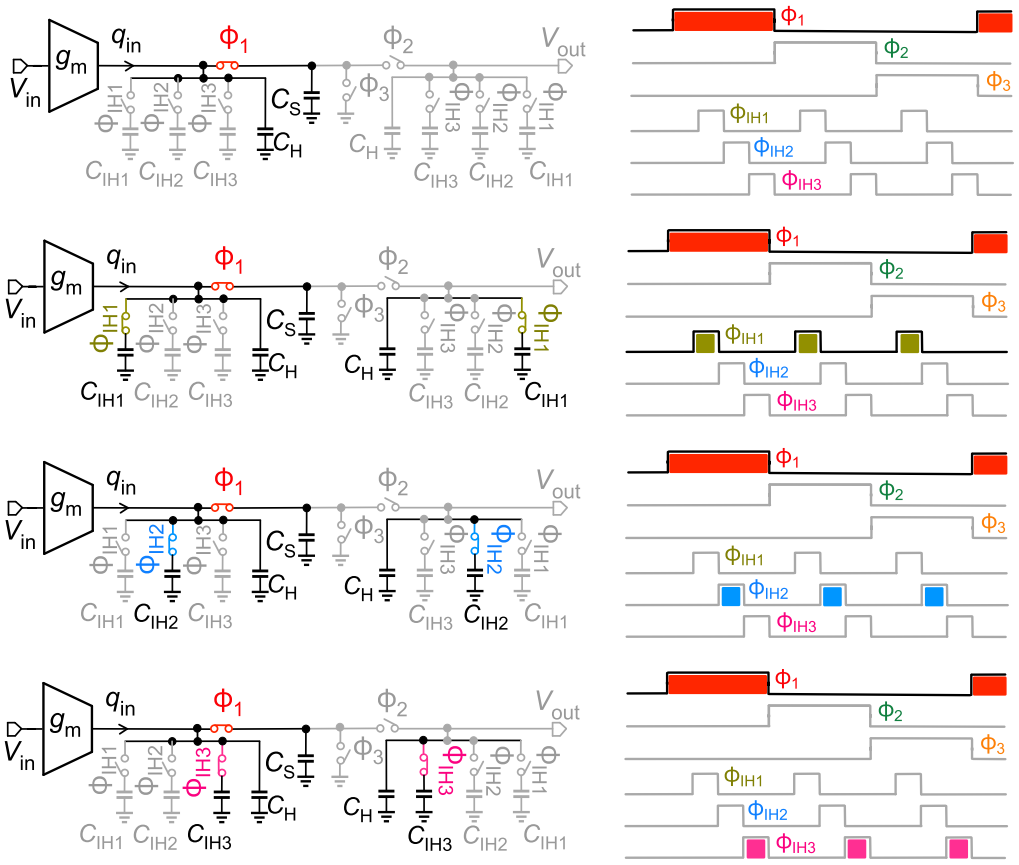

Fig. 9. Operation of second-order IIR filter ($N = 3$) with proposed local LPF at ϕ_1.

CS process. By adding C_{IH1}, its charge is now shared with the previous charge on C_H and C_S. In the third sub-phase, the remaining charge on C_H and C_S from the previous sub-phase (i.e., ϕ_{IH1}) is shared with the remaining charge on C_{IH2} of the prior phase, ϕ_3. Finally, during the last sub-phase, ϕ_{IH3}, the third incremental history capacitor gets involved in the CS process.

During the second phase, ϕ_2, C_S gets disconnected from the input stage and another similar CS process occurs in the second branch without the direct contribution from q_{in}. Finally, at ϕ_3, C_S is reset while the output voltage V_{out} can be readily probed. Since local LPF is carried out during each phase, ϕ_1 to ϕ_3, the overall filtering significantly improves, as shown in Section II-C.

C. Transfer Function Analysis of Intra-C_H Re-Engagement

The TF of a single unit of the dynamically re-engaged history capacitor is now calculated. By considering the composite C_H scheme of Fig. 7, the voltages on each incremental node $v_{n1}, \ldots, v_{n3}$ can be recursively calculated as dependent on the main fixed-capacitor node v_n as

$$@\phi_{IH3}\colon\ v_{n3}[k] = \alpha_{o3} v_{n3}\left[k - \frac{1}{N}\right] + \alpha_3 v_{n2}\left[k - \frac{1}{4N}\right]$$

$$@\phi_{IH2}\colon\ v_{n2}\left[k - \frac{1}{4N}\right] = \alpha_{o2} v_{n2}\left[k - \frac{1}{4N} - \frac{1}{N}\right] + \alpha_2 v_{n1}\left[k - \frac{2}{4N}\right]$$

$$@\phi_{IH1}\colon\ v_{n1}\left[k - \frac{2}{4N}\right] = \alpha_{o1} v_{n1}\left[k - \frac{2}{4N} - \frac{1}{N}\right] + \alpha_1 v_n\left[k - \frac{3}{4N}\right] \quad (1)$$

where N is the number of main phases ($N = 3$ in Figs. 8 and 9). Note that a single total delay equals the entire sampling period, which is divided into N main phases.

The z-domain equivalent of (1) is given as

$$\begin{aligned} V_{n3}(z) &= \alpha_{o3} z^{-\frac{1}{N}} V_{n3}(z) + \alpha_3 z^{-\frac{1}{4N}} V_{n2}(z) \\ z^{-\frac{1}{4N}} V_{n2}(z) &= \alpha_{o2} z^{-\frac{1}{N}} z^{-\frac{1}{4N}} V_{n2}(z) + \alpha_2 z^{-\frac{2}{4N}} V_{n1}(z) \\ z^{\frac{-2}{4N}} V_{n1}(z) &= \alpha_{o1} z^{-\frac{1}{N}} z^{-\frac{2}{4N}} V_{n1}(z) + \alpha_1 z^{-\frac{1}{N}} V_n(z). \end{aligned} \quad (2)$$

By simplifying (2), the TF from V_n (at ϕ_{IH0}, that is, just before ϕ_{IH1}) to V_{n3} (at ϕ_{IH3}) is equal to

$$\frac{V_{n3}}{V_n} = \frac{\alpha_3 \alpha_2 \alpha_1 z^{-\frac{1}{N}}}{\left(1 - \alpha_{o3} z^{-\frac{1}{N}}\right)\left(1 - \alpha_{o2} z^{-\frac{1}{N}}\right)\left(1 - \alpha_{o1} z^{-\frac{1}{N}}\right)}. \quad (3)$$

To calculate the TF of the second-order IIR filter structure with the proposed additional local LPF, as shown in Fig. 8(a), the first sub-phase of ϕ_2 is analyzed (i.e., marker ϕ_{IH0} associated with v_n that is conspicuously absent in Fig. 8(b) since all incremental capacitors are disconnected). At ϕ_{IH0}, voltage v_2 is a function of its value at the previous cycle (T_s delay) and sample v_{13} of the prior sub-phase ($T_s/12$ delay). Likewise, at ϕ_{IH3}, v_{13} is a function of its value at the previous phase ($T_s/3$ delay) and a sample of v_{12} from its last sub-phase

($3T_s/12$ delay). In the same way, CS equations are derived for the other sub-phases as follows:

$$
\begin{aligned}
&@\phi_{2,\text{IH0}}\colon\ v_2[k] = \alpha v_2[k-1] + (1-\alpha)v_{13}\left[k-\frac{1}{12}\right]\\
&@\phi_{1,\text{IH3}}\colon\ v_{13}\left[k-\frac{1}{12}\right] = \alpha_{o3}v_{13}\left[k-\frac{1}{12}-\frac{1}{3}\right]+\alpha_3 v_{12}\left[k-\frac{2}{12}\right]\\
&@\phi_{1,\text{IH2}}\colon\ v_{12}\left[k-\frac{2}{12}\right] = \alpha_{o2}v_{12}\left[k-\frac{2}{12}-\frac{1}{3}\right]+\alpha_2 v_{11}\left[k-\frac{3}{12}\right]\\
&@\phi_{1,\text{IH1}}\colon\ v_{11}\left[k-\frac{3}{12}\right] = \alpha_{o1}v_{11}\left[k-\frac{3}{12}-\frac{1}{3}\right]+\alpha_1 v_1\left[k-\frac{1}{3}\right]\\
&@\phi_{1,\text{IH0}}\colon\ v_1\left[k-\frac{4}{12}\right] = \alpha v_1\left[k-\frac{4}{12}-1\right]+\beta q_{\text{in}}\left[k-\frac{1}{3}\right]
\end{aligned}
\tag{4}
$$

where α, β, α_{o3-o1}, and α_{3-1} are calculated as

$$
\begin{aligned}
\alpha &= \frac{C_H}{C_H+C_S},\quad \alpha_{o3} = \frac{C_{\text{IH3}}}{C_{\text{IH3}}+C_H+C_S}\\
\alpha_{o2} &= \frac{C_{\text{IH2}}}{C_{\text{IH2}}+C_H+C_S},\quad \alpha_{o1} = \frac{C_{\text{IH1}}}{C_{\text{IH1}}+C_H+C_S}\\
\beta &= \frac{1}{C_H+C_S},\quad \alpha_3 = (1-\alpha_{o3}),\quad \alpha_2 = (1-\alpha_{o2})\\
\alpha_1 &= (1-\alpha_{o1}).
\end{aligned}
\tag{5}
$$

The z-domain equivalent of (4) is

$$
\begin{aligned}
V_2(z) &= \alpha z^{-1}V_2(z) + \alpha z^{-\frac{1}{12}}V_{13}(z)\\
z^{-\frac{1}{12}}V_{13}(z) &= \alpha_{o3}z^{-\frac{1}{12}}z^{-\frac{1}{3}}V_{13}(z) + \alpha_3 z^{-\frac{2}{12}}V_{12}(z)\\
z^{-\frac{2}{12}}V_{12}(z) &= \alpha_{o2}z^{-\frac{2}{12}}z^{-\frac{1}{3}}V_{12}(z) + \alpha_2 z^{-\frac{3}{12}}V_{11}(z)\\
z^{-\frac{3}{12}}V_{11}(z) &= \alpha_{o1}z^{-\frac{3}{12}}z^{-\frac{1}{3}}V_{11}(z) + \alpha_1 z^{-\frac{4}{12}}V_1(z)\\
z^{-\frac{4}{12}}V_1(z) &= \alpha z^{-\frac{4}{12}}z^{-1}V_1(z) + \beta z^{-\frac{1}{3}}Q_{\text{in}}(z).
\end{aligned}
\tag{6}
$$

By simplifying (6), V_2/Q can be expressed as

$$
\frac{V_2}{Q_{\text{in}}} = \frac{(1-\alpha)\alpha_3\alpha_2\alpha_1\beta z^{-1/3}}{\left(1-\alpha z^{-1}\right)^2\left(1-\alpha_{o3}z^{-1/3}\right)\left(1-\alpha_{o2}z^{-1/3}\right)\left(1-\alpha_{o1}z^{-1/3}\right)}.
\tag{7}
$$

Finally, the overall TF of the filter, which is available at the end of the last sub-phase is a cascade of two TFs

$$
H(z) = \frac{V_2}{Q_{\text{in}}}\times\frac{V_{23}}{V_2}.
\tag{8}
$$

Using (3), (5), and (7), the TF of the proposed filter of Fig. 8(a) is derived in (9), as shown at the bottom of the page.

To examine the efficacy of the proposed local LPF technique, its derived analytical TF is compared with that of the conventional second-order IIR filter of Fig. 8(c), whose TF is calculated as

$$
H^{(2)}_{\text{conv}}(z) = \frac{V_{\text{out}}(z)}{Q_{\text{in}}(z)} = \frac{1}{C_S}z^{-\frac{1}{3}}\left(\frac{(1-\alpha)}{1-\alpha z^{-1}}\right)^2
\tag{11}
$$

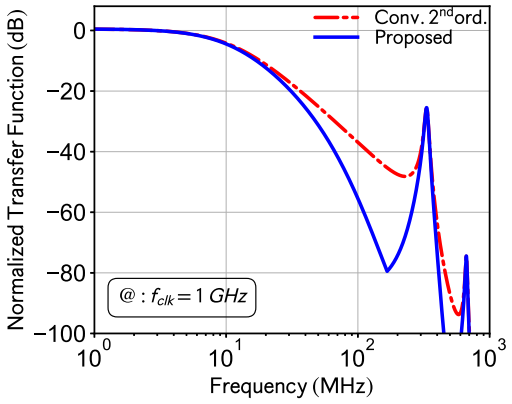

Fig. 10. Analytical TF of second-order IIR filter with proposed local LPF compared to TF of conventional second-order IIR filter ($\alpha = 0.9$, $\alpha_{o1} = \alpha_{o2} = \alpha_{o3} = 0.5$, $f_{\text{clk}} = 1$ GHz, and $N = 3$, thus $f_s = 333.3$ MHz).

where α is defined as $C_H/(C_H + C_S)$. Fig. 10 compares the two TFs where for both filters the same factor $\alpha = 0.9$ is chosen. Moreover, the coefficients $\alpha_{o1} = \alpha_{o2} = \alpha_{o3} = 0.5$ and a clock reference frequency, $f_{\text{clk}} = 1$ GHz (i.e., the sampling frequency of $f_s = f_{\text{clk}}/3$) are chosen. Furthermore, to enable a fair comparison between the concepts, the same BW is constrained. Nonetheless, it is evident that the stopband rejection of the proposed filter drastically outperforms the conventional one due to the local LPF employed. Hence, by changing the history capacitors gradually, the skirt of the filter is dramatically enhanced while maintaining the same f_s as in the conventional filter. When attempting to obtain the same skirt with the conventional filter, more phases and a reduction of f_s would be needed. It is worth mentioning that as all poles are real, rejection around the roll-off frequencies does not improve significantly (i.e., it is quite similar as in the prior-art structure in [15]).[2]

Lastly, we would like to remind that the pseudo-triangular time window integration scheme of the sampling capacitor is not yet applied in this example. Hence, for both the proposed and conventional second-order CS IIR filter [Fig. 8(a) and (c), respectively], only the $\text{sinc}(\pi f/f_s)$ anti-aliasing filtering is achieved.

D. Proposed Low-Pass Filter

By combining the two introduced techniques, we arrive at the proposed LPF in Fig. 11. It is based on the conventional fourth-order filter ($N = 5$) of Fig. 4(a) as a foundation.

[2]As demonstrated in [15], a digital post-emphasis equalizer can sharpen the transient band to rectify this issue while still offering the overall benefits of filtering, noise, and power efficiency.

$$
H^{(2)}(z) = \frac{V_{23}(z)}{Q_{\text{in}}(z)} \approx \frac{\beta}{C_S}\left(\frac{(1-\alpha)\alpha_3\alpha_2\alpha_1 z^{-1/3}}{\left(1-\alpha z^{-1}\right)\left(1-\alpha_{o3}z^{-1/3}\right)\left(1-\alpha_{o2}z^{-1/3}\right)\left(1-\alpha_{o1}z^{-1/3}\right)}\right)^2
\tag{9}
$$

$$
H^{(4)}(z) \approx \frac{\beta}{C_S}\left(\frac{(1-\alpha)\alpha_3\alpha_2\alpha_1 z^{-1/5}}{\left(1-\alpha z^{-1}\right)\left(1-\alpha_{o3}z^{-1/5}\right)\left(1-\alpha_{o2}z^{-1/5}\right)\left(1-\alpha_{o1}z^{-1/5}\right)}\right)^4
\tag{10}
$$

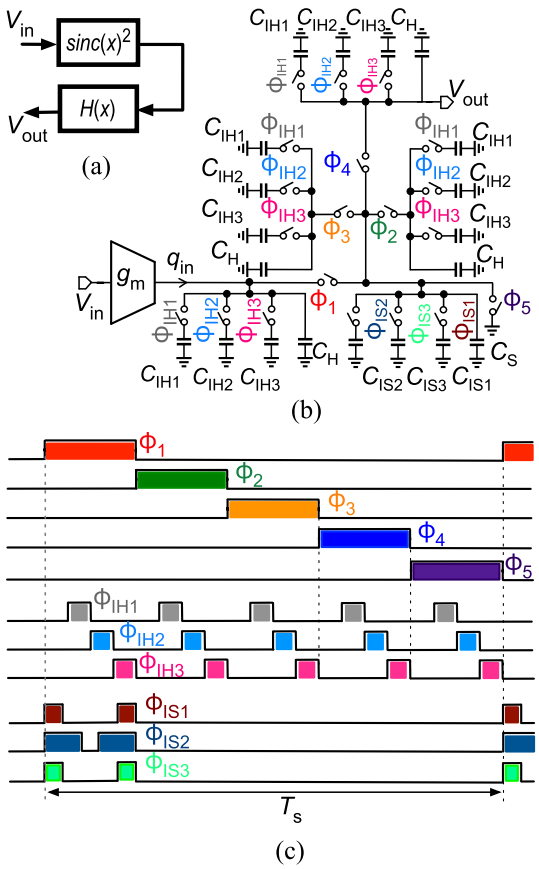

Fig. 11. Proposed IIR filter: (a) provided filtering, (b) schematic (i.e., by applying both proposed techniques: #1 pseudo-triangular window integration (see Fig. 5), #2 local LPF [see Fig. 7)], (c) timing scheme.

It replaces the fixed history and sampling capacitors of the conventional scheme with the proposed dynamically re-engaged C_H and C_S capacitors. The sub-phases $\phi_{\text{IS1}-3}$ are used to change the sampling capacitor in a way somewhat similar to that by $\phi_{\text{IH1}-3}$. All phases are carried out within one sampling period T_s, resulting in the sampling rate of $f_s = 1/T_s$. The clocking scheme for enabling the primary history capacitors, the dynamically re-engaged history capacitors, and the constituent sampling capacitors is plotted in Fig. 11(c). It should be pointed out that the sampling frequency can be readily extended via the interleaving technique introduced in [15]. With $N = 5$ interleaved paths, the sinc^2 notches will be placed at the new sampling frequency and its harmonics.

The TF of the proposed filter is approximately calculated as (10), shown at the bottom of the previous page, by following the same derivations as outlined above for the second-order LPF. It is compared with the TF of the conventional fourth-order CS IIR filter in Fig. 12. Referring back to Fig. 10, a further improvement around the sampling frequency and its harmonics can be observed. Due to the additional pseudo-triangular time window integration, further damping of around 25 dB can be realized. As explained, the charge is not delivered to the output uniformly; it is conveyed in multiple steps (four steps in this case) at a fraction of the sampling period, like in an L-fold linear interpolation [32]. Hence, the anti-aliasing TF mimics sinc$^2(\pi f/f_s)$ for values of L greater than 2.

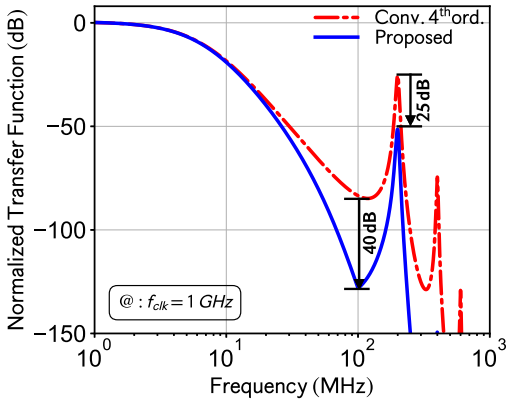

Fig. 12. TF of the proposed fourth-order-based IIR filter compared to TF of conventional fourth-order IIR filter ($\alpha = 0.9$, $\alpha_{o1} = \alpha_{o2} = \alpha_{o3} = 0.5$, $f_{\text{clk}} = 1$ GHz, and $N = 5$, thus $f_s = 200$ MHz).

It is important to emphasize that the same sampling frequency is used for the proposed fourth-order-based LPF as for the conventional one while achieving significantly better filtering characteristics. A much higher order of filtering of the conventional structure would be needed to match the newly reached performance, leading to an increase in the number of phases. Consequently, this would require increasing the sampling period T_s, respectively, decreasing the sampling frequency f_s if the same fixed duration of the individual phases is maintained. By means of calculating the slope of the proposed filter around its skirt, the conventional design's order should be increased to seventh just to now match the performance. Hence, eight phases would be required, decreasing the sampling frequency to 0.625 of the initial one.

III. Circuit Implementation

The proposed DT LPF with the improved filtering is constructed using g_m-cells, switches, capacitors, and rail-to-rail clock waveform generator circuitry. It is, therefore, amenable to the digital deep nanoscale CMOS technology, whereby each new technology node will improve the speed and area of these building blocks.

The implemented schematic is depicted in Fig. 13. The differential input v_I is converted to a current by the pseudo-differential ac-coupled inverter-based g_m-cell. A bias voltage V_{B1} to the pMOS transistors is supplied externally. The common-mode output of the g_m-cell is set to $V_{\text{DD}}/2$ by the common-mode feedback (CMFB) circuit. AC-coupling capacitors (C_c) and bias resistors (R_B) define a lower limit of the frequency response. By choosing sufficiently large C_c and R_B, the corner frequency of this high-pass filter (HPF) is low enough to measure its TF for the minimum designed BW (i.e., 900 kHz). The device dimensions of the g_m-cell components are shown in Table I.

The generated current is integrated into the corresponding time-varying history capacitor, $C_{\tilde{H}} = C_H + C_{\text{IH1}-3}$, and shared with the time-varying sampling capacitor, $C_{\tilde{S}} = C_S + C_{\text{IS1}-3}$. Capacitor $C_{\tilde{S}}$ samples the charge during the sampling phase of the IIR filter (i.e., ϕ_1) while its value changes during the sub-phases, as discussed in Section II-D. In each phase,

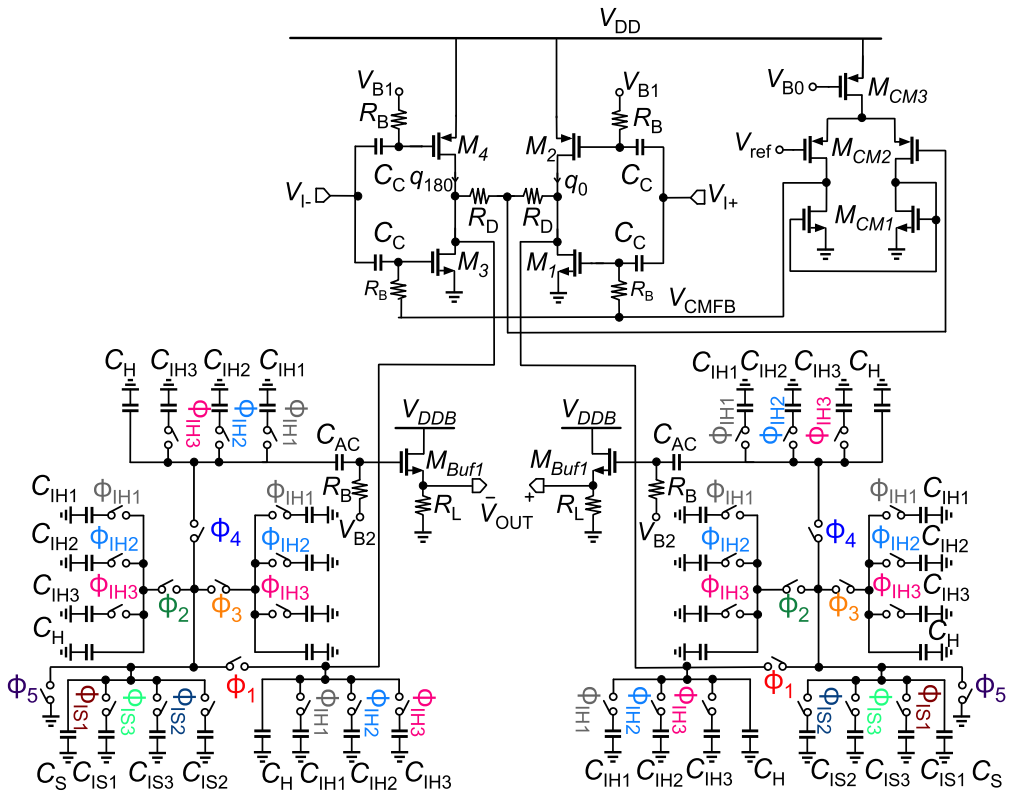

Fig. 13. Full circuit implementation of the proposed LPF. (The clock circuitry is shown in Fig. 14.)

TABLE I
DEVICE DIMENSIONS OF THE g_m-CELL

$M_{2,4}$	(1.2 μm/200 nm)×20	$M_{1,3}$	(0.6μm/200 nm)×20
M_{CM3}	(1μm/500 nm)×24	M_{CM2}	(0.7μm/1 μm)×4
M_{CM1}	(1μm/1 μm)×1	R_D	33 kΩ
R_B	450 kΩ	C_c	5.5 pF

$C_{\tilde{S}}$ shares the charge with other $C_{\tilde{H}}$'s. Finally, during the last phase, C_S is reset. Because the reset occurs only once per sampling period, the overall noise degradation is kept to a minimum, thus improving the SNR. Moreover, the BW of the filter is precisely defined based on the capacitor ratio (i.e., $C_{\tilde{S}}/C_{\tilde{H}}$) and sampling frequency f_s. It could approximately be calculated based on a CT TF of IIR filter introduced in [15] as $f_c = C_S f_s/(2\pi C_H)$. By providing the control bits for both history and sampling capacitors, the BW of the filter is fully tunable.

Metal–oxide–metal (MOM) capacitors are used for all history and sampling capacitors with the standard metal interconnect layers providing excellent matching. They are implemented as two single-ended capacitors for each differential path. It is worth mentioning that the parasitic capacitances might slightly change the size of C_Hs and C_S, consequently affecting the filter's BW. These parasitics are much smaller than C_Hs and C_S (50 fF). However, one of the critical features of the proposed DT IIR filter is its tunability. By changing the control bits of C_Hs and C_S, any changes in BW due to the parasitics can be compensated.

Fig. 14 illustrates the clock generator circuitry. The input sinewave signal at 2 GHz is injected into the waveform generator through the buffer. It converts the sinewave signal to square-wave through M_{B1-4}. By utilizing two rail-to-rail inverters, with the first stage being self-biased with a resistor of approximately 50 kΩ, the input sinewave becomes a square wave. The transistor sizes in both stages are the same. They are chosen by considering the trade off between power consumption and sufficient strength to load the parasitic capacitance of the loading stage. Two sets of dividers utilizing the 50% duty-cycle square-wave signals are needed to produce three different sets of clock phases, including five main phases (i.e., ϕ_1, ϕ_2, ϕ_3, ϕ_4, ϕ_5) for the main functionality of the filter, three sub-phases for incrementally changing $C_{\tilde{H}}$ (i.e., ϕ_{IH1}, ϕ_{IH2}, ϕ_{IH3}), and three sub-phases to dynamically vary the value of $C_{\tilde{S}}$ (i.e., ϕ_{IS1}, ϕ_{IS2}, ϕ_{IS3}). Both dividers are based on rail-to-rail circulating D-flip-flops. The first divider consists of three D-flip-flops and combinatorial logic to create the sub-phases for $C_{\tilde{H}}$ and $C_{\tilde{S}}$. The second divider consists of 20 D-flip-flops to create the five main phases, as shown in Fig. 14. Table II shows the transistor sizes used in the clock generator circuitry.

Finally, an on-chip output test buffer is used to drive the 50-Ω load of the measurement equipment. As shown in Fig. 13, the output buffer consists of the pseudo-differential source-follower amplifiers, each utilizing $R_L = 50\ \Omega$ resistor at its source. The transistors are wide long-channel devices to provide minimum loss. Moreover, the ac-coupling capacitor,

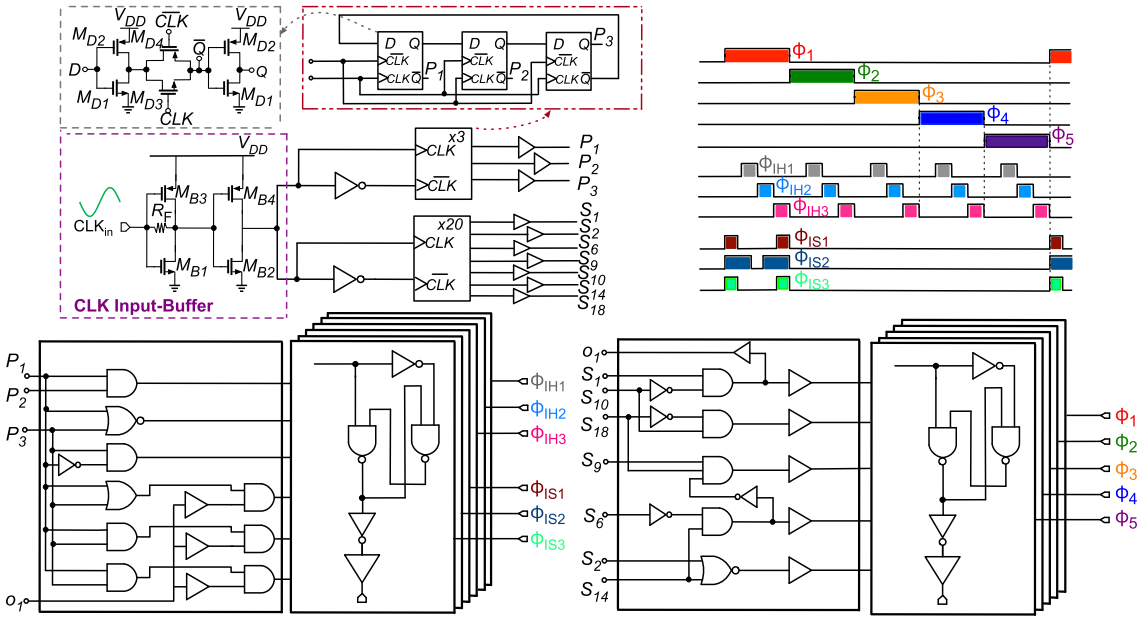

Fig. 14. Circuit schematic of the clock generator circuitry.

TABLE II
DEVICE DIMENSIONS OF THE CLOCK INPUT BUFFER AND D-FF OF THE CLOCK GENERATOR

$M_{B1,2}$	(0.6 μm/30 nm)×4	M_{D1}	(0.5μm/30 nm)×1
$M_{B3,4}$	(1μm/30 nm)×4	M_{D2}	(0.78 μm/30 nm)×1
R_F	50 kΩ	M_{D3}	(1.5μm/30 nm)×1
–	–	M_{D4}	(1μm/30 nm)×1

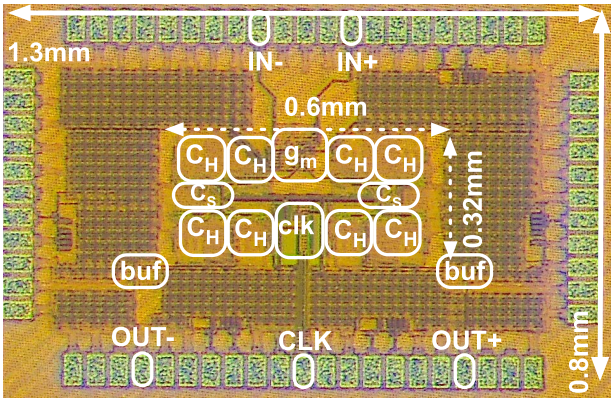

Fig. 15. Chip micrograph.

C_{ac}, and its bias resistor, R_B, at the filter's output create an HPF with a 500-kHz cutoff frequency.

IV. EXPERIMENTAL RESULTS

The proposed filter is realized in TSMC 28-nm LP CMOS. Fig. 15 shows the chip micrograph. The total chip area is 1.04 mm^2, with the active area occupying only 0.192 mm^2. All CS capacitors are implemented as binary-controlled

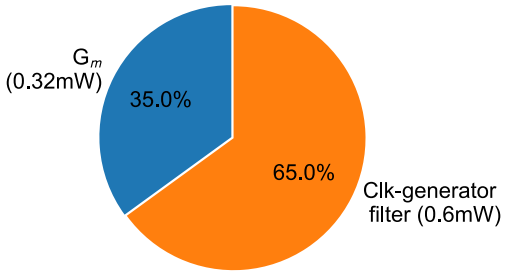

Fig. 16. Power break-down.

MOM capacitors. To provide BW tunability, four, three, and two bits are used for C_H, C_S, and C_{IH}, respectively. This tunes the range from 1 to 19 pF for C_H, from 0.5 to 4 pF for C_S, and from 1 to 6 pF for C_{IH}.

The filter is supplied at 0.9 V and consumes 0.92 mW in total. The power breakdown is illustrated in Fig. 16, where the g_m-cell and 2-GHz waveform generator drain 0.32 and 0.60 mW, respectively. In addition, the power consumption of the external interface circuitry: input clock buffer and test output buffers are 1 and 7 mW, respectively.

The non-normalized TF of the proposed filter is illustrated in Fig. 17. The measured dc gain is 14.7 dB.

Fig. 18 shows the measured normalized TFs in the proposed and conventional modes. To keep the 3-dB BW of both modes identical, the size of the history capacitors (C_H) in the conventional mode is chosen larger than the composite $C_{\tilde{H}}$ in the proposed mode. As indicated, the out-of-band rejection improves by >20 dB.

To demonstrate the filter's tunability, the TF was measured for different values of the history capacitor. In fact, we keep C_S constant and change the size of the history capacitors. For having wider BW, the smaller history capacitors are used.

TABLE III
SUMMARY AND COMPARISON WITH STATE-OF-THE-ART FILTERS

	This work	[15] JSSC'14	[20] ISSC'17	[17] VLSI'17	[21] ESSCIRC'18	[16] TCASI'18	[19] JSSC'20	[22] JSSC'20
Topology	CS-IIR	CS-IIR	FBA	CS-IIR	FSF	CS-IIR	AFIR	CSF
Technology [nm]	28 CMOS	65 CMOS	65 CMOS	130 CMOS	28 CMOS	180 CMOS	22 FDSOI	180 CMOS
Order	4th	7th	4th	3th	4th	4th	–	5th
Pole types	Real	Real	Real	Real & Complex	Complex	Complex	Real	Real & Complex
BW [MHz]	1∼9.9	0.4∼30	2.5∼40	0.54	100	0.49∼13	0.06∼3.4	20
Max Stop-band Reject. [dB]	120	100	70	45**	60**	100	70**	80**
Gain [dB]	14.7	9.3	23	–	-2.6	17.6	31.5	0
IRN [$nV/\sqrt{Hz}$]	3.5	4.57	–	23.3	8***	6.54	12	15.3
IB IIP3 [dBm]	+17.7	+16	+8	–	+2.5∼+12.5	+11.1	–	+11.5∼+24.5
OB IIP3 [dBm]	+26.6	–	+21	+55.1	–	+15	-3.5*	–
VDD [V]	0.9	1.2	1.2	1.2	1	1.8	0.7	1.3
Power [mW]	0.92	1.96	76.8∼ 100.8	0.15	0.97	4.3	0.092	0.65
Active area [mm^2]	0.192	0.42	0.23	0.06	0.026	2.9	0.09	0.12

* Calculated from reported OIP3 in dB as IIP3 = OIP3 − Gain; ** Estimated from figure; *** Simulated result.

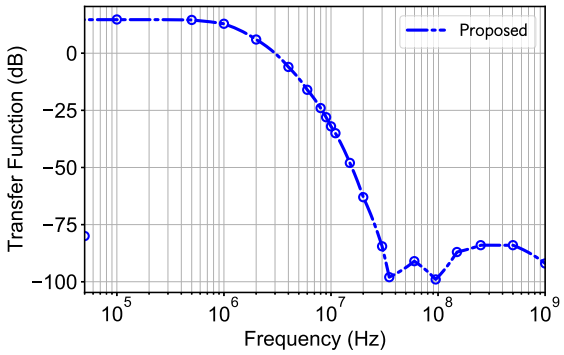

Fig. 17. Measured gain of filter (non-normalized TF).

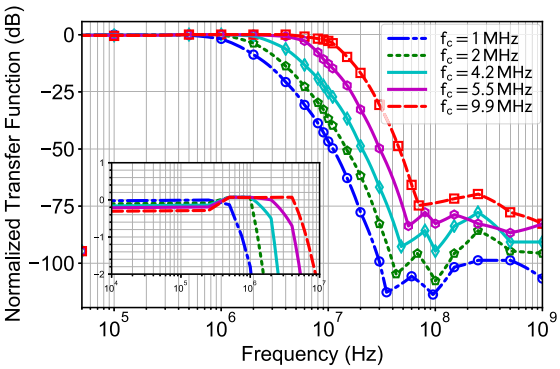

Fig. 19. Measured normalized TFs: BW programmability.

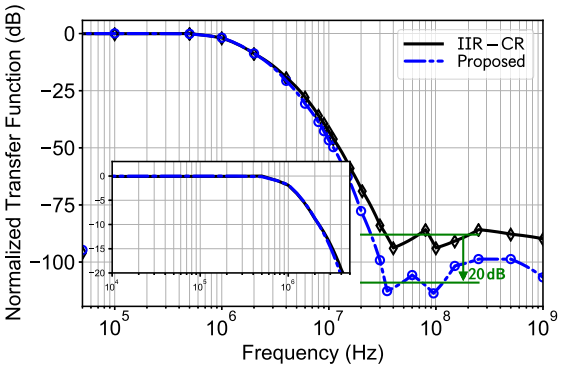

Fig. 18. Measured normalized TFs in two filtering modes: conventional [see Fig. 4(a)] and proposed for the 3-dB BW of 1 MHz.

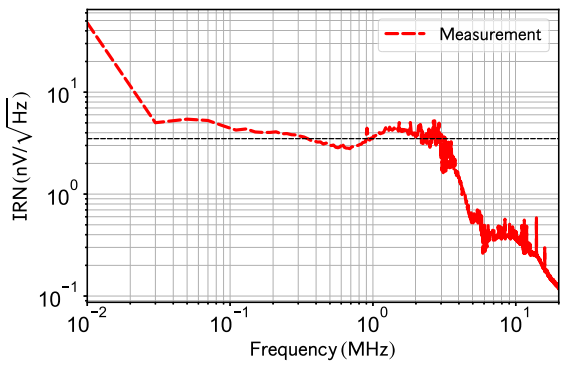

Fig. 20. Measured input-referred noise of the filter.

As a result, the stopband rejection decreases for wider BW. Fig. 19 shows the 3-dB BW programmability of 1–9.9 MHz.

Fig. 20 illustrates the measured input-referred noise (IRN) of the proposed filter. The flicker noise of the g_m-cell at the lower frequencies causes the higher noise while the kT/C noise is shaped by the filter's TF at the higher frequencies.

The in-band (out-of-band) IIP3 is measured in Fig. 21 using a two-tone test at 5 and 6 MHz (100 and 110 MHz). The achieved in-band (out-of-band) IIP3 is +17.7 dBm (+26.63 dBm).

The performance of the proposed filter is summarized in Table III and compared to state-of-the-art LPFs. It achieves a record-high stopband rejection of 120 dB while providing best-in-class linearity and noise performance. Tohidian *et al.* [15] achieves a 100-dB stopband attenuation by using seventh-order filtering, but it requires more clock phases and consumes

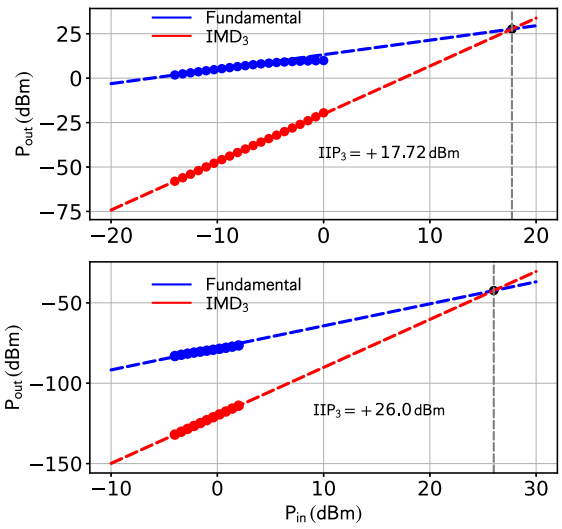

Fig. 21. Measured IIP3: (top) in-band and (bottom) out-of-band.

twice the power. Besides featuring the best stopband rejection, the proposed filter maintains better in-/out-of-band linearity, power consumption, and noise performance than [20] and [16]. Although [19] achieves higher gain and lower power consumption using an AFIR filtering technique, its linearity, and noise performances are significantly worse.

V. Conclusion

A new low-pass IIR filter was introduced and experimentally verified in 28-nm CMOS. It adopts the $\text{sinc}^2(\pi f/f_s)$ anti-aliasing filtering alongside the new local LPF in each phase that greatly enhances the stopband rejection. It achieves the best stopband rejection ever reported while maintaining the same duty cycle for the sampling clock as in a conventional CS-IIR filter design. It also allows for an easy tunability of its BW through the control bits. As a result, the proposed LPF architecture, which takes advantage of technology scaling, can be readily employed as a suitable candidate for various challenging applications, such as in DT cellular receivers.

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