A Wideband IQ-Mapping Direct-Digital RF Modulator for 5G Transmitters

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***Abstract*— This article presents a wideband 2 × 12-bit direct-digital RF modulator (DDRM) operating in a 0.5-to-3-GHz band for 5G transmitters. The proposed digital Cartesian modulator features an advanced IQ-mapping technique to boost RF power by 3 dB and suppress the I/Q image. To verify the proposed concept, a 40-nm CMOS prototype is implemented whose RF peak output power at 2 GHz is more than 14 dBm. It achieves an adjacent-channel leakage ratio (ACLR) of −52 dBc and an error vector magnitude (EVM) of −40 dB for a 20-MHz 256-QAM signal at 2.4 GHz. With a 320-MHz 256-QAM signal, the measured ACLR and EVM performances are better than −43 dBc and −32 dB at 2.4 GHz, respectively, without using any digital pre-distortion.**

***Index Terms*— Current-steering digital-to-analog converter (DAC), digital pre-distortion (DPD)-free, digital-intensive transmitter (DTX), direct-digital RF modulator (DDRM), I/Q image, IQ-mapping, mixing DAC, PA pre-driver, quadrature up-converter, radio-frequency digital-analog converter (RFDAC).**

I. Introduction

NOWADAYS, wireless cellular communication is stepping into its fifth generation (5G), driven by the demand for faster mobile access and higher throughput. 5G applications utilize larger modulation bandwidth and higher order modulation schemes, requiring higher system efficiency, flexibility, and integration in transmitter (TX) design. An essential building block in the TX system is the RF modulator that converts baseband data to an RF signal. Fig. 1(a) depicts a traditional analog up-converter [1]–[5]. It consists of a pair of baseband digital-to-analog converters (DACs), low-pass filters (LPFs), and mixers. This architecture can handle large modulation bandwidth due to its linear summation of the in-phase (I) and quadrature (Q) signals. In recent years, digital-intensive TXs (DTXs) have been a popular research direction. Among various DTXs' architectures, the direct-digital RF modulators (DDRMs) [6]–[19] are rapidly gaining popularity due to their power-efficient mixing operation, inherent compatibility with nanoscale CMOS, compact area, and frequency-agile

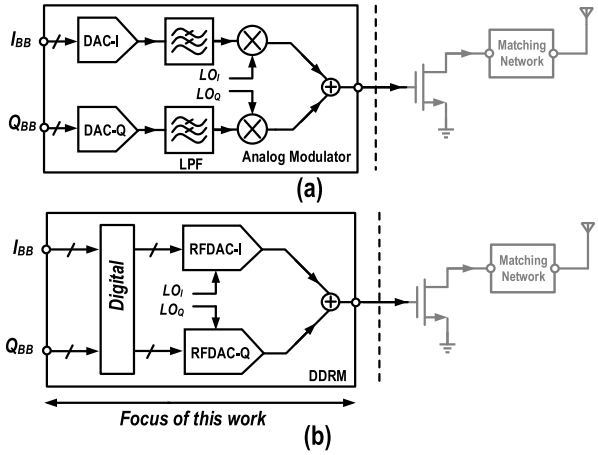

Fig. 1. (a) Conceptual diagram of conventional analog up-converters in [1]–[5]. (b) Conceptual diagram of DDRM in [6].

operation. Meanwhile, it also avoids linearity degradation in other blocks, such as IQ up-converting mixers. Fig. 1(b) shows the DDRM concept. This DDRM consists of a pair of current-steering I/Q mixing DACs [radio-frequency digital-analog converters (RFDACs)], which are derived from the Gilbert Cell. In this configuration, the unsigned complementary baseband signals I_{BB} and Q_{BB} are interpolated in the digital domain to adequately suppress the sampling spectral replicas. The resulting high-speed data streams are subsequently up-converted to orthogonal I and Q RF signals by current-steering RFDACs using quadrature clocks. Eventually, these I and Q signals are summed. Unfortunately, existing DDRMs with these operation principles still confront some challenges.

First, as shown in Fig. 2(a), similar to analog modulators, conventional DDRMs are typically realized using two (separate) RFDACs. Consequently, an I/Q mismatch is present, yielding an unwanted I/Q image component in the output spectrum [20]. To mitigate this problem, an IQ-sharing topology is proposed [21], in which I and Q RFDACs share the same unit cells. Nonetheless, this technique requires non-overlapping quadrature clocks (i.e., are 25% duty-cycle clocks), yielding less RF output power. Furthermore, the dominant culprits degrading spectral purity of 25% duty-cycle systems are duty-cycle/phase errors, which are significantly more difficult to achieve in these configurations than 50% duty-cycle clocks, especially at high LO frequencies.

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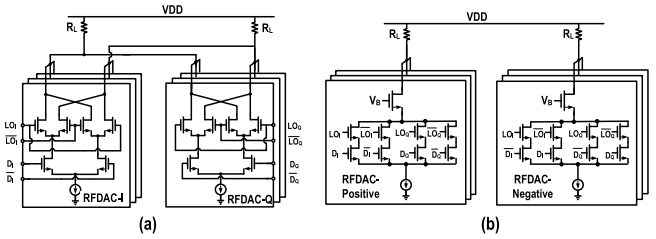

Fig. 2. Detailed schematic of (a) conventional DDRM [6] and (b) IQ-interleaving DDRM [9].

Second, although the IQ-interleaving DDRM proposed in [9] [see Fig. 2(b)] can suppress odd-order distortion, it still employs two current-mode XOR/XNOR complementary IQ RFDACs with two separate sets of current sources for differential operations. Therefore, any mismatch between these two sets of current sources leads to even-order distortion. Furthermore, its current-mode XOR operation inside unit cells results in output current pulses with a duty-cycle of 75%. It exacerbates the finite settling time, limiting the achievable linearity performance for wideband signals. Meanwhile, in Fig. 2(b), the current sources have to switch ON/OFF every RF cycle, leading to memory effects and degraded linearity performance.

Recently, an advanced, low-complexity IQ-mapping technique that improves the output power and image rejection of a Cartesian DDRM has been proposed in [22]. This article investigates architectural analysis and elaborates on the system- and circuit-level design considerations and extensive measurement results. This article is organized as follows. Section II focuses on the causes yielding an increased I/Q image in conventional DDRMs. Section III introduces the proposed IQ-mapping technique and gives theoretical support for its improved image suppression and enhanced output power. Its circuit implementation is given in detail in Section IV. Section V presents the measurement results and compares the proposed DDRM with state-of-the-art modulators. Section VI concludes this article.

II. Causes for I/Q Image Degradation in Conventional DDRMs

In conventional DDRM implementations, three sources degrade the I/Q image rejection: first, the phase mismatch of the quadrature-phase LO generation; second, amplitude mismatch of the current sources in the RFDACs due to geometry and doping differences among unit cells; and third, delay mismatch of the data and LO clock signals among the RFDACs' unit cells. These three types of image sources are visualized in Fig. 3. The phase error in Fig. 3(a) is caused by the LO generation circuits, while the delay mismatch in Fig. 3(b) is due to the LO distribution network and varies among unit cells. A single-tone operation is used here to quantify the image-rejection performance. Consequently, the I and Q signals at the RF output are ideally

$$\begin{cases} x_I = \cos(\omega_{\mathrm{LO}}t)\cos(\omega_{\mathrm{BB}}t) \\ x_Q = \sin(\omega_{\mathrm{LO}}t)\sin(\omega_{\mathrm{BB}}t) \end{cases} \tag{1}$$

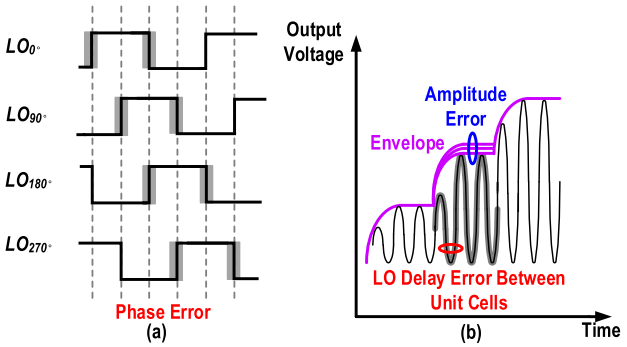

Fig. 3. (a) Phase error in LO generation circuits. (b) Amplitude and phase errors in RFDACs.

respectively, where ω_{LO} is the angular frequency of the LO signal and ω_{BB} is the angular frequency of baseband signal.

Assume that the transfer functions of the I and Q branches of the DDRM are equal to

$$\begin{cases} I(x_I) = a_1 x_I + a_3 {x_I}^3 + a_5 {x_I}^5 + \cdots \\ Q(x_Q) = b_1 x_Q + b_3 {x_Q}^3 + b_5 {x_Q}^5 + \cdots \end{cases} \tag{2}$$

where a_n and b_n are coefficients of a memoryless nonlinear representation. There are no even-order terms in (2) due to the differential nature of DDRM. In the case of a phase error θ_{Err} between LO_I and LO_Q, assuming that there is no mismatch in their amplitude transfer function between two branches, the related I/Q image due to the θ_{Err} is equal to [20]

$$\mathrm{Image}_{\mathrm{phase}} = 10\log_{10}\left|\frac{1-\cos\theta_{\mathrm{Err}}}{1+\cos\theta_{\mathrm{Err}}}\right|. \tag{3}$$

If only an offset in linear gain coefficient (a_1 and b_1) exists in (2), assuming that there is no phase error and higher order non-linearity, the resulting I/Q image can be expressed as

$$\mathrm{Image}_{\mathrm{gain}} = 20\log_{10}\left|\frac{a_1-b_1}{a_1+b_1}\right| \tag{4}$$

which is derived by replacing (1) into (2) and performing some mathematical calculations. The impact of the higher order terms will be discussed in Section III.

The delay mismatch due to the LO distribution network and buffers can vary for each unit cell due to imperfections. Delay sources are asymmetries in the layout or delay mismatch in the logic gates, as well as its exposure to (external) interfering signals. As a result, the coefficients of the (2) can become complex, representing both amplitude and delay mismatches. It should be noted that, in practical situations, a background calibration can track the process, voltage, and temperature (PVT) variations in the current cells since they are referred to as "slow error." However, it is not trivial to do a background calibration for these delay mismatches, and consequently, randomization techniques are used in [23] and [24] to suppress these errors.

In analog-intensive up-converters, auxiliary calibration circuits are often added to calibrate out amplitude and phase errors [3], [25]. Their underlying principle is mainly based on digital signal processing (DSP) techniques that use an FFT on the down-converted TX signal and utilizes input baseband

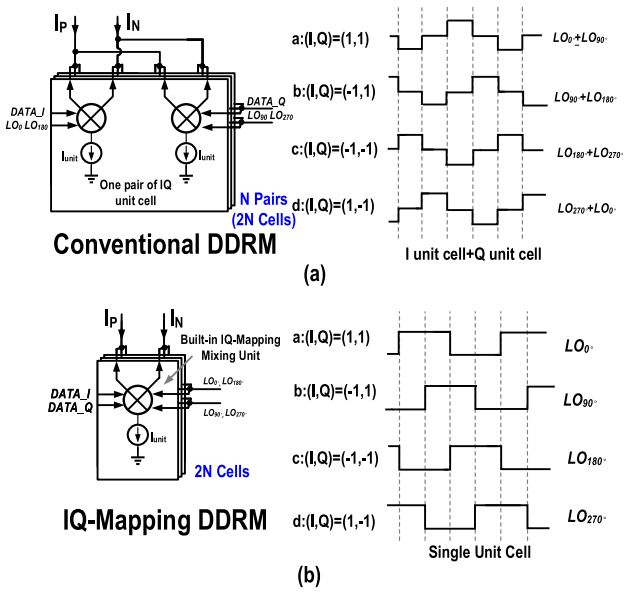

Fig. 4. (a) Conceptual diagram and waveforms of one pair of unit cells in conventional DDRMs. (b) Conceptual diagram and waveforms of one single unit cell in the proposed IQ-Mapping DDRM.

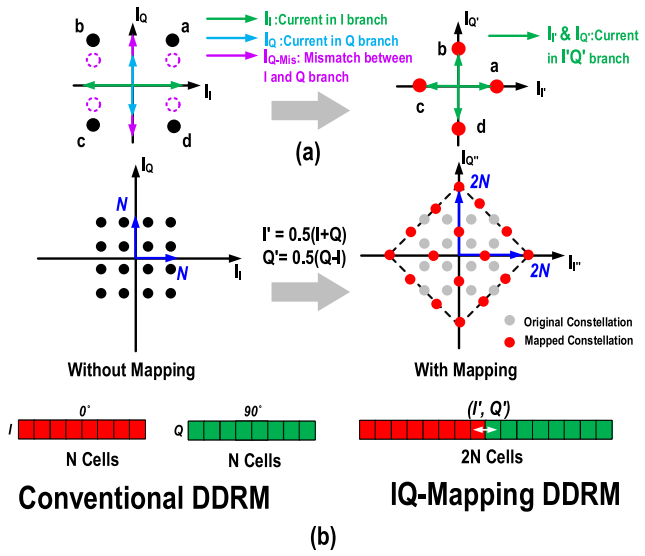

Fig. 5. Current constellation diagram of (a) unit cells and (b) overall unit-cell array in conventional DDRMs and IQ-Mapping DDRMs.

data adaptation until the TX signal's image suppression meets the requirement. Typically, several iterations are needed to reach the optimal point. This latter approach increases TX complexity, e.g., requiring an extra down-conversion step and ADCs. In Section III, a low-cost IQ-mapping technique is proposed to inherently cancel the I/Q image.

III. IQ-Mapping Technique

A. Concept

To improve the DDRM performance in terms of RF output power, modulation bandwidth, and, most importantly, in-band linearity, a novel IQ-mapping technique has been proposed in [22]. It relies on using an interleaved IQ DDRM that utilizes 50% duty-cycle LOs to drive its unit cells. At the highest output current drive level, all unit cells operate on the same phase, which strongly reduces the I/Q interaction and increases its effective RF fundamental output current. To understand the benefits of the proposed topology, the conventional DDRM architecture in Fig. 4(a) should be considered first. For each IQ unit-cell pair, the four constellation points translate to the four waveforms shown on the right. After vector summation, the resulting fundamental of these four waveforms in Fig. 4(a) is given in the following:

$$\begin{cases} \mathscr{F}[\mathrm{OUT}_a](\omega_{\mathrm{LO}}) = \mathrm{Sa}(\omega_{\mathrm{LO}}) \times \left(\sqrt{2} \times e^{j\pi/4}\right) \times e^{j0} \\ \mathscr{F}[\mathrm{OUT}_b](\omega_{\mathrm{LO}}) = \mathrm{Sa}(\omega_{\mathrm{LO}}) \times \left(\sqrt{2} \times e^{j\pi/4}\right) \times e^{j\pi/2} \\ \mathscr{F}[\mathrm{OUT}_c](\omega_{\mathrm{LO}}) = \mathrm{Sa}(\omega_{\mathrm{LO}}) \times \left(\sqrt{2} \times e^{j\pi/4}\right) \times e^{j\pi} \\ \mathscr{F}[\mathrm{OUT}_d](\omega_{\mathrm{LO}}) = \mathrm{Sa}(\omega_{\mathrm{LO}}) \times \left(\sqrt{2} \times e^{j\pi/4}\right) \times e^{j3\pi/2} \end{cases} \tag{5}$$

where $\mathrm{Sa}(\omega)$ is the Fourier transform of a 50% square-wave. Equation (5) shows that the maximum amplitude of the fundamental is $2\sqrt{2}/\pi$ occurring at the phases of $\pi/4$, $3\pi/4$, $5\pi/4$, and $7\pi/4$.

The proposed IQ-mapping technique aims to replace the composite signals of (5), with relatively simple 50% duty-cycle square wave signals [see Fig. 4(b)]. To achieve this goal, the IQ-constellation (diagonal points) as provided by conventional DDRM unit cells is mapped to the diamond-shaped $I'Q'$-constellation, as shown in Fig. 5(a). The related mapping is given as follows:

$$\begin{cases} I = 1 \ \& \ Q = 1 \ \Rightarrow \ I' = 1 \ \& \ Q' = 0 \\ I = -1 \ \& \ Q = 1 \ \Rightarrow \ I' = 0 \ \& \ Q' = 1 \\ I = -1 \ \& \ Q = -1 \ \Rightarrow \ I' = -1 \ \& \ Q' = 0 \\ I = 1 \ \& \ Q = -1 \ \Rightarrow \ I' = 0 \ \& \ Q' = -1 \end{cases} \tag{6}$$

where (I', Q') is the vector after the mapping operation. Note that the original vector (I, Q) needs two unit current sources, while its new phase mapped vector (I', Q') needs only one unit current source for its representation. This IQ-mapping can be extended from a single unit cell to the whole DDRM array. Mathematically, the operation in (6) is the mapping of the traditional I and Q vectors into two new orthogonal vectors

$$\begin{aligned} &\frac{1}{\sqrt{2}}\mathrm{Re}\left[(I + jQ)e^{j\omega_{\mathrm{LO}}t}e^{-\mathrm{j}\pi/4}\right] \\ &\quad = \frac{1}{2}\mathrm{Re}\left[(I + jQ)(1 - j)e^{j\omega_{\mathrm{LO}}t}\right] \\ &\quad = 0.5 * \mathrm{Re}\left[((I + Q) + j(Q - I))e^{j\omega_{\mathrm{LO}}t}\right]. \end{aligned} \tag{7}$$

The scaling factor of $(1/\sqrt{2})$ stems from the fact that the vector norm after mapping is scaled by $(1/\sqrt{2})$ compared to its original vector norm. Namely, I' and Q' can be expressed as

$$\begin{cases} I' = 0.5 \cdot (I + Q) \\ Q' = 0.5 \cdot (Q - I). \end{cases} \tag{8}$$

Equation (8) indicates that it would only need half the number of unit current sources than a conventional DDRM implementation.

Two main advantages resulting from the proposed IQ-mapping technique are: 1) better power (efficiency) performance and 2) intrinsic TX-image rejection. These two rather unique properties will be discussed in detail in the following.

B. Improved Output Power and Efficiency

Compared to prior-art DDRMs, for a given drain current budget, the proposed IQ mapping technique enhances its peak output power and efficiency twofold. Namely, if $2N$ unit cells are available for representing I and Q in conventional DDRMs, this would yield a maximum fundamental output current at the outer corners of the IQ-constellation diagram of, i.e., vector summation

$$I_{\max IQ} = I_{\text{unit}}|N + jN| = I_{\text{unit}} \cdot \sqrt{2} \cdot N. \tag{9}$$

In contrast, with the proposed IQ-mapping technique [see Fig. 5(b)], at the outer corners of the constellation diagram, all $2N$ cells can be directed to the same output phase. As such, its maximum current budget for these points is

$$I_{\max I'Q'} = I_{\text{unit}} \cdot 2 \cdot N \tag{10}$$

which is, indeed, derived based on scalar summation. Therefore, for the same dc current budget, the proposed IQ-mapping DDRM topology provides a peak RF output power that is 3 dB higher than that of a conventional DDRM. Thus, the drain efficiency could be doubled effectively. Meanwhile, since all $2N$ cells can go for I or Q, the number of bits from (I, Q) to (I', Q') also increases by one. Mathematically, based on (9) and (10), this can also be explained from

$$\left|\left|\left(I_{\max I'}, I_{\max Q'}\right)\right|\right|^2 = 2\left|\left|\left(I_{\max I}, I_{\max Q}\right)\right|\right|^2. \tag{11}$$

C. Intrinsic Image Rejection

In the proposed IQ-mapping technique, the I' and Q' branches employ a single current source and, therefore, are identical in their transfer function. Consequently, the TX image is inherently canceled.

Fig. 5(a) graphically explains the impact of I/Q mismatch inside the unit cells. In conventional DDRMs, a difference in the I and Q current sources [pink arrow in Fig. 5(a) (left)] yields asymmetry/mismatch in the constellation points over the diagonal axis. As a result, the vector will fail to align with the diagonal perfectly. In contrast, the proposed mapping operation requires only one current source. Therefore, the resulting mapped (I', Q') constellation [green arrows in Fig. 5(a) (right)] is symmetric. Consequently, although the vectors' amplitude can be different among unit cells, there is no mismatch inside one single cell.

Therefore, in the IQ-mapping DDRM, the absence of I/Q mismatch enforces that the corresponding polynomial coefficients in (2) become equal

$$a_1 = b_1, \quad a_3 = b_3, \ a_5 = b_5, \ldots \tag{12}$$

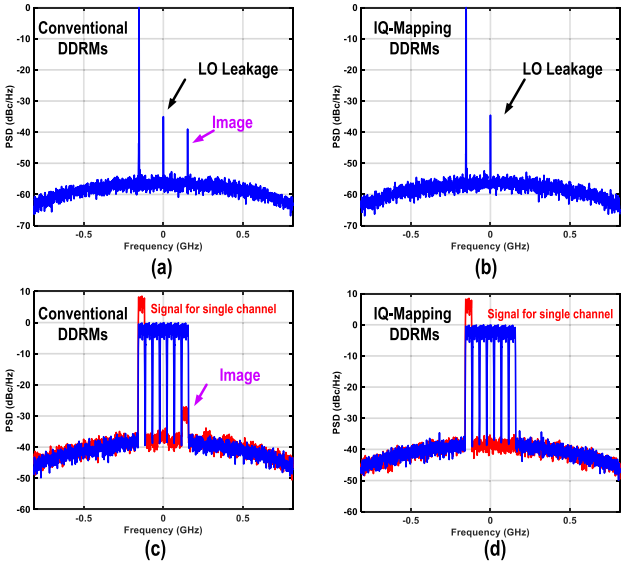

Fig. 6. Simulated spectra in behavior MC simulation with single-sideband signals: (a) conventional DDRMs and (b) proposed IQ-mapping DDRMs. Simulated spectra with the whole multi-carrier signals and one signal channel: (c) conventional DDRMs and (d) proposed IQ-mapping DDRM.

With the single-sideband one-tone signal of (1), the output of the proposed DDRM is

$$\text{OUT}(t) = \sum_{n=1}^{\infty} a_{2n-1}\left[(\cos(\omega_{\text{LO}}t)\cos(\omega_{\text{BB}}t))^{2n-1} + (\sin(\omega_{\text{LO}}t)\sin(\omega_{\text{BB}}t))^{2n-1}\right]. \tag{13}$$

Consequently, when $n = 1$, there is no image component in (4).

To explore if there is still an image created by the higher order terms, the Binomial theorem is applied for each term in (13), yielding a set of tones at

$$(2k-1)\cdot(\omega_{\text{LO}} - \omega_{\text{BB}}) \pm 2\cdot(n-k)\cdot(\omega_{\text{LO}} + \omega_{\text{BB}}) \ (n \geq k) \tag{14}$$

where n and k are integers. According to this derivation, since there is no spurious or image component located at $(\omega_{\text{LO}} + \omega_{\text{BB}})$, the TX image is effectively canceled. The detail of the expansion of (13) can be found in the Appendix.

Monte Carlo (MC) simulations of the whole DDRM confirm the effectiveness of this cancellation. Fig. 6(a) shows a typical spectrum for a conventional DDRM, and Fig. 6(b) exhibits a representative spectrum for an IQ-mapping DDRM when performing these MC simulations with the same mismatch pattern, proving that the IQ image is canceled completely with the proposed IQ-mapping technique. The simulations with multi-carrier signals in Fig. 6(c) and (d) also verify such cancellation. As demonstrated in Fig. 6(c), without mapping technique, the image of a single-channel TX signal can fall inside another channel and, as such, corrupts its SNR. In contrast, with the proposed IQ-mapping technique, there is no image, resulting in boosted in-band linearity. Note that, in Fig. 6(c) and (d), dc calibration is conducted to suppress the LO leakage.

Simulation results of Fig. 6 are performed without considering any phase errors whose impact has been quantified

by (3). In addition, another important source of IQ image is the duty-cycle mismatch among quadrature phases. Assume that the pulsewidth is $T/2 + \Delta t$. Therefore, the fundamental coefficients in the Fourier series of the LO signal are

$$\begin{cases} a_1 = \dfrac{2}{T}\displaystyle\int_0^{T/2+\Delta t} \cos(\omega_{\rm LO} t)dt \approx -\frac{2}{\pi}\frac{\omega_{\rm LO}\Delta t}{2} \\ b_1 = \dfrac{2}{T}\displaystyle\int_0^{T/2+\Delta t} \sin(\omega_{\rm LO} t)dt \approx \frac{2}{\pi}. \end{cases} \tag{15}$$

The phase error $\Delta\theta_{\rm dc}$ and the normalized amplitude error $\Delta\rho_{\rm dc}$ caused by the LO duty-cycle mismatch are

$$\begin{cases} \Delta\theta_{\rm dc} = \arctan\left(-\dfrac{\Delta t\omega_{\rm LO}}{2}\right) \approx -\dfrac{\omega_{\rm LO}\Delta t}{2} \\ \Delta\rho_{\rm dc} \approx \left(\dfrac{\omega_{\rm LO}\Delta t}{2}\right). \end{cases} \tag{16}$$

The resulting IRR with LO duty-cycle mismatch can be obtained by substituting (16) into (3) and (4). Therefore, the duty-cycle mismatch among quadrature phases is as important as the phase mismatch among them.

In summary, although the IQ-mapping technique can cancel the image caused by amplitude mismatch effectively, it still needs accurate quadrature phases in practice. By utilizing high-performance phase-locked loop (PLL) and quadrature dividers with the appropriate layout, the phase error can be adequately minimized.

D. Comparison With IQ-Sharing Techniques

The proposed IQ-mapping technique is different from previous digital PA (DPA) IQ-sharing techniques reported in the literature [21], [26]–[31]. Namely, in [21], 25% duty-cycle clocks are deployed to avoid overlap among the quadrature clocks. The use of non-overlapping clock schemes, in theory, mitigates IQ-interaction and facilitates achieving better linearity performance. However, it leads to less RF output power than its 50% duty-cycle counterpart. Besides, the use of asymmetrical 25% duty-cycle clocks yields linearity limitations in practical DDRM implementations and requires TX calibration and digital pre-distortion (DPD) when supporting large modulation bandwidth.

In [26] and [27], to boost output power and efficiency, also, a diamond-shaped constellation diagram with 50% duty-cycle clocks is employed. However, in contrast to our work, signed IQ data was used, so the related I and Q cannot occupy a single unit cell simultaneously, yielding I/Q mismatch again. Furthermore, in [26] and [27], pre-processing of the baseband data is required, which was implemented by clipping the data [26] or by piecewise decoding [27]. Those solutions increased system complexity and the overall TX line-up power consumption. Besides, such operations resulted in strong IQ-interaction, and also, DPD was required to maintain the linearity [26].

Compared with these works, the IQ-mapping technique in this work is applied in a linear current-steering DDRM using unsigned IQ data as input. First, the (I, Q) to (I', Q') mapping has been implemented within the DDRM unit cells, as such, avoiding any (extra) signal processing overhead. This allows faster data throughput and facilitates operation with a very large modulation bandwidth. Second, the resultant 50% duty-cycle current pulses [see Fig. 4(b)] in the unit cells considerably alleviate the settling requirements and directly contribute to superior linearity performance compared to conventional DDRMs that use 75% duty-cycle current pulses. Meanwhile, since every unit cell requires four LO phases, the delay mismatches between two paths caused by LO networks are also effectively suppressed. Finally, the proposed unsigned IQ-mapped DDRM uses its full (in-phase) current capability for addressing its outer constellation points, rather than the complex summing of two current sources, yielding improved RF output power and efficiency.

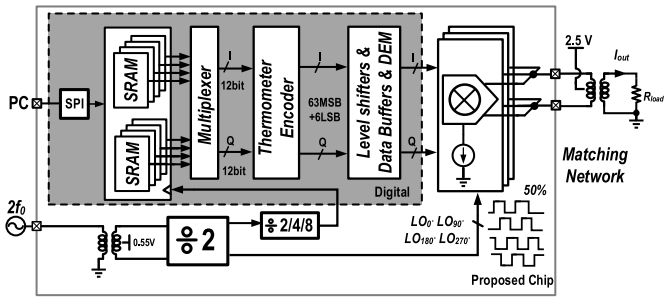

Fig. 7. Block diagram of the proposed DDRM.

IV. Circuits' Implementations

A. System Block Diagram

Fig. 7 depicts the overall system diagram. The baseband data are fed to SRAMs using an SPI. Four on-chip SRAMs are time-interleaved to support large modulation bandwidth, achieving a bit-stream throughput of half of its operating frequency, $f_{\rm LO}$. The external LO signal is divided by two by an on-chip divider to generate the quadrature LO phases, each with a 50% duty-cycle. The 12-bit DDRM is implemented in a segmented structure. 6-bit MSBs are thermometer-coded, while the remaining bits are implemented in a binary fashion after compromising area, power, and linearity [23]. Preceding the IQ-mapping DDRM, there are thermometer encoders, level shifters, and data buffers. Dynamic element matching (DEM) is also employed to randomize high-speed mismatches. Since the principle and implementations of DEM are well analyzed in other literature [24], and it is not the main focus in this article, the discussion about DEM is skipped, and all measurements are performed without DEM. Finally, the differential output signal is fed to an off-chip balun.

B. Unit Cell Implementation

A novel unit cell topology that implements the proposed IQ mapping technique of (8) is shown in Fig. 8. It performs the bit-wise ANDing of (DATA_I, DATA_Q), ($\overline{\text{DATA\_}I}$, DATA_Q), ($\overline{\text{DATA\_}I}$, $\overline{\text{DATA\_}Q}$), (DATA_I, $\overline{\text{DATA\_}Q}$), and subsequent bit-wise multiplication, using current-mode XOR/XNOR logic, with the 50% quadrature LO clocks whose phases are 0°, 90°, 180°, and 270°. As such, it provides the rotated four-point diamond-shaped constellation diagram directly without any data pre-processing or demanding additional clock phases.

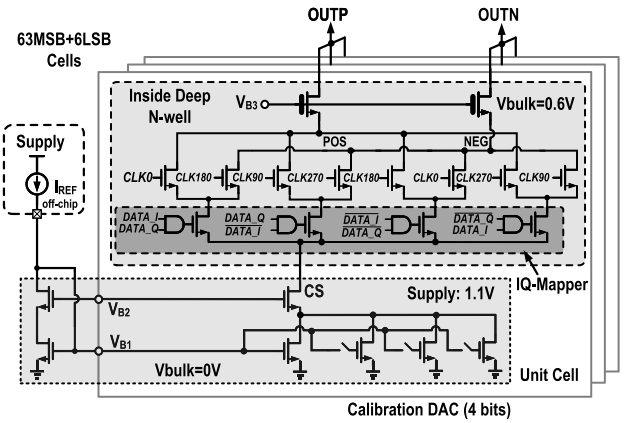

Fig. 8. Detailed unit-cell schematic of the proposed DDRM.

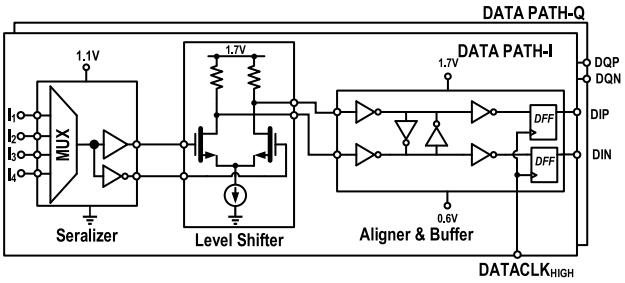

Fig. 9. Schematic of the data buffer chain and level shifter.

In each unit cell, thick-oxide cascode transistors are employed at the top of the stack, which boosts the output impedance and enables better linearity. The LO and data signal are shifted up to the voltage domain of 0.6–1.7 V to enlarge the output swing. Also, such a design can boost the output impedance further to achieve superior linearity. Therefore, switches and output transistors are put inside a deep n-well (DNW), with an elevated bulk voltage of 0.6 V, which protects transistors from substrate coupling. In each MSB cell, the current source consists of an array of transistors with an aspect ratio of $W/L = 800\mu$ m/2.5μm. The current cell transistors are surrounded by dummy cells to decrease gradients mismatch. As shown in Fig. 8, 4-bit foreground calibration DACs have been added to allow current source calibration.

C. Data Buffer and Level Shifter

The schematic of the data buffer and the level shifter is shown in Fig. 9. Two sets of data for the I and Q paths are provided by the thermometer encoders, comprising four data streams for each path, which are serialized by a multiplexer, yielding two data streams with a maximum frequency of $f_{LO}/2$. A current-mode logic (CML) buffer is employed as a level shifter to transfer the signal from 0–1.1 to 0.6–1.7 V. The differential CML buffer is designed with thick-oxide transistors to avoid breakdown, and the CML level shifter is followed by CMOS aligners and buffers. Finally, the data

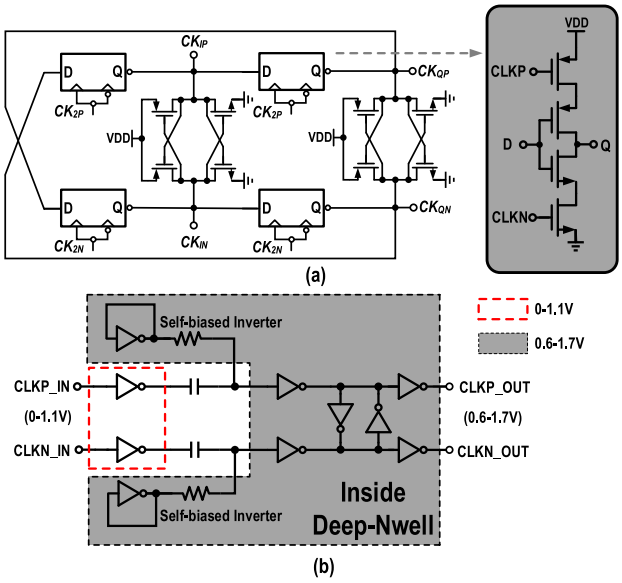

Fig. 10. Schematic of (a) C^2MOS divider and (b) LO level shifter.

streams are retimed by D-flip-flops (DFFs) before driving the data switches.

D. LO Generator

As discussed in Section III, phase mismatch among the quadrature phases leads to I/Q image. A quadrature divider is deployed to minimize such phase mismatch and generate four phases with a 50% duty-cycle. The topology of this divider is shown in Fig. 10(a), which includes clocked CMOS (C^2MOS) latches [32]. However, its transistor stack is swapped compared with a conventional C^2MOS latch to mitigate the delay from input to output and boost its operating frequency range [33]. Also, the LO signals need to get shifted from a voltage domain of 0–1.1 to 0.6–1.7 V. Different from the level shifter in the data buffer chain, to accommodate with the voltage, a bias-Tee is deployed here, where the bias voltage is set by a self-biased inverter and followed by the buffer and aligner [see Fig. 10(b)]. Based on simulations with PVT variations, these circuits can operate with a frequency range from 100 MHz to 6 GHz.

E. Layout and Floorplan

The floorplan of DDRM implementation is shown in Fig. 11. Unlike a conventional baseband DAC [34], the unit cells are placed in a row instead of a 2-D array to minimize the losses of the output network. As shown in Fig. 11, the output is connected in a "twisted" style to suppress the mismatch between positive and negative branches. The floorplan of one slice (one unit cell) is also shown in the figure. The array of current sources and calibration DAC array is located at the bottom. Thermometer encoders are placed between the current source and switches. The thermometer data go to data buffers and drive the data switches. The clock switches and cascode transistors are on the top of the whole layout inside a DNW. The current routes (green lines in Fig. 11) pass other circuitry in the layout. Therefore, ground shielding is used to mitigate

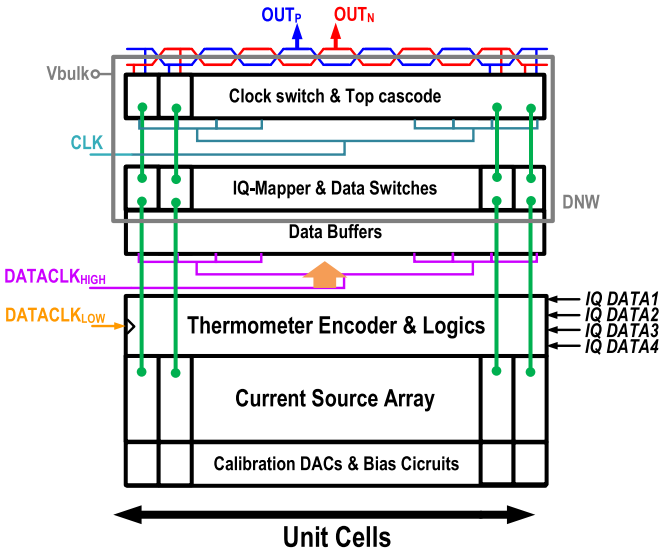

Fig. 11. Floorplan of the implemented DDRM.

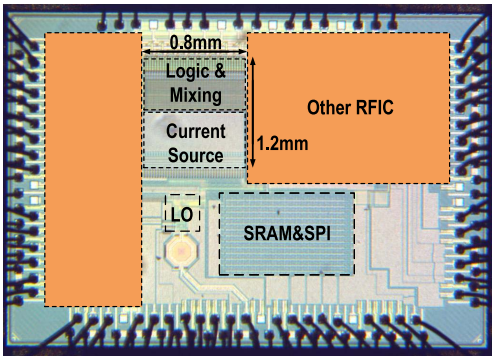

Fig. 12. Chip micrograph of the realized IQ-mapping DDRM.

the crosstalk between the LO clocks and output current caused by capacitive coupling.

Between different parts, LO and data clock distribution networks are placed. As a tradeoff between reducing the delay mismatch due to the clock-tree topology, area, complexity, and power consumption of the distribution networks, the LO tree is designed as a quadtree instead of a fully binary tree [35]. The LO traces are distributed over one metal layer, shielded by adjacent metal layers, and driven by local LO buffers. The same LO distribution pattern goes for $\text{DATACLK}_{\text{HIGH}}$ and $\text{DATACLK}_{\text{LOW}}$. Based on the MC simulations, the standard deviation (1σ) of timing mismatch LO among all of the cells was less than 0.3 ps, leading to an IM3 better than -65 dBc in simulations.

V. Experimental Results

The proposed DDRM was fabricated in a 40-nm CMOS process, and its micrograph is shown in Fig. 12. The active area is 1.1 mm^2 without the testing SRAMs and input balun. The measurement setup used for the characterization of the DDRM is shown in Fig. 13. A Keysight E8257D provides the input LO signal. The differential output is first converted to a single-ended signal by an off-chip balun. Next, it is passed to the spectrum analyzer and power meter. The measurements

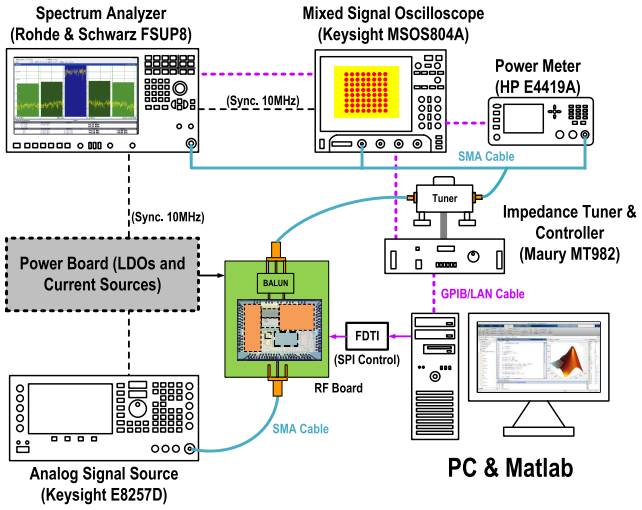

Fig. 13. Measurement setup used for the characterization of the IQ-mapping DDRM.

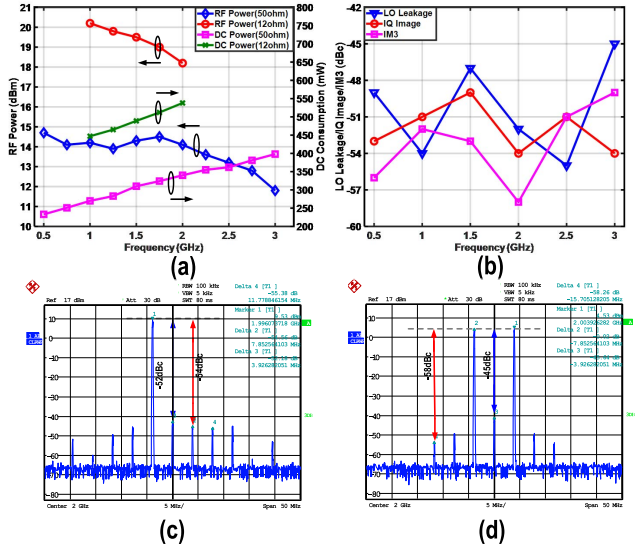

Fig. 14. (a) Measured peak output power and dc power consumption (with 50 and 12 Ω) versus frequency. (b) Measured LO leakage, I/Q image, and IM3 performance versus frequency. Measured spectrum in (c) single-tone test and (d) two-tone test.

are carried out under two load conditions: 50 and 12 Ω. An impedance tuner is used to provide 12 Ω. A high-speed oscilloscope samples the data, and the error vector magnitude (EVM) is calculated in MATLAB. In all measurements, DPD is omitted.

The DDRM is characterized first using continuous-wave (CW) measurements. Fig. 14(a) shows the peak output power P_{out} versus carrier frequency when driving a 50-Ω differential load. The peak P_{out} is 14.1 dBm, and the dc power consumption P_{dc} is 340 mW (excluding the testing SRAMs) at 2 GHz. When the load is set to 12 Ω by the impedance tuner, the peak P_{out} exceeds 18 dBm. As can also be interpreted in Fig. 14(a), an overall system efficiency of more than 24% is achieved at 1 GHz with a 12-Ω load, indicating large current handling capability and high power efficiency of the proposed DDRM when used as a modulator/PA driver. Due to the limited RF

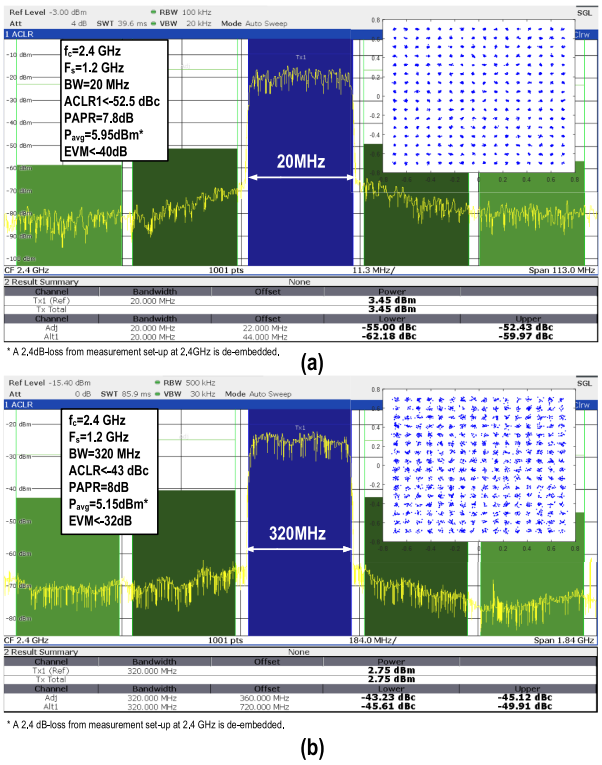

Fig. 15. Measured spectrum and constellation diagram of the single carrier: (a) 20-MHz 256-QAM and (b) 320-MHz 256-QAM signals at 2.4 GHz.

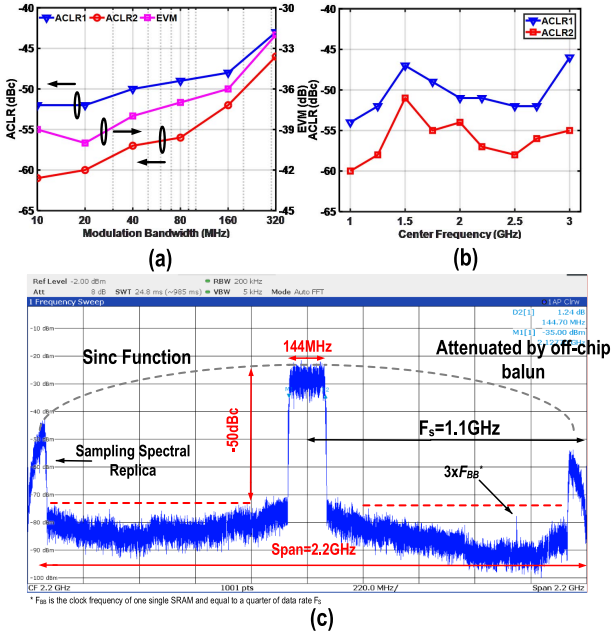

Fig. 16. (a) EVM and ACLR performance over modulation bandwidth at 2.4 GHz. (b) ACLR performance versus carrier frequency when the modulation bandwidth is 10 MHz. (c) Measured full spectrum of the 144-MHz 64-QAM signal at 2.2 GHz.

bandwidth of the impedance tuner, all following results are measured with 50 Ω.

Following that, single- and two-tone measurements are carried out without IQ calibration. The results are shown in Fig. 14(b)–(d). Over a range of 0.5–3 GHz, the I/Q image is below −48 dBc with respect to the maximum wanted sideband and is mainly restricted by the accuracy of the quadrature divider. At 2 GHz, the IQ image is −54 dBc with the output power, and the IRR can be kept below −44 dBc within the 12-dB power range. At 2 GHz, the IM3 is lower than −58 dBc.

Complex modulated signals are also applied to the proposed DDRM to verify its linearity performance. Fig. 15(a) shows the spectrum and the corresponding constellation plot of a 20-MHz bandwidth single-carrier 256-QAM signal at 2.4 GHz. The adjacent-channel leakage ratio (ACLR) and EVM are better than −52 dBc and −40 dB with more than 5-dBm average output power and 7.8-dB peak-to-average power ratio (PAPR). Similarly, the measured spectrum of a "320-MHz 256-QAM" signal at 2.4 GHz is shown in Fig. 15(b), with a measured ACLR and EVM better than −43 dBc and −32 dB, respectively.

In Fig. 16(a), the linearity performance over modulation bandwidth at 2.4 GHz is shown, and in Fig. 16(b), the ACLR performance versus f_{LO} with a modulation bandwidth of 10 MHz is demonstrated, showing the excellent linearity over the whole f_{LO} range. The spectrum of a "144-MHz 64-QAM" signal with a span of 2.2 GHz is shown in Fig. 16(c), demonstrating a clean far-out spectrum with a noise floor lower than −50 dBc. The level of sampling spectra replicas is attenuated by the Sinc function in Fig. 16(c) due to the sampling, and the upper replica is extra suppressed by off-chip output matching work.

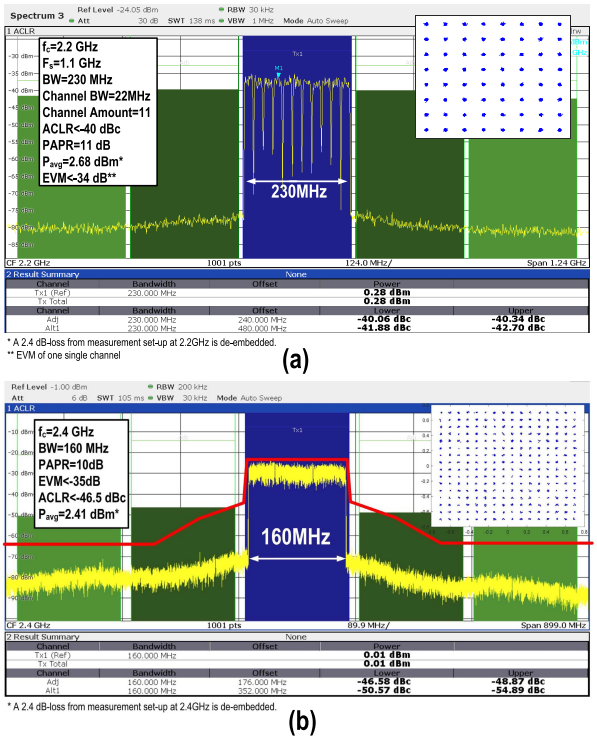

Fig. 17. (a) Measured spectrum of 11-channel 64-QAM multi-carrier signal with the worst measured constellation diagram in one channel. (b) Measured spectrum of the 256-QAM 160-MHz OFDM signal with spectral mask of 802.11ax.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART MODULATORS AND DPAS

Reference		This Work		Su ISSCC20	Mehrpoo JSSC18	Su JSSC21	Roverato ISSCC17	Yoo ISSCC20	Deng ISSCC16	Qian JSSC21	Zheng ISSCC20	Beikmirza ISSCC21	Qi ISSCC20	Lee ISSCC21
Architecture		DDRM		DDRM	DDRM	DDRM	DDRM	CDAC	DPA	DPA	DPA	DPA	Analog[3]	Analog
Matching Network		Off-Chip		On-Chip	Off-Chip	Off-Chip	On-Chip	On-Chip	Off-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip
Technology	[nm]	40		65	40	65	28	65	40	40	55	40	28	14
Frequency	[GHz]	0.5-3		1.4-3	0.9-3.1	0.9-5.2	0.85	2.2	2.4	2.3-3.5	0.85	4.6-6	1.4-2.7	0.5-6
Peak P_{out}	[dBm]	14.1/18.2[1]		22	9.2	15	3	13	19[4]	23.6	29.3	27.4	3[3,4]	7.2[4]
DC Power	[mW]	340/540[1]		1350	146[2]	900	150	N.A.	830	790	1974	1793	70.5	N.A.
Sys. Efficiency η_{PEAK}/η_{6dB}	%	7.4/1.7[1] 12.2/3[1]		11.7/N.A.	5.7/ N.A.	3.5/ N.A.	1.3 / N.A.	N.A.	N.A.	29 /17	43.4/N.A.	30.7/26.4	N.A.	N.A.
IQ Image.	[dBc]	-54 @ 2GHz		N.A.	-49	N.A.	<-36	N.A.	N.A.	N.A.	N.A.	-57	<-40	<-30
f_{LO}	[GHz]	2.4		2.2	3	2.4	0.85	2.2	2.4	3.3	0.85	5.4	2.5	3.7
Bandwidth	[MHz]	20	320	20	57	20	20	40	40	20	10	120	20	100
Modulation Schemes		256 QAM	256 QAM	256 QAM	64 QAM	256 QAM	LTE20	802.11ax 1024 QAM	802.11ac 64 QAM	64 QAM	64 QAM	64 QAM	5G-NR n7	5G-NR n78
ACLR1	dBc	-52	-43	-45	-44	-42	-61	<-45	<-40	-30	-32	-32	-44	-41[5]
EVM	dB	-40	-32	-40	-30	-42	N.A.	-42[6]	<-30	-29	-26	-24	-35	-37
DPD	Y/N	No		Yes	No	No	No	No	Yes	Yes	No	Yes	No	No

[1]Measured at 50Ω and 12Ω at 2 GHz, respectively. [2]Not include LO generation circuits. [3] Not include baseband DAC. [4]Average power. [5] Estimated from the figure. [6] Measured at -3dBm output

The DDRM was also tested with multiple-carrier QAM and orthogonal frequency-division multiplexing (OFDM) signals. An 11-channel signal with a PAPR of 11 dB and an overall bandwidth of 230 MHz was incorporated in Fig. 17(a). For each channel, the signal is a single-carrier 64-QAM signal. The overall ACLR is better than −40 dBc, and the worst EVM for a channel is better than −34 dB. In Fig. 17(b), with a 256-QAM 160-MHz OFDM signal, the DDRM's output is compliant with the spectral mask of 802.11ax standard. In addition, the ACLR is better than −46.5 dBc, and the EVM is better than −35 dB, respectively.

The performance of the proposed IQ-mapping DDRM is summarized in Table I and compared to that of prior art DDRMs, Cartesian DTX, and conventional analog RF modulators. The proposed DPD-free DDRM achieves the highest video bandwidth (320 MHz) with an ACLR of better than −43 dBc and an EVM of −32 dB. To meet the stringent requirements for future applications, such as 802.11be, the DDRM should be implemented with a higher resolution. Although Roverato *et al.* [8] present a better ACLR performance, its peak power efficiency and carrier frequency range are considerably lower. Meanwhile, this work achieves a low image rejection ratio without IQ calibration. In general, the efficiency in DDRM is lower than Cartesian DTXs' [26], [27], [30] due to its current-steering topology. However, DDRM provides better linearity in return. This overview table indicates that, with the IQ-mapping technique, the proposed DPD-free DDRM achieves superior spectral purity up to 320-MHz modulation bandwidth with a peak RF output power of more than 14 dBm.

VI. CONCLUSION

This article presents a wideband linear DDRM with a novel IQ-mapping technique. This technique incurs 3 dB more RF output power and suppresses the I/Q image. The demonstrator, which is implemented in a 40-nm process, can operate at a frequency range of 0.5–3 GHz and generate +14-dBm peak RF output power with a dc power consumption of only 340 mW at 2 GHz. It also achieves an ACLR/EVM of −43 dBc/−32 dB, respectively, for a "320-MHz, 256-QAM" signal at 2.4 GHz, with more than 5-dBm average output power. This proposed IQ-mapping technique can be applied in an energy-efficient modulator/driver for future WLAN applications or a PA pre-driver in the 5G cellular network.

APPENDIX

The expansion of the each higher order term in (13) is

$$\begin{aligned}
&(\cos(\omega_{\mathrm{LO}}t)\cos(\omega_{\mathrm{BB}}t))^{2n-1} + (\sin(\omega_{\mathrm{LO}}t)\sin(\omega_{\mathrm{BB}}t))^{2n-1} \\
&\quad = 0.5^{2n-1}[\cos(\omega_{\mathrm{LO}}t-\omega_{\mathrm{BB}}t)+\cos(\omega_{\mathrm{LO}}t+\omega_{\mathrm{BB}}t)]^{2n-1} \\
&\qquad +0.5^{2n-1}[\cos(\omega_{\mathrm{LO}}t-\omega_{\mathrm{BB}}t)-\cos(\omega_{\mathrm{LO}}t+\omega_{\mathrm{BB}}t)]^{2n-1} \\
&\quad = 0.5^{2n-2}\sum_{k=1}^{n} C_{2n-1}^{2k-1}\cos^{2k-1}(\omega_{\mathrm{LO}}t-\omega_{\mathrm{BB}}t) \\
&\qquad \cdot\cos^{2n-2k}(\omega_{\mathrm{LO}}t+\omega_{\mathrm{BB}}t) \\
&\quad = 0.5^{2n-2}\sum_{k=1}^{n} C_{2n-1}^{2k-1}\left(\frac{\cos(2\omega_{\mathrm{LO}}t-2\omega_{\mathrm{BB}}t)+1}{2}\right)^{k-1} \\
&\qquad \cdot\cos(\omega_{\mathrm{LO}}t-\omega_{\mathrm{BB}}t)\cdot\left(\frac{\cos(2\omega_{\mathrm{LO}}t+2\omega_{\mathrm{BB}}t)+1)}{2}\right)^{n-k}
\end{aligned}$$

yielding the conclusion that there is no I/Q image component $(\omega_{\mathrm{BB}}+\omega_{\mathrm{LO}})$ in the output signal.

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Prof. de Vreede was a (co)recipient of the IEEE Microwave Prize in 2008 and a Mentor of the Else Kooi Prize awarded for Ph.D. work in 2010 and the Dow Energy Dissertation Prize awarded for Ph.D. work in 2011. He was a recipient of the TUD Entrepreneurial Scientist Award in 2015. He (co)guided several students who won (best) paper awards at various conferences.