A Patient-Specific Closed-Loop Epilepsy Management SoC With One-Shot Learning and Online Tuning

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***Abstract*— Epilepsy treatment in clinical practices with surface electroencephalogram (EEG) often faces training dataset shortage issue, which is aggravated by seizure pattern variation among patients. To facilitate future optimization of the detection accuracy as new datasets are available, a fully programmable patient-specific closed-loop epilepsy tracking and suppression system-on-chip (SoC) is proposed with the first-in-literature one-shot learning and online tuning to the best of our knowledge. The proposed two-cycle analog front end (2C-AFE) obtains a 9.8-b effective number of bits (ENOB) with 8× capacitive digital-to-analog converter (CAPDAC) area reduction and 4× switching energy saving compared to a conventional 10-b SAR with an identical unit capacitor size. The entire SoC with 16 surface EEG recording channels consumes an ultra-low energy of 0.97 μJ/class and occupies a miniaturized area of 0.13 mm^2/ch. in 40-nm CMOS, achieving real-time concurrent seizure detection and raw EEG recording. Verified with the CHB-MIT database, the guided time–channel averaging (GTCA) neural processor achieves the vector-based sensitivity, the specificity, and the latency of 97.8%, 99.5%, and <1 s, respectively. The initial one-shot learning and follow-up online tuning function is validated with the EEG recording from a local hospital patient, which demonstrates a 1.8× vector-based sensitivity boost.**

***Index Terms*— Area–energy efficiency, analog front end (AFE), closed loop, digital back end (DBE), electroencephalogram (EEG), epilepsy management, fully programmable stimulation, guided time–channel averaging (GTCA), neural processor, one-shot learning, online tuning, patient-specific, seizure detection, support vector machine (SVM), surface EEG, system-on-chip, two-cycle analog front end (2C-AFE), vector-based sensitivity.**

I. Introduction

EPILEPSY is a chronic neurological disorder that affects over 50 million people worldwide [1]. Traditional treatments of the symptom include recording long-term electroencephalogram (EEG) with bulky systems [2] and medications to suppress the unwanted neural activities [3], which are inconvenient and difficult to provide timely and patient-specific seizure suppression. In contrast, closed-loop systems on chip (SoCs) in a wearable form factor that are capable of EEG recording, seizure classification, and programmable stimulation aim to realize ambulatory epilepsy treatment (see Fig. 1) [4].

Surface EEG and intracranial EEG (iEEG) are frequently adopted for seizure tracking. While seizure-related pattern in the surface EEG is concentrated between 0.5 and 30 Hz [4], iEEG can utilize a higher frequency band oscillation (HFO) (up to ∼500 Hz) that shows a good correlation with seizure pattern [5], at the cost of larger bandwidth and higher computation speed, and, most importantly, invasive incision on a subject. In contrast, surface EEG has a great advantage for its non-invasiveness.

In most seizure tracking clinical cases with surface EEG, only a few seizure onset datasets per patient are available [6], [7]. Hence, patients are periodically hospitalized for EEG recording at a huge societal expense. The seizure pattern varies from person to person, and unlike in the iEEG case, seizure from surface EEG is particularly muffled and can be inconspicuous and often what is a seizure pattern for a patient may well be a normal pattern for another patient. Also, the spectral energy of seizure onset can be even lower than the normal pattern (instead of normally being higher as in iEEG with HFO) [6], [7]. To make matters worse, it may vary with aging even for the same patient. Therefore, the algorithm needs to be trained with only several onset data (one-shot learning) and has the flexibility to record and apply new data to the classifier (online tuning) for long-term seizure tracking and treatment. As the seizure pattern variation also requires customized stimulation parameters [8], a fully programmable stimulator is necessary to provide efficient and patient-specific seizure treatment (see Fig. 1).

For closed-loop EEG systems that utilize the classification result to suppress the seizure through stimulation, prompt and accurate stimulator response for *both onset/termination*

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This work involved human subjects in its research, which was reviewed and approved by the National University of Singapore's Institutional Review Board (IRB).

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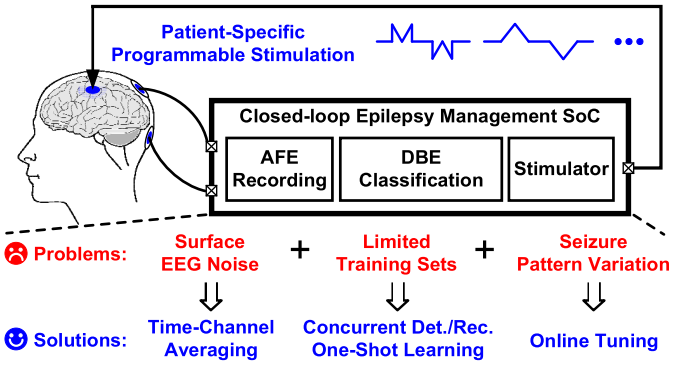
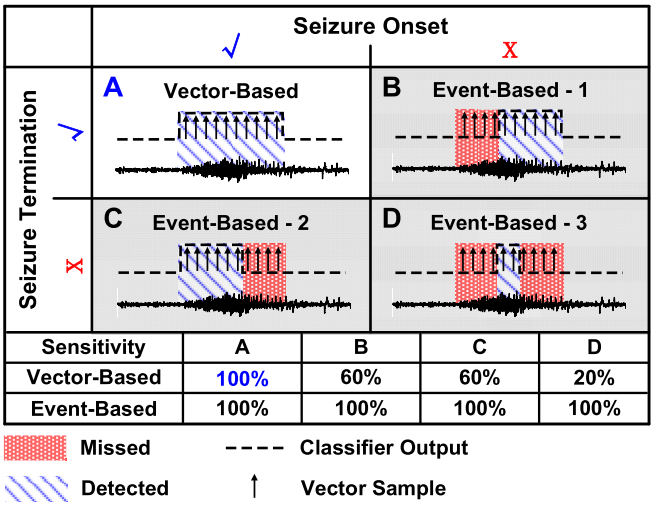


Fig. 1. Closed-loop epilepsy management SoC with its problems and proposed solutions.



Sensitivity	A	B	C	D
Vector-Based	100%	60%	60%	20%
Event-Based	100%	100%	100%	100%

Fig. 2. Vector-based versus event-based detection.

detection is critical. There are two methods of evaluating seizure detection accuracy in the literature. In an event-based detection [9], the target is to detect seizure *occurrence* regardless of seizure duration; as shown in Fig. 2, the stimulation following the seizure detection could happen after a long while of actual seizure onset and finish before the seizure ceases (cases B–D). In contrast, the vector-based detection [7] accurately captures both the seizure onset and termination and hence is possible to provide prompt and accurate seizure suppression via stimulation (see case A). In all four cases, event-based sensitivity would be 100%, but only case A would show the vector-based sensitivity of 100%, while cases B–D show only 60%, 60%, and 20%, respectively (which would miss the accurate time to activate the stimulation). Therefore, having high vector-based sensitivity is crucial for a closed-loop epilepsy management system.

To address the aforementioned issues, this article presents the fully programmable closed-loop epilepsy management SoC (see Fig. 1), where surface EEG is selected over intracranial EEG to save energy and to avoid intracranial surgery [7]. The surface EEG noise is handled by time–channel averaging. To adapt to the inter-patient and intra-patient seizure pattern variations, *real-time concurrent seizure detection and raw EEG recording* enable offline classifier retraining with newly recorded datasets. Furthermore, initial one-shot learning

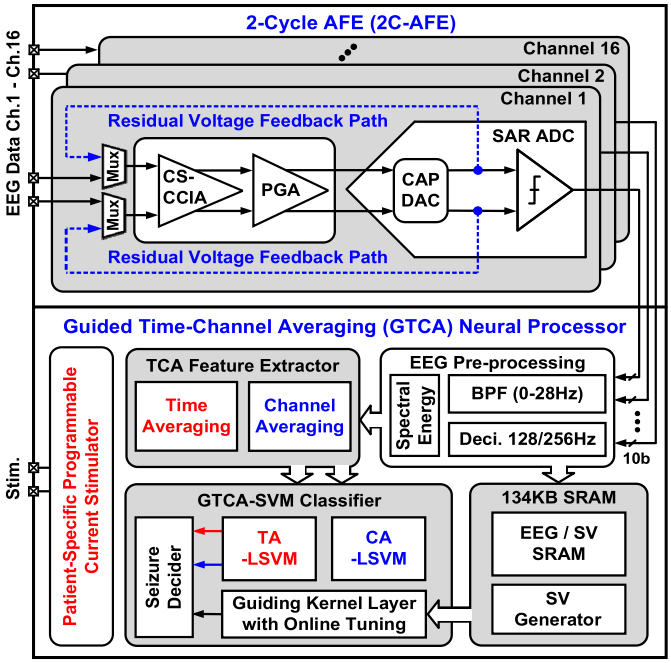


Fig. 3. Proposed closed-loop epilepsy management SoC architecture.

and follow-up online tuning function is proposed to tune the decision boundary while facing limited training datasets. Finally, a fully programmable (waveform, amplitude, frequency, and phase) current stimulator is implemented to close the loop and provide better stimulation efficacy.

This article is organized as follows. Section II describes the SoC architecture with design motivation. Sections III and IV detail the design considerations and circuits of the two-cycle analog front end (2C-AFE) and the guided time–channel averaging (GTCA) support-vector-machine (SVM) neural processor, respectively. Section V discusses the measurement results and analysis. Finally, Section VI concludes this article.

II. System Architecture

The proposed closed-loop epilepsy management SoC is shown in Fig. 3. To optimize area–energy efficiency, the 16-channel 2C-AFE reuses the amplifier + 7-b binary SAR to re-amplify the residual voltage from the first cycle and to generate an additional 3 b at the second cycle (see Fig. 4); the resulting 10-b data are processed by the GTCA neural processor that realizes the real-time concurrent *vector-based* seizure detection and raw EEG recording for long-term ambulatory treatment. The GTCA neural processor adopts the time–channel averaging feature extraction (TCA-FE) to mitigate the signal instability from gain mismatch and motion/emotion artifact, thus achieving high vector-based seizure detection accuracy. With the classification result, a bi-phasic current stimulator (2 μ–930 μA) with full programmability is proposed to provide prompt and accurate patient-specific seizure suppression.

Various state-of-the-art epilepsy management systems are proposed to realize accurate seizure detection and suppression. The NURIP processor [9] reduces noise and feature dimension with an autoencoder, achieving 97.7% event-based seizure detection sensitivity on the EU-iEEG database, but with a

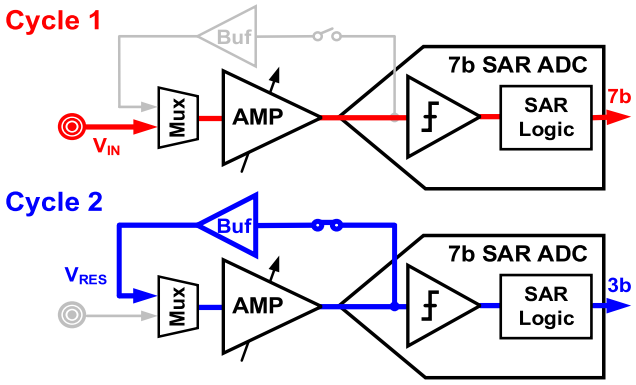


Fig. 4. 2C-AFE architecture and its operation principle.

high digital back-end (DBE) energy of 168.8 μJ/class. A two-level classification [10] realizes 97.8% vector-based sensitivity on the CHB-MIT database [11], but it is challenging for the threshold-based coarse classifier to detect inconspicuous seizure patterns where the spectral energy decreases during seizure onset. An energy-efficient decision tree classifier [12] consumes only 41.2 nJ/class with a relatively low vector-based sensitivity of 83.7% on the IEEG.ORG database. A convolutional neural network (CNN) classifier with hardware-efficient implementation works well [13], but the huge training data requirement makes it difficult to apply to clinical cases with only limited training sets. An online training function [14], [15] performs optimization algorithms in real time to improve the seizure detection accuracy for long-term usage, but the optimization algorithm takes time to show the effects and yields a high system power of 2.9 mW in [14]. Current epilepsy tracking systems are facing several pain points while being used in practical cases, which are addressed in the proposed work. First, transient and localized noise-induced false-positive/false-negative (FP/FN) classification results are reduced by TCA-FE, which averages the feature in both temporal and spatial domains. Second, for long-term epilepsy management, real-time concurrent seizure detection and raw EEG recording can store new seizure patterns for retraining of the classifier. Furthermore, the online tuning function can tune the decision boundary with only several new support vectors added. Third, the system area–energy efficiency is optimized by the low sampling rate of 2C-AFE and the efficient implementation of the SVM classifier. Finally, the proposed programmable current stimulator provides effective stimulation with independent programmability of amplitude, frequency, duration, and waveform.

III. Two-Cycle Analog Front End (2C-AFE)

For a multi-channel closed-loop SoC, area efficiency is an important design consideration. Also, surface EEG of μV-amplitude resides in the baseband range, which requires a low-noise and high-resolution sensor interface to retain the signal fidelity [16]. Compared to the conventional amplifier cascaded by an ADC structure, the proposed 2C-AFE stands out in area–energy efficiency and accuracy with the two-cycle operation.

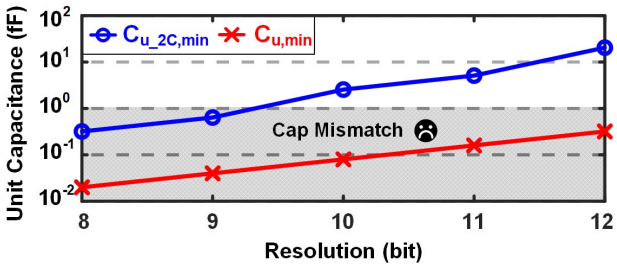


Fig. 5. Unit capacitance size versus ADC resolution of a two-cycle SAR (blue) and a conventional SAR (red), assuming that the overall CAPDAC area remains constant.

A. Residual Voltage Feedback-Based 2C-AFE

Among the Nyquist-rate ADCs, a binary SAR ADC has been extensively chosen for energy efficiency. Exponentially increasing with the resolution, the large capacitive digital-to-analog converter (CAPDAC) sets stringent constraints for the amplifier drivability and multi-channel scalability in a wearable form factor. The switching energy and *RC* settling time also scale up proportionally. Furthermore, the higher resolution requires a faster comparator when responding to smaller input voltages. Insufficient power or device mismatch could limit the comparator speed and affect the output polarity.

The traditional N-bit SAR ADC requires $(N-1)$ rounds of CAPDAC switching (excluding the most significant bit (MSB), which is compared directly without switching) to obtain the N-bit digitized result. The final switching state is determined by the most significant $(N-1)$ bits regardless of the least significant bit (LSB). If based on LSB, one more switching is applied to the unit capacitor switch, the voltage at the comparator differential inputs is exactly the residual voltage V_{RES}, which is the difference between the input voltage and the quantization level of the N-bit result [17].

The switching procedure of conventional SAR has been illustrated in [18]. If the unit capacitor switch state is adjusted according to LSB, then the residual voltage V_{RES} is always a positive value, providing that the comparator has generated correct digital bits. With V_{RES} between the comparator inputs, multiple rounds of amplification and digitization can be done using the same AFE through a feedback loop. Compared to the conventional SAR, the cyclic operation effectively saves the CAPDAC area and energy while boosting the resolution. The comparator requirement is also relaxed by the larger LSB (due to fewer bits per cycle) and re-amplification of the residual voltage. Nevertheless, the final effective number of bits (ENOB) is still dependent on the V_{RES} stability and gain accuracy.

B. Unit Capacitor Size Analysis

When choosing the size of CAPDAC, the minimum allowed unit capacitor is constrained by both matching and kT/C noise. For an N-bit SAR with a full-scale voltage of V_{FS}, the thermal noise bounded minimum total capacitance ($C_{\mathrm{tot,min}}$) can be calculated as in (1). Hence, within the same *total CAPDAC area constraint*, the minimum allowed unit capacitance for the cases of conventional SAR ($C_{u,\mathrm{min}}$) and 2C-AFE ($C_{u\_2C,\mathrm{min}}$)

(with half the conventional CAPDAC size) is obtained as in (2) and (3), where (3) includes a ceiling function when N is an odd number. Fig. 5 plots the thermal noise bounded $C_{u,\min}$ and $C_{u\_2C,\min}$ for a resolution of 8–12 bits, assuming the same overall CAPDAC area. Due to routing and device parasitics, current technology nodes can hardly guarantee the matching of sub-fF capacitance [19], [20]. For binary SAR, the unit capacitance is less than 0.5 fF, and thus, the total CAPDAC size has to be scaled up to meet the >fF matching requirement (above the gray area). In contrast, the 2C-AFE of resolution >9 b can satisfy the unit capacitor matching requirement.

$$\frac{kT}{C_{\text{tot}}} \le \frac{\left(V_{\text{FS}}/2^N\right)^2}{12} \quad \text{or} \quad C_{\text{tot,min}} = \frac{12kT}{\left(V_{\text{FS}}/2^N\right)^2} \tag{1}$$

$$C_{u,\min} = \frac{C_{\text{tot,min}}}{2^N} \tag{2}$$

$$C_{u\_2C,\min} = \frac{C_{\text{tot,min}}}{2^{\text{ceil}(N/2)}} \tag{3}$$

C. Gain and Switching Energy Analysis

Suppose that the CAPDAC is composed of N-bit capacitors, and the ADC operates in M cycles for each sample. The signal flow of the cyclic AFE in the first two cycles can be summarized in Fig. 6(a). During Cycle 1 ($C1$), the input voltage is amplified to $\pm V_{\text{REF}}$ range and digitized into the most significant N-bit. The residual voltage V_{RES} is positive and in the range of $V_{\text{REF}}/2^{N-1}$, which is fed back to the amplifier input. When Cycle 2 ($C2$) initiates, V_{RES} is re-amplified to 0–V_{ref} range so that the ADC could utilize its full resolution to convert the next $(N-1)$ bits ($C2$ sign bit omitted). Similarly, the next cycle would amplify V_{RES} from $C2$ and convert another $(N-1)$ lower bits, and the cycle continues. Thus, to maintain the linearity, the amplifier gain for $C1$ can be flexible depending on the input signal strength, while for the remaining $(M-1)$ cycles, the gain should be exactly 2^{N-1}.

For an N-bit binary SAR ADC, assume that the output code is equally distributed at all the quantization levels, and the average switching energy for a conventional SAR ($E_{\text{avg,conv}}$) [18] is

$$E_{\text{avg,conv}} = \sum_{i=1}^{N} 2^{N+1-2i}\left(2^i - 1\right) C V_{\text{REF}}^2. \tag{4}$$

For an M-cycle ADC conversion with N-bit CAPDAC, the total average switching energy ($E_{\text{avg,cyclic}}$) is

$$E_{\text{avg,cyclic}} = M \times \sum_{i=1}^{N} 2^{N+1-2i}\left(2^i - 1\right) C V_{\text{REF}}^2. \tag{5}$$

The overall resolution for the M-cycle N-bit DAC is $N + (M-1)\times(N-1)$. The additional $(M-1)\times(N-1)$ bits entail additional switching energy ($E_{\text{add,cyclic}}$) of

$$E_{\text{add,cyclic}} = (M-1) \times E_{\text{avg,conv}}. \tag{6}$$

In contrast, for the case of conventional binary SAR, the additional switching energy ($E_{\text{add,conv}}$) is

$$E_{\text{add,conv}} = 2^{(M-1)\times(N-1)} \times E_{\text{avg,conv}}. \tag{7}$$

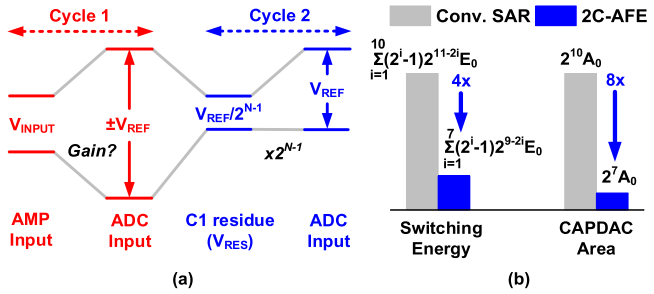


Fig. 6. (a) 2C-AFE signal flow. (b) 2C-AFE energy and area saving.

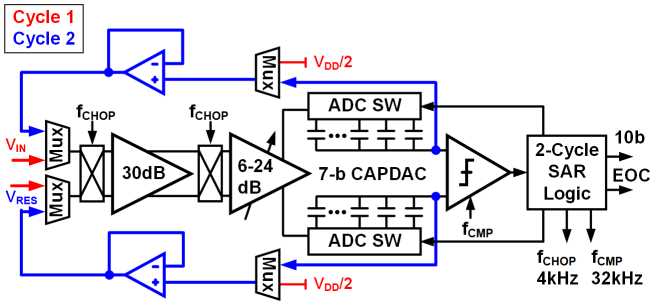


Fig. 7. Proposed 2C-AFE structure.

Compared to the *exponential scaling* of switching energy for conventional SAR, the *linear increase* for M-cycle SAR energy shows the greater energy saving. Theoretically, with more cycles of operation, the resolution and energy efficiency can be improved significantly. However, since the residual voltage has no active source, with each feedback round, there will be certain accuracy loss due to gain and residual inaccuracy; hence, it is infeasible to repeat too many cycles. The dynamic range of surface EEG is around 60 dB (signal ranges from a few μV to below mV level), and thus, 10-b resolution is sufficient. The cycle number M and CAPDAC size N chosen in this work are $M = 2$ and $N = 7$ (extra 3 b for gain and residual inaccuracy tolerance), respectively. The target is to design a 2C-AFE that realizes a 10-b resolution with 7-b capacitor bank. Assuming the same unit capacitor size (4 fF in this design), the total CAPDAC area and the switching energy of the proposed 2C-AFE are saved by 8× and 4×, respectively, compared to a 10-b binary SAR [see Fig. 6(b)].

D. 2C-AFE Implementation

The proposed 2C-AFE structure comprises a 30-dB chopper-stabilized capacitive-coupled instrumentation amplifier (CS-CCIA) followed by a 6–24-dB programmable gain amplifier (PGA), 7-b CAPDAC, comparator, two-cycle SAR logic, buffer, and analog mux (see Fig. 7).

The amplifier gain of $C2$ for V_{RES} should be close to 2^{N-1} (which is 64× or 36 dB for 7-b DAC) to maintain the ADC linearity. Hence, special attention has been paid to the OTA structure, trimming capacitor bank as well as TCA-FE to form a three-layer safety net to guarantee gain accuracy: L1) high open-loop gain of 73 dB of the telescopic OTA (see Fig. 8) ensures a precise closed-loop gain and the current-reuse inverter-based core amplifier is chosen to optimize the noise–current tradeoff [21]; L2) the fabricated chip might have

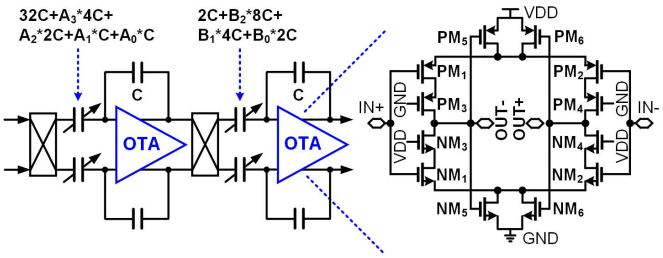


Fig. 8. Proposed two-stage amplifier and core OTA structure.

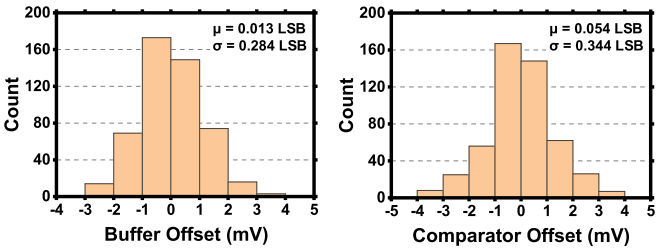


Fig. 9. Monte Carlo simulation of buffer and comparator offsets.

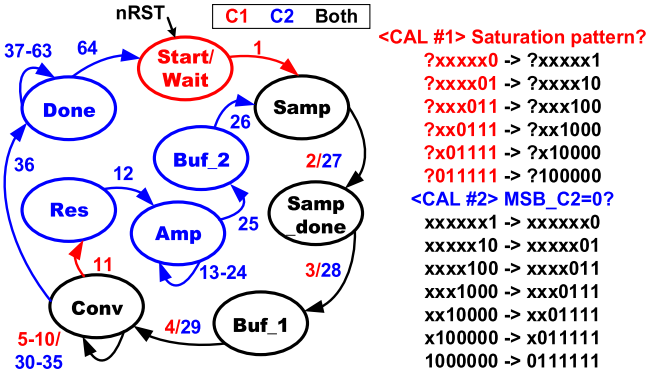


Fig. 10. 2C-AFE control logic and two-step calibration.

a small gain deviation from the simulation due to process variation and, hence, a small-cap bank has been adopted to the input capacitor of the CCIA to fine-tune the $C2$ gain to be exactly 36 dB (see Fig. 8); and L3) the TCA-FE adopts averaging algorithm among the active channels to alleviate the effect of multi-channel gain mismatch on the spatial information.

Since the largest surface EEG signal amplitude is a few hundred μV, for a typical structure of amplifier + ADC with 60-dB gain, the output range of amplifier is about 1 V_{pp}. However, the amplifier gain and output range for 2C-AFE can be less with the second cycle amplification. In this design, the maximum two-stage gain is 54 dB, corresponding to a 500-mV_{pp} differential output range. Hence, the maximum level at each amplifier output end is only 550 mVdc $\pm$ 125 mVac, sparing sufficient headroom for the stacking transistors and ensuring the amplifier linearity.

The 7-b CAPDAC is designed with customized MOMCAP using high-layer metals $M6$ and $M7$ to minimize GND coupling. The interdigitated structure achieves high area efficiency and good matching [20]. With the two-cycle amplification of 2C-AFE, the comparator noise and speed constraints for each cycle are much relaxed. To minimize dynamic power consumption, the comparator is clock gated to operate only in 14 cycles out of the 64 clock cycles for each sample, saving about 78% power compared to the always-ON case.

Since the residual voltage V_{RES} is held by the charge stored in the CAPDAC without any active source, a buffer is necessary on the feedback path to maintain the voltage by isolating the amplifier input capacitor. The controlling switches on the residual feedback path use thick-oxide transistors to minimize the leakage. As the common-mode voltage of the residual is always near $V_{DD}/2$, whenever the residual feedback path is OFF, the buffer input will be connected to a fixed voltage of $V_{DD}/2$ through the mux, which prevents the floating-gate-induced leakage. The power overhead of the buffer is 40 nW (included in the amplifier power), which is less than the saved CAPDAC switching energy of 112 nW. Also, the saved CAPDAC area is more than 10$\times$ of the added feedback buffer area of 1496 μm^2. Furthermore, the Monte Carlo simulation (see Fig. 9) has been conducted to verify that the input offsets from both buffer and comparator are less than $\pm$0.5 LSB of 7-bit SAR, and hence, the residual voltage can be sustained during the feedback.

E. 2C-AFE Control Logic With Two-Step Calibration

As shown in Fig. 10, the SAR logic is realized by a finite-state machine (FSM) with nine states to control the 2C-AFE operation. For each sample, 64 fundamental clock periods (32 kHz) are assigned to finish the two-cycle conversion. The states in red color are $C1$, blue are $C2$, and black are reused in $C1$ and $C2$. To compensate for the possible comparator error when its differential inputs are very close, calibration is critical since the wrong residual level could affect all bits in $C2$. Hence, a two-step calibration is designed for the 2C-AFE.

Assuming that the $C1$ LSB is supposed to be "1," but the comparator decision is "0," then V_{RES} would exceed the largest possible input for $C2$ ($V_{REF}/2^{N-1}$) and cause saturation in $C2$. Such errors could occur at the LSB as well as any higher bit of $C1$, which would waste the whole $C2$ operation. To compensate for this error, at the end of $C1$, a "1" is intentionally added to the $C1$ result whenever the "saturation pattern" (see Fig. 10) has been detected (Cal #1). Hence, the final switching state of $C1$ is modified accordingly and the resultant residual voltage no longer saturates $C2$. In case the "saturation pattern" is the actual input voltage, then Cal #1 is redundant, where Cal #2 would detect and correct the final output automatically.

Since the theoretical V_{RES} should always be positive, it can be used as an error flag. The wrong polarity of V_{RES} could be due to the wrong comparator decision in $C1$ or redundant Cal #1 operation. Even though the $C2$ MSB is wrong (which is omitted in the final 13-b output), the remaining 6 bits obtained in $C2$ are unaffected due to the 2's complement format of differential ADC. Thus, whenever the sign bit of $C2$ is "0" (error flag), Cal #2 is carried out by simply subtracting "1" from the first 7 bits obtained in $C1$, and the over-subtracted portion can be compensated without changing $C2$ results. With the proposed two-step calibration to reduce the comparator quantization error rate, the overall SNDR can be improved by 6 dB compared to the raw data.

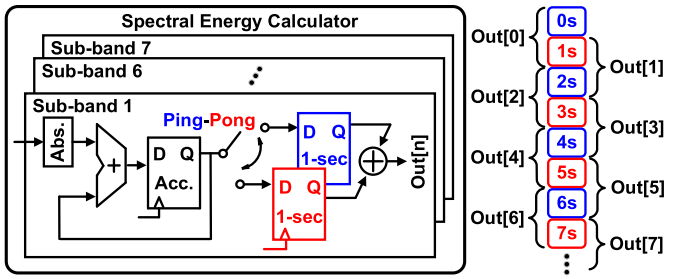


Fig. 11. Circuit implementation of spectral energy calculator.

IV. GTCA Neural Processor

The structure of the proposed GTCA neural processor with an online tuning function is shown in Fig. 3. After pre-processing, the TCA-FE extracts the time-averaging (TA) and channel-averaging (CA) features, which are processed by the GTCA-SVM classifier to decide whether the signal is a seizure. In the classifier, a second-order polynomial guiding kernel layer is incorporated to improve the vector-based detection accuracy and realize online tuning. With the proposed TCA-FE and GTCA-SVM classifier, the false-positive rate (FPR) and false-negative rate (FNR) are dramatically reduced by 65% and 26%, respectively. Due to initial one-shot learning and follow-up online tuning, even with limited training datasets (as we frequently face patients in the clinic), the vector-based sensitivity can be further boosted. Also, the proposed patient-specific programmable current stimulator module can provide arbitrary waveforms to suppress seizures.

A. EEG Pre-Processing

The EEG pre-processing module first decimates the raw EEG signal and then extracts spectral energy for 16 channels of seven different sub-bands from 0 to 28 Hz as in [6] and [22]–[24]. Two decimation filters are implemented with the size of 24-tap (128 Hz for seizure tracking) and 18-tap (256 Hz for seizure onset EEG recording), enabling real-time concurrent seizure detection and raw EEG recording, which facilitates long-term ambulatory treatment. The 18-tap decimation filter is clock and data gated such that it is activated only when a seizure is confirmed by the GTCA-SVM classifier.

The spectral energy calculator converts the bandpass filtered EEG sample to its absolute value and accumulates samples to form the non-overlapping 2-s window spectral feature. However, the latency of the system will be 2 s, which is not ideal for real-time seizure detection and suppression. Hence, the ping-pong strategy is applied to buffer 1 s of accumulated spectral energy and output overlapped 2-s spectral energy, as shown in Fig. 11. Together with the proposed zig–zag data buffer, the overall circuit latency is reduced from 2 to 1 s.

B. Time–Channel Averaging Feature Extraction

The surface EEG electrodes suffer from multiple noise sources—extrinsically (e.g., loose contact of the surface electrode and sudden rapid body movement of patients) and intrinsically (e.g., dramatic emotional change of patient) [25]–[29]. Transient and localized noise is introduced in the surface EEG signal, which could lead to a high FPR and FNR. The proposed TCA-FE module performs averaging in both time and spatial domains to reduce noise-induced FPs/FNs and achieves 49% and 75% reduction, respectively, compared with [6] while consuming 1.9% of DBE power.

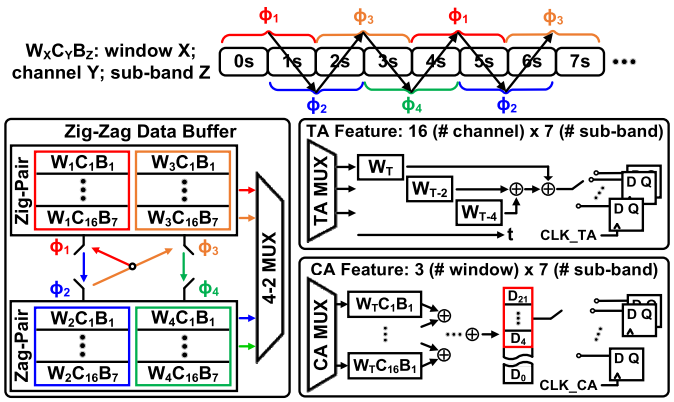


Fig. 12. Architecture of TCA-FE module.

The TA and CA are performed on the pre-TCA feature that has a size of 3 (# of non-overlapping 2-s window) × 16 (# of channels) × 7 (# of the sub-band). The architecture of the TCA-FE module is shown in Fig. 12. The proposed zig–zag data buffer is designed to reduce the circuit latency from 2 to 1 s. It has four register banks—two forming zig pairs and the other two forming zag pairs. Each register bank has a size of 112 × 18 bit, which stores 2-s spectral energy. While performing TA and CA, the zig/zag pair is selected and combined with the next 2 s to form the pre-TCA feature. After performing TA and CA, the zig-zag data buffer accepts the next 2-s spectral energy to update one of the four register banks in a zig-zag fashion (Φ_1–Φ_4) (see Fig. 12).

Time multiplexing and resource sharing are considered in the TCA-FE module to reduce area overhead. At each step, the spectral energy of three non-overlapping 2-s windows of one channel and one sub-band is selected to perform TA resulting 16 × 7 times of calculation, whereas in CA, the spectral energy of 16 channels of one non-overlapping 2-s window and one sub-band is selected to perform 3 × 7 times of calculation. To match the TA and CA process, different clocks are applied—CLK_TA is 4× faster than CLK_CA. The TA requires dividing the spectral energy summation result by 3, which needs a divider. Based on the MATLAB simulation, removing the divider in TA only has a <0.5% accuracy degradation. Thus, the divider is removed in TA to achieve higher area–energy efficiency. The CA involves the dividing of spectral energy of 16 channels (or 8/4/2 based on the active channel numbers), which is easy to implement using a right shifter that has barely any area overhead. Furthermore, both TA and CA modules are clock gated to obtain better energy efficiency.

Seven seizure events from the CHB-MIT database that contain transient and localized noise are used for the noise analysis. The TA/CA (after averaging) and pre-TCA (before averaging) features with seizure and non-seizure clusters are extracted. With the presence of transient and localized noise, the distance between seizure and non-seizure cluster centroids

TABLE I
FEATURE ANALYSIS OF TCA-FE

Feature	Dimension	Cluster centroid distance	Normalized cluster centroid distance
pre-TCA	336	133056	396
TA	112	230496	2058
CA	21	183309	8729

would be reduced, representing worse feature separability. The normalized cluster centroid distance (by dimension) is used to make a fair comparison. The resulting TA, CA, and pre-TCA normalized cluster centroid distances are 2058, 8729, and 396, respectively (see Table I). Hence, the feature separability improves after averaging, even in the presence of transient and localized noise.

C. GTCA-SVM Classifier With Online Tuning Function

Wang *et al.* [10] proposed a coarse-to-fine dual-classifier structure to cope with the power–performance tradeoff. Even though the fine classifier is only activated for 15% of the runtime, it still consumes 14.2 μJ/class with DBE only. In [6], the D^{2}A-SVM has one classifier trained for high sensitivity (C_{SEN}) and the other one trained for high specificity (C_{SPE}). However, the digital hysteresis could perform badly by simply adopting previous decisions when C_{SEN} and C_{SPE} disagree at the seizure onset/offset edges, resulting in the high FNR and FPR of 4.3% and 2.0%, respectively.

The proposed GTCA-SVM classifier structure resolves the above problems by introducing nonlinear classification ability to the linear dual-classifier structure to realize high seizure detection accuracy and low energy consumption. The classifier can be programmed with four operation modes: 1) and 2) TA (CA) mode that only activates TA (CA) feature extractor and classifier; 3) TCA mode that activates TA and CA feature extractors and classifiers with digital hysteresis [6] to make the final decision; and 4) GTCA mode that involves all classifiers, and the guiding kernel layer will make the final decision when TA and CA classifiers have different outputs.

To boost the performance of the SVM classifiers, normalization is applied during offline training as in the following equation:

$$x_n = \frac{x_i - \mu}{\beta \cdot \sigma} \cdot \mathrm{Scale} = (x_i - \mu) \cdot P_{\mathrm{BSS}} \tag{8}$$

where x_i denotes the input feature, μ denotes the mean of support vectors, σ denotes the standard deviation of support vectors, and β and Scale are the scaling factors introduced in offline training. The two parameters β and σ are combined with Scale as P_{BSS} to simplify the calculation to one fixed-point addition and one floating-point multiplication.

Although the guiding kernel layer activation rate is <5%, it is necessary to be designed in an area–energy efficient way. Hence, the second-order polynomial kernel is serialized, and computation resources are shared. The square and summation operation reuses the floating-point multiplier and adder, resulting in only two floating-point multipliers and two floating-point adders (see Fig. 13). Based on the MATLAB

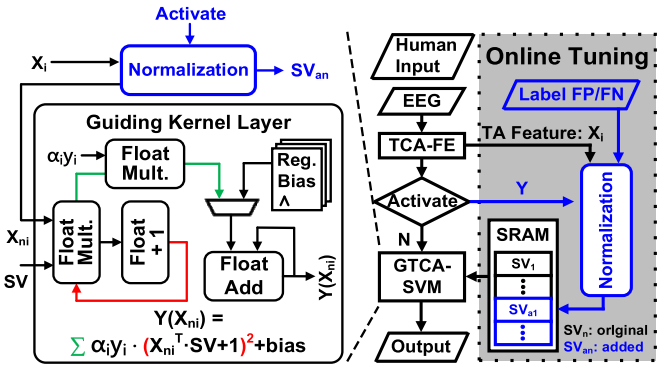


Fig. 13. Architecture of guiding kernel layer and flowchart of online tuning.

simulation, the maximum and average numbers of support vectors used across 24 cases in the CHB-MIT database are 148 and 63 (16-Ch mode), respectively. With the GTCA mode, 70 kB out of the 134-kB EEG recording SRAM can be programmed to store 256 support vectors under 16-Ch mode (512/1024/2048 under 8/4/2-Ch mode). The choice of 256 support vectors (>1.7× of the maximum requirement) leaves enough room for extreme cases and online tuning. The guiding kernel layer operates at 1 MHz for low-power purposes, which also guarantees the decision to be made within 31.25 ms under the maximum number of channels and support vector.

When facing limited training datasets in practical cases, the TCA-FE can extract distinct features such that the classifier could achieve a good event-based performance at initial training. In the later stage, once the FP/FN classification result is observed, by activating the online tuning function once, one FP/FN TA feature can be added as a support vector to the SRAM to tune the decision boundary with immediate effect. The newly added support vector also needs to be normalized using the same parameter sets. Therefore, the normalization module is shared between the guiding kernel layer and the support vector generation (see Fig. 13).

D. Patient-Specific Programmable Stimulator

State-of-the-art closed-loop epilepsy management systems [6], [9], [30], [31] often offer a limited choice of testable waveforms—changing one parameter (e.g., stimulation frequency) automatically changes another (e.g., current pulsewidth) resulting in less effective stimulation [8], [32]. To address these problems, we demonstrate the LUT-based patient-specific programmable current stimulator.

The stimulator structure is shown in Fig. 14. The stimulator consists of a digital control unit operating at 2 MHz and a current DAC. The digital control unit has an FSM parameter block, a switch LUT that stores the arbitrary waveform configuration (C_0–C_8), and an FSM that controls different stimulation phases. The switch LUT configurations are shared in the anodic and cathodic phases to save area and guarantee a balanced charge delivered to the human body.

The digital control unit is designed with individual programmability of the parameters, which enables the patient-specific waveform generation. The parameter M controls how many clock cycles each current value

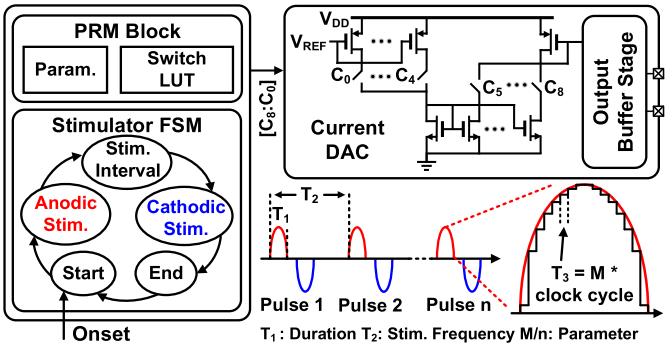


Fig. 14. Proposed patient-specific programmable current stimulator.

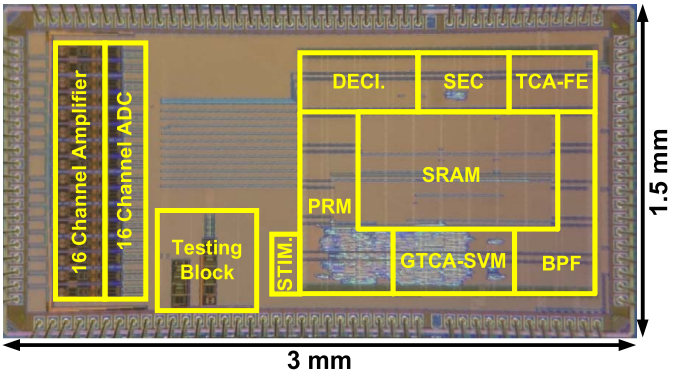


Fig. 15. Chip microphotograph.

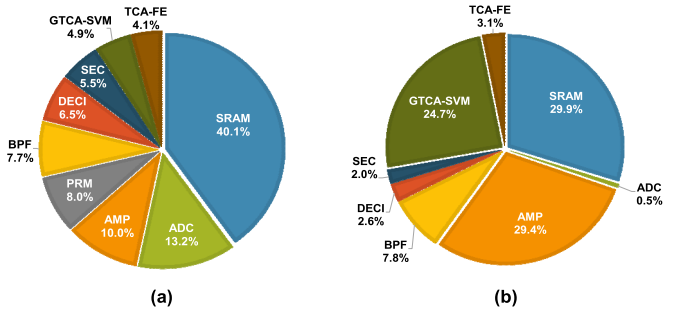


Fig. 16. (a) SoC area breakdown. (b) SoC power breakdown.

lasts, resulting in the programmable stimulation duration of $T_1 = 128 \times T_3 = 128 \times M \times 50\ \mu$s. The pre-uploaded parameter n controls the number of stimulation pulses to be generated. Finally, the stimulation frequency can be programmed via controlling the clock cycles between each stimulation pulse. The proposed current stimulator realizes arbitrary waveform generation with independent control of different parameters to improve stimulation efficiency.

V. Measurement Results

The proposed 16-Ch epilepsy management SoC fabricated in the 40-nm 1P8M CMOS process occupies an area of 3 mm × 1.5 mm, where the active area per channel is 0.13 mm^2 (see Fig. 15). The area and the power breakdown of the SoC are shown in Fig. 16. Table II shows the comparison with state-of-the-art works.

Fig. 17(a) shows the gain performance of the proposed 2C-AFE. The two-stage gain can be programmed from 36.1 to

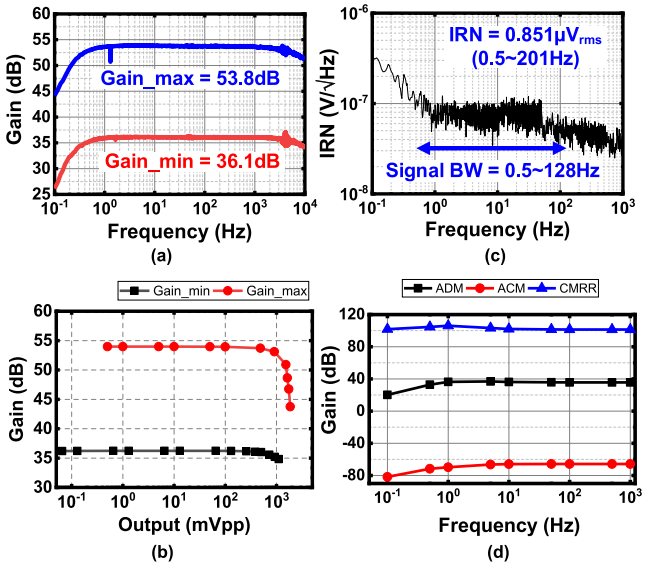


Fig. 17. (a) Two-stage amplifier gain range. (b) Amplifier linearity. (c) Noise spectrum. (d) Common-mode rejection ratio.

53.8 dB. The high- and low-pass corners are <0.5 and >128 Hz, respectively, which cover the entire surface EEG signal bandwidth. Fig. 17(b) shows that the amplifier linearity is maintained within the 500-mV$_{pp}$ output range for both maximum and minimum gains. The noise spectrum of the CS-CCIA is plotted in Fig. 17(c). The input-referred noise (IRN) integrated from 0.5 to 201 Hz ($(\pi/2)$ times the signal bandwidth) is 851 nV$_{rms}$. Hence, the noise efficiency factor (NEF) is calculated to be 2.94. The common-mode rejection ratio (CMRR) of the two-stage amplifier is larger than 100 dB, as shown in Fig. 17(d).

To determine the dynamic performance of 2C-AFE, a single-tone sine wave of 5.875 Hz is directly fed into the ADC. Coherent sampling is used for SNDR measurement to avoid spectral leakage. As shown in Fig. 18(a), the output power spectrum demonstrates 60.7-dB SNDR with 4096 FFT points. Hence, the 10-b resolution 2C-AFE achieves 9.8-b ENOB. To verify the 2C-AFE performance under different input conditions, the sine-wave frequency is swept across the target bandwidth. As shown in Fig. 18(b), the SNDR for each frequency is stable around 61 dB. To obtain the dynamic range, the sine-wave amplitude is swept from V_{FS} down to 0.22 mV$_{pp}$. The measured SNDR corresponding to each input magnitude is plotted with a dynamic range of 67 dB [see Fig. 18(c)]. Fig. 18(d) summarizes the performance comparison with state-of-the-art 10-b ADC works [18], [36]–[41]. The proposed 2C-AFE achieves a Walden FoM of 81.5 fJ/conversion with the total CAPDAC size of only 1.024 pF, demonstrating a high area–energy efficiency.

The CHB-MIT database [11] is used to verify the performance of the proposed GTCA neural processor. The database contains 24 cases of >990 h of surface EEG recordings, during which there are 180 seizure events with various seizure types. The seizure file used for the classifier training of each patient is shown in Fig. 19. With the proposed TCA-FE, the classifier can be trained in *one shot* with 34.5% of the total seizure

TABLE II

COMPARISON WITH STATE-OF-THE-ART EPILEPSY MANAGEMENT SOCS

		This Work	JSSC '20 [14]	VLSI '21 [15]	ISSCC '20 [35]	ISSCC '20 [10]	JSSC '18 [33]	JSSC '18 & '20 [9] [34]	JETCAS '18 [12]	JSSC '15 [6]
SoC	Process (nm)	40	40	28	65	180	180	130	65	180
	Integration	AFE+DBE	DBE	DBE	AFE+DBE	AFE+DBE	AFE+DBE	AFE+DBE	DBE	AFE+DBE
	Supply Voltage (V)	1.1 (A) 0.7 (D)	0.58	0.5	1.2	1.5	1.8	1.2	0.8	1.8 (A) 1 (D)
	Energy (μJ/class.)	0.97	170.9 (DBE only)	0.0015 (DBE only)	0.036 (DBE only)	174*	64*	178.7*	0.041 (DBE only)	2.73
	Area/ch. (mm^2)	0.13	0.32 (DBE only)	0.0125 (DBE only)	0.19	0.73*	1.33*	0.24	0.03 (DBE only)	1.55*
	Stimulator Programmability	Waveform Frequency Duration	X	X	X	X	X	Waveform	X	X
AFE	Gain (dB)	36-54 (C1) 36 (C2)	X	X	X	14-44	50-70	X	X	52-80
	IRN (μV_{rms})	0.851 (0.5-201 Hz)	X	X	X	1.2 (LFP) 1.8 (AP)	2.09 (0.59-117 Hz)	1.6 (0.1-500 Hz)	X	0.9 (0.5-100 Hz)
	ADC Type	2-Cycle SAR	X	X	Noise Shaping SAR	SAR	DMSAR	Track and zoom $\Delta^2\Sigma$	X	SAR (Bridge)
	ENOB (bits)/ Resolution (bits)	9.8 / 10	X	X	4.9 / 6	# / 16	7.8 / 10	11.3 / #	X	# / 10
DBE	Verification (no. patients)	CHB-MIT+ Local Hospital (24+1)	CHB-MIT+ Local Hospital (24+2)	CHB-MIT + UoM (24+3)	EU-iEEG #	CHB-MIT (23)	Custom (5)	EU-iEEG (4)	IEEG.ORG (20)	CHB-MIT (14)
	Classifier	GTCA-SVM	NL-SVM	Logistic Regression	EDM-DF	Coarse (TH) Fine (LS-SVM)	Ridge Regression	EDM-SVM	XGB-DT	D^2A-LSVM
	Sensitivity (%) Vector	97.8	96.6^	97.7^	96.7^	97.8^	96.0^	#	83.7	95.7
	Sensitivity (%) Event	100						97.7	#	#
	Specificity (%)	99.5	99.5^	98.2^	0.80FP/hr^	99.7^	100^	0.19FP/hr	88.1	98.0
	Latency (s)	0.74	0.78	2.1	#	<0.3 (with 1.2s sliding window)	0.76	0	1.1	1
	Online Tuning Method	GTCA	ADMM	SGD	X	X	X	X	X	X

* estimated # not reported ^ vector/event-based unspecified

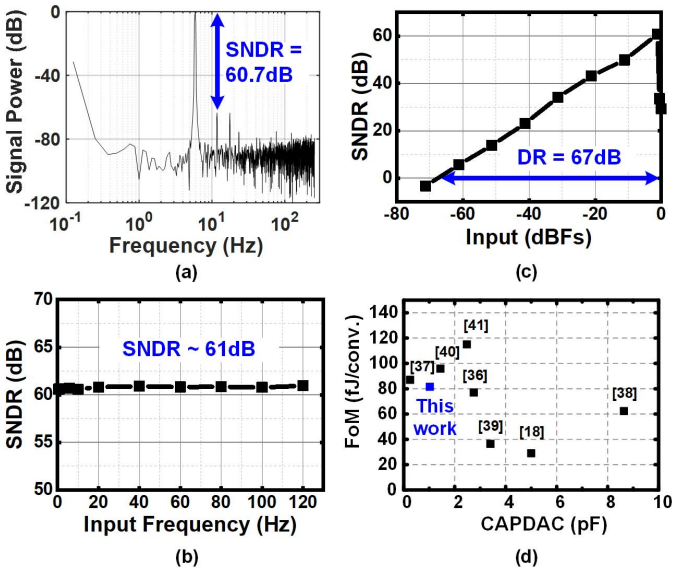


Fig. 18. 2C-AFE dynamic performance: (a) output power spectrum with single-tone input, (b) SNDR of varying frequencies, (c) SNDR of varying amplitudes, and (d) comparison with 10-b ADCs in literature.

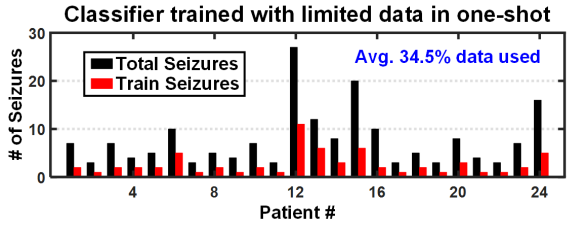


Fig. 19. Training seizures of each patient from the CHB-MIT database.

events on average. The block-wise data arrangement [12] is adopted to prevent the classifier from foreseeing the test data during the training phase. To cope with the data imbalance issue due to the rareness of seizure events, the training data are selected with the seizure event plus a 100–300-s window applied before and after the seizure event respectively; furthermore, ∼10% of non-seizure files are combined with the training seizure files to form the training files. Those non-seizure files are used as validation data and the FPs are used as training data. The remaining seizure and non-seizure files form the test files.

Fig. 20 shows the GTCA neural processor performance on the CHB-MIT database. During the training phase, the best-performing operation mode is specifically selected for each patient. Except for the test seizure files, at least 2-h non-seizure recordings are used to verify the performance of each patient. Across all the 24 patients from the CHB-MIT database, the proposed GTCA neural processor obtains an average *vector-based sensitivity* of 97.8% and a specificity of 99.5%. As shown in Fig. 21, besides pronounced seizure patterns as in patient 9, for inconspicuous cases such as patient 6 (problematic low sensitivity and specificity in [6] and [10]), our SoC outperforms in both sensitivity and specificity. Based on the measurement results, there are only three patients with a seizure detection latency of >2 s (worst case is 3 s), and

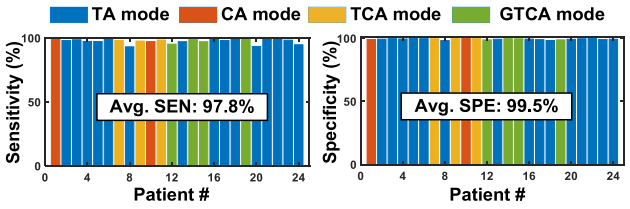


Fig. 20. Performance of GTCA neural processor on the CHB-MIT database.

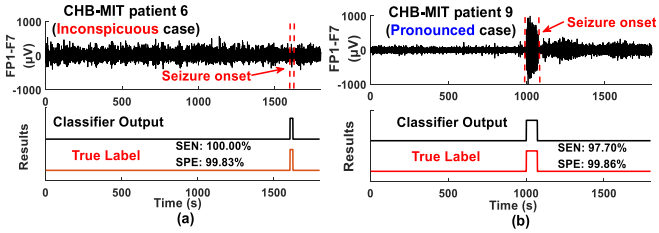


Fig. 21. Classification results: (a) inconspicuous seizure case (patient 6) and (b) pronounced seizure case (patient 9).

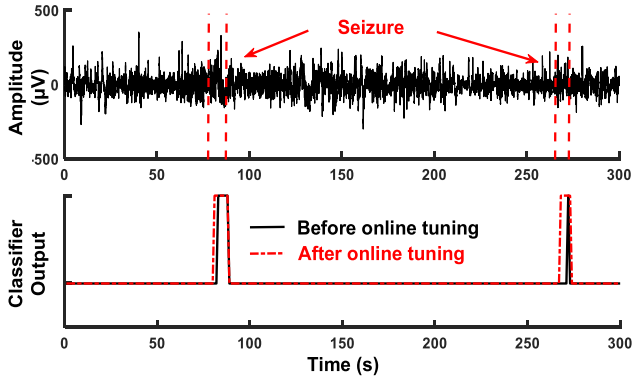


Fig. 22. Online tuning performance of the local hospital patient with an inconspicuous seizure pattern.

17 out of 24 patients have a latency of <1 s. In summary, the average seizure detection latency of 0.74 s is achieved across all 24 patients.

The online tuning function is verified on a recruited patient from a local hospital. There are seven seizure events captured during the 4 h of EEG recording, which lasts from several to tens of seconds. To demonstrate one-shot learning with a follow-up online tuning performance, the first seizure event is used to train the classifier, resulting in an event-based sensitivity of 83.3%, a vector-based sensitivity of 39.5%, and a specificity of 98.9%. Then, online tuning is applied and new support vectors are added using the FNs/FPs of the follow-up test seizure events (three FNs and one FPs) to tune the decision boundary. Fig. 22 shows the classifier performance on two of the test seizure events before and after online tuning. On the six test seizure events, the classifier achieves a 1.8× vector-based sensitivity boost to 71.9% (100% event-based sensitivity) with an acceptable specificity degradation of 2.5% P. The initial one-shot learning and follow-up online tuning has also been carried out on the two worst performing patients (vector-based sensitivity <90%) in the CHB-MIT database to demonstrate the effectiveness on longer EEG data

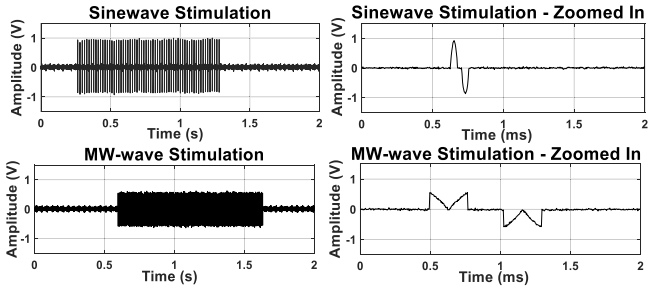


Fig. 23. Programmable stimulation measurement.

(>20 h). The initial one-shot learning is applied using the first 1 (2) out of 5 (8) seizure events of patient 8 (20), with a vector-based sensitivity of 70.5% (67.8%) and a specificity of 98.8% (98.8%). After adding 12 (5) support vectors with online tuning, the vector-based sensitivity achieves 81.7% (76.6%) with a specificity of 98.3% (98.2%) for patient 8 (20).

Fig. 23 shows the measured sine- and MW-wave stimulation. The sine wave is programmed to stimulate at 50 Hz and the MW-wave at 100 Hz. The stimulation amplitude of the sine wave is 2× and the stimulation duration of the sine wave is 1/8 of the MW-wave. Based on the measured results, it shows that the proposed stimulator can realize independent parameter programmability to maximize the stimulation efficiency.

VI. Conclusion

The proposed closed-loop epilepsy management SoC provides patient-specific seizure detection and fully programmable stimulation treatment with only 0.97-μJ/class energy consumption. The proposed one-shot learning with online tuning solves the long-term challenges, including limited training data and seizure pattern variation with aging and among patients. The 2C-AFE obtains 9.8-b ENOB with 1/8 CAPDAC area and 1/4 switching energy compared to conventional 10-b SAR with an identical unit capacitor. With TCA-FE to average out the localized and transient noise, the GTCA neural processor achieves the vector-based sensitivity, the specificity, and the latency of 97.8%, 99.5%, and <1 s, respectively. Validated with the EEG recording from a local hospital patient, the online tuning function successfully boosts the vector-based sensitivity by 1.8× after one-shot learning.

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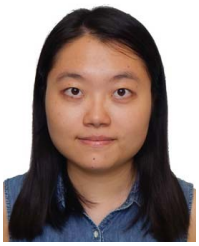

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