# A 28-GHz Phased-Array Relay Transceiver for 5G Network Using Vector-Summing Backscatter With 24-GHz Wireless Power and LO Transfer

Michihiro Ide⬤, Atsushi Shirane, *Member, IEEE*, Kiyoshi Yanagisawa, Dongwon You,
Jian Pang⬤, *Member, IEEE*, and Kenichi Okada⬤, *Senior Member, IEEE*

*Abstract*— **This article introduces a wirelessly powered phased-array transceiver for fifth-generation (5G) relay systems. To realize the battery-less relay operation, 24-GHz wireless power transfer (WPT) is employed. This relay transceiver consists of the proposed vector-summing backscatter for Transmitter (Tx) and a passive phase-shifting self-heterodyne Receiver (Rx) with a rectifier for Rx and WPT. The receiver generates dc power from the 24-GHz WPT signal, which is also used as a local oscillator (LO) signal to down-convert the 28-GHz 5G modulated data to a 4-GHz IF. The vector-summing backscatter up-converts the 4-GHz IF signal to 28-GHz using a 24-GHz LO signal while working as a 360° phase shifter with a 7-bit resolution. Both transmitter and receiver operate only using the generated power from the 24-GHz WPT. The chip area of the eight-path transceiver is 1.8 mm² and the transceiver is mounted on a 32-element phased-array antenna board. This module generates 3.1-mW dc power from 6.7-mW/cm² received power density at 24 GHz. The transmitter achieves a −2.2-dBm measured saturated equivalent isotropically radiated power (EIRP) and supports a −30° to +30° beam range. The measured error vector magnitude (EVM) values are −27.5 dB for Tx mode and −31.3 dB for Rx mode with a 400-MHz 64-QAM orthogonal frequency division multiple access (OFDMA)-mode signal (5G new radio (NR), MCS 19). The power consumption for each path is 0.03 mW in both Tx and Rx modes.**

*Index Terms*— **Backscatter, CMOS, fifth-generation (5G) mobile network, phased array, rectifier, relay transceiver, self-heterodyne, vector summing, wireless power transfer (WPT).**

## I. INTRODUCTION

**M**ILLMETER-WAVE fifth-generation (5G) communication is expected to be used for enhanced mobile broadband (eMBB), mission-critical communication, and massive Internet of Things (IoT) as the next-generation wireless communication. However, the communication distance
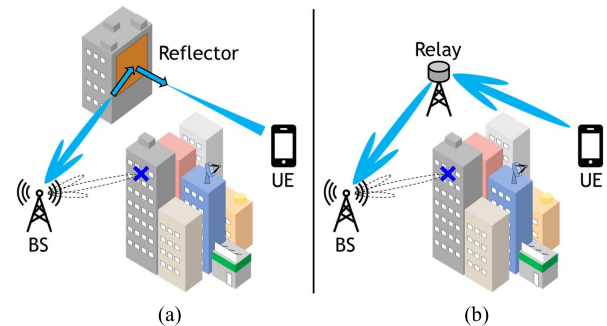
Fig. 1. Two types of relay systems for 5G networks: (a) metasurface reflector and (b) relay transceiver.

is limited because of the high free-space path loss at the millimeter-wave frequencies. Therefore, phased-array implementation has become the most important key technology to extend the transmission distance and realize spatial multiplexing communication by beamforming. High-performance phased-array transceiver designs and high-efficiency communication techniques using multiple-input–multiple-output (MIMO) systems have been actively researched and developed [1]–[6]. On the other hand, the present use cases are still limited to the line-of-sight (LoS) communication due to the large transmission loss caused by buildings and the very narrow directivity of the millimeter-wave radio. To expand network coverage and maintain seamless network connectivity by using non-line-of-sight (NLoS) links, the massive deployment of relay nodes can be a promising solution.

As shown in Fig. 1, two types of relay systems for 5G communication have been previously introduced. The first one is based on metasurface reflectors [7], [8]. The reflectors can establish NLoS communication by reflecting the received radio waves toward the user equipment (UE), bypassing the obstacles in the LoS link path. High reflected power is achieved using large-scale reflectors while maintaining wide beamwidth [7]. To further improve the wireless data rate and to maintain the architectural esthetics of buildings, the optically transparent dual-polarized reflectarray is reported [8]. Although low fabrication and maintenance costs and flexible deployment are achieved, the path loss of the NLoS link is still tens of decibels higher than the LoS link [9]. In addition, reflectors cannot control the reflection beam angle actively.

To realize a beam-steerable relay operation, active relay transceivers are introduced, as shown in Fig. 1(b). When an LoS link blockage occurs, the base station (BS) can steer the

beam direction to a relay node nearby UE, and the relay node performs the beamforming again toward UE from the received signal. The relay transceiver can achieve an NLoS link flexibly by the beam-steerable operation, but an external power supply is necessary. As a result, the battery can be a bottleneck for the product life and causes the relay transceiver to require regular maintenance. Moreover, the recent active phased-array transceivers consume large power to obtain high spatial resolution and data rate. Power-efficient transceivers have been reported [3]–[6], but they still consume over several hundred milliwatts for each path. In terms of massive deployment, the total cost of the active relay transceivers and their power consumption are the main drawbacks when compared to the passive reflectors.

This article introduces a wirelessly powered relay transceiver for millimeter-wave 5G communication, which realizes outdoor-to-indoor communication. We assume that the obstacles are the walls of the buildings. The transmitted wave from BS on the outdoor side is transferred to UE on the indoor side with low loss. To realize beam-steerable and battery-less relay operation, we introduce 24-GHz wireless power transfer (WPT) so that the relay transceiver operates only using the wirelessly supplied power. The proposed transceiver is one of the most suitable options for massive deployment because it does not require any external power supply and can reduce the maintenance cost. In addition, the transceiver is compatible with the 5G new radio (NR) as a simple relay system. This transceiver can be utilized not only for indoor-to-outdoor relay systems but also for reflective systems that use metasurface reflectors.

According to the WPT measured results, the proposed Receiver (Rx) generates a 3.1-mW dc power at 6.7-mW/cm$^2$ received power density and achieves a wide-angle coverage from $-30°$ to $+30°$. Due to the proposed vector-summing backscattering technique, the $4 \times 8$ array module realizes beam-steerable relay operation with a power consumption of 0.03 mW for each path. The error vector magnitudes (EVMs) for Transmitter (Tx) and Rx mode are also measured using 5G NR orthogonal frequency division multiple access (OFDMA)-mode modulated signals.

This article is organized as follows. Section II describes the issues of the current relay transceivers and the advantages of the proposed one and introduces the entire relay system. Section III explains the circuit operation of the transmitter and the detailed analysis for phase calculation. Section IV presents the concept of the proposed WPT system and the circuit operation of the receiver. Section V demonstrates the circuit implementation of the transmitter and receiver. Section VI shows the measurement results, and finally, the conclusion is presented in Section VII.

## II. Wirelessly Powered Relay Transceiver

Fig. 2 shows the concept of the proposed relay system. As shown in Fig. 2(a), by applying the conventional active transceiver architecture to the relay systems, the need of cable wiring, the relatively short product life due to the outdoor circumstances, the large circuit size including the baseband unit (BBU), and the regular maintenance cost are the main issues to face. As the massive deployment of the relay nodes
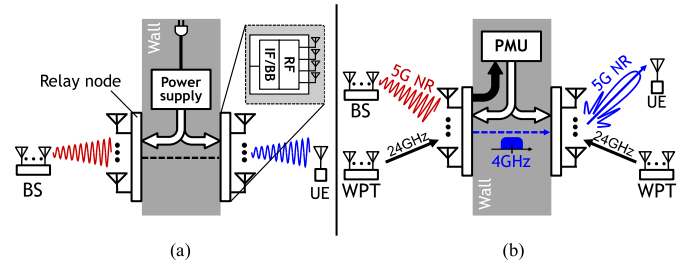


Fig. 2. System block diagrams of (a) conventional active transceiver and (b) proposed wirelessly powered transceiver.

is required and the installation space is limited, the traditional ground-based power supply is not suitable. Moreover, batteries cannot be used due to the unsuitable environment, including the small installation space, dust, rain, and sunlight [10]. To avoid damaging the power supply unit, the wall-mounted concealed installation was considered. However, it may be difficult to get permission from building owners. Besides the power supply issues, the circuit volume is also a problem. As mentioned above, there is not enough space for installing BBU in the massive deployment.

To overcome such problems, we propose a wirelessly powered relay system using 24-GHz WPT. As shown in Fig. 2(b), all the required power for the relay operation is delivered by 24-GHz WPT. The 24-GHz continuous wave is radiated to two relay nodes from a WPT BS. Rectifiers generate dc power from the received 24-GHz WPT signal. The generated power is regulated by a power management unit (PMU) and supplied to the two relay nodes. Thus, the two relay nodes operate without any external power supply. This relay transceiver is 5G NR compatible. The received 28-GHz RF signal is down-converted to a 4-GHz IF signal by using 24-GHz WPT as a local oscillator (LO) signal. The 4-GHz IF signal is transferred to the transmitter side and up-converted to the 28-GHz RF signal in the same way. The simple relay structure makes it easy to apply 5G NR modulated signals.

Fig. 3 shows the block diagram of the entire relay system. The transmitter transmits a 28-GHz 5G signal to UE or BS. The beam angle is controlled by the proposed vector-summing backscattering technique. The receiver receives the 28-GHz 5G signal from BS or UE and the 24-GHz WPT signal from WPT BS. Thus, it can communicate with them while generating dc from the received 24-GHz WPT signal. The receiver can also steer the beam direction for both Rx mode and WPT by the proposed 1-bit passive phase shifter. The receiver utilizes both the 28- and 24-GHz paths, and the same beam pattern can be obtained for 28- and 24-GHz WPT as the phase characteristics of the 1-bit phase shifter are independent of the frequency.

In addition to the 1-bit passive phase shifters, the receiver consists of four-way power combiners and *LC*-loaded rectifiers. The *LC*-loaded rectifier works not only as an RF-dc convertor but also as a self-heterodyne mixer. Therefore, it can down-convert the 28-GHz RF signal to a 4-GHz IF signal by using 24-GHz WPT as an LO signal while generating dc power from the 24-GHz WPT signal. The 4-GHz IF signals are further combined after fine phase shifting and transferred to the transmitter side in a wired way.

The transmitter consists of a 7-bit vector-summing backscatter and an I/Q generator. In the same way as the
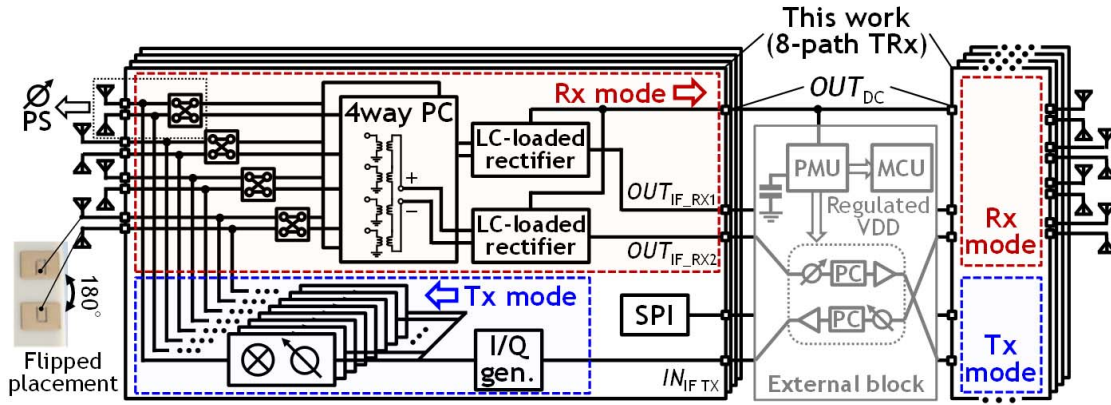
Fig. 3. Block diagram of the entire relay system.

self-heterodyne technique, the 4-GHz IF signal is up-converted to the 28-GHz RF signal using the 24-GHz LO signal. At the same time, phase shifting is achieved with a 360° phase range and 7-bit resolution utilizing the I/Q vector-summing technique.

In this design, eight-path transmitters and receivers are implemented on each chip. Because both transmitter and receiver work only using the generated power from 24-GHz WPT, they do not require any external power supply. The generated power from 24-GHz WPT is boosted to supply voltage at PMU and consumed by the internal bias circuit, external logic controller such as MCU, and IF amplifiers. Note that the IF chain, PMU, and MCU are not implemented on a chip and a prototype module. To prove fully wirelessly powered operation, the breakdown of the generated and consumed power will be shown in Section VI.

## III. TRANSMITTER ARCHITECTURE

To realize low power consumption and beam-steerable transmitter, the vector-summing backscattering technique is introduced in this article. Two transistors with variable gate width are used. Both IF up-conversion and phase shifting by I/Q vector-summing are performed at the same time. Before describing the proposed backscatter, the operation of the most common backscatter and the IF backscatter is discussed.

### A. Load Switching-Based Backscattering

Fig. 4(a) shows the circuit operation of a common binary backscatter [11], [12]. The backscatter receives the carrier frequency signal and reflects a modulated signal by switching the load impedance. It can operate by consuming very low power because phase-locked loops (PLLs) and LO oscillators are not required. On the other hand, it is difficult to apply multi-level modulation schemes and to improve the spectral efficiency. The QAM backscatters based on load switching are reported to enhance spectral efficiency [13]. However, they are difficult to implement because a large number of load impedances are required to achieve a high-order modulation scheme.

### B. IF Backscattering

To achieve low power consumption and high spectral efficiency, the IF backscattering technique is reported [14],
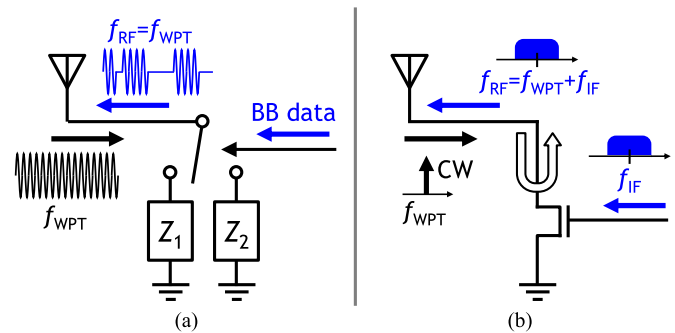


Fig. 4. Conventional backscattering techniques: (a) load switching-based backscatter and (b) IF backscatter.

as shown in Fig. 4(b). Assuming that the gate–source voltage $V_{GS}$ and the drain–source voltage $V_{DS}$ are sinusoidal waves at different frequencies, the up-converted signal appears in drain current $I_{DS}$. This means that the IF backscatter uses the received signal from the antenna as an LO signal and up-converts the IF signal to the RF frequency. Because the modulation is done at the IF frequency, multi-level modulation schemes can be applied. Although an LO is required to up-convert the BB signal to the IF frequency, the operation frequency is lower than the LO frequency of heterodyne and direct-conversion architectures, and the power consumption of the local circuit can be reduced. As a result, high spectral efficiency is achieved while keeping the power consumption low.

### C. Vector-Summing Backscattering

In addition to low power consumption and high spectral efficiency, in order to achieve beamforming, we propose the vector-summing backscattering technique, as shown in Fig. 5. The proposed backscatter consists of two transistors with variable widths and an I/Q generator. It performs both the IF backscatter and the vector-summing phase shifting simultaneously. The basic operation of the two backscatters is the same as the IF backscatter and frequency up-conversion is performed at each backscatter. In addition to the up-converting operation, the phase shifting is also possible by the I/Q vector-summing architecture. Each transistor is assigned to I or Q, and the up-converted I/Q signals are combined at the drain nodes. As the power of the up-converted signal is proportional to the
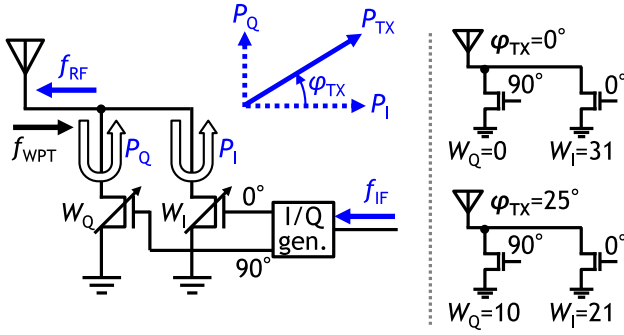
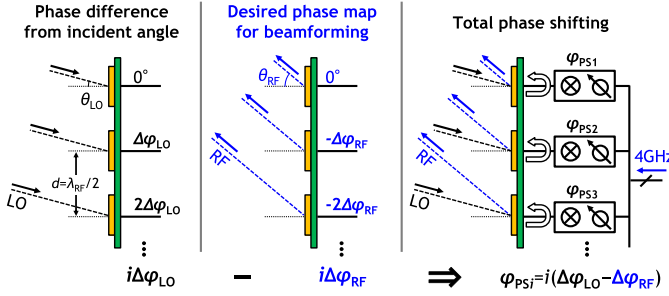Fig. 5.   Circuit operation of the vector-summing backscatter.



Fig. 6.   Phase calculation for beamforming.

square of gate width, the vector-summing is realized without voltage-controlled amplifiers (VCAs) and the output phase is controlled by setting the two gate widths.

Since the backscatter reflects the received signal, the output phase depends on the phase difference of the received signals. Hence, we must consider not only the output phase difference for beamforming but also the input phase difference from the incident angle. Fig. 6 shows the example of the phase calculation for each signal. Here, $\lambda_{RF}$ and $\lambda_{LO}$ are the wavelengths of the transmitted signal and the received signal, respectively. Since $\lambda_{RF} < \lambda_{LO}$, we assume that the antenna distance is $d = \lambda_{RF}/2$. Each phase difference is represented by

$$\begin{cases} \Delta\varphi_{RF} = \dfrac{\pi}{2} \sin\theta_{RF} \\ \Delta\varphi_{LO} = \dfrac{\pi\,\lambda_{RF}}{\lambda_{LO}} \sin\theta_{LO} \end{cases} \quad (1)$$

where $\theta_{RF}$ is the beam angle of the transmitted signal and $\theta_{LO}$ is the incident angle of the received signal.

The total phase difference $\Delta\varphi$ is equal to the difference between $\Delta\varphi_{RF}$ and $\Delta\varphi_{LO}$, and the phase shift amount of each phase shifter is calculated as in the following equation:

$$\varphi_i = i\,\Delta\varphi = i\pi\left(\frac{1}{2}\sin\theta_{RF} - \frac{\lambda_{RF}}{\lambda_{LO}}\sin\theta_{LO}\right) \quad (2)$$

where $i$ is the element number.

In the Tx beam pattern measurement, we calculate and set the phase map using (2).

Table I presents a comparison of backscatters and active phased arrays. The proposed vector-summing backscatter operates with quite lower power consumption than the active phased arrays. Unlike the other backscatters, the proposed backscatter can steer the beam's direction.

TABLE I
COMPARISON BETWEEN TRANSMITTER ARCHITECTURES

| | Load switching-based backscatter [11-12] | IF backscatter [14] | Active phased-array [1-2] | Vector-summing backscatter |
|---|---|---|---|---|
| Power consumption | Low | Low | High | Low |
| Available modulation | ASK | n-QAM | n-QAM | n-QAM |
| Beamforming | No | No | Yes | Yes |

In addition, high-speed communication can be achieved utilizing high-order modulation schemes.

## IV.  RECEIVER ARCHITECTURE

The receiver operates as a rectifier that converts the WPT signal to dc and as a mixer that down-converts the RF signal to IF frequency. Therefore, the following different performance characteristics are required:

1)  high power conversion efficiency (PCE) and long transmission distance for WPT;
2)  beam steering for Rx mode.

First, the PCE represents how efficiently the rectifier converts the RF signal to dc. It is defined by the output dc power $P_{OUT}$ divided by the input RF power $P_{IN}$. Assuming that the input power equals the sum of the rectifier power loss $P_{RL}$ and the output power, PCE can be written as follows:

$$\text{PCE} \equiv \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{RL}}. \quad (3)$$

The loss of the rectifier is due to the turn-on voltage and the reverse leakage current [15]. Therefore, low threshold voltage and low leakage current are important to achieve high PCE. When the total performance, including antennas, power combiners, and transmission lines, is considered, the input power is further degraded by the insertion loss (IL) of each component and the losses of the printed circuit board (PCB). If an $N$-way power combiner is inserted between the rectifier and antennas, then the input power is multiplied by $N$. Therefore, the PCE can be represented by

$$\text{PCE} = \frac{P_{OUT}}{N \times P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{RL} + P_{IL}} \quad (4)$$

where $P_{IL}$ is the total IL between the antenna and the rectifier. Because the PCE can be significantly degraded even with a few dB loss, the IL needs to be kept quite low. Second, similar to the transmitter, the receiver is also required to perform beam steering. However, there is a tradeoff between the resolution of the phase shifter and the PCE. If we increase the number of phase shifters to improve the resolution, the IL will increase and the PCE will significantly drop. To realize the beam steering while maintaining PCE, we utilize a 180° phase shifter with low loss. The phase shifter is shared by the 24- and 28-GHz paths and both beam directions are the same.

### A. Phased-Array Rectifier

Fig. 7 shows the concept of the conventional and the proposed WPT systems. In addition to the PCE mentioned
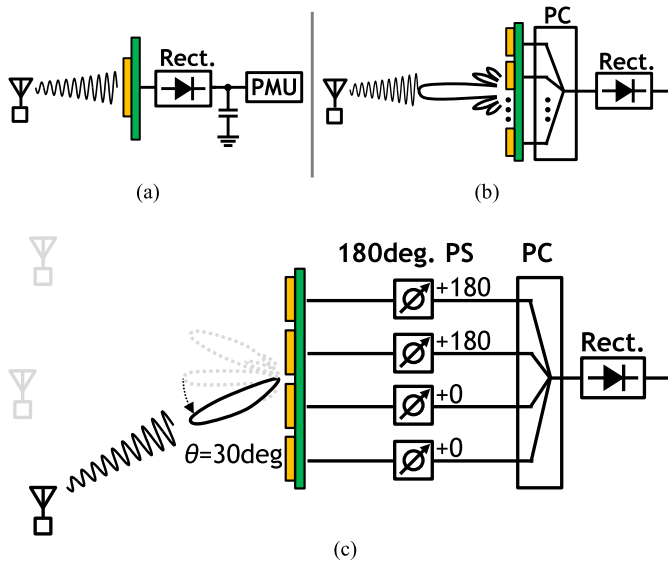
Fig. 7. WPT system block diagram of (a) rectenna, (b) rectenna array, and (c) proposed phased-array rectifier.



Fig. 9. Two circuit operation of the rectifier: full-wave rectifier and self-heterodyne mixer.
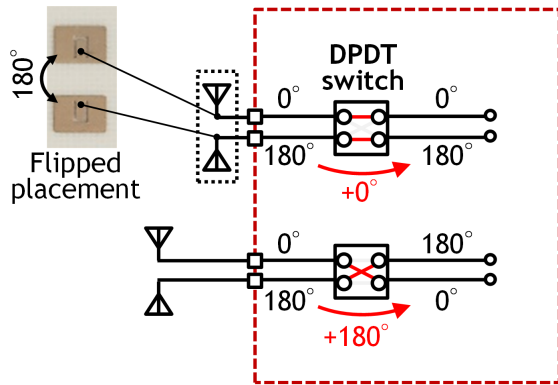


Fig. 8. Circuit operation of the proposed phase shifter.

above, the transmission distance from BS to the harvester is also essential. The theoretical received power of the harvester is calculated from the Friis transmission formula

$$P_R = \text{EIRP}_{\text{BS}} - 20\log_{10}\left(\frac{4\pi d}{\lambda}\right) + G_R \qquad (5)$$

where $\text{EIRP}_{\text{BS}}$ is the effective isotropic radiation power from BS, $G_R$ is the antenna gain of the harvester, $d$ is the transmission distance, and $\lambda$ is the wavelength at the operating frequency.

Various types of rectifiers using a Schottky diode and a diode-connected CMOS transistor have been reported to improve the PCE at low input power [14]–[19]. The Schottky diode type [17] has a shunt resistor before the rectifying diode and it generates the self-bias voltage from a part of the rectified wave, reducing the required RF input power. The diode-connected type [15], [16], [19] utilizes $V_{\text{th}}$ cancellation technique and differential scheme. The source nodes of NMOS and PMOS are biased with half of the output voltage, and the negative balk-source voltage reduces threshold voltages. In addition, twice the input voltage is applied to the gate–source nodes, resulting in a steeper $I - V$ curve and higher PCE. However, these structures still require more
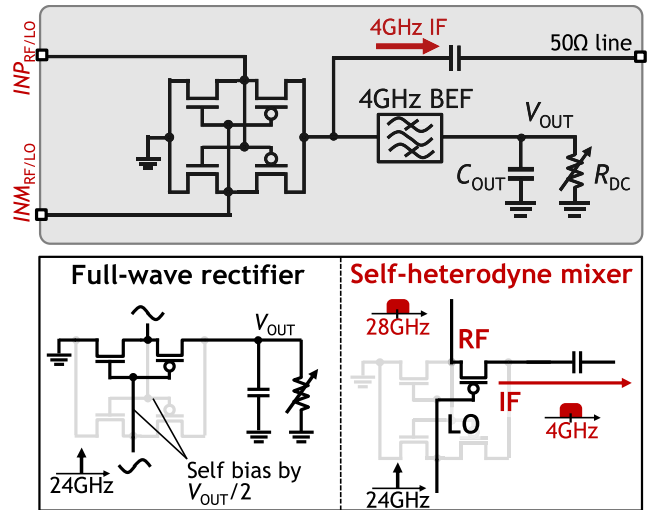
than 6-dBm input power to achieve the maximum PCE at millimeter-wave frequencies. Therefore, the transmission distance of the single rectenna is quite short. Assuming that the WPT frequency is 24 GHz, the equivalent isotropically radiated power (EIRP) is 43 dBm, and the patch antenna gain is 3 dBi, the maximum transmission distance is limited to less than 10 cm. Hence, it is necessary to increase the input power by power combining and make the transmission distance longer. To achieve that, the rectenna array as shown in Fig. 7(b) is reported [20], [21]. However, the beam direction is fixed due to the lack of phase shifters and the PCE can be extremely low when the incident angle is not 0°. To overcome such problems, we propose the phased-array rectifier, as shown in Fig. 7(c). The 180° phase shifters are inserted before the power combiners, and they enable the beam-steerable WPT operation. As mentioned above, since the IL degrades the PCE significantly, the phase shifter consists of a flipped antenna pair and a double-pole double-throw (DPDT) switch to keep the IL low.

### B. 180° Phase Shifter With Flipped Antenna Pair

Various types of phase shifters have been reported for millimeter-wave phased-array. One of these types is the switch-type phase shifter (STPS) with a high-pass-to-low-pass topology [22]. The high-pass filter and the low-pass filter realize +90 and −90° phase shifts, respectively, and a 180° phase difference can be obtained. The IL can be more than 1 dB even with a 1-bit phase shifter. Another type is the reflection-type phase shifter (RTPS) with a 3-dB quadrature coupler [23]. The impedance of the reflection load is changed by the switches and a 180° phase shift is achieved. However, the IL is theoretically more than 3 dB.

To realize a phase shifter loss of less than 1 dB, the flipped antenna pair is utilized as a 0° and 180° signal source in this work. Fig. 8 shows the circuit architectures of the proposed phase shifter. The flipped antenna pair is a set of two antennas arranged symmetrically in the vertical direction. Since the feeding points are opposite, they receive 0° and 180° signals. The two received signals are toggled by the DPDT switch so
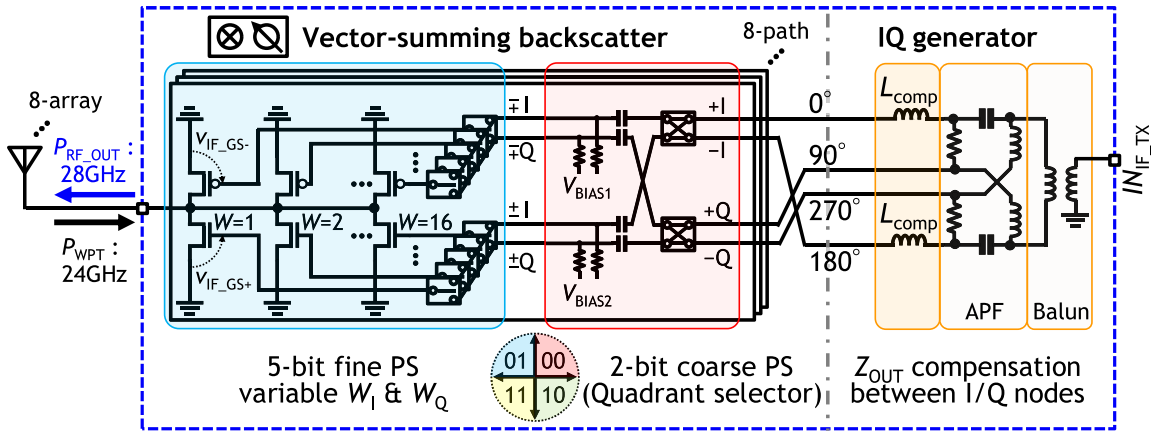
Fig. 10.　Circuit implementation of transmitter.

that the 180° phase shifting can be realized. The simulated maximum IL of the DPDT switch is 0.85 dB. Since the 180° phase difference is determined by the arrangement of the flipped antenna pairs, this phase shifter does not depend on the frequency. Therefore, the same beam direction is obtained for Rx and WPT.

### C. Self-Heterodyne Mixer and Rectifier

The receiver is required to play two different roles: a rectifier that converts WPT signal to dc and a mixer that down-converts the RF signal to IF frequency. Furthermore, the mixer should operate with low power consumption so that it can operate using only the generated power from WPT. However, the conventional heterodyne mixer needs the LO, and it is difficult to reduce the power consumption.

Therefore, the self-heterodyne conversion [24] is adopted in this work. The receiver down-converts the RF signal to the IF frequency without the LO by using the WPT signal as an LO signal. Fig. 9 shows the circuit architecture of the rectifier. For 24-GHz WPT signal, it works as a highly efficient full-wave rectifier [15]. Each MOS transistor is biased with about half of the output voltage $V_{\text{OUT}}$ by the cross-coupled CMOS configuration. In addition, the gate node of transistors is actively biased by a differential signal. Due to the above biasing, the turn-on voltage effectively decreases, and a high PCE can be obtained. On the other hand, for the 28-GHz RF signal, the PMOS part in the rectifier works as a self-heterodyne mixer. The 28-GHz RF signal at the drain node is down-converted by the 24-GHz LO signal at the gate node, and the 4-GHz IF signal is obtained from the source node. Because the rectifier outputs two signals simultaneously, the band eliminate filter (BEF) is added to separate these signals.

## V. CIRCUIT IMPLEMENTATION AND ANTENNA DESIGN

The detailed block diagram of the transceiver is already shown in Fig. 3. All circuits are designed with the standard 65-nm CMOS process. Although both transmitter and receiver require 0–1-V bias voltages generated by internal digital-to-analog converters (DACs), the supply voltage is not needed since they are passive circuits. The transmitter generates an image signal at 20 GHz. However, the phase shift for

28-GHz beamforming causes misalignment at 20-GHz image frequency, so as a result, the image signal at 20 GHz can be suppressed for the desired direction due to smaller array factor. In addition, the 20-GHz image signal is further suppressed in Tx- and Rx modes by BPF characteristics of matching network and antenna.

### A. Transmitter Implementation

Fig. 10 shows the circuit implementation of the transmitter. The I/Q generator is comprised of the balun and the differential all-pass filter (APF) [25]. The APF generates 0°, 90°, 180°, and 270° signals from differential IF signals. The quadrant selector selects an I/Q signal pair for vector-summing from four-quadrature phase signals. When the 0° and 90° are selected as a pair, the output phase is controlled in the range of 0°–90°, i.e., the pair of 180° and 90° covers 90°–180°, the pair of 180° and 270° covers 180°–270°, and the pair of 0° and 270° covers 270°–360°. Since the operation of the quadrant selector is equivalent to determining the quadrant for phase shift, it can be regarded as a 2-bit phase shifter. The vector-summing backscatter has a 5-bit binary-weighed transistor array and realizes fine phase shifting between 0° and 90°. Therefore, the transmitter covers a 360° phase range with 7-bit resolution.

The phase and amplitude mismatch between paths and chips can be compensated by controlling phase setting and bias voltages for each backscatter. The Tx conversion gain (CG) changes by 8 dB between 0- and 0.5-V gate bias voltage.

*1) 5-Bit Binary-Weighted Transistor Array:* The 5-bit binary-weighted transistor array consists of five CMOS structures with different gate widths. Since the gate width doubles, the gate width of the $i$th bit equals $W_0*2^i$, where $W_0$ is the minimum gate width. The variable width as mentioned in Section II is equivalently realized by assigning I or Q signal to each CMOS structure. The selection range of the gate widths $W_I$ and $W_Q$ is from 0 to 31 and each gate width is set so that the sum of them can be 31 when $W_I = 8$ and $W_Q = 23$; 1 LSB is equal to 2.9° phase shift since the backscatter covers a 90° phase range with a 5-bit resolution. From the simulated results, the maximum integral non-linearity (INL) is less than 1.5 LSB, as shown in Fig. 11. Note that the I/Q assignment is
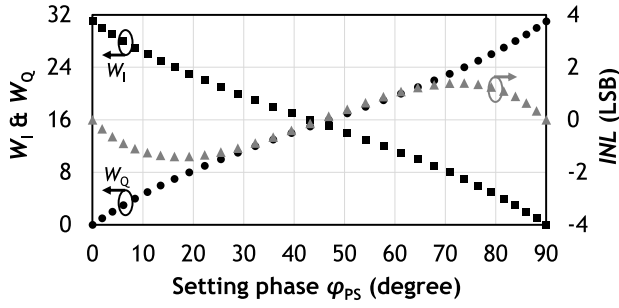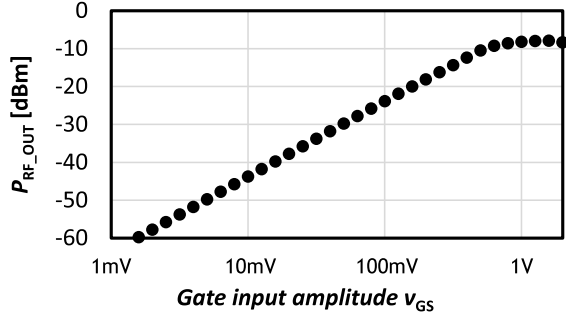
Fig. 11.   Simulated equivalent widths and INL.



Fig. 13.   Simulated Tx CG versus the 24-GHz input power.



Fig. 12.   Simulated Tx output power versus the gate input amplitude.



Fig. 14.   (a) Load capacitance reduction of CMOS structure and (b) output impedances of APF without and with $Z_{OUT}$ compensation.

for phase shift, not for the IF modulation. Therefore, the INL does not affect the EVM and the adjacent channel leakage ratio (ACLR).

Fig. 12 shows the simulated Tx output power as a function of the gate input amplitude $v_{GS}$. When $v_{GS}$ is larger than 0.5 V, the output signal is saturated and distorted. Since the input signal is already modulated, the output signal is degraded only by saturation. Fig. 13 shows the dependency of the output power on the 24-GHz input power. The reflected power depends on drain-to-source and gate-to-source voltages, so the lower input power of 24-GHz WPT signal, the lower CG. However, the Tx EIRP can be improved by increasing the number of elements.

*2) Output Impedance Compensation of APF:* The IF differential signals are generated by the balun and four-quadrature phase signals are generated from them at the APF. In this design, each of the four signals is shared by eight-parallel backscatters. As a result, the load capacitances looked from output nodes of APF are large and degrade the output amplitude of four-quadrature phase signals. To reduce the gate capacitance of backscatters, the binary-weighed transistor array utilizes a CMOS structure. As shown in Fig. 14(a), the CMOS structure requires differential input signals, while a single-ended input is enough for the NMOS-only structure. However, compared to the NMOS-only, the CMOS can reduce the gate width by half, and the gate capacitance can also be halved. Hence, the CMOS structure is more suitable for the APF than the NMOS-only structure.

In addition, the imbalance between the two output impedances of the I- and Q-nodes degrades the phase accuracy and increases the amplitude difference. To match these impedances, two additional inductors are added to the I-nodes. The additional inductors cancel out the capacitive component
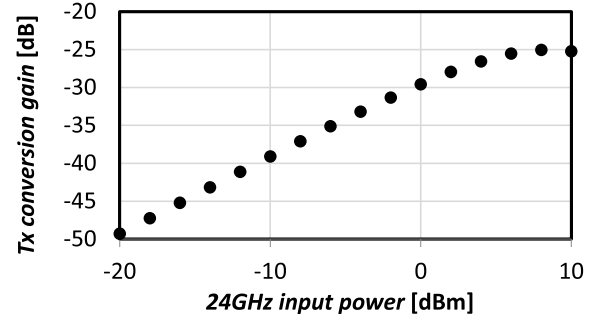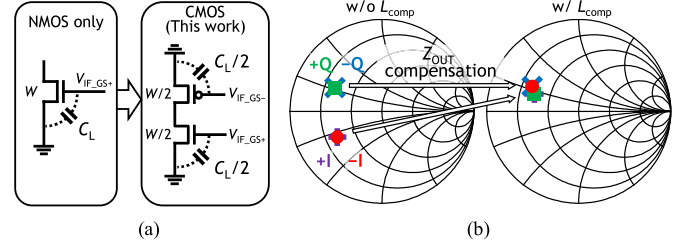
of APF and make four-output impedances equal, as shown in Fig. 14(b). As a result, the phase linearity of a backscatter is improved.

*B. Receiver Implementation*

Fig. 15 shows the schematic of the receiver. The received signals are phase-shifted by the flipped antenna-type phase shifters and power-combined by two four-way power combiners. One of the combiners combines four 0° signals and the other one combines four 180° signals. The capacitance $C_m$ is for impedance matching on the input side and is 250 fF. After the power combining, the *LC*-loaded rectifiers convert the 24-GHz WPT signal to dc and down-convert the 28-GHz RF signal to 4-GHz IF frequency. The two generated dcs' are connected in parallel and applied to the load resistor. The two 4-GHz IF signals are connected to separate output ports since they have different phases.

*1) RF DPDT Switch:* Fig. 16 shows the detailed circuit diagram of the RF DPDT switch. The switched parallel resonance network topology [26] is utilized to reduce the IL. To connect the input port IN1 to the output port OUT1, MOS transistors $M_2$ and $M_4$ turn off and $M_1$ and $M_3$ turn on. The OFF-capacitance of transistors $M_2$ and $M_4$ resonates with the inductor and blocks the path from port IN1 to port OUT2. The ports IN1 and OUT1 are connected by the ON-resistance of transistor $M_1$, and the ports IN2 and OUT2 are connected by the transistor $M_3$. Thus, the signal from port IN1 can be routed to port OUT1 while isolating ports IN1 and OUT2. The sizes of the MOS transistors are determined by considering the tradeoff between the IL and the isolation. As the gate width increases, the OFF-capacitance $C_{off}$ increases proportionally, while the ON-resistor $R_{on}$ decreases inversely. A small $R_{on}$ results in a low IL, but a large $C_{off}$ degrades the isolation [26]. In this design, the gate width is set to 76.8 $\mu$m to achieve low IL.
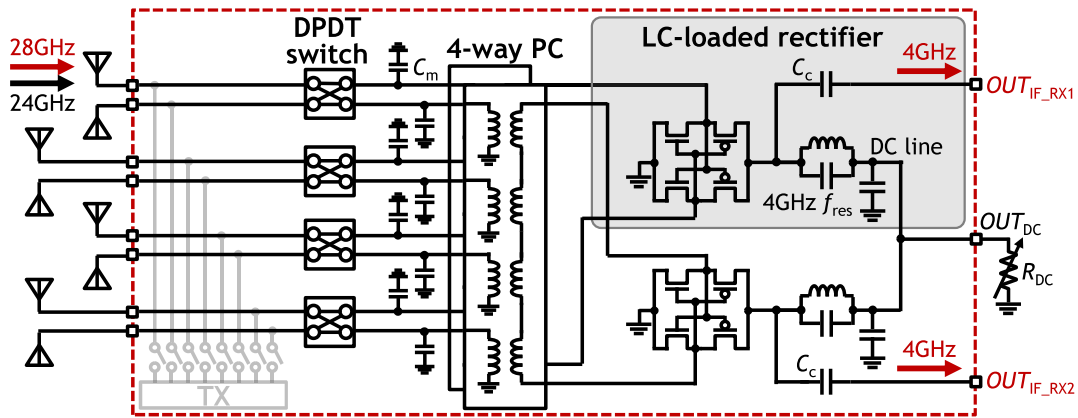
Fig. 15.    Circuit implementation of receiver.



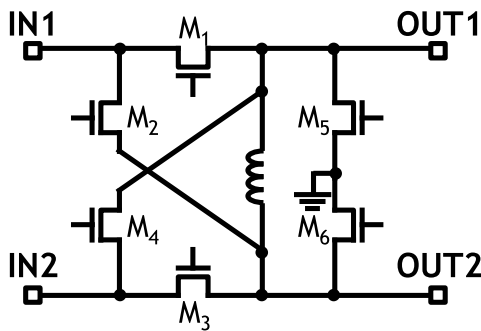Fig. 16.    Detailed circuit diagram of RF DPDT switch.
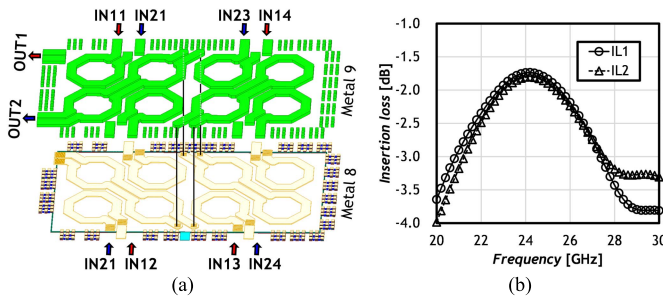


Fig. 17.    (a) Simulated model and (b) IL of four-way power combiner.

*2) Four-Way Power Combiner:* The model of the four-way power combiner is shown in Fig. 17(a). It was designed using an electromagnetic field simulator. To simplify the wiring on chip and the transmission line on the PCB, the two power combiners are joined in a complex way. Half of the secondary coil is formed on metal 8, and the other half is formed on metal 9. The primary coils are also formed on metals 8 and 9, and two coils share the ground port. As shown in Fig. 17(b), the simulated IL is −1.7 and −1.8 dB for each combiner. In the case of input phase mismatches, the IL increases, but the input impedances do not change.

*3) LC-Loaded Rectifier:* Since the rectifier outputs dc and the 4-GHz IF signal simultaneously, the filter is required to separate these signals. Hence, the *LC* load with 4-GHz resonate frequency is inserted to the output side. The *LC* load has a high impedance at 4 GHz, and the 4-GHz IF signal passes through the 50-$\Omega$ impedance line. The capacitance $C_c$ is
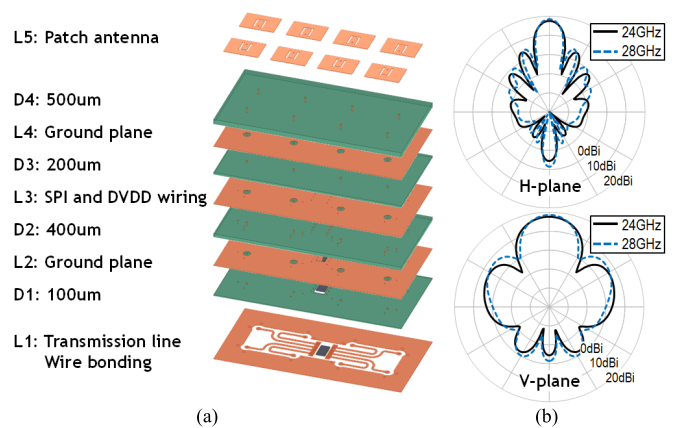


Fig. 18.    (a) Illustration of phased-array antenna and (b) simulated beampattern of 4 × 8 phased-array antenna.

for dc block, and its value is 1.2 pF. On the other hand, at other frequencies, the large capacitance for stabilizing the output voltage $C_{OUT}$ can be found in the rectifier. Therefore, the *LC* load does not affect the performance of RF-to-dc conversion. The generated dc goes through the inductor and appears at the load resistance $R_{dc}$. $R_{dc}$ is determined to maximize PCE at the desired input power. The optimum value is 250 $\Omega$ in this design.

*C. Antenna Design*

The dual-band phased-array antenna is shown in Fig. 18(a). Since the proposed transceiver utilizes 24 GHz for WPT and 28 GHz for 5G communication, the phased-array antenna is designed to receive and transmit signals at dual bands. In addition, the phase shifter uses the pair of two antennas as a 0° and 180° signal source. Therefore, the upper and lower antennas are symmetrically arranged in the vertical direction.

The antenna board is fabricated using Megtron6 R5775K, which has a dielectric constant of 3.6 and a dielectric loss tangent of 0.004. The antenna board is composed of five copper layers: L1 for transmission line and wire bonding, L2 for the ground plane, L3 for the supply voltage and SPI wiring, L4 for the ground plane, and L5 for the patch antennas. The antenna distance $d$ is 5.3 mm, which corresponds to half of
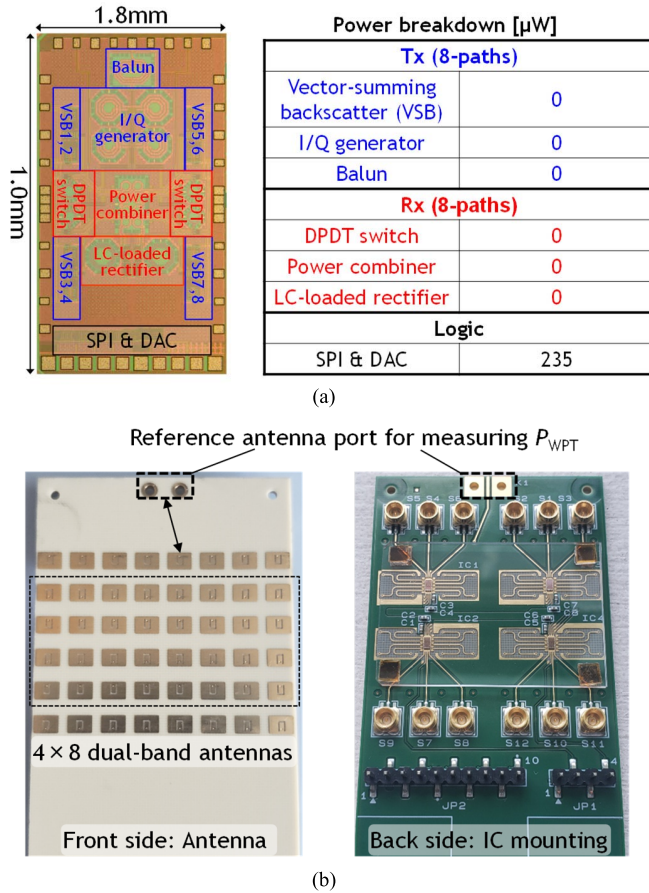
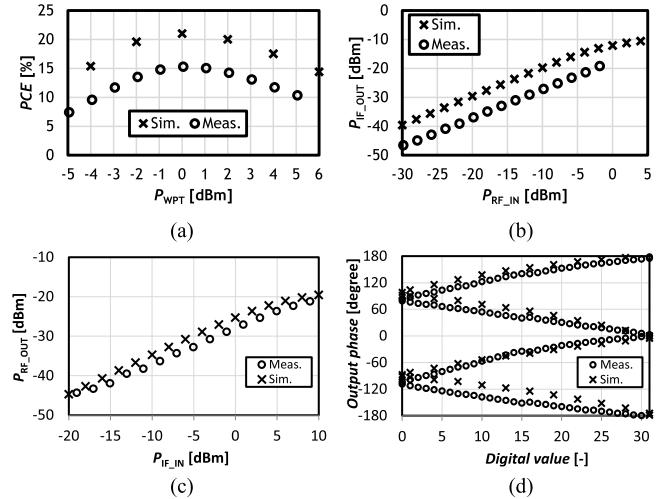Fig. 19. (a) Die photograph and power breakdown table. (b) Photograph of 4 × 8 phased-array module.



Fig. 20. Simulated and on-wafer measured results: (a) PCE, (b) Rx linearity, (c) Tx linearity, and (d) Tx phase linearity.

the wavelength at 28 GHz. To achieve the dual-band gain, the U-slot antenna is utilized. The main patch and U-slot resonate at different frequencies, and the dual-band characteristic can be obtained. The simulated beam pattern of the 4 × 8 array is shown in Fig. 18(b). The total realized gain is 17.5 and 18.5 dBi at 24 and 28 GHz, respectively.

## VI. MEASUREMENT RESULTS

Fig. 19(a) shows the die photograph and power breakdown. The chip was fabricated in a standard 65-nm CMOS process. The chip size of the eight-path phased-array transceiver is 1.8 mm × 1.0 mm. Since all circuit blocks except for the logic part are passive, the power consumption is only 240 $\mu$W for the bias circuit. As shown in Fig. 19(b), four chips are wire-bonded to a PCB with a 4 × 8 phased-array antenna. The prototype module is used to evaluate the over-the-air (OTA) performance. The module has a row of dummy antennas at the top and bottom of the active antenna array. One of them is connected to a connector and used as a reference antenna port. The 24-GHz input power $P_{\text{WPT}}$ is determined by measuring the received power of the reference antenna. It is used to calculate PCE in (4). The WPT performance can also be plotted as a function of power density [27]. The power density is calculated by (6) using $P_{\text{WPT}}$

$$P_D = \frac{4\pi P_R}{\lambda^2 G_R} \cong \frac{4\pi P_{\text{WPT}}}{\lambda^2 G_R} \qquad (6)$$

where $G_R$ represents the antenna gain of the receiver, measured by the reference antenna. In the WPT and TRX measurements, the distance from a horn antenna (BS) to the module is set to be 0.2 m.

First, the probe measurement results of the proposed transceiver are shown in Fig. 20, which summarizes the simulated performance and the measured performance. In the on-wafer measurement, one of two receivers and four of eight backscatters are measured using four paths. The single-ended signals are input to the four ports, leaving the remaining four ports as open. For Tx and Rx measurement, a directional coupler is used to mix and separate 28- and 24-GHz signals. Fig. 20(a) shows the measured PCE. Note that the total input power is $P_{\text{WPT}} + 6$ dB due to the four-input power combining. These results include the IL of the power combiners and the DPDT switch. The maximum PCE is 15% at the 24-GHz input power of 0 dBm. Due to the power combining, the input power for the maximum PCE is reduced by 6 dB. Fig. 20(b) presents the simulated and measured output power for Rx mode. $P_{\text{IF\_OUT}}$ on the vertical axis is the output power of the 4-GHz IF signal and $P_{\text{RF\_IN}}$ on the horizontal axis is the input power of the 28-GHz RF signal. The measured CG is −17 dB and the measured IP1dB and OP1dB are −3.8 and −21.8 dBm, respectively. Fig. 20(c) and (d) shows the simulated and measured Tx-mode linearity and phase linearity. $P_{\text{IF\_IN}}$ on the horizontal axis represents the input power of the 4-GHz IF signal and $P_{\text{RF\_OUT}}$ on the vertical axis represents the output power of the 28-GHz RF signal. The measured saturated output power $P_{\text{sat}}$ is −21 dBm and a 360° phase range can be covered.

The OTA performance is measured using a 4 × 8 dual-band phased-array antenna board. Fig. 21 summarizes the OTA measured performance. Fig. 21(a) and (b) shows the generated power plotted as a function of $P_{\text{WPT}}$ and as a function of the antenna array size. In this measurement result, the IL caused by the PCB and the bonding wires is included. The 32-element module generates a 3.1-mW dc power from a 17-dBm total input power at the incident angle of 0°. Note that the total input power equals $P_{\text{WPT}} + 15$ dB for 32-element configuration. Here, the equivalent power density $P_D$ is 6.7 mW/cm² at 24 GHz. As the antenna area increases, the generated
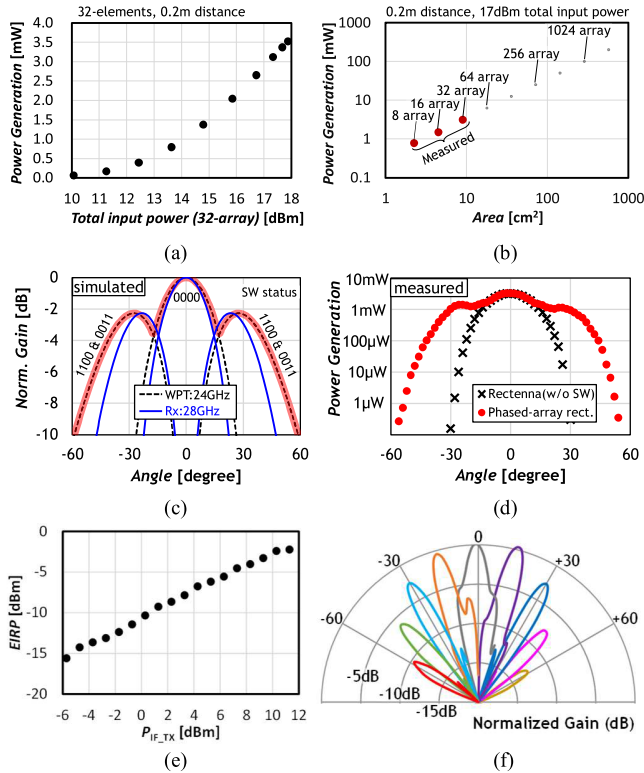
Fig. 21. OTA measurement results: power generations as functions of (a) input power, (b) array size, (c) simulated beam pattern for Rx and WPT, (d) measured beam patterns for WPT, (e) Tx EIRP, and (f) Tx beam pattern.

power also increases proportionally. In the case of 256 arrays, 24.9 mW can be estimated. Fig. 21(c) and (d) shows the simulated beam patterns for Rx and WPT mode and measured beam patterns for WPT. By switching the status of the DPDT switch, three effective beams are formed. The red highlighted line is a composite of the three beam patterns and is consistent with the measured beam pattern. Compared with the conventional rectenna array where the switch status corresponds to "0000," the phased-array rectifier can generate more than 1 mW in the range from $-30°$ to $+30°$. The beam pattern of Rx and WPT modes is misaligned due to their different frequencies. However, the wavelengths of 24 and 28 GHz are close and the same beam patterns can be achieved between $-30°$ to $+30°$. Fig. 21(e) and (f) shows the measured EIRP and the measured beam pattern in the azimuth plane. The saturated EIRP is $-2.2$ dBm at 11-dBm input power. Although the achievable EIRP is quite lower than that of an active relay transceiver, it can be enhanced by increasing the number of elements. The beam pattern of the $4 \times 8$ array is also measured in the azimuth plane with a 15° step. The proposed transmitter covers a beam angle range of $-30$ to $+30°$. The beam-steerable range is defined by the $-3$-dB point from the main lobe power at 0° of the azimuth angles.

In addition to the above results, EVM, ACLR, and spectrum are measured for both Tx and Rx modes with a 5G NR modulated signal. Fig. 22 shows the equipment setup for Rx- and Tx-mode EVM measurements. The beam angle is optimized for the direction of the 28-GHz horn antenna and the communication distance is 0.2 m similar to the WPT measurement.
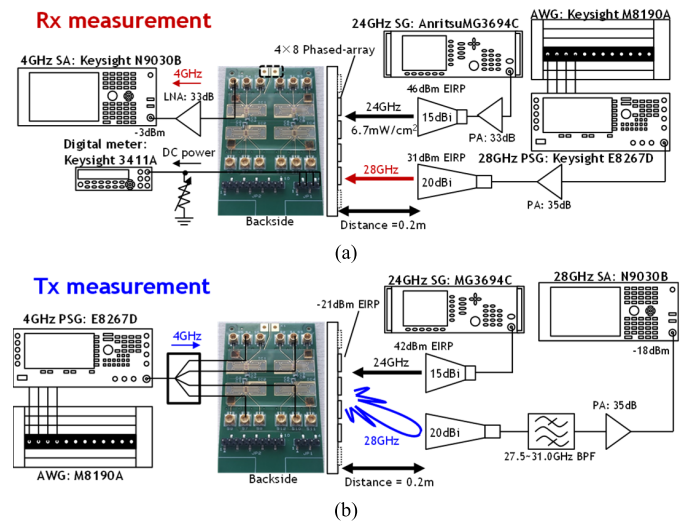


Fig. 22. EVM measurement setup for (a) Rx mode and (b) Tx mode.



Fig. 23. Measured EVMs and constellations for Tx and Rx modes.

The OFDMA-mode modulated signal is generated by the Keysight arbitrary waveform generator (AWG) M8190A and programmable signal generator (PSG) E8267D with the Signal Studio N7631C. The four I/Q modulated signals are generated by the AWG and up-converted by the internal mixer and LO signal of the PSG. The received signal is analyzed by the Keysight PXA spectrum analyzer (SA) N9030B with vector signal analyzer (VSA) 89601A. The power density of the 24-GHz signal is about 6.7 mW/cm² for both Tx and Rx modes. In the Rx-mode measurement, only one of four output signals is amplified by an LNA and analyzed by SA. In the Tx-mode measurement, four modulated signals are generated by a four-output divider and all four input ports of the module are used. Fig. 23 shows the measured constellations and EVMs for Tx and Rx modes. The power back-off (PBO) is set to 9 dB to improve the transmitter linearity. The 400-MHz standard-compliant 5G NR OFDMA-mode signals are used for both Tx and Rx modes. As shown in Fig. 23, the proposed 32-element module can transmit the 400-MHz OFDMA-mode signal using QPSK with $-27.9$-dB EVM, 16-QAM with $-27.8$-dB EVM, and 64-QAM with $-27.5$-dB EVM.

Table II shows the comparison between this work and the state-of-the-art 28-GHz phased-array transceivers [1], [2]. Since the rectifier is implemented, the receiver can generate dc power from the 24-GHz WPT signal. Furthermore, due to the
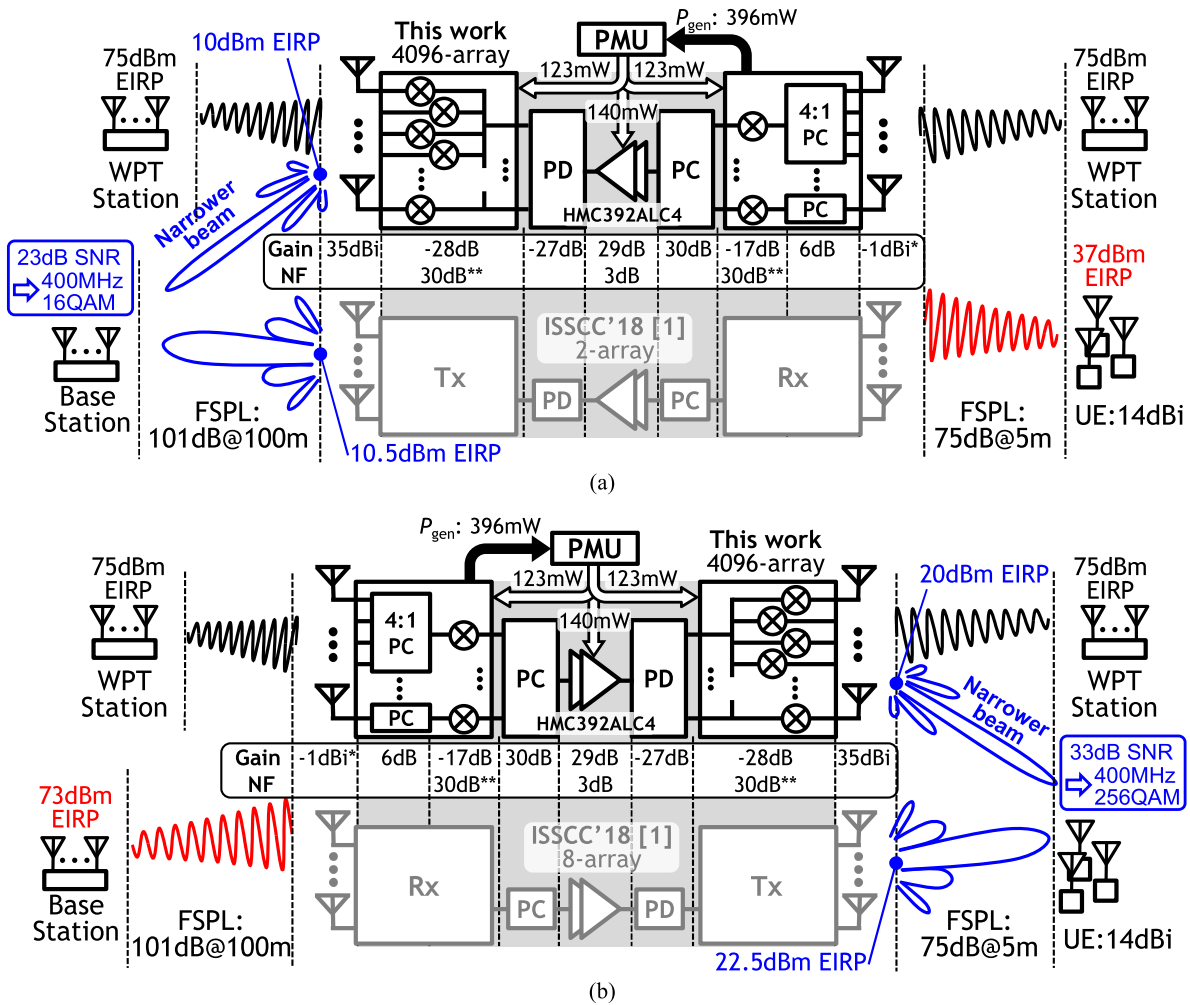
\* Single antenna gain considering -4dB gain loss due to the Rx beam forming, \*\*estimated NF from the simulation results (Rx:24.6dB, Tx:28.3dB).

Fig. 24. Level diagrams for (a) uplink and (b) downlink.

proposed vector-summing backscatter and *LC*-loaded rectifier, the beam-steerable relay operation is achieved while consuming only 0.03 mW for each path. Note that the transmitter and receiver do not consume power because they are passive circuits. However, the biasing DACs and the SPI module used for bias control consume power. Thus, 0.03 mW/path of power consumption is mainly from the biasing circuit. Table III presents the comparison between this work and the millimeter-wave rectifiers [16]–[18]. The power generation at 30° of azimuth angle is calculated from the generated power at 0° and the beam pattern. The power density $P_D$ is almost unified at 6.7mW/cm$^2$. Due to the phased-array rectifier, larger power generation is achieved at 30°.

Fig. 24 shows the level diagrams for the uplink and downlink. The conditions are shown in Table IV. We assume that the transmission distance for WPT is 5 m and the communication distance with UE and BS is 5 and 100 m, respectively. To compare the performance with other transceivers and explain the advantages of the proposed one, the active phased-array transceiver [1] is added to both level diagrams. The array size of the active transceiver is calculated to achieve the same EIRP as the proposed one: two arrays for uplink and eight arrays for downlink. The proposed module with 4096 arrays can relay

## TABLE II
PERFORMANCE COMPARISON WITH 5G PHASED-ARRAY TRANSCEIVERS

| | This work | Active Phased-Array VLSI2020 [2] | Active Phased-Array ISSCC2018 [1] |
|---|---|---|---|
| **Process** | 65nm CMOS | 65nm CMOS | 65nm CMOS |
| **Frequency** | 28GHz | 28GHz | 28GHz |
| **Number of array** | 4×8 | 4×16 | 2×4 |
| **Power generation** | 3.1mW | No | No |
| **Power consumption / path** | Tx: 0.03mW Rx: 0.03mW | Tx: 186mW Rx: 88mW | Tx: 119mW Rx: 42mW |
| **Rx IP1dB** | -3.8dBm | -22.7dBm | N/A |
| **Tx EIRP @$P_{sat}$** | -2.2dBm | 52.2dBm | 35dBm |
| **Tx phase shift** | Vector-summing backscattering 360° / 7bit | Active vector-summing 360° / 5bit | Passive type 360° / 3bit |
| **Chip area / path** | 0.2mm$^2$ | 1.5mm$^2$ | 1.2mm$^2$ |

400-MHz modulated signal in 256-QAM for downlink and in 16-QAM for uplink. The estimated power consumption of transmitters, receivers, and IF chain is 386 mW, which can be supplied only by 24-GHz WPT. Moreover, compared to the active transceivers, when EIRPs are almost the same, the

TABLE III

PERFORMANCE COMPARISON WITH MILLIMETER-WAVE RECTIFIERS

|  | This work | TMTT2016 [16] | TCAS2014 [17] | WPTC2017 [18] |
|---|---|---|---|---|
| Process | 65nm CMOS | 65nm CMOS | Schottky diode | Schottky diode |
| Frequency | 24GHz | 24GHz | 24GHz | 24GHz |
| Number of elements | 4×8 | 1 | 2×2 | 2×2 |
| Phase shifting | 180° phase shifter | No | No | No |
| PCE* from 0° | 5.7% | 21% | 22% | 8.3% |
| PCE* from 30° | 3.5% | 15.0% | 1.6% | 0.3% |
| Power gen.* from 0° | 3.1mW | >0.9mW** | 3.3mW | 0.9mW |
| Power gen.* from 30° | 1.0mW | >0.2mW** | 0.4mW | 0.2mW |

\* 6.7mW/cm$^2$ power density, \*\* at 6.4mW/cm$^2$

TABLE IV

CONDITIONS FOR LEVEL DIAGRAM CALCULATION

|  |  | 32-element (measured) | 4096-element (estimated) |
|---|---|---|---|
| Tx | Distance | 0.2m from horn antenna (HA) | UL: 100m from BS<br>DL: 5m from UE |
|  | EIRP | -11dBm @9dB PBO | UL: 10dBm @-18.2dBm $P_{\text{IF\_IN}}$<br>DL: 20dBm @-8.2dBm $P_{\text{IF\_IN}}$ |
| Rx | Distance | 0.2m from HA | UL: 5m from UE<br>DL: 100m from BS |
| WPT | Distance | 0.2m from HA | 5m from WPT station |
|  | Power generation | 3.1mW @6.7mW/cm$^2$ | 396.8mW @6.7mW/cm$^2$ |

proposed module can provide a higher spatial resolution by a 4096-array antenna.

## VII. CONCLUSION

This article has presented the wirelessly powered relay transceiver for 5G communication, which realizes beam-steerable relay operation with low power consumption and achieves a wide-angle coverage in WPT. The proposed transmitter with vector-summing backscatter covers the 360° phase range with a 7-bit resolution and achieves a −2.2-dBm saturated EIRP. The phased-array rectifier generates 3.1 mW at 6.7 mW/cm$^2$ power density and realizes a wider receiving angle than the conventional rectenna arrays. Both transmitter and receiver consume only 0.03 mW/path and operate only using the generated power from the WPT signal. From the EVM measurement, the standard-compliant 5G NR OFDMA-mode modulated signal with 400-MHz bandwidth can be transmitted and received for both the uplink and the downlink. The proposed transceiver can contribute to the spread of the 5G network as a repeater between outdoors and indoors.

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**Michihiro Ide** received the B.E. degree from the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan, in 2020. He is currently pursuing the M.S. degree in electrical and electronic engineering with the Tokyo Institute of Technology.

His research interests include CMOS millimeter-wave transceiver systems, fifth-generation (5G) communication, phased-array transceiver, and wireless power transfer systems.

**Atsushi Shirane** (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motor with wireless communication. He is currently an Assistant Professor with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include RF CMOS transceiver for the Internet of Things (IoT), fifth generation (5G), and satellite communication.

Dr. Shirane is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE).

**Kiyoshi Yanagisawa** received the B.E. and M.E. degrees in information science from Tohoku University, Sendai, Japan, in 1998 and 2000, respectively.

From 2013 to 2019, he was with Rohde & Schwarz, Munich, Germany, where he was engaged in the test and measurement of wireless systems. From 2019 to 2020, he was a Researcher with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan. His research interest includes new technology in wireless systems and devices.

Mr. Yanagisawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE).

**Dongwon You** received the B.S degree in electrical and computer engineering from Ajou University, Suwon, Korea, in 2017, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2019, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His current research interests include CMOS analog/RF/millimeter-wave transceiver systems, multiple-input–multiple-output (MIMO), mixed signal, wireless communication, satellite communication, and device modeling.

**Jian Pang** (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

From 2019 to 2020, he was a Post-Doctoral Researcher with the Tokyo Institute of Technology. He is currently a Special Appointed Assistant Professor with the Tokyo Institute of Technology, focusing on fifth-generation (5G) millimeter-wave systems. His current research interests include high-data-rate area-efficient millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile system, multiple-input–multiple-output (MIMO), and mixed-signal systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Predoctoral Achievement Award for the term 2018–2019, and the Seiichi Tejima International Student Research Award in 2020. He serves as a Reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, and IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

**Kenichi Okada** (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science at Kyoto University. In 2003, he joined the Tokyo Institute of Technology as an Assistant Professor. He is currently a Professor of electrical and electronic engineering at the Tokyo Institute of Technology, Tokyo, Japan. He has authored or coauthored more than 400 journal articles and conference papers. His current research interests include millimeter-wave CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for fifth generation (5G), WiGig, satellite and future wireless systems, digital phase-locked loop (PLL), synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth Low Energy, and sub-GHz applications.

Dr. Okada is/was a member of the Technical Program Committee of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), and Radio Frequency Integrated Circuits Symposium (RFIC). He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC Prolific Author Award in 2020, the Kenjiro Takayanagi Achievement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC Best Paper Award in 2020, and more than 50 other international and domestic awards. He is/was a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).