A 3.2-GHz 405 fs_{rms} Jitter −237.2 dB FoM_{JIT} Ring-Based Fractional-N Synthesizer

Ahmed Elmallah, *Member, IEEE*, Junheng Zhu, *Member, IEEE*, Amr Khashaba, *Student Member, IEEE*, Karim M. Megawer, *Member, IEEE*, Ahmed Elkholy, *Member, IEEE*, and Pavan Kumar Hanumolu, *Fellow, IEEE*

***Abstract*— A ring-oscillator (RO)-based low-jitter digital fractional-N frequency synthesizer is presented. It employs a frequency doubler (FD) that doubles the reference clock frequency, a 2-bit time-to-digital converter (TDC) with optimized thresholds to minimize the quantization error, and a high-resolution digital-to-time converter (DTC) to cancel the quantization error of the delta-sigma fractional divider (FDIV). DTC's linearity is improved using a piecewise linear (PWL) function-based correction scheme. On-chip digital calibration is extensively used to correct imperfections of the FD, TDC, and DTC. A prototype synthesizer incorporating the proposed techniques and implemented in a 65-nm CMOS produces a 3.2-GHz output clock from a 96-MHz input clock. The worst-case integrated jitter is 306 and 405 fs in integer and fractional-N modes, respectively. The synthesizer consumes 11.7 mW from a 1-V supply of which 7.84 mW is consumed by the oscillator. The jitter figure-of-merit of the synthesizer is −237.2 dB.**

***Index Terms*— Fractional-N, high-resolution digital-to-time converter (DTC), optimum-threshold time-to-digital converter (TDC), piecewise linear (PWL) nonlinearity correction, quantization error cancellation (QEC), ring voltage-controlled oscillator (VCO), serializer–deserializer (SerDes).**

I. Introduction

LOW-jitter fractional-N frequency synthesizers play a crucial role in wireline transceivers. They synthesize fractional frequencies from a fixed-frequency reference clock typically provided by a crystal oscillator. Because the output frequency can be set very precisely, fractional-N synthesizers are used in wireline transceivers to set the data rate precisely in the transmitter [1] and to perform clock recovery in the receiver [2]. They also provide a great deal of flexibility in a multi-lane serializer–deserializer (SerDes) for setting the data rates in a fine-grained manner. For instance, they allow data rate optimization on a per-lane basis depending on the data demand and provide maximum flexibility in supporting a wide range of standards with backward compatibility. In order to leverage these significant benefits in practice, the synthesizers must be designed in an area- and power-efficient manner.

Low-jitter fractional-N frequency synthesizers are traditionally implemented using LC-oscillator-based analog phase-locked loops (PLLs) [3]. While they are shown to achieve excellent jitter and spurious performance, they suffer from several drawbacks. These include limited output frequency range, large silicon area, and electromagnetic (EM) coupling susceptibility. These shortcomings are exacerbated when many lanes in a multi-lane transceiver are packed in a small space [4].

In a typical multi-lane SerDes, the per-lane PLL is subjected to EM-coupling from PLLs, transmitter drivers, and receivers in adjacent lanes. Strong nearby EM aggressors can introduce large spurs, degrade phase noise, and even push the synthesizer out of the lock. These effects become more pronounced when the adjacent lanes operate at slightly different data rates, a situation typically encountered in re-timer applications [4].

In addition, it is becoming increasingly difficult to implement analog PLLs in advanced CMOS processes [5]. Digital PLLs have recently emerged as an alternative to analog PLLs, even in high-performance applications [6]. By replacing the phase-frequency detector (PFD), charge-pump, and large RC filter in an analog PLL with a time-to-digital converter (TDC) and a digital filter, digital PLLs can alleviate scaling issues that plague analog PLLs. While their performance has traditionally been inferior to their analog counterparts, especially when using ring oscillators (ROs), recent efforts have been successful in reducing the performance gap [6], [7]. In this article, we present several techniques to improve their performance further. These include: 1) a highly linear high-resolution digital-to-time converter (DTC) architecture that improves resolution and linearity by reusing newly added fine step to cancel the nonlinearity of the coarse first stage; 2) an optimum threshold TDC, which reduces the quantization noise with minimal power/area penalty; and 3) a digitally calibrated reference frequency doubler (DUB) to increase reference clock frequency. The proposed techniques help

Manuscript received July 25, 2021; revised October 18, 2021 and December 15, 2021; accepted January 2, 2022. Date of publication January 27, 2022; date of current version February 24, 2022. This article was approved by Associate Editor Farhana Sheikh. This work was supported by Analog Devices. *(Corresponding author: Ahmed Elmallah.)*

Ahmed Elmallah and Amr Khashaba were with the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. They are now with MediaTek, Irvine, CA 92620 USA (e-mail: elmalla2@illinois.edu).

Junheng Zhu was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. He is now with Qualcomm Inc., San Diego, CA 92121 USA.

Karim M. Megawer was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. He is now with Apple, San Diego, CA 92122 USA.

Ahmed Elkholy was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. He is now with Broadcom, Irvine, CA 92618 USA.

Pavan Kumar Hanumolu is with the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3143468.

Digital Object Identifier 10.1109/JSSC.2022.3143468

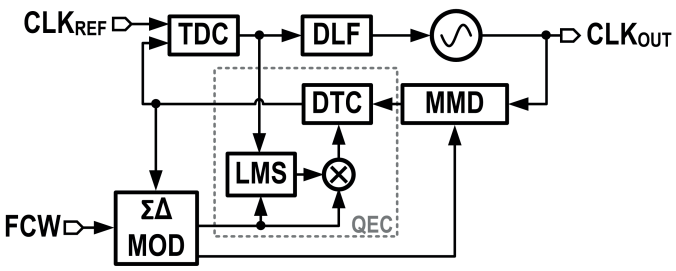


Fig. 1. Conventional DTC-based digital fractional-N frequency synthesizer.

increase the loop bandwidth to suppress RO phase noise and achieve low jitter in a power-efficient manner [4]. The prototype RO-based synthesizer, fabricated in a 65-nm CMOS process, achieves a worst-case integrated jitter of 405 fs with an excellent jitter figure-of-merit (FoM_{JIT}) of −237.2 dB.

The rest of the article is organized as follows. After providing a brief overview of the digital RO-based synthesizers in Section II, we present the proposed synthesizer architecture, along with a description of the main components in Section III. System and circuit implementation details are discussed in Section IV, and the measurement results obtained from the prototype synthesizer are presented in Section V, and the key contributions of this article are summarized in Section VI.

II. Brief Overview of RO-Based Synthesizers

RO-based frequency synthesizers offer many attractive features compared to their LC counterparts. These include lower susceptibility to EM coupling, wide frequency range (essential for supporting multi-standard operation), and smaller area. They can also provide multi-phase clocks that are needed in high-speed sub-rate transmitters and receivers. While these advantages are substantial, their poor phase noise performance has precluded their usage in high data rate applications. The inferior noise performance is mainly attributed to the higher intrinsic phase noise of the RO compared to the LC oscillator. Conflicting noise bandwidth requirements that prohibit simultaneous suppression of fractional divider (FDIV) quantization error and oscillator phase noise further exacerbate this issue [8].

Quantization error cancellation (QEC) techniques [3], [9], [10] in which FDIV quantization error is canceled before it appears as phase noise at the synthesizer output can help extend the bandwidth. However, for any of these QEC schemes to be effective, a high-resolution and highly linear TDC is needed, which is challenging to design and, perhaps more importantly, incurs a hefty power penalty [8]. Recently reported QEC techniques based on DTCs hold much promise in eliminating the need for a high-performance TDC [11]. As shown in Fig. 1, the DTC placed at the output of the divider performs the QEC, thus reducing the amount of phase error seen by the TDC. As a result, the required TDC range is significantly reduced. However, the quantization error, especially when a 1-bit TDC (bang-bang phase detector) is used, still has a significant detrimental impact on the synthesizer jitter performance [8]. In this event, because the TDC quantization error is low-pass filtered by the PLL, a narrow bandwidth may be needed to reduce output jitter degradation. However, this introduces an undesirable tradeoff since a wide bandwidth is required to suppress the RO's phase. An alternate approach to reducing the impact of TDC quantization error is based on amplifying the input phase error before feeding it to the TDC [9]. This reduces the input-referred TDC quantization error by the time-amplification factor (i.e., time amplifier gain). This approach helped reduce the effective quantization step from about 15 ps to 1 ps in [8]. While this improvement is significant, the output jitter was still large, and reducing it by further is difficult because of the challenges associated with implementing high-gain, low-noise, linear time amplifiers [8].

A DTC-based QEC can relax TDC's linearity and range requirements [11]. However, for this method to be effective, the DTC needs to fulfill the stringent range/resolution/linearity requirements. The range of the DTC must span at least one oscillator period, and its resolution must be better than a few hundred femtoseconds. Because the DTC's entire range is exercised during QEC, DTC's integral nonlinearity (INL) must be small to avoid introducing fractional spurs. Unfortunately, it is challenging to simultaneously achieve a wide range, low jitter, small INL, high supply noise immunity, and low power consumption [12]. For instance, increasing the range usually requires reducing the slope of the input clock, which increases DTC's sensitivity to both random noise and supply noise. Furthermore, reducing the slope also degrades linearity because it makes the time constant associated with the charging/discharging process a function of the slope of the input signal [1].

Constant-slope DTCs can alleviate the nonlinearity of variable-slope DTCs. The main idea is to charge or discharge the capacitive load at a constant rate and then compare the resulting constant-slope signal to a fixed threshold [13], [14]. The programmable delay is achieved by using a digital-to-analog converter (DAC) to set the initial voltage across the load capacitor according to the desired delay. Another variant of this approach uses a DAC to change the threshold voltage at which the constant slope signal is sliced instead of setting an initial charge on the load. In addition to the constant-slope method, several other approaches were reported to improve DTC linearity. For instance, in [15], both edges of the feedback clock were used to reduce the required DTC range by half, while background nonlinearity calibration techniques were explored in [9]. Other methods include adding redundancy in the DTC and randomizing the INL errors to make them appear as white noise [16]. In Section III, we propose circuit-level techniques and a simple nonlinearity calibration to improve the DTC linearity and resolution significantly.

III. Proposed Architecture

The block diagram of the proposed fractional-N synthesizer [4] is shown in Fig. 2. It is composed of a frequency doubler (FD), a PFD, a TDC, a proportional-integral (PI) loop filter, a digitally-controlled RO (DCRO), a sigma-delta ($\Sigma\Delta$) FDIV, and a DTC. An XOR-based FD doubles the input clock (CLKIN) frequency and generates the reference clock (REF) used in the synthesizer. Jitter caused by the duty-cycle error in the input clock is suppressed using a digital correction scheme that operates in the background. At startup, the PLL feedback loop is closed using the

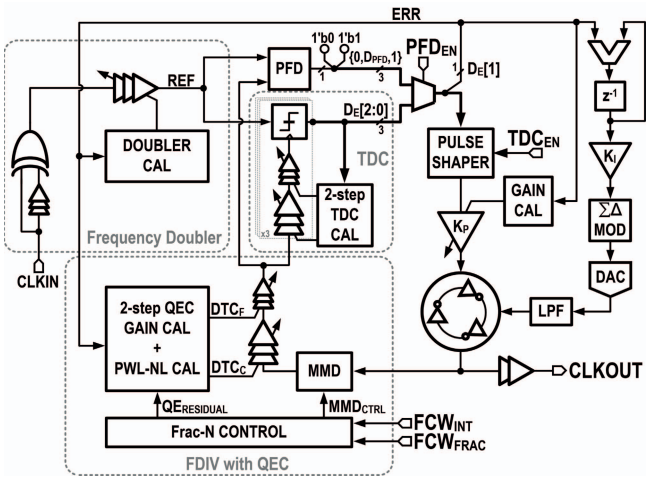


Fig. 2. Block diagram of the proposed fractional-N frequency synthesizer.

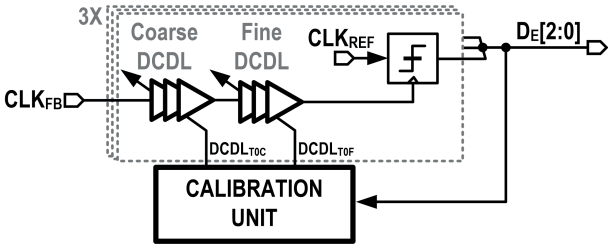


Fig. 3. TDC schematic.

PFD output and the DCRO is frequency-locked to the reference clock. After the initial frequency-locking phase, the four-level TDC output ($D_E[2:0]$) is used, instead of the PFD output, as the phase error signal within the feedback loop. Calibrated digitally-controlled delay lines (DCDLs) are used to set the TDC thresholds such that TDC resolution is maximized. The proportional control portion of the PI loop filter is implemented by directly controlling the DCRO frequency with the TDC output, and the gain (K_P) is calibrated such that the bandwidth is kept at its optimum across PVT where the BW is maximized and limit-cycles are minimized simultaneously. In the integral control path, the sign of the phase error (given by $D_E[1]$ and also denoted as ERR) is accumulated, scaled by the integral-path gain (K_I), and used to tune the DCRO frequency with the aid of a sigma-delta DAC. The DCRO output is fed to a multi-modulus divider (MMD) controlled by a $\Sigma\Delta$ modulator to implement fractional division ratio. The phase quantization error ($QE_{RESIDUAL}$) introduced by the FDIV is canceled using a high-resolution DTC placed at the output of the MMD. Next, we describe the details of the key building blocks of the synthesizer, starting with the TDC.

A. Time-to-Digital Converter (TDC)

A simplified block diagram of the TDC is shown in Fig. 3. It is based on the optimum-threshold TDC reported in [6]. The TDC consists of three parallel segments, wherein each segment detects the sign of the phase difference between the reference clock (CLK_{REF}) and appropriately delayed feedback clock (CLK_{FB}). The delay is implemented using a cascade of coarse and fine DCDLs. In other words, dedicated DCDLs set

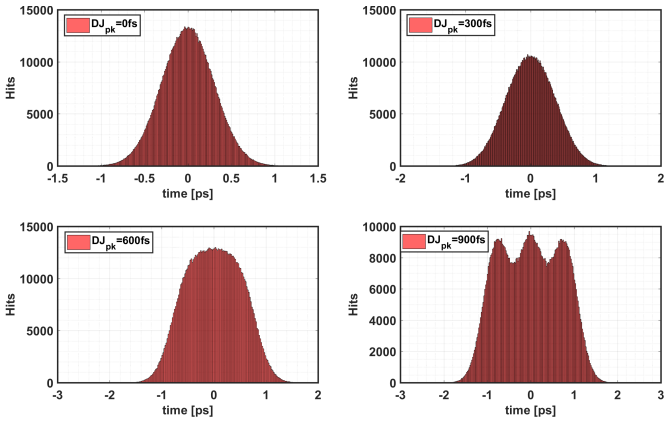


Fig. 4. Histograms from statistical simulation results (1M run) with a random noise ($\sigma = 300$ fs) in addition to a sinusoidal signal with different amplitude.

the timing threshold in each of the TDC segments. Assuming the timing error at the TDC input is Gaussian-distributed (standard deviation $= \sigma_{ERR}$), the impact of TDC quantization error is minimized in the mean-square sense when the timing thresholds are placed at σ_{ERR}, 0, and $-\sigma_{ERR}$ [6]. While it may be reasonable to assume timing error at TDC input in an integer-N PLL has Gaussian distribution, it is unclear whether the same assumption would be valid in a fractional-N PLL.

The phase error at the input of the TDC in the fractional-N case has a deterministic phase error component coming from the quantization error of the FDIV in addition to the random noise component. In fractional-N PLLs employing DTC-based QEC such as the one reported in this article, the magnitude of the deterministic phase error component depends on DTC linearity and resolution. Typically, the residual phase quantization error appears as spurs at the fractional offset frequency and its harmonics. To understand the impact of such deterministic phase error on the TDC behavior, we simulated TDC's response when its input phase error has both the Gaussian-distributed random noise and sinusoidal jitter components of varying magnitudes (see Fig. 4). The TDC's transfer characteristic is not significantly impacted as long as the amplitude of the sinusoidal jitter component is small (less than 600 fs), as shown in Fig. 5. This transfer function applies to the bang-bang phase detector as well, where only the gain of the phase detector is reduced when adding a sinusoidal jitter. Note that the residual phase quantization error is high-pass filtered before it appears at the TDC output. So, when the fractional frequency offset is small (less than the synthesizer bandwidth), it gets attenuated and has minimal impact on the TDC's calibration. On the other hand, if the fractional frequency offset is large (greater than the synthesizer bandwidth), the error is not filtered and, therefore, can have a detrimental impact on the TDC, as discussed above. So, we implemented the DTC used to cancel the FDIV's phase quantization error with high resolution and linearity such that phase error at the TDC's input is guaranteed to be significantly smaller than 600 fs under all fractional frequency offset conditions. Thus, ensuring the optimal thresholds of the TDC remain at σ_{ERR}, 0, and $-\sigma_{ERR}$ even in the fractional-N mode.

The DCDL used to set the optimum timing thresholds must have an adequate range to cover the input jitter and mismatch between the three segments of the TDC. To ensure both wide

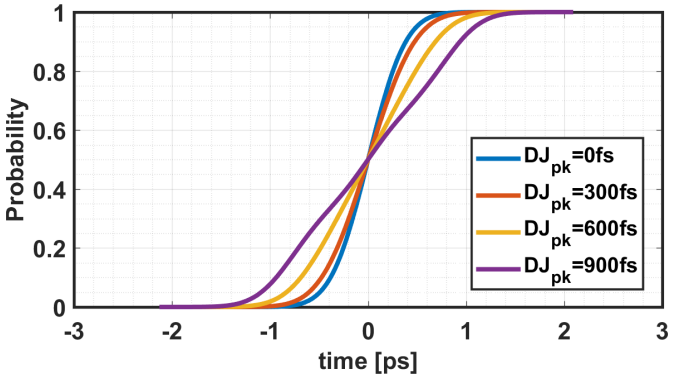


Fig. 5. Cumulative distribution function (CDF) output from statistical simulation results (1M run) with a random noise ($\sigma = 300$ fs) in addition to a sinusoidal signal with different amplitude.

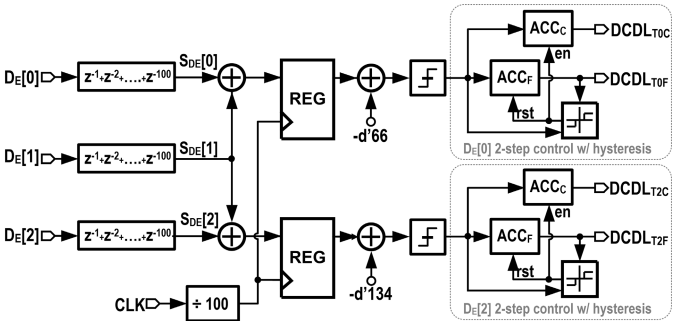


Fig. 6. TDC threshold calibration scheme.

range and high resolution, the DCDL is implemented using a cascade of coarse ($DCDL_C$) and fine ($DCDL_F$) DCDLs. The input control words of the DCDLs in the middle segment, which detects the sign of the input phase error, are set at mid-code (half the full-scale). Using the middle segment as the reference, the DCDLs in the adjacent segments are calibrated to remove the offsets and set the optimum thresholds using the calibration algorithm shown in Fig. 6.

First, the three TDC outputs, $D_E[0]$, $D_E[1]$, and $D_E[2]$, are accumulated over 100 reference clock cycles resulting in outputs $S_{DE}[0]$, $S_{DE}[1]$, and $S_{DE}[2]$, respectively. Then, the sum of $S_{DE}[0]$ and $S_{DE}[1]$ is compared with a digital code of d'66, and the accumulator ACC_C accumulates the resulting output. The output of ACC_C is used to control coarse DCDL, $DCDL_C$. When a change in the sign of the digital comparator's output is detected, the contents of ACC_C are frozen, and the accumulator ACC_F starts accumulating the comparator output. In steady state, assuming phase error at the input of the TDC is Gaussian-distributed, the DCDLs in the zeroth-segment of the TDC will have a delay σ_{ERR} higher than the total delay of the DCDLs in the first segment. Similarly, by comparing the sum of $S_{DE}[2]$ and $S_{DE}[1]$ to the digital code d'134, the DCDLs in the second segment of the TDC are set to provide a delay σ_{ERR} lower than the total delay of the DCDLs in the first segment. As a result, thresholds used in the three segments are forced to be equally separated by σ_{ERR}, a condition proved to be near optimum in [6]. The coarse control is adjusted in foreground at the beginning of the calibration and is kept fixed during normal operation, while the fine control is continuously adjusted in the background to correct any errors induced by

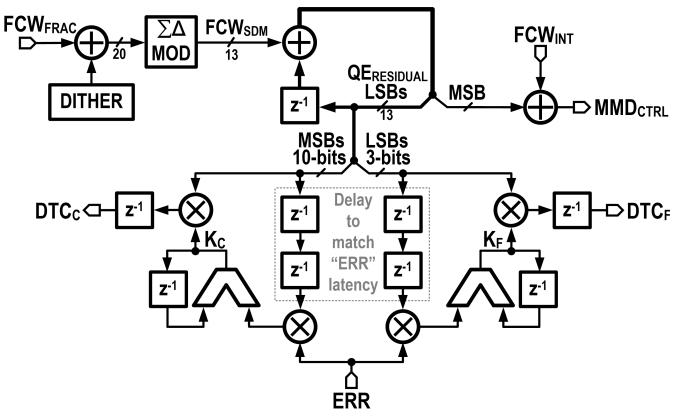


Fig. 7. Fractional frequency control and DTC calibration using the LMS algorithm.

temperature variation. A hysteresis controller is used to switch between the coarse and fine controls.

B. Fractional Division Control

The fractional division control and the signals needed for QEC are generated using the schematic depicted in Fig. 7. The 20-bit fractional frequency control word (FCW_{FRAC}) is truncated to 13-bits (FCW_{SDM}) using a second-order sigma-delta modulator. The 13-bit FCW_{SDM} is accumulated using a 14-bit accumulator, and the most significant bit (MSB) of the resulting output is added to the integer frequency control word (FCW_{INT}) to generate the MMD division control signal MMD_{CTRL}. The remaining 13 least significant bits (LSBs) of the accumulator output ($QE_{RESIDUAL}$) are used for QEC. Put differently, the accumulator can be viewed as a first-order sigma-delta modulator that quantizes 13-bit FCW_{SDM} to 1-bit, and the rest of the output ($QE_{RESIDUAL}$) represents the accumulated quantization error. Out of the $QE_{RESIDUAL}$'s 13-bits, the ten MSBs and three LSBs are scaled by K_C and K_F and used to control coarse and fine DTCs, respectively. K_C /K_F represent the gain correction factors for the coarse/fine DTCs, respectively. They are separately estimated using a least mean square (LMS) algorithm. Coarse calibration of the DTC range is done in the foreground by tuning the DTC supply, and background calibration is used to match its range to one period of the output frequency. The calibration of fine DTC is necessary to avoid INL errors due to mismatch between the coarse/fine steps.

The block diagram of the proposed DTC is shown in Fig. 8. It consists of a cascade of a 10-bit coarse DTC and a 7-bit fine DTC. The coarse DTC, whose range is calibrated to be one DCRO period, is used to cancel the phase quantization error introduced in the FDIV. On the other hand, the fine DTC is used to cancel the residual phase quantization error present at the output of the coarse DTC. The coarse DTC is composed of eight identical delay stages, wherein each delay stage is implemented using a CMOS inverter loaded by a binary-weighted 7-bit capacitor array. Realizing the delay in multiple stages results in superior linearity because it significantly reduces the second-order nonlinearity present in DTCs implemented using a single delay stage [12]. Linearity is further improved by switching the load capacitance in one stage fully before switching on the load capacitors in the next

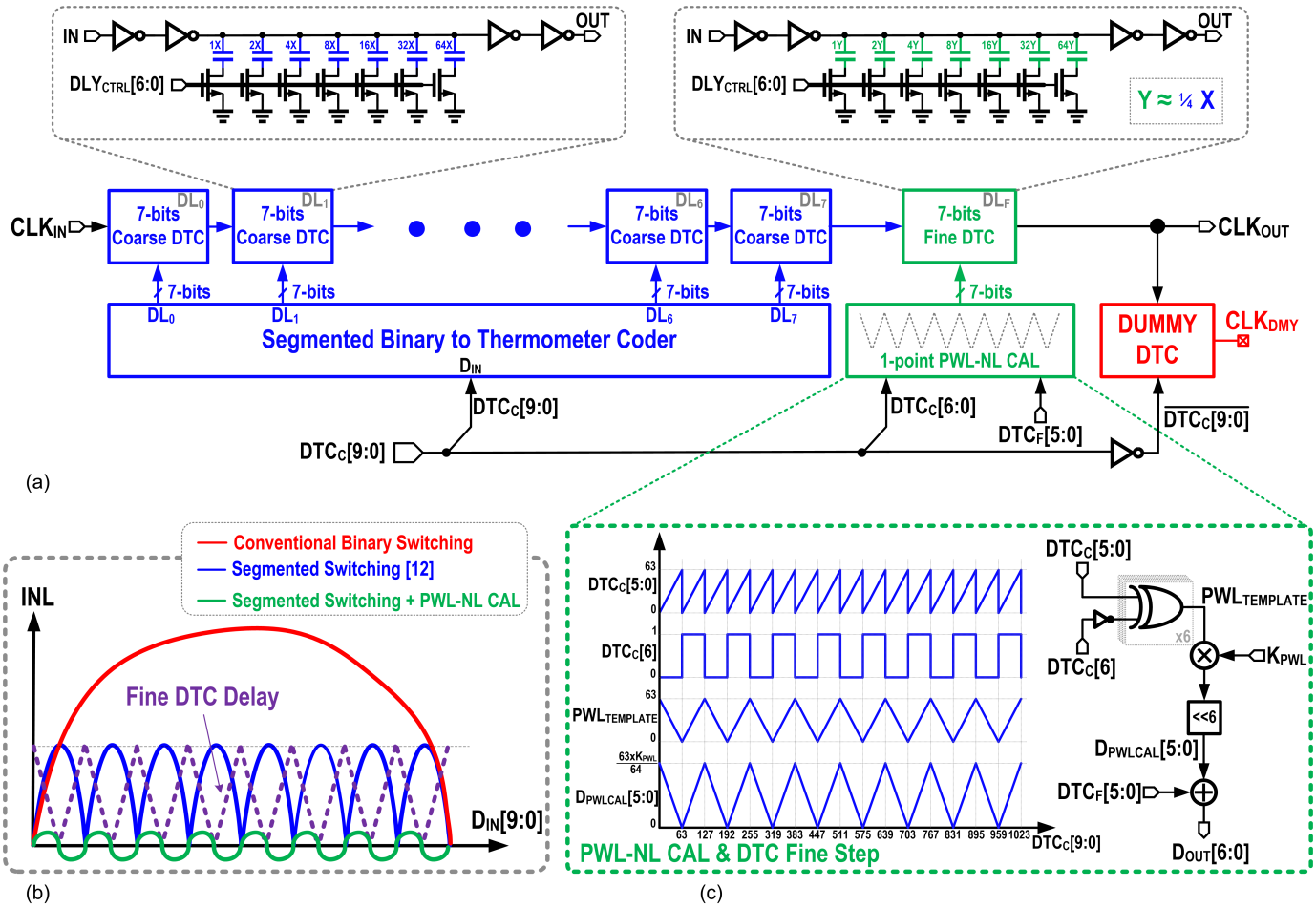


Fig. 8. Proposed DTC and one-point piecewise linear nonlinearity correction. (a) QEC DTC with segmented switching and PWL-NL correction. (b) Illustration of the INL using different switching schemes. (c) Waveform and block diagram of PWL-NL calibration.

stage [12]. In other words, this scheme reduces the DTC's systematic nonlinearity to that of one delay stage by preventing the accumulation of the nonlinear [see Fig. 8(b)]. By limiting the maximum change in delay to 1-LSB, this approach also avoids missing codes from occurring.

The fine DTC was added at the output of the coarse DTC to improve the overall DTC resolution. The fine DTC has an identical structure to that of the coarse DTC stages but uses smaller unit capacitors. This allows good delay tracking between the two DTCs across PVT. Even though fine DTC helps improve the resolution significantly, it turns out the nonlinearity of the coarse DTC still limits the overall performance. To address this limitation, we reuse the fine DTC to cancel the systematic nonlinearity of the coarse DTC. To this end, we first note that the main source of systematic nonlinearity is the dependence of the inverter's delay on the signal-dependent slope of its input (i.e., the previous stage inverter's output). Consequently, as illustrated in Fig. 8(b), the second-order nonlinearity of each stage in the coarse DTC appears as a repeated pattern in the coarse DTC's overall transfer characteristic (shown in blue). By re-using the fine stage DTC, we can approximate the reasonably well-behaved nonlinearity using a piecewise linear (PWL) function (shown in purple). This results in the cancellation of the second-order nonlinearity and only higher order nonlinearities remain as shown in green.

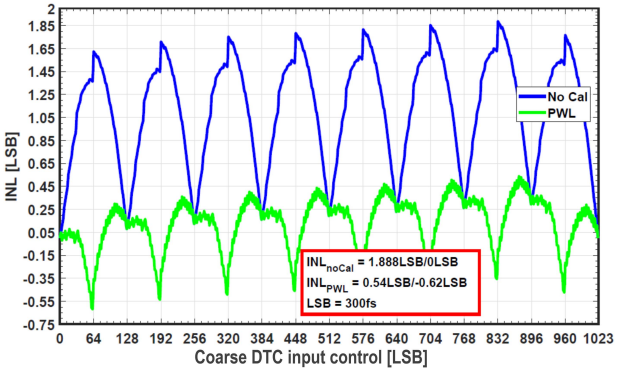


Fig. 9. Simulation results showing the impact of PWL-based nonlinearity correction on DTC's INL.

As shown in Fig. 8(c), the 7 LSBs of DTC_C ($\text{DTC}_C[6:0]$) are used to generate a PWL output ($\text{PWL}_{\text{TEMPLATE}}$) using simple XOR digital logic. The $\text{PWL}_{\text{TEMPLATE}}$ is then scaled by K_{PWL} to match coarse DTC's nonlinearity. K_{PWL} is determined at startup using a foreground calibration step. The output of the nonlinearity cancellation block (D_{OUT}) is added to DTC_F.

The transistor-level DTC was simulated, and its INL is plotted in Fig. 9. The proposed PWL-based nonlinearity correction improved INL by almost three times (from 1.85 to 0.62 LSBs).

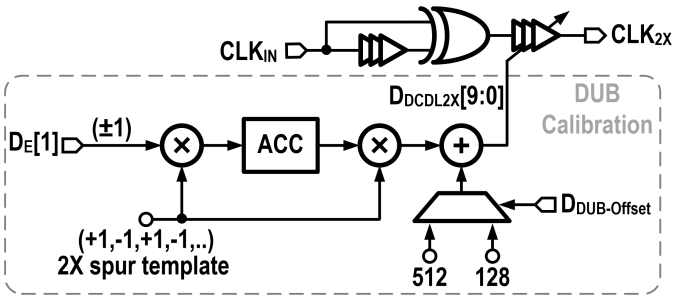


Fig. 10. Calibrated frequency doubler.

It should be noted that PWL-based nonlinearity correction improves the INL error across the whole repeating pattern, so the whole rms value is enhanced not just the peak error. It is clear from the figure that the INL pattern repeats eight times over the full-scale of the DTC, which means that the fractional spur will appear at 8× the fractional offset frequency. We note that having the INL correction in the DCDL circuit reduces the fractional spur level regardless of its absolute frequency. While the proposed PWL-NL calibration makes use of the segmented architecture to mimic the INL shape, the algorithm can be generalized for any DTC architecture and can be improved by adding multiple PWL sections and/or increasing the order of the template.

C. Frequency Doubler (FD)

Fig. 10 shows the block diagram of the FD. It consists of a simple XOR-based FD followed by 10-bit DCDL ($DCDL_{2X}$). The XOR-based FD doubles the input clock (CLKIN) frequency and generates the reference clock (REF) used in the synthesizer. A higher REF clock frequency allows extending the PLL BW, which helps suppress the RO phase noise, the dominant noise contributor in an RO-based PLL. A large bandwidth for the PLL makes the jitter performance sensitive to the noise from the reference path (i.e., reference clock source, reference clock buffer, DTC, and FD), so great attention is needed to maintain low jitter in the reference clocking path. It should be noted that the reference clock source and reference clock receiver are shared between different lanes in a SerDes module, so their power is amortized. The XOR-based implementation allows a small impact on the jitter performance from the DCDL, where the range of duty cycle correction is traded off with the amount of added jitter. The primary source of jitter in this architecture is the input clock's duty cycle error, which manifests as period error that alternates between two values ($\pm\Delta T$). Since the period error is deterministic, it can be canceled using a DCDL at the output of the FD [17]. For this cancellation technique to be effective, $DCDL_{2X}$'s gain must be precisely known under all PVT conditions, which is not possible in practice. So, an LMS loop that continuously runs in the background is used to estimate the gain of $DCDL_{2X}$. It uses the known error pattern and the TDC output (ERR) as the error signal and adjusts the gain of $DCDL_{2X}$ such that the period jitter of FD's output is minimized. In the prototype, $DCDL_{2X}$ is designed to have a range of 300 ps to compensate about 3% duty-cycle error in the input clock. At startup, the $DCDL_{2X}$ input control word is initialized to its mid-code (512 for 10-bit unsigned input), which translates to a significant offset delay.

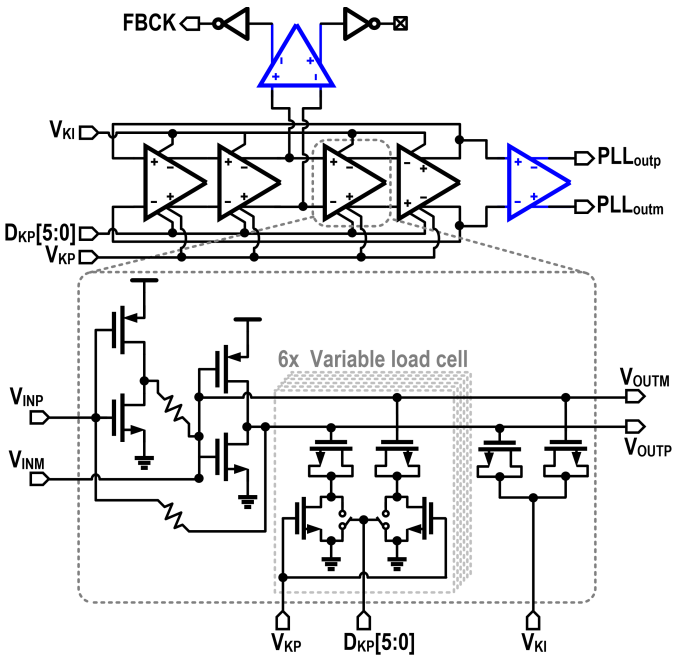


Fig. 11. Block diagram of the pseudo-differential digitally controlled RO (DCRO).

Such a large offset delay, while needed for correcting a large duty-cycle error, can add significant additive jitter even when the duty-cycle error is small. We reduce the jitter penalty under low duty-cycle error scenarios by initializing the $DCDL_{2X}$ to have a smaller offset delay by setting the initial code to be 128 instead of 512.

IV. System and Circuit Implementation Details

A. Digitally Controlled Ring Oscillator (DCRO)

The schematic of the DCRO is depicted in Fig. 11. It comprises four pseudo-differential delay stages and two differential buffers that symmetrically load the DCRO. One of the buffers' output is used as the PLL output, while the other buffer's output is fed to the MMD. Each delay stage is implemented using two CMOS inverters that are coupled by feed-forward resistors. Frequency tuning is performed with varactors placed at the output of inverters. One of the varactors is controlled by the integral-path control voltage (V_{KI}) generated by the $\Sigma-\Delta$ DAC. The TDC switches turn on/off the other varactors through a MOS resistor to implement the proportional control. The MOS resistor is biased by voltage V_{KP} based on the desired proportional-path gain similar to [6]. V_{KP} is generated by using $\Sigma-\Delta$ DAC. Thanks to the pseudo-differential operation, DCRO's supply ripple is minimized, which prevented the need for huge decoupling capacitors. An essential consideration in the DCRO design is the sizing of coupling resistors. While coupling resistors are needed to ensure differential operation [18], they also play a crucial role during the startup of the oscillator [19]. To understand this, consider the delay stage under common-mode excitation [see Fig. 12(a)], a situation that may arise during oscillator startup. Under this condition, the two CMOS inverters and the coupling resistors in each delay stage can be simplified to an inverter with resistor feedback, as illustrated in Fig. 12(b), and

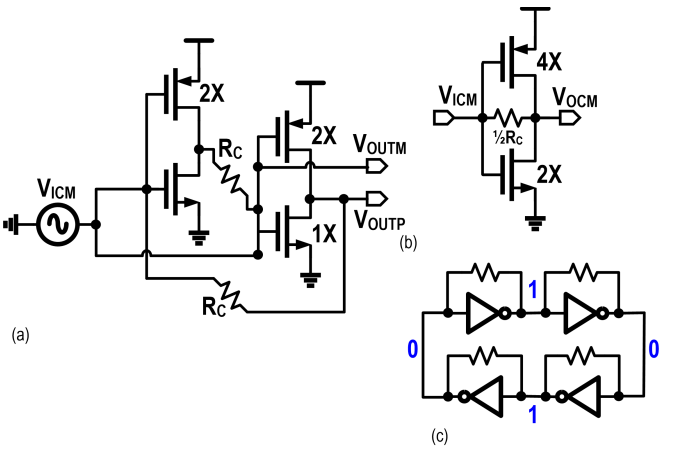


Fig. 12. Illustration of the impact of common-mode excitation on DCRO. (a) Pseudo-differential inverter cell under CM excitation. (b) Equivalent circuit under CM excitation. (c) DCRO under CM excitation.

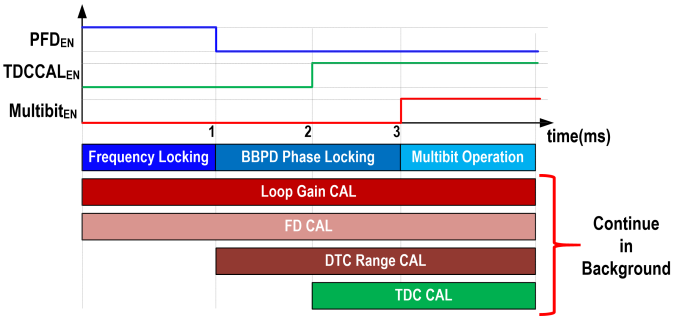


Fig. 13. PLL startup sequence.

the DCRO can be re-drawn as shown in Fig. 12(c). Because the common-mode gain of the delay stages is proportional to the coupling resistor, a smaller coupling resistor is desirable for preventing the oscillator from getting stuck in an undesirable state [see Fig. 12(c)]. However, a small coupling resistor would load the previous delay stage and increases power consumption. Because of this tradeoff, coupling resistance needs to be optimized to guarantee robust startup across PVT without burning excessive power [18], [19].

B. PLL Startup

It is critical to prevent interaction between different calibration loops during the startup and steady state. To this end, the three-step startup sequence depicted in Fig. 13 is used. For simplicity, the switching between the three main modes of operation is performed manually. In the first mode, denoted as the frequency-locking mode, a PFD is used to lock DCRO to CK_{REF}. PFD provides a nearly unlimited pull-in range and avoids locking issues associated with using a narrow-range TDC. After frequency-locking is achieved, the PLL is switched to the phase-locking mode in which TDC's sign bit (DE[1]) is used to drive the PLL toward phase lock, akin to a bang-bang PLL. Digital calibration of the FD, TDC thresholds, and DTC range are performed in the background during this phase. After the calibration loops converge, the synthesizer enters mission mode, in which all the four levels of the TDC are used. Although switching between the modes is performed manually in the prototype, automatic switching can be easily

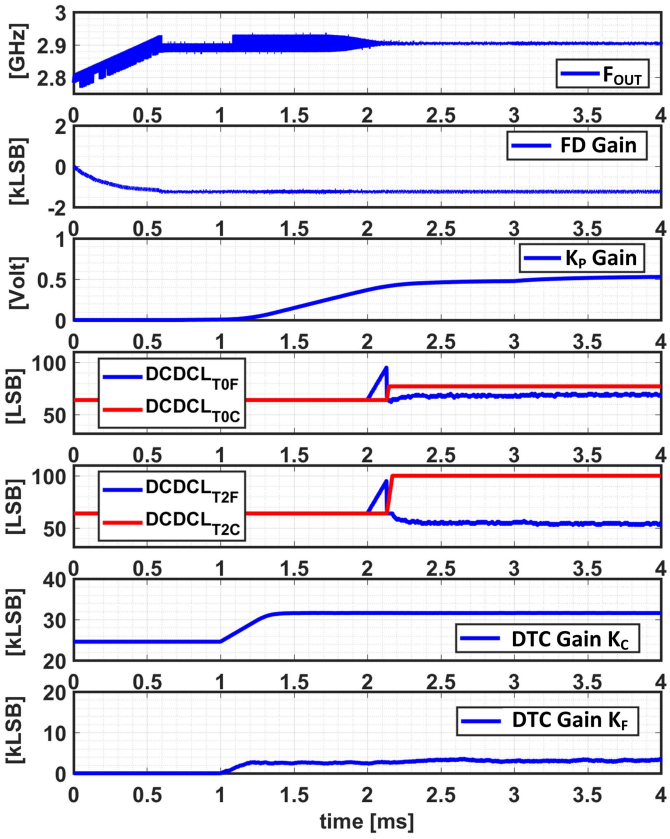


Fig. 14. Simulated convergence of the PLL calibration loops at startup.

implemented using either lock detectors or timers. It can be noted that the TDC thresholds are correctly calibrated in the second mode, while the proportional gain reaches its final value in the third mode of operation. The proportional gain calibration re-settles in the last step to compensate the gain difference between the BBPD and the multibit TDC.

Fig. 14 shows the simulated PLL behavior during startup, which shows the convergence of all the calibration loops. During the first phase (0–1 ms), the PLL achieves frequency lock quickly using PFD. The FD calibration also settles to the optimum periodic jitter (PJ) correction gain. In the second phase (1–2 ms), the PLL uses BBPD to achieve phase locking. In this phase, the DTC range calibration loops (fine and coarse) are enabled and they converge within 2 ms. The TDC calibration is enabled after BBPD achieves lock, and the offsets in the thresholds are corrected. Note how the fine DCDL tries to achieve lock and once it passes the hysteresis range (systematic offset is added in this simulation), the controller switches to the coarse calibration and automatically switches back to the fine DCDL once coarse-lock is achieved. In the final stage of operation (after 3 ms), the multi-bit TDC operation is enabled, and the PLL gain calibration converges to a new gain that is optimized for the multi-bit operation.

V. Experimental Results

A prototype synthesizer was implemented in a 65-nm CMOS technology, and its die micrograph is shown in Fig. 15. It occupies an active area of 0.134 mm^2 and consumes 11.7 mW from 1-V supply at 3.2-GHz output frequency. The synthesizer performance is characterized using

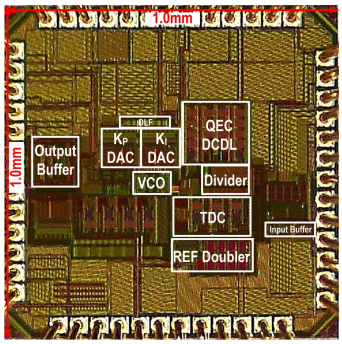


Fig. 15. Die photo of the prototype synthesizer.

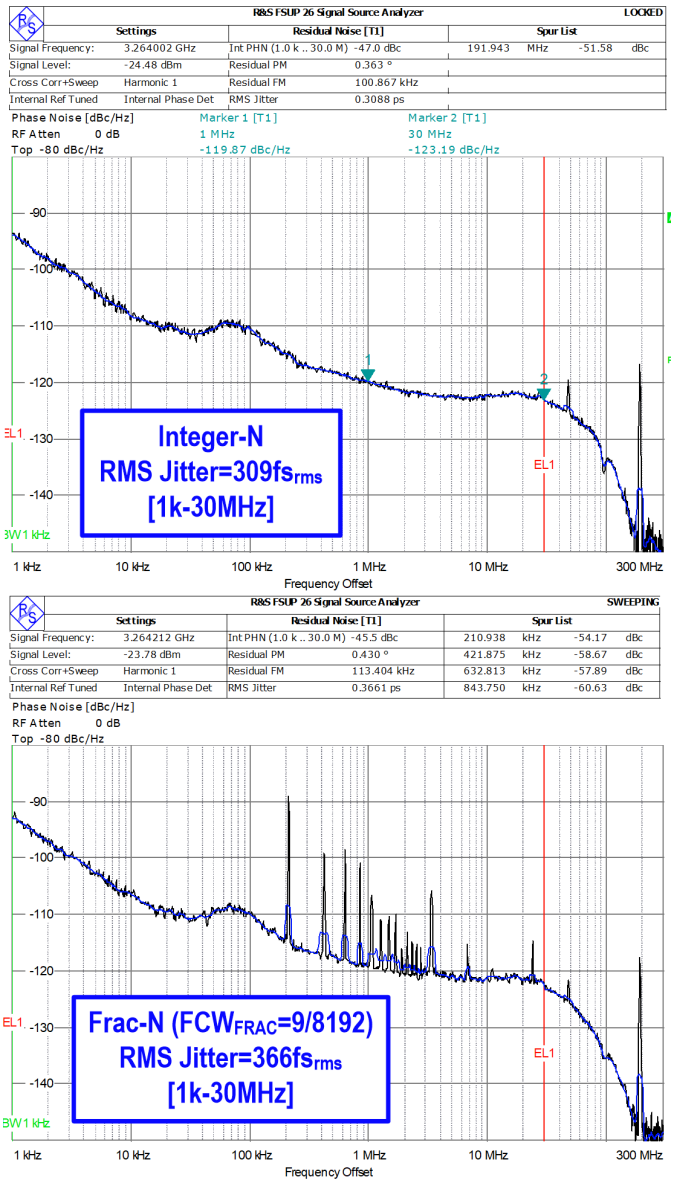


Fig. 16. Measured phase noise plots of the frequency synthesizer in two modes: (a) integer-N (top) and (b) fractional-N with $FCW_{FRAC} = 9/8192$ (bottom).

a 96-MHz external input clock generated by the Si5347 evaluation board. The measured output phase noise plot when the synthesizer is operated in the integer-N mode is shown

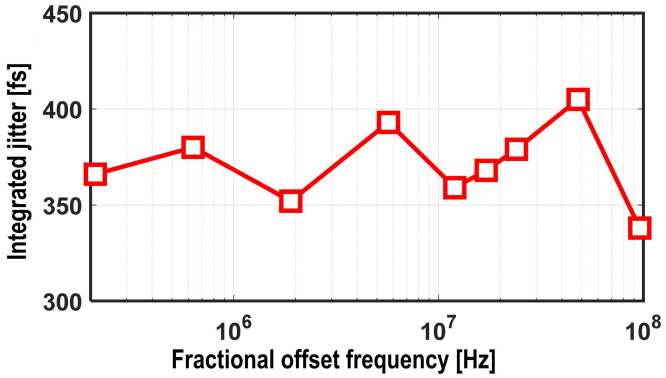


Fig. 17. Measured integrated jitter at different fractional output frequencies.

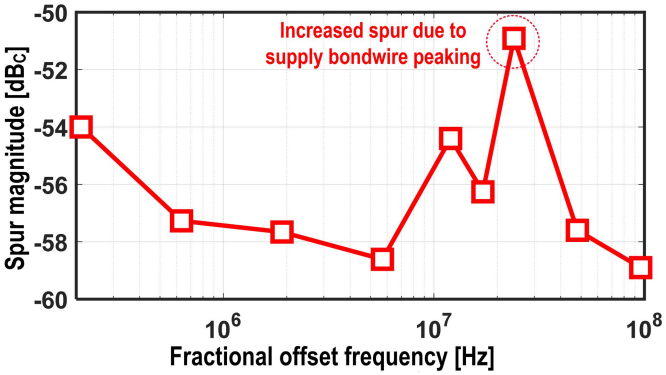


Fig. 18. Measured spur level at different fractional output frequencies.

in Fig. 16(a). The spot phase noise at 1 MHz offset frequency is −120 dBc/Hz and the integrated jitter (1 kHz to 30 MHz) is 309 fs. In the fractional-N mode, when the synthesizer is operated at a near-integer division ratio ($FCW_{FRAC} = 9/8192$), the integrated jitter (1 kHz to 30 MHz) increases to 367 fs [see Fig. 16(b)]. The worst-case in-band fractional spur is −54 dBc. Comparing the jitter performance in integer-N and fractional-N modes shows the total jitter is increased by 55 fs in the fractional-N mode at near-integer fractional frequencies. The increase in jitter is attributed to several factors such as supply/substrate coupling, DTC nonlinearity, and $\Sigma\Delta$ quantization noise. Note that this jitter is added as bounded PJ, which makes it less severe compared to the random jitter (RJ) as it contributes less to the eye closure.

Figs. 17 and 18 show the integrated jitter and spur magnitude as a function of FCW_{FRAC}, respectively.

The maximum integrated jitter and spur are 405 fs and −51 dBc, respectively, which we believe are caused by resonance in the power supply network and folding of a high-frequency spur to around 30 MHz. The QFN package used for the prototype has long bondwire which adds large inductance and cause the peaking in supply network. It should be noted that for actual SerDes application, ball grid array package is typically used which reduces the inductance by an order of magnitude to about 100 pH which should improve the impedance peaking and out-of-band spur.

Fig. 19 shows the performance difference of the synthesizer using (a) BB mode versus (b) the multibit optimum

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART FRACTIONAL-N PLLS

	ISSCC'18 L. Bertulessi [20]	JSSC'16 A. Elkholy [7]	ISSCC'17 L. Kong [21]	RFIC'18 J. Gong [22]	CICC'18 B. Liu [23]	JSSC'19 A. Santiccioli [15]	ISSCC'20 T. Seong [16]	This Work
Technology [nm]	65	65	45	40	65	65	65	65
Architecture	LC DPLL DTC	Ring DPLL DTC	Ring SLF PLL FIR Filter	Ring IL-PLL	Ring IL-PLL	Ring MDLL Range-reduced DTC	Ring DPLL DTC randomization	Ring DPLL 2-step DTC + PWL-NL
Reference Freq. [MHz]	52	50	22.6	64	100	100	100	96
Output Freq. [GHz]	3.85	5	2.416	2.431	1.2	1.65	5.5	3.264
Tuning range [GHz]	3.7-4.1	2.0-5.5	2.31-3.05	1.8-2.7	0.6-1.7	1.6-3.0	4.5-6.0	3.0-3.5
Multiplication factor [N]	74	100	107	38	12	16.5	55	34
Equivalent full integration BW† [MHz]	20.5	19.6	8.87	25.5	41.6	40.8	39.5	38.3
Integrated jitter [fs] (Integration Range)	183 (1kHz - 30MHz)	1900 (1kHz - 20MHz)	1500 (10kHz - 50MHz)	1600 (10k - 10MHz)	1200 (10k - 10MHz)	397 (30k - 30MHz)	648 (1kHz - 30MHz)	405 (1kHz - 30MHz)
In-Band Frac Spur [dBc] (Offset freq)	-50 (500kHz)	-41.6 (200kHz)	-41 (0.3kHz)	-45.8 (16kHz)	-58.8 (1.0725MHz)	-51.5 (1.96MHz)	-58 (3.1kHz)	-54 (211kHz)
Power [mW]	5.28	4	10	1.33	2.5	2.5	9.88	11.7
Area [mm^2]	0.61	0.084	0.096	0.13	0.12	0.0275	0.108	0.134
$\text{FoM}_{\text{JIT}}^{\dagger\dagger}$ [dB]	-247.5	-228.4	-226.5	-234.7	-234.4	-244.0	-234.0	-237.2
$\text{FoM}_{\text{JIT,N}}^{\ddagger}$ [dB]	-266.2	-248.4	-246.7	-250.5	-245.2	-256.2	-251.4	-252.5
$\text{FoM}_{\text{NORM}}^{\ddagger\ddagger}$ [dB]	-245.4	-227.8	-225.1	-228.5	-226.2	-240.1	-230.2	-233.4

† $f_{BW} = f_{REF} \times \frac{\sqrt{1.5}}{\pi} \frac{N}{\sqrt{(N-1)(N-0.5)}}$ †† $\text{FoM}_{\text{JIT}} = 10\log\left(\sigma_{\text{rms}}^2 \times P_{\text{mW}}\right)$ ‡ $\text{FoM}_{\text{JIT,N}} = 10\log\left(\frac{\sigma_{\text{rms}}^2 \times P_{\text{mW}}}{N}\right)$ ‡‡ $\text{FoM}_{\text{NORM}} = \text{FoM}_{\text{JIT}} - 10\log\left(\frac{2}{\pi}\tan^{-1}\left(\frac{f_{\text{mean}}}{f_{BW}}\right)\right)$

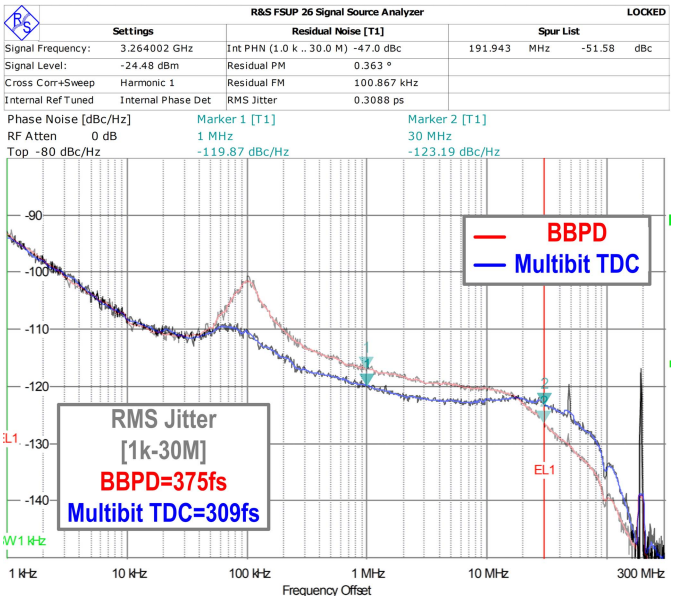


Fig. 19. Measured phase noise of the frequency synthesizer in two modes: (a) BB mode (in red) and (b) Multibit mode (in blue).

threshold TDC. The multibit operation reduces the overall jitter by 66 fs, an excellent improvement for a minor power penalty. Note that the mid-frequency phase noise is improved by 3 dB. Also, the PLL BW got extended as the K_P gain calibration pushes the operation to a higher BW benefiting from the reduced quantization noise.

The effectiveness of the PWL-based nonlinearity correction of the DTC is evaluated by measuring the synthesizer output spectrum with and without the correction scheme. As illustrated by the spectra shown in Fig. 20, the proposed scheme reduces the DTC-nonlinearity induced spur by 13.5 dB. Note that the fractional spur caused by DTC's nonlinearity appears at $8F_{\text{OFFSET}}$ due to 8-stage segmentation in the coarse DTC. The measured reference spur at 192 MHz offset frequency is -52 dBc (see Fig. 21). No noticeable spur was observed at 96 MHz, which indicates the effectiveness of the duty-cycle calibration loop. Fig. 22 shows the breakdown of the power consumed in the frequency synthesizer. The DCO consumes nearly two-thirds of the power as it is the most significant source of jitter in the synthesizer. It is worth mentioning that

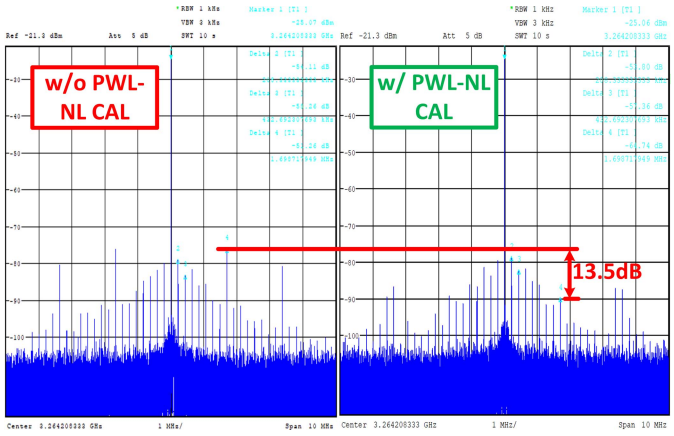


Fig. 20. Measured output spectrum ($\text{FCW}_{\text{FRAC}} = 9/8192$) with PWL correction OFF (left graph) and ON (right graph).

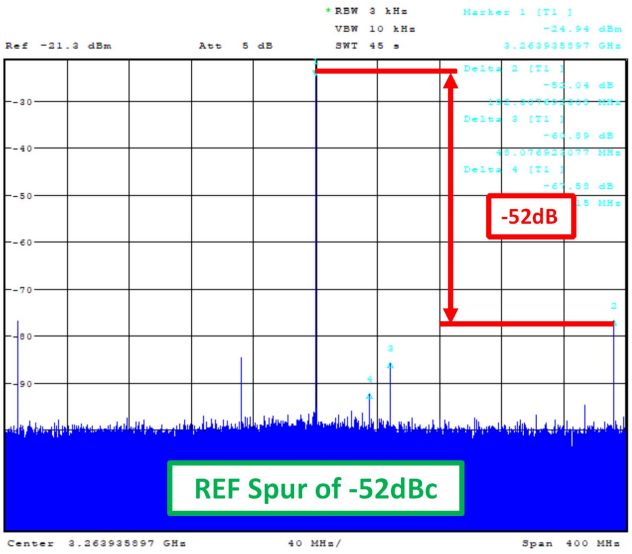


Fig. 21. Measured spectrum of the output clock of the frequency synthesizer in integer-N mode.

the digital calibration power is only 5% of the total power, which shows the efficiency of using digital calibration without adding a significant power penalty.

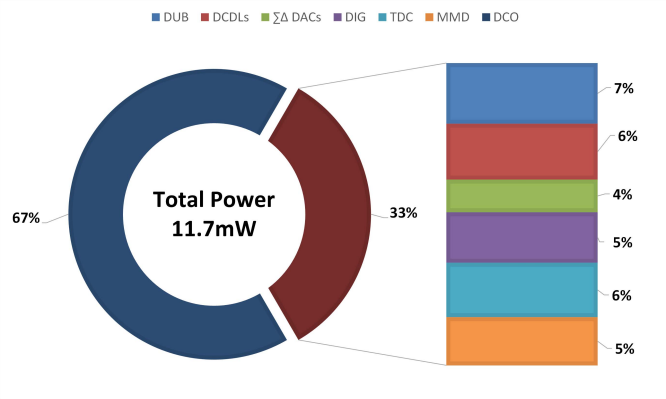


Fig. 22. Breakdown of the synthesizer power consumption.

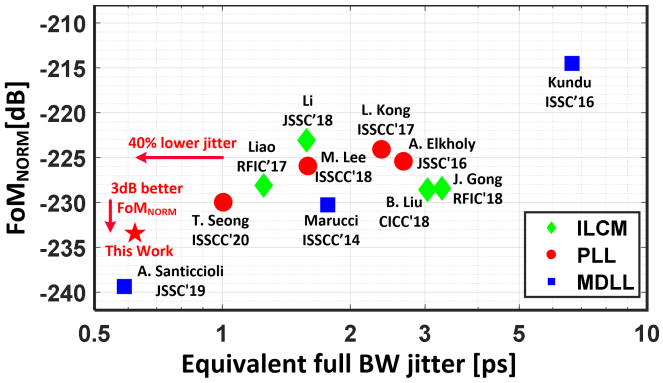


Fig. 23. Normalized FoM of state-of-the-art fractional synthesizers.

The detailed performance summary of the prototype synthesizer and its comparison with the state-of-the-art digital frequency synthesizers are shown in Table I. The proposed synthesizer achieves the lowest jitter (lower by 40%) while achieving the best figure-of-merit (3 dB better) over the state-of-the-art RO-based fractional-N DPLLs. As shown in Fig. 23, the proposed architecture achieves a significant improvement in FoM_{NORM} [15] compared to state-of-the-art synthesizers.

VI. Conclusion

Digital RO-based fractional-N frequency synthesizers have many attractive features, such as generating multiple phases, reduced susceptibility to EM coupling, and smaller area. However, they suffer from poor phase noise compared to their LC counterparts. In this article, we presented several techniques to improve their performance further. These include implementing a highly linear high-resolution DTC, a TDC with reduced quantization error, and a digitally calibrated reference FD. The proposed techniques help increase the loop bandwidth to suppress RO phase noise and power efficiently achieve low jitter. The prototype shows that using digital calibration for analog blocks can help efficiently optimize performance especially for highly scaled technology nodes. The prototype RO-based synthesizer, fabricated in a 65-nm CMOS process, achieves a worst-case integrated jitter of 405 fs_{rms} with an excellent jitter figure-of-merit (FoM_{JIT}) of −237.2 dB. This demonstrates that digital RO-based fractional-N frequency synthesizers can be employed in high-performance SerDes applications.

Acknowledgment

The authors would like to thank Berkeley Design Automation for providing the AFS simulator.

References

[1] A. Elkholy, S. Saxena, G. Shu, A. Elshazly, and P. K. Hanumolu, "Low-jitter multi-output all-digital clock generator using DTC-based open loop fractional dividers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1806–1817, Jun. 2018.

[2] G. Shu *et al.*, "A 4-to-10.5 Gb/s continuous-rate digital clock and data recovery with automatic frequency acquisition," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 428–439, Feb. 2016.

[3] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

[4] A. Elmallah, J. Zhu, A. Khashaba, K. Megawer, A. Elkholy, and P. Hanumolu, "A 3.2 GHz 405 fs_{rms} jitter −237.2 dB-FoM_{JIT} ring-based fractional-N synthesizer using two-step quantization noise cancellation and piecewise-linear nonlinearity correction," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2021, pp. 1–2.

[5] D. Turker *et al.*, "A 7.4-to-14 GHz PLL with 54 fs_{rms} Jitter in 16 nm FinFET for integrated RF-data-converter SoCs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 378–380.

[6] T. Seong, Y. Lee, S. Yoo, and J. Choi, "A 320-fs RMS jitter and −75-dBc reference-spur ring-DCO-based digital PLL using an optimal-threshold TDC," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2501–2512, Sep. 2019.

[7] A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly, and P. K. Hanumolu, "A 2.0–5.5 GHz wide bandwidth ring-based digital fractional-N PLL with extended range multi-modulus divider," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1771–1784, Aug. 2016.

[8] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, Apr. 2015.

[9] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.

[10] C.-M. Hsu, M. Straayer, and M. Perrott, "A low-noise, wide-BW 3.6 GHz digital fractional frequency synthesizer with a noise shaping time-to-digital converter and quantization noise cancellation," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 340–341.

[11] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs_{rms} integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[12] A. Elmallah, M. G. Ahmed, A. Elkholy, W.-S. Choi, and P. K. Hanumolu, "A 1.6 ps peak-INL 5.3 ns range two-step digital-to-time converter in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[13] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, Jun. 2015.

[14] H. Liu *et al.*, "A 0.98 mW fractional-*N* ADPLL using 10b isolated constant-slope DTC with FOM of −246 dB for IoT applications in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 246–248.

[15] A. Santiccioli, M. Mercandelli, A. L. Lacaita, C. Samori, and S. Levantino, "A 1.6-to-3.0-GHz fractional-N MDLL with a digital-to-time converter range-reduction technique achieving 397-fs jitter at 2.5-mW power," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3149–3160, Oct. 2019.

[16] T. Seong *et al.*, "A −5 8dBc-worst-fractional-spur and −234 dB-FoMjitter, 5.5 GHz ring-DCO-based fractional-N DPLL using a time-invariant-probability modulator, generating a nonlinearity-robust DTC-control word," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 270–272.

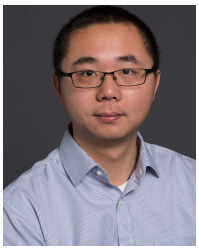
[17] A. Elkholy, D. Coombs, R. K. Nandwana, A. Elmallah, and P. K. Hanumolu, "A 2.5–5.75-GHz ring-based injection-locked clock multiplier with background-calibrated reference frequency doubler," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2049–2058, Jul. 2019.

[18] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec. 2012.
[19] J. Parker, D. Weinlader, and J. Sonntag, "A 15 mW 3.125 GHz PLL for serial backplane transceivers in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2005, pp. 412–607.
[20] L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori, and S. Levantino, "A low-phase-noise digital bang-bang PLL with fast lock over a wide lock range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 252–254.
[21] L. Kong and B. Razavi, "A 2.4 GHz RF fractional-N synthesizer with 0.25 f_{REF} BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 330–331.
[22] J. Gong *et al.*, "A 1.33 mW, 1.6 ps_{rms}-integrated-jitter, 1.8–2.7 GHz ring-oscillator-based fractional-N injection-locked DPLL for Internet-of-Things applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 44–47.
[23] B. Liu *et al.*, "A 1.2 ps-jitter fully-synthesizable fully-calibrated fractional-N injection-locked PLL using true arbitrary nonlinearity calibration technique," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

Ahmed Elmallah (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2006 and 2014, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2020.

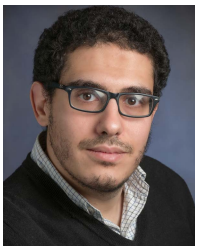
From 2006 to 2014, he was a Staff Engineer with Si-Ware Systems, Cairo, where he worked on designing high-performance circuits and systems for interfacing MEMS inertial sensors. In 2018, he was with Verily Life Sciences, San Francisco, CA, USA, where he developed high dynamic range front-end for neural modulation interface. He also joined Facebook Reality Labs, Redmond, WA, USA, where he developed system-level models for inertial sensors, benchmarking simulator for visual inertial odometry (VIO) application as well as a closed-loop VIO SLAM algorithm for power-consumption optimized SLAM camera. He is currently working with the SerDes Team at Mediatek, Irvine, CA, where he is developing timing solutions for high-speed serial links.

Dr. Elmallah was a recipient of the Analog Devices Outstanding Student Designer Award in 2016. He serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the IEEE International Symposium on Circuits and Systems (ISCAS), and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.



Junheng Zhu (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2014, 2016, and 2019, respectively.

He worked with the RF/mixed-signal circuit groups at Huawei Technologies, Rolling Meadows, IL, USA, Qualcomm Inc., San Diego, CA, USA, and Finisar, Urbana-Champaign, IL, USA in the Summer of 2015, 2017, and 2018, respectively. He is currently a Senior Engineer at Qualcomm Inc.



Amr Khashaba (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2012 and 2016, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2016.

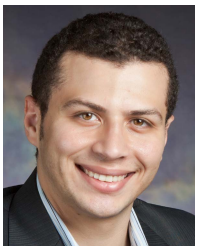
From 2012 to 2016, he was a Design Engineer with Si-Ware Systems, Cairo, where he worked on designing high-performance mixed signal circuits and sensor interfaces. He was with Silicon Labs, Nashua, NH, USA, and Samsung, San Jose, CA, USA, during the summers of 2017 and 2019, respectively. In 2020, he joined Mediatek, Irvine, CA, where he is currently working on high-speed wireline systems. His research interests include high-performance clock generation, temperature-compensated oscillators, sensor interfaces, and wireline systems.

Dr. Khashaba serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.

Karim M. Megawer (Member, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees in electronics and communications engineering from Cairo University, Cairo, Egypt, in 2013 and 2016, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2020.

From 2014 to 2016, he was an Analog/RF Design Engineer at Silicon Vision, Cairo, Egypt, designing ADCs, crystal oscillators, DCDC converters, and LNAs. In 2017, he was with Xilinx, San Jose, CA, USA, working on high-performance fractional-N frequency synthesizers. From June 2018 to December 2018 and May 2019 to July 2019, he was with Qualcomm, San Diego, CA, developing low-power low-jitter reference clock generators. He is currently with Apple, San Diego. His research interests include developing techniques for frequency multiplying and fast startup crystal oscillators for low-jitter high-performance clock multipliers.

Dr. Megawer received the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award in 2020, the Analog Devices Outstanding Student Designer Award in 2019, the M. E. Van Valkenburg Graduate Research Award from the University of Illinois at Urbana–Champaign in 2019, and the IEEE SSCS Student Travel Grant Award in 2018. He serves as a Reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, and TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.



Ahmed Elkholy (Member, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2008 and 2012, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2016.

From 2008 to 2012, he was with Si-Ware Systems, Cairo, designing high-performance clocking circuits. In 2016, he was with Silicon Labs, Austin, TX, USA. In 2017, he was a Post-Doctoral Research Associate with the University of Illinois at Urbana–Champaign. From 2017 to 2019, he was a Co-Founder of PhaseBits, Inc., Champaign, IL, developing high-performance timing solutions. He is currently a Senior Staff Scientist with Broadcom, Irvine, CA, USA, developing high-speed transceivers for optical and backplane/cable applications. His current research interests include frequency synthesizers, high-speed serial links, and data converters.

Pavan Kumar Hanumolu (Fellow, IEEE) received the Ph.D. degree from the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA, in 2006.

He subsequently served as a Faculty Member at Oregon State University until 2013. He is currently a Professor with the Department of Electrical and Computer Engineering and a Research Professor with the Coordinated Science Laboratory, University of Illinois at Urbana–Champaign, Urbana, IL, USA. His current research interests include energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.

Dr. Hanumolu is the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.