A Charge-Sharing Locking Technique With a General Phase Noise Theory of Injection Locking

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***Abstract*— This article presents a millimeter-wave (mmW) frequency synthesizer based on a new charge-sharing locking (CSL) technique. A charge-preset capacitor is introduced for charge sharing with a resonant *LC*-tank for phase correction, while the resulting charge residue on the sharing capacitor is processed by a digital frequency-tracking loop (FTL) against the process, voltage, and temperature (PVT) variations. Furthermore, a general phase noise (PN) theory of CSL, with injection locking (IL) being a special case, is proposed based on a unified multirate z-domain model, supporting any frequency division ratio N and CSL (or IL) strength β. The new theory sheds light not only on all IL-like PN phenomena (chiefly, its "loop" bandwidth being up to half of the reference frequency, and the oscillator PN increasing 3 dB beyond the "loop" cutoff frequency) but also on how to choose the CSL bandwidth via the sharing capacitor in order to optimize the rms jitter performance. The prototype in 28-nm CMOS achieves 77-fs rms jitter in 21.75—26.25 GHz while consuming 16.5 mW for mmW quadrature frequency generation.**

***Index Terms*— 5G communication, charge-sharing locking (CSL), frequency-tracking loop (FTL), injection locking (IL), millimeter-wave (mmW), quadrature frequency generation.**

I. Introduction

THE emerging 5G/6G and other high-speed communication standards (e.g., WIFI-6/7) pose very tough phase noise (PN) and rms jitter requirements on phase-locked loops (PLLs) [1], [2]. To support 256 QAM in the 28-/39-GHz millimeter-wave (mmW) bands [1] and 1024 QAM in the sub-6-GHz bands, error-vector magnitude (EVM) contributed by the PLL's PN should be as low as 1.4% and 0.4%, respectively. This accounts for around 16% of the total EVM's budget (i.e., $\text{EVM}_{\text{PLL}}^2/\text{EVM}^2$ in Fig. 1), while the other main contributors come from the transmitter's non-idealities (i.e., nonlinearity, LO leakage, I/Q imbalance, and so on). Consequently, the required rms value of absolute jitter, J_{rms}, can be derived as

$$J_{\text{rms}} = \frac{\sqrt{2 \times 10^{\text{IPN}_{\text{dBc}}/10}}}{2\pi f_0} < \frac{\sqrt{10^{\text{EVM}_{\text{dB}}/10}}}{2\pi f_0} = \frac{\text{EVM}}{2\pi f_0} \quad (1)$$

where f_0 is the carrier frequency and IPN_{dBc} is the integrated PN. As revealed in Fig. 1, the rms jitter for a 5G PLL (in both sub-6 GHz and mmW) must be below 100 fs.

There are two technical routes toward achieving the sub-100-fs rms jitter: 1) various sampling techniques [3]–[10] relying on a high phase detector (PD) gain (e.g., sub-sampling

Modulation Scheme for 5G PDSCH ($\text{EVM}^2 = \text{EVM}_{\text{PLL}}^2 + \text{EVM}_{\text{TX}}^2$)

QAM	64	256	1024
Required EVM	8%	3.5%	1% (est.)
EVM by PLL	3.2%	1.4%	0.4%
EVM by TX	7.33%	3.2%	0.91%

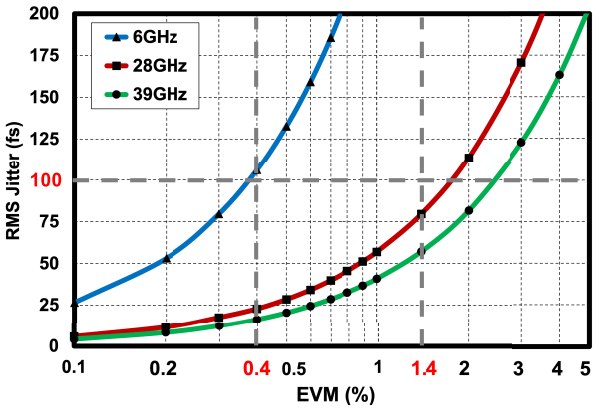

Fig. 1. EVM and rms absolute jitter requirements for 5G communications [1]. EVM_{PLL} and EVM_{TX} are the respective EVM contributions from the PLL and transmitter.

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[3]–[7] by exploiting sharp edges of the oscillator's sinusoidal waveform,[1] sampling an RC waveform at the reference rate [8], and a bang-bang operation [10]) to increase the loop bandwidth and suppress the oscillator's PN while using a reference of high-frequency and low PN [10]; and 2) injection locking (IL), including phase realigning techniques [13]–[21] based on the oscillator's instantaneous phase correction (with virtually no loop delay). The intrinsic PN mechanisms in the above two techniques are entirely different: the former tunes the oscillator's frequency (e.g., via the LC-tank capacitance), while the latter changes the instantaneous phase (e.g., changing the charge in an LC-tank).

The main challenges of the sampling-based PLLs with high PD gain stem from the consequent limited phase detection range, requiring an additional frequency-locked loop (FLL) to enhance their process, voltage, and temperature (PVT) robustness [3]. A careful design of an isolating buffer between the sampler and oscillator is also necessary to reduce the reference spurs [6]. On the other hand, the circuitry for IL itself is usually quite simple, whereas much more effort must be focused on its frequency-tracking loop (FTL) to maintain the oscillator's free-running frequency *close* to $N\times$ reference frequency against PVT variations [14]–[17]. There exists a significant danger of a timing-race problem between the injection of reference events and FTL since the phase error may be corrected by the IL *before* the FTL can sense its corresponding frequency error. The early high-speed time-to-digital converter (TDC)-based [14] or VCO-replica-based FTLs [15] consume huge power and area. A gated-pulse technique was applied in [16] and [19] in which some reference cycles are exclusively devoted for IL, while others stop the IL altogether and exclusively use the FTL. Unfortunately, this requires a relatively complex timing control based on several digitally controlled delay lines (DCDLs). Yoo *et al.* [17] and Kim *et al.* [20] proposed a low-power phase-sampling-based FTL with an assumption that, in a quadrature VCO (Q-VCO), the phase of Q-VCO's Q-component could record the frequency deviation with the normal injection into its in-phase (I)-component (exploiting a natural delay for the I-component's injection affecting its Q-component). A similar idea was extended to a differential VCO in [22]. Irrespective of the choice of analog FTL (or FLL), the analog loop filter usually occupies a large area [6], [7], [17], resulting in high costs in advanced CMOS. Another challenge in IL oscillators (ILOs, including phase-realigned oscillators) is how to control the "loop" bandwidth in order to reduce the effect of the reference PN on the optimized rms jitter. Failing to address this, the output jitter in ILOs might not be any better than the reference jitter [16], [23].

Surprisingly, a general PN theory in IL is still missing [24]–[26]. The conventional s- or z-domain (at reference rate) analyzing techniques [16], [19], [26], [27] model ILOs in the same manner as in the conventional type-I PLLs with a single integrating pole [28], but they fail to predict the ILO's special PN phenomena, such as the extremely strong suppressing ability of the oscillator's PN and the PN folding effect resulting in the ILO's PN being 3 dB higher outside of the "loop" bandwidth than when the oscillator is free-running [22], [23], [29]–[31]. Combining a discrete-time model with a continuous-time zero-order hold (ZOH) function, Ye *et al.* [13] derived a pioneering but provisional PN model of an ILO. It exhibits quite a good agreement when the frequency ratio N is large (e.g., $N > 10$) and the realigning factor (i.e., injection strength[2]) β is small (e.g., $\beta < 0.2$), but it cannot predict the PN folding. Gierkink's [29] and Maffezzoni and Levantino's [30] continuous-time PN models (for $N > 10$) consider the ILO's cyclostationary nature and are accurate for any β, but they do not consider the reference PN itself. A multirate discrete-time model [36], [37] (for any N) applied in [31] accounts for the ILO's PN contribution from the reference, oscillator, and oscillator's PN folding but is only limited to the ideal IL (i.e., $\beta = 1$, similar as in [23]).

To be able to optimize the "loop" bandwidth in the IL with an additional benefit of ultralow-power and low-cost FTL, we propose a charge-sharing locking (CSL) manner of frequency synthesis [38]. In addition, we introduce a complete PN theory of CSL (covering the IL), exploiting a unified multirate timestamp model for any β and N with consideration of all noise sources (including the PN folding), which is also useful for optimizing the CSL's rms jitter. The rest of this article is organized as follows. Section II presents the basic operating principles of the CSL, while a general PN theory of CSL is laid out in Section III. Section IV discusses the design and analysis of the inherent FTL. Circuit implementation of key building blocks is presented in Section V, followed by experimental results in Section VI.

II. Basic Concept of Charge-Sharing Locking

A. Basic Operation

Fig. 2(a) shows the basic concept of CSL. At the heart lies the LC-tank oscillator generating a (near) sinusoidal waveform $V_{\rm osc}(t)$ of frequency $f_{\rm osc} = 1/2\pi\sqrt{LC_{\rm osc}}$. During the high level of reference clock *ref* (of frequency $f_{\rm ref}$), the digital logic (DIG) driving the DAC presets $V_{\rm share}$ on the sharing capacitor $C_{\rm share}$ (via switch S_1) to the expected oscillator waveform voltage at the significant reference instances [defined as *ref*'s falling edges in Fig. 2(a)]. Afterward, a narrow pulse *clk_csl* shortly connects $C_{\rm share}$ to $C_{\rm osc}$ (i.e., S_1 OFF, S_2 ON) for the actual CSL operation.

Without any loss of generality but for ease of explanation, an integer-N mode is introduced first in which $V_{\rm share}$ is conveniently set at the zero-crossing level (including dc offset) of $V_{\rm osc}$[3] [see Fig. 2(b)]. Assuming a perfect lock, if the oscillator's free-running frequency $f_{\rm osc}$ *suddenly* gets a little lower than $N\times$ the reference frequency (i.e., $Nf_{\rm ref}$), then, at the following reference event, the sharing charge

[1]The PD gain from the reference's sinusoidal waveform is roughly $N\times$ lower than the oscillator's, limiting the jitter performance in [11] and [12].

[2]It can be calculated analytically by the slope of "phase domain response (PDR)" [27], including the methods of "impulse sensitivity function (ISF)" [25], [26], "perturbation projection vector (PPV)" [32], [33] (i.e., a more rigorous version of ISF, considering the phase shift of ISF itself when perturbation happens [34], which enables the ISF to predict some IL phenomena [35]), and others [16], [27].

[3]For a fractional-N operation, the DAC would set an aliased [4] version of the sinusoidal waveform of $V_{\rm osc}$.

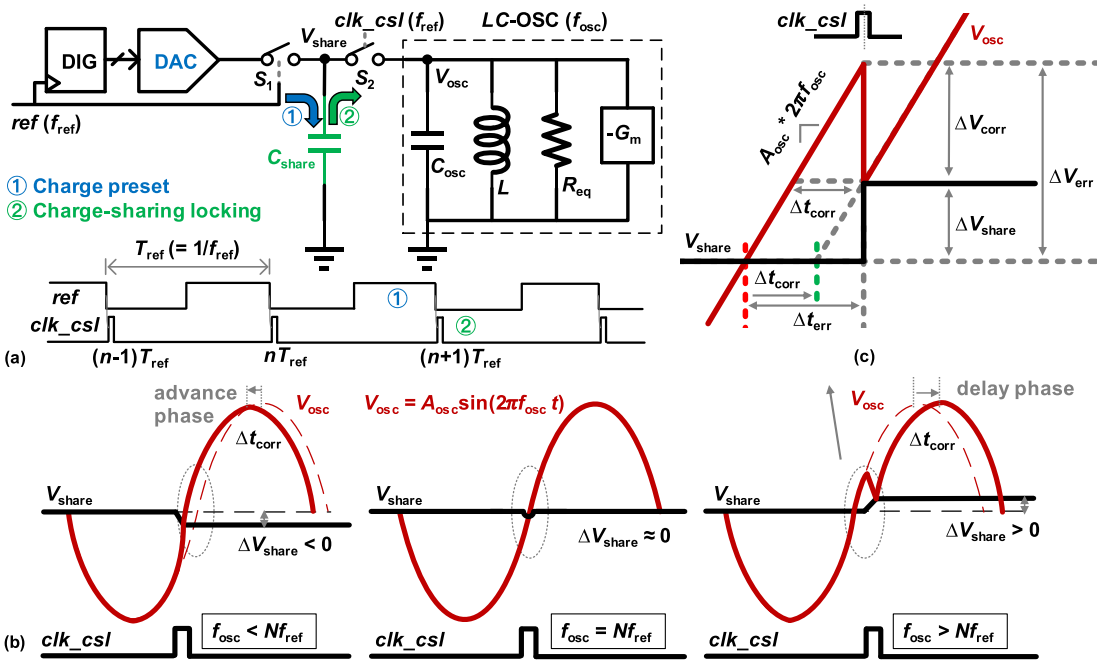


Fig. 2. (a) Basic concept of CSL and its timing diagram. (b) Impact on waveforms of $V_{share}(t)$ and $V_{osc}(t)$ due to the CSL events at zero-crossings for three conditions of the $f_{osc}-Nf_{ref}$ relationship. (c) Idealized zoomed-in view of $V_{share}(t)$ and $V_{osc}(t)$.

that was preset on C_{share} will increase V_{osc}, while lowering its own V_{share} a bit, thus leaving a negative-charge excess (henceforth, termed residue) ΔV_{share}. The sudden increment in V_{osc} *instantaneously* advances the phase of the digitally controlled oscillator (DCO), substantially correcting the phase error caused by the frequency error (as well as PN, if any). In the opposite case, if $f_{osc} > N \times f_{ref}$, the sharing charge delays the phase of the DCO, leaving a positive change ΔV_{share}. If $f_{osc} = N \times f_{ref}$, the sharing charge is only used to correct the (zero-mean) PN, causing $\Delta V_{share} \approx 0$.

B. Charge-Sharing Locking Strength β

With the help of Fig. 2(b) and (c), we can quantitatively study the CSL mechanism from the timestamp domain[4] and voltage (charge) domain.

1) Zero-Crossing Timestamp Domain Behavior: Let us formally define f_{ref} and f_{osc} as *average* frequencies of the incoming reference clock and *free-running* oscillator, respectively. Assuming a small frequency offset (deviation) between the oscillator's free-running frequency and $N\times$ reference's (i.e., $\Delta f_{dev} = f_{osc} - Nf_{ref} \neq 0$), but neglecting for now their own the intrinsic PN, the oscillator could change its *average* frequency to Nf_{ref} under some locking conditions. Among them, the CSL's fundamental locking condition in the zero-crossing timestamp (briefly termed as "timestamp") domain can be straightforwardly derived as (see Fig. 3)

$$T_{ref} = NT_{osc} + \Delta t_{corr} \tag{2}$$

[4]The timestamp domain is mathematically related to the phase domain via a normalizing factor of the sampling rate, but the latter (referencing the sampling rate itself) unfortunately cannot readily handle the multirate signals.

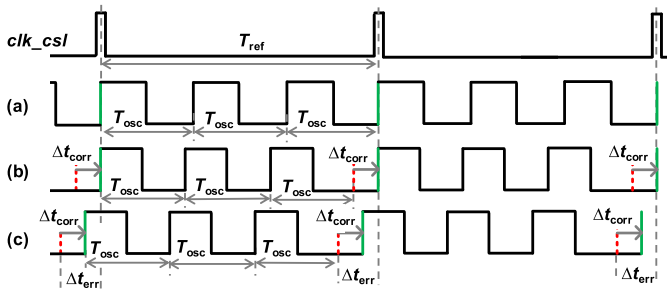


Fig. 3. Rectangularized steady-state $V_{osc}(t)$ to emphasize their zero-crossing timestamps under a charge-sharing lock, assuming (a) $T_{ref} = NT_{osc}$ & $\beta > 0$, (b) $T_{ref} = NT_{osc} + \Delta t_{corr}$ & $\beta = 1$ (i.e., $\Delta t_{corr} = \Delta t_{err}$), and (c) $T_{ref} = NT_{osc} + \Delta t_{corr}$ & $\beta < 1$. Conditions: $N = 3$ and neglecting PN.

where Δt_{corr} is the extent of timestamp correction, while $T_{ref} = 1/f_{ref}$ and $T_{osc} = 1/f_{osc}$. In other words, the oscillator's timestamp deviation caused by its frequency offset must be corrected at *each* reference cycle.

2) Voltage (Charge) Domain Behavior: Fig. 2(c) shows the relationship between the timestamp and voltage domains in the CSL. A CSL strength factor, β, is defined as[5]

$$\beta \equiv \frac{\Delta t_{corr}}{\Delta t_{err}} = \frac{\Delta V_{corr}}{\Delta V_{err}} \tag{3}$$

where Δt_{err} is the "timestamp error"[6] between the actual zero-crossing of the oscillator waveform and the reference

[5]The internal CSL switch resistance (S_2 in Fig. 2) is assumed small enough so as to neglect the V_{share} and V_{osc} transition times for simplicity but with no loss of generality. If this is not satisfied, β will be somewhat smaller than $C_{share}/(C_{share} + C_{osc})$; the actual value can be ascertained from SPICE simulations.

[6]Analogous to the closely related "phase error," which is a common term in PLLs.

event (actually the midpoint of injection pulse), including a static time offset [i.e., $\Delta t_{\rm err} - \Delta t_{\rm corr}$; see Fig. 3(c)] and $\Delta t_{\rm corr}$. Accordingly, $\Delta V_{\rm err}$ is the voltage error, while $\Delta V_{\rm corr}$ is the actual voltage correction. β indicates how effective the sharing capacitor $C_{\rm share}$ is in pulling the tank capacitor $C_{\rm osc}$ to the expected zero-crossing level. Per the principle of charge sharing between the two capacitors (i.e., $C_{\rm share}$ and $C_{\rm osc}$), $\Delta V_{\rm share}$ and $\Delta V_{\rm corr}$ in Fig. 3(c) can be easily written as

$$\Delta V_{\rm share} = \frac{C_{\rm osc}}{C_{\rm share} + C_{\rm osc}} \Delta V_{\rm err} \tag{4}$$

and

$$\Delta V_{\rm corr} = \Delta V_{\rm err} - \Delta V_{\rm share} = \frac{C_{\rm share}}{C_{\rm share} + C_{\rm osc}} \Delta V_{\rm err}. \tag{5}$$

Substituting (5) into (3), β equals to

$$\beta = \frac{C_{\rm share}}{C_{\rm share} + C_{\rm osc}}. \tag{6}$$

On the other hand, assuming that $V_{\rm osc}(t) = A_{\rm osc} \sin 2\pi f_{\rm osc} t$, we get

$$\frac{\Delta V_{\rm corr}}{\Delta t_{\rm corr}} = \frac{\Delta V_{\rm err}}{\Delta t_{\rm err}} \approx \left. \frac{{\rm d}V_{\rm osc}}{{\rm d}t} \right|_{t=0} = 2\pi f_{\rm osc} A_{\rm osc} \tag{7}$$

where $A_{\rm osc}$ is the amplitude of the oscillating waveform. Under CSL [i.e., (2) is satisfied], and combining (4) and (5) and then (7) and (2), we get

$$\begin{aligned} \Delta V_{\rm share} &= (T_{\rm ref} - N T_{\rm osc}) \times 2\pi f_{\rm osc} A_{\rm osc} \times C_{\rm osc}/C_{\rm share} \\ &= N \Delta f_{\rm dev,norm} \times 2\pi A_{\rm osc} \times (1-\beta)/\beta \end{aligned} \tag{8}$$

where

$$\Delta f_{\rm dev,norm} = \frac{f_{\rm osc} - N f_{\rm ref}}{N f_{\rm ref}} \tag{9}$$

is defined as the oscillator's normalized frequency offset (deviation). Thus, the polarity and magnitude of charge residue on $C_{\rm share}$ represent the frequency error between $f_{\rm osc}$ and $N f_{\rm ref}$, which we will naturally exploit to realize an FTL in Section IV. If $C_{\rm share} \gg C_{\rm osc}$ (i.e., $\beta \to 1$), the charge reservoir based on $C_{\rm share}$ becomes a voltage source, and the CSL degenerates into conventional *perfect* IL, but $\Delta V_{\rm share}$ [≈ 0, see (4)] cannot record any frequency deviation. In contrast, if $C_{\rm share} \ll C_{\rm osc}$ [i.e., $\beta \to 0$, (2) and (8) are not necessarily satisfied], $C_{\rm share}$ has little ability to correct the oscillator's timestamp (i.e., phase) error [i.e., $\Delta V_{\rm corr} \approx 0$; see (5)], but at least it can sample the phase error [i.e., such as in sub-sampling PLLs (SS-PLLs), $\Delta V_{\rm share} \approx \Delta V_{\rm err}$; see (4)]. Thus, how to choose $C_{\rm share}$ for a given LC-tank (i.e., choice of β) is the key question in designing the CSL frequency synthesizer, which could significantly affect its phase correction ability and the FTL design.

III. Phase Noise of Charge-Sharing Locking

We now analyze the PN mechanism in CSL by including perturbations to the instantaneous periods of reference and oscillator from their own noise. For ease of analysis, we remove the frequency offset of the free-running oscillator (i.e., $T_{\rm ref} = N T_{\rm osc}$), which, in practice, could be done at startup by an additional FLL or a coarse all-digital PLL (ADPLL) while subsequently maintained by the proposed FTL (discussed later in Section IV).

A. Timestamps of Oscillator and Reference

Let us start by discussing some basics of a multirate timestamp model. As shown in Fig. 4(a), a free-running oscillator's kth timestamp (see the mid-points of the $V_{\rm osc}$ sinusoid's rising slopes in Fig. 2), $t_{\rm osc}[k]$, is modeled by [39]

$$t_{\rm osc}[k] = k T_{\rm osc} + \Delta t_{\rm osc}[k] = \sum_{m=1}^{k} (T_{\rm osc} + \Delta T_{\rm osc}[m]) \tag{10}$$

where $\Delta t_{\rm osc}[k]$ and $\Delta T_{\rm osc}[k]$ are the oscillator's instantaneous "absolute jitter" and "period jitter" (also called "cycle jitter"), respectively [40]. On the other hand, the nth reference timestamp, $t_{\rm ref}[n]$ (e.g., locations of mid-points of injection pulses *clk_csl*, triggered by falling edges of *ref* in Figs. 2 and 3), is

$$t_{\rm ref}[n] = n T_{\rm ref} + \Delta t_{\rm ref}[n] \tag{11}$$

where $\Delta t_{\rm ref}[n]$ is the reference's "instantaneous absolute jitter," normally incorporating both the intrinsic jitter and that added by its on-chip reference path.

Accordingly, we introduce two z-variables, $z_{\rm ref}$ and $z_{\rm osc}$, for the z-transforms of the above multirate discrete-time system, in which $z_{\rm ref}^{-1} = z_{\rm osc}^{-N}$ and $z_{\rm osc}^{-1} = z_{\rm ref}^{-1/N}$ signify one reference delay being equal to $N\times$ oscillator delays, while one oscillator delay is the same as $1/N$ reference delay. Specifically, substituting

$$\begin{cases} z_{\rm ref} = e^{j2\pi \Delta f / f_{\rm ref}} \\ z_{\rm osc} = e^{j2\pi \Delta f / f_{\rm osc}} \end{cases} \tag{12}$$

into the multirate z-transform, a Fourier analysis can be conducted on the PLL for PN analysis, where Δf is the frequency offset of interest.

B. Downsampling of Oscillator Timestamps

To interface a high sampling-rate (i.e., $f_{\rm osc}$) domain with a low sampling-rate (i.e., $f_{\rm ref}$) domain, a downsampling operation is required.[7] As shown in Fig. 4(a), if the timestamps $t_{\rm osc}[k]$ are downsampled by N, new timestamps of $t_{\rm osc,down}[n]$ are obtained, whose z-transform[8] is given as follows [42]:

$$\begin{aligned} &\widehat{T}_{\rm osc,down}(z_{\rm ref}) \\ &\quad = \frac{1}{N} \widehat{T}_{\rm osc}\left(z_{\rm ref}^{1/N}\right) + \frac{1}{N} \sum_{m=1}^{N-1} \widehat{T}_{\rm osc}\left(z_{\rm ref}^{1/N} e^{-j2\pi m/N}\right) \\ &\quad = \frac{1}{N} \widehat{T}_{\rm osc}(z_{\rm osc}) + \frac{1}{N} \sum_{m=1}^{N-1} \widehat{T}_{\rm osc}\left(z_{\rm osc} e^{-j2\pi m f_{\rm ref}/f_{\rm osc}}\right) \end{aligned} \tag{13}$$

where $\widehat{T}_{\rm osc}(z_{\rm osc})$ is the z-transform of $t_{\rm osc}[k]$ and $\widehat{T}_{\rm osc}(z_{\rm osc} e^{-j2\pi m f_{\rm ref}/f_{\rm osc}})$ represents the spectral replica of $\widehat{T}_{\rm osc}(z_{\rm osc})$ shifted by $m f_{\rm ref}$. The PN of $t_{\rm osc,down}[n]$ can be

[7] The downsampling operation could model the edge removal or frequency division in divider-based PLLs [41], a sub-sampling operation in divider-less PLLs (e.g., ADPLLs [28], [37] or SS-PLLs [3]), and CSL/IL. Intrinsically, there should be no fundamental difference between the divider-based PLLs or divider-less PLLs.

[8] The hat in $\widehat{T}(\cdot)$ is employed to indicate a z-transform of timestamps $t[\cdot]$, in order to better distinguish it from $T_{\rm ref}$ and $T_{\rm osc}$, which are the average periods of reference and free-running oscillator, respectively.

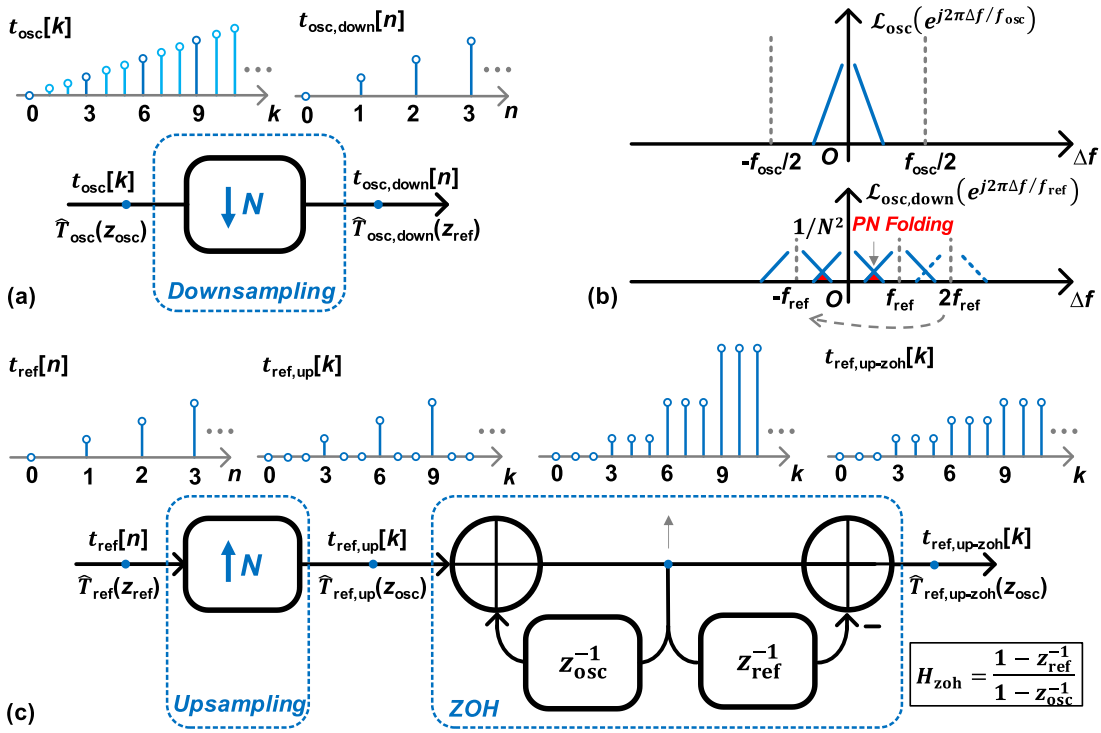


Fig. 4. (a) Downsampling of timestamps of a free-running oscillator: from $t_{\text{osc}}[k]$ to $t_{\text{osc,down}}[n]$. (b) PN spectra of $t_{\text{osc}}[k]$ and $t_{\text{osc,down}}[n]$ showing that the downsampling causes PN scaling and folding (i.e., aliasing). (c) Upsampling and zero-order hold of a reference's timestamps: from $t_{\text{ref}}[n]$ to $t_{\text{ref,up-zoh}}[k]$. Examples with $N = 3$ and all the timestamp sequences are null when $n \leq 0$ or $k \leq 0$.

calculated by taking the square of $|\widehat{T}_{\text{osc,down}}|$ and normalizing it into phase domain as[9]

$$\mathcal{L}_{\text{osc,down}}(z_{\text{ref}}) = \frac{1}{N^2}\mathcal{L}_{\text{osc}}(z_{\text{osc}}) + \frac{1}{N^2}\sum_{m=1}^{N-1}\mathcal{L}_{\text{osc}}(z_{\text{osc}}e^{-j2\pi m f_{\text{ref}}/f_{\text{osc}}}) \quad (14)$$

where $\mathcal{L}_{\text{osc}}(z_{\text{osc}})$ represents the PN of $t_{\text{osc}}[k]$ and $\mathcal{L}_{\text{osc}}(z_{\text{osc}}e^{-j2\pi m f_{\text{ref}}/f_{\text{osc}}})$ represents the replica[10] of $\mathcal{L}_{\text{osc}}(z_{\text{osc}})$ shifted by mf_{ref}, causing "PN folding" [see Fig. 4(b)]. The $1/N^2$ factor, induced by downsampling, models the PN scaling from the oscillator's to reference's phase domain.[11] On account of the sampling rate reduction from f_{osc} to f_{ref} in $\mathcal{L}_{\text{osc,down}}$, $|\Delta f|$ in its z-variables is within $f_{\text{ref}}/2$ (i.e., $|\Delta f| < f_{\text{ref}}/2$).

For oscillators of ultralow flicker PN [44]–[50], their "instantaneous period jitter," $\Delta T_{\text{osc}}[k]$, mainly induced by the thermal PN,[12] is normally distributed with zero-mean and standard deviation of $\sigma_{\Delta T,\text{osc}}$ (i.e., the rms value of $\Delta T_{\text{osc}}[k]$). $\sigma_{\Delta T,\text{osc}}$ can be calculated by solving

$$\mathcal{L}_{\text{osc}}(z_{\text{osc}}) \approx \frac{(2\pi\sigma_{\Delta T,\text{osc}}/T_{\text{osc}})^2}{f_{\text{osc}}} \cdot \left|\frac{1}{1-z_{\text{osc}}^{-1}}\right|^2 \quad (15)$$

where it is modeled by a power spectral density (PSD) of Gaussian noise passing through an accumulator and $|\Delta f| < f_{\text{osc}}/2$. For example, substituting $\mathcal{L}_{\text{osc}} = 10^{-140/10}$ rad^2/Hz (i.e., -140 dBc/Hz) at $\Delta f = 10$ MHz and $f_{\text{osc}} = 10$ GHz into (15) yields $\sigma_{\Delta T,\text{osc}} = 1$ fs.

C. Upsampling and ZOH of Reference Timestamps

An upsampling followed by "discrete-time zero-order hold (ZOH)" was proposed in [37] to bridge from the low to high sampling-rate domains. As shown in Fig. 4(c), $t_{\text{ref}}[n]$ is upsampled N times, and the resulting $t_{\text{ref,up}}[k]$ passes through the discrete-time ZOH as $t_{\text{ref,up-zoh}}[k]$. Their corresponding z-transforms are [42]

$$\begin{aligned}\widehat{T}_{\text{ref,up-zoh}}(z_{\text{osc}}) &= H_{\text{zoh}}(z_{\text{osc}}) \cdot \widehat{T}_{\text{ref,up}}(z_{\text{osc}}) \\ &= H_{\text{zoh}}(z_{\text{osc}}) \cdot \widehat{T}_{\text{ref}}(z_{\text{osc}}^N) = H_{\text{zoh}}(z_{\text{osc}}) \cdot \widehat{T}_{\text{ref}}(z_{\text{ref}})\end{aligned} \quad (16)$$

where $\widehat{T}_{\text{ref,up}}(z_{\text{osc}}) = \widehat{T}_{\text{ref}}(z_{\text{osc}}^N) = \widehat{T}_{\text{ref}}(z_{\text{ref}})$ captures the upsampling itself and

$$H_{\text{zoh}}(z_{\text{osc}}) = \frac{1-z_{\text{ref}}^{-1}}{1-z_{\text{osc}}^{-1}} = \frac{1}{N}\frac{1-z_{\text{ref}}^{-1}}{1-z_{\text{osc}}^{-1}} \cdot N \quad (17)$$

[9]The cross products of two $\widehat{T}_{\text{osc}}$ at different harmonics of f_{ref} could be practically neglected as compared to the self-squares.

[10]The replica appearing at mf_{ref} ($m \geq N/2$) could be seen mathematically as that at $m - N$; thus, the replicas cause the same influence on the upper sideband as on the lower sideband of the original PN [31], [43].

[11]This is a justification as to why the original explanation of SS-PLL's low PN mechanism highlighting "PD/CP noise not multiplied by N^2" due to the divider-less arrangement [3] is not entirely correct since the $1/N$ factor could be also added in the feedback path of the divider-less PLL for the phase domain normalization from the oscillator's to the reference's sampling rate. On the other hand, the PD/CP noise is actually in the time domain with the reference sampling rate, whose translation into the output PN has to be normalized with the oscillator sampling rate, leading to N^2, which is independent of whether the actual divider is present or not.

[12]A timestamp modeling technique for $\Delta T_{\text{osc}}[k]$ considering both thermal PN and flicker PN was described in [39] and [47].

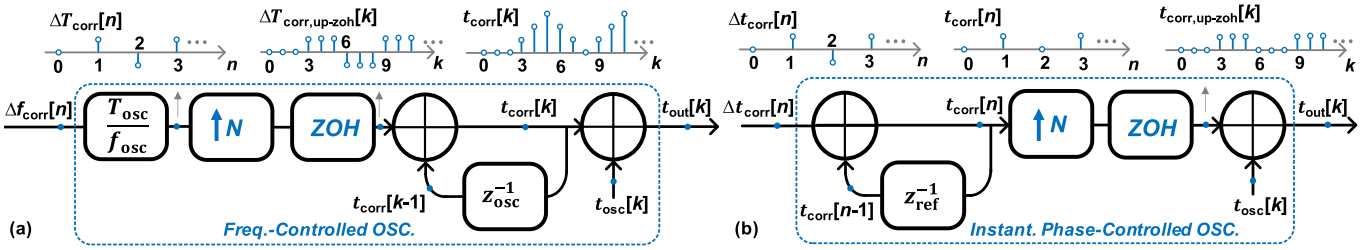


Fig. 5. Multirate timestamp models of (a) frequency-controlled oscillators (e.g., VCOs or DCOs) and (b) instantaneous phase-controlled oscillators (e.g., charge-sharing locked or IL oscillators). Examples with $N = 3$ and all the timestamp sequences are null when $n \le 0$ or $k \le 0$.

is the z-transform of discrete-time ZOH,[13] whose dc gain (i.e., $\Delta f \to 0$) is N. The PN of $t_{\text{ref,up-zoh}}[k]$ can be calculated by taking the square of $|\widehat{T}_{\text{ref,up-zoh}}|$ and normalizing it into phase domain as

$$\mathcal{L}_{\text{ref,up-zoh}}(z_{\text{osc}}) = \left|\frac{1}{N}\frac{1-z_{\text{ref}}^{-1}}{1-z_{\text{osc}}^{-1}}\right|^2 \cdot N^2 \mathcal{L}_{\text{ref}}(z_{\text{ref}}) \tag{18}$$

where $\mathcal{L}_{\text{ref}}(z_{\text{ref}})$ represents the PN of $t_{\text{ref}}[n]$. The N^2 factor, produced by upsampling and ZOH, models the PN scaling from the reference's to the oscillator's phase domain. Due to the sampling rate expansion to f_{osc} in $\mathcal{L}_{\text{ref,up-zoh}}$, its effective $|\Delta f|$ extends to $f_{\text{osc}}/2$ (i.e., $|\Delta f| < f_{\text{osc}}/2$).

Neglecting the flicker PN, the reference's instantaneous absolute jitter, $\Delta t_{\text{ref}}[n]$, is normally distributed with zero-mean and standard deviation of $\sigma_{\Delta t,\text{ref}}$ (i.e., its rms jitter and the rms value of $\Delta t_{\text{ref}}[n]$). Thus, the reference's PN could be modeled by the PSD of the Gaussian noise as

$$\mathcal{L}_{\text{ref}}(z_{\text{ref}}) \approx \frac{(2\pi\sigma_{\Delta t,\text{ref}}/T_{\text{ref}})^2}{f_{\text{ref}}} \tag{19}$$

where $|\Delta f| < f_{\text{ref}}/2$. For a reference of $f_{\text{ref}} = 200$ MHz and in-band PN $\mathcal{L}_{\text{ref}} = 10^{-160/10}$ rad^2/Hz (i.e., -160 dBc/Hz), we obtain $\sigma_{\Delta t,\text{ref}} = 112.5$ fs.

D. Frequency- and Phase-Controlled Oscillators

Fig. 5(a) and (b), respectively, shows the multirate time-stamp model for "frequency-controlled oscillators" (e.g., conventional VCOs/DCOs in PLLs) and "instantaneous phase-controlled oscillators" used in this work for CSL (or IL). In the former, its frequency correcting sample $\Delta f_{\text{corr}}[n]$ (e.g., modeling the tuning capacitance in an LC-tank in response to the detected phase error at f_{ref}) is translated to the period correcting value $\Delta T_{\text{corr}}[n]$ by the linear approximating factor $T_{\text{osc}}/f_{\text{osc}}$. After the upsampling and ZOH, it is accumulated on each oscillator cycle, resulting in the final correcting timestamp $t_{\text{corr}}[k]$ applying on the free-running oscillator timestamp $t_{\text{osc}}[k]$. By combining the multirate timestamp models of downsampling, upsampling, and ZOH, and the frequency-controlled oscillator, we can accurately predict the behavior of *wideband*, low-jitter PLLs [e.g., various (sub)sampling-based PLLs with high PD gain].

On the other hand, for the instantaneous phase-controlled oscillator's model in Fig. 5(b), the correcting timestamp adjusting the internal free-running oscillator timestamp $t_{\text{osc}}[k]$ is modeled by passing $t_{\text{corr}}[n]$ (at f_{ref} rate) through the upsampling and ZOH, to obtain $t_{\text{corr,up-zoh}}[k]$, which stays constant until the next reference cycle [i.e., no accumulation of phase at f_{osc}, as in Fig. 5(a), but adjusting it merely at f_{ref}]. $\Delta t_{\text{corr}}[n]$ represents the nth input correcting timestamp for the phase-controlled oscillator, while the reference-rate accumulator models the memory effect of the timestamp correction (i.e., phase correction). The above proposed multirate timestamp models help us to clearly distinguish between the two phase correction mechanisms, which would not be feasible in the straightforward single-rate z-domain or s-domain model.

E. Multirate Timestamp Model of CSL (or ILO)

Based on the proposed model of "instantaneous phase-controlled oscillator," a new multirate timestamp model for CSL (or ILO) is introduced in Fig. 6. It takes into account the PN of oscillator and reference while neglecting the DAC-induced kT/C noise on V_{share} due to C_{share} being large (on the order of ~pF). In the feedforward path, the timestamp error $\Delta t_{\text{err}}[n]$ is first attenuated by the CSL strength factor[14] β to obtain the input correcting timestamp $\Delta t_{\text{corr}}[n]$ for the instantaneous phase-controlled oscillator. However, a grave modeling difficulty prevents us from generating $\Delta t_{\text{err}}[n]$. Due to the nature of CSL/IL, the lack of any significant delay in the feedforward path makes it impossible to directly downsample the final $t_{\text{out}}[k]$ by N to obtain $t_{\text{out,down}}[n] = t_{\text{out}}[nN]$ for the purpose of feeding it back to compare it with $t_{\text{ref}}[n]$. Since $t_{\text{out}}[k]$ has already been corrected at $k = nN$ (i.e., $t = nT_{\text{ref}}$), doing so anyway would cause an incomputable "delay-free loop" in the discrete-time model, such as in [26].

To solve this fundamental difficulty, we propose a scheme in which the uncorrected $t_{\text{out}}[k]$ at $k = nN$ (i.e., $t_{\text{out,down,uncorr}}[n]$) is actually at $t = nT_{\text{ref}}^- = nT_{\text{ref}} - \epsilon_t$ ($\epsilon_t \ll T_{\text{osc}}$), which can be calculated as

$$t_{\text{out,down,uncorr}}[n] = t_{\text{corr}}[n-1] + t_{\text{osc,down}}[n] \tag{20}$$

where $t_{\text{corr}}[n-1]$ is the $(n-1)$th correcting timestamp (i.e., before being updated to $t_{\text{corr}}[n]$ at $t = nT_{\text{ref}}^-$) for the free-running oscillator. The downsampled signal $t_{\text{osc,down}}[n]$

[13] It is simplified as $N(1-e^{sT_{\text{ref}}})/sT_{\text{ref}}$ in s-domain [51].

[14] Although (6) was derived based on a frequency offset of the oscillator, it holds true in face of all other Δt_{err} perturbations, such as PN of the reference or oscillator.

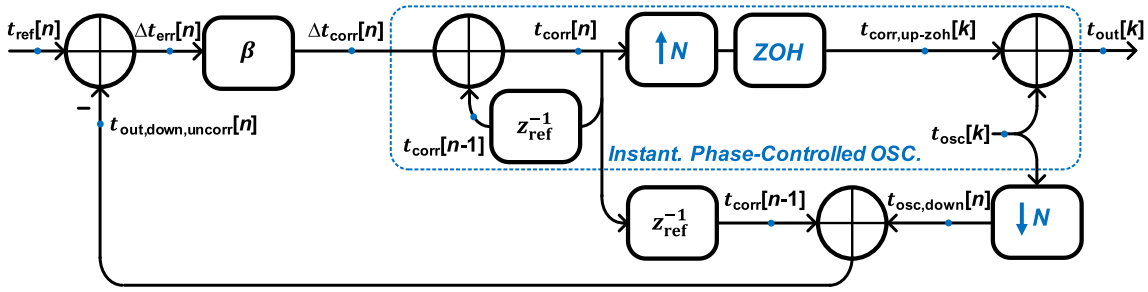


Fig. 6. Multirate timestamp model of CSL oscillators or IL oscillators.

of $t_{\rm osc}[k]$ is assumed identical to the latter when $t = nT_{\rm ref}^-$ and $t = nT_{\rm ref}$ due to $\epsilon_t \ll T_{\rm osc}$. The z-transform of $t_{\rm out}[k]$, $\widehat{T}_{\rm out}(z_{\rm osc})$, in Fig. 6 can be derived as (see the Appendix)

$$\widehat{T}_{\rm out}(z_{\rm osc}) = \frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}N\widehat{T}_{\rm ref}(z_{\rm ref}) + \left(1-\frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}\right)\widehat{T}_{\rm osc}(z_{\rm osc}) - \frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}\sum_{m=1}^{N-1}\widehat{T}_{\rm osc}(z_{\rm osc}e^{-j2\pi m f_{\rm ref}/f_{\rm osc}}). \quad (21)$$

By taking the square of $|\widehat{T}_{\rm out}(z_{\rm osc})|$ and normalizing it into phase domain, we get[15]

$$\mathcal{L}_{\rm out}(z_{\rm osc}) = \left|\frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}\right|^2 N^2\mathcal{L}_{\rm ref}(z_{\rm ref}) + \left|1-\frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}\right|^2\mathcal{L}_{\rm osc}(z_{\rm osc}) + \left|\frac{1}{N}\frac{1-z_{\rm ref}^{-1}}{1-z_{\rm osc}^{-1}}\frac{\beta}{1-(1-\beta)z_{\rm ref}^{-1}}\right|^2\sum_{m=1}^{N-1}\mathcal{L}_{\rm osc}(z_{\rm osc}e^{-j2\pi m f_{\rm ref}/f_{\rm osc}}) \quad (22)$$

where $|\Delta f| < f_{\rm osc}/2$, while its first, second, and third terms represent PN contributions from the reference, oscillator, and oscillator's PN folding due to downsampling, respectively. The PN folding becomes significant with rising β. The in-band PN of (22) could be dominated by $N^2\mathcal{L}_{\rm ref}$ when $\Delta f \to 0$. Interestingly, neglecting the third term in (22) and assuming $N(1-z_{\rm osc}^{-1}) \approx sT_{\rm ref}$, the output PN coincides with [13, eqs. (10) and (11)]. On the other hand, assuming $\mathcal{L}_{\rm ref} = 0$ and $\beta = 1$, it is simplified into [31, eq. (7)].

F. Numerical Verification

To verify the proposed equation (22), we compare it with simulation results of the CSL frequency synthesizer's behavioral model implemented in Cadence Spectre AMS Designer. The reference source and oscillator are modeled by Verilog-AMS in the timestamp domain (described in more detail in [47]), generating rectangular-like waveforms, as in Fig. 3, while the modeling of charge-sharing moment (i.e., phase-realigned) is based on Figs. 2 and 3 and (3) with a specific value of β. The CSL oscillator's timestamps are recorded and post-processed by MATLAB to exhibit its PN and spurious content [39].

First, assuming $\mathcal{L}_{\rm ref} = 0$, we verify the second and third terms of (22). For example, considering a 10-GHz oscillator with $\mathcal{L}_{\rm osc}$ @10 MHz $= 10^{-140/10}$ rad^2/Hz in a free-running mode [see (15)] being charge-sharing locked with a clean reference, its PN plots are shown in Fig. 7(a)–(c) for different N's and β's. The predicted analytical results by (22) [i.e., black curves in Fig. 7(a)–(c)] have a near perfect agreement with the simulation results, thus demonstrating its efficacy. Specifically, in Fig. 7(a), for $N = 50$ and $\beta = 1$ (i.e., ideal IL), the 3-dB "noise bandwidth" for the filtered oscillator's PN is close to 60% $f_{\rm ref}$. On the other hand, the PN at the high-frequency offset is ~3 dB higher than that in the oscillator's free-running mode due to the PN folding, which cannot be predicted in the conventional s- or z-domain models. As shown in Fig. 7(b) and (c), the PN folding [i.e., the third term of (22)] can be neglected when $\beta < 0.5$.

For a practical CSL frequency synthesizer, PN of the reference must be considered. In this case, taking $N = 50$ (i.e., $f_{\rm ref} = 200$ MHz) and $\mathcal{L}_{\rm ref} = 10^{-160/10}$ rad^2/Hz [i.e., rms jitter $\sigma_{\Delta t,\rm ref} = 112.5$ fs; see (19)] into consideration, the simulated PN and analytical results from (22) for different β are shown in Fig. 7(d), both of which match nearly perfectly. Due to the strong ability of suppressing the oscillator's PN in CSL, the reference's PN contribution dominates [i.e., the first term of (22)] in the output, especially for $\beta = 1$. The CSL jitter-tracking bandwidth (describing how much information in the output is influenced by the reference injection, i.e., "loop" bandwidth), $f_{\rm BW,ref}$, can be derived by forcing the first term (excluding $N^2\mathcal{L}_{\rm ref}$) of (22) to equal 0.5 (i.e., 3-dB bandwidth). It can also be used to estimate the "one-sided" lock range $f_{\rm LR}$ of CSL (or IL) [24], [26], [27]. When $\beta \ll 1$, it is simplified as

$$f_{\rm BW,ref} \approx \frac{1}{2\pi}\frac{\beta}{1-\beta}f_{\rm ref} \approx \frac{\beta}{2\pi}f_{\rm ref} \approx f_{\rm LR} \quad (23)$$

which degenerates into [27, eq. (30)]. Fig. 7(e) plots the normalized jitter tracking bandwidth (i.e., $f_{\rm BW,ref}/f_{\rm ref}$) based on (22) and its simplified expression in (23), both of which are relatively well matched for $\beta < 0.2$. However, the maximum jitter-tracking bandwidth, $f_{\rm BW,ref}$, based on the conventional s- or z-models in [26] and [27] is grossly underestimated

[15]There are no cross products between $\widehat{T}_{\rm ref}$ and $\widehat{T}_{\rm osc}$ (with its replicas) due to their independence.

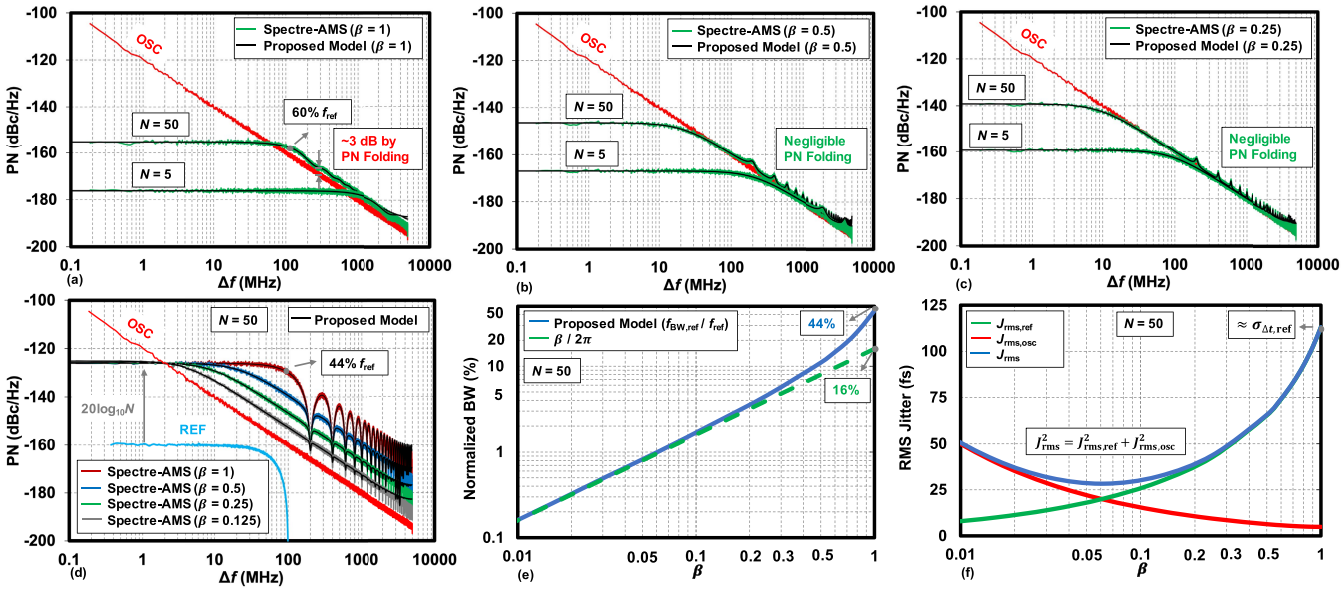


Fig. 7. Calculated [based on (22)] and simulated PN of a 10-GHz charge-sharing locked oscillator with $\mathcal{L}_{\rm osc}$ @10 MHz $= 10^{-140/10}$ rad^2/Hz and (a)–(c) clean (i.e., $\mathcal{L}_{\rm ref} = 0$) or (d) noisy (e.g., $\mathcal{L}_{\rm ref} = 10^{-160/10}$ rad^2/Hz) reference clock for different N and β. Calculated (e) normalized jitter-tracking bandwidth $f_{\rm BW,ref}/f_{\rm ref}$ and (f) rms jitter versus β with $\mathcal{L}_{\rm osc}$ @10 MHz $= 10^{-140/10}$ rad^2/Hz, $\mathcal{L}_{\rm ref} = 10^{-160/10}$ rad^2/Hz, and $f_{\rm ref} = 200$ MHz (i.e., $N = 50$).

at $f_{\rm ref}/2\pi$ (i.e., ~16% $f_{\rm ref}$), much less than the accurately predicted at ~44% $f_{\rm ref}$ (i.e., nearly half of $f_{\rm ref}$).

The effect of the ILO/CSL strength factor β on the output rms jitter is captured in Fig. 7(f). We conservatively apply the full integration bandwidth from 10 kHz to the maximum of $f_{\rm osc}/2 = 5$ GHz. The output rms jitter $J^2_{\rm rms} = J^2_{\rm rms,ref} + J^2_{\rm rms,osc}$ has two components: the filtered reference jitter $J_{\rm rms,ref}$ [i.e., integration applied on the first term of (22)] and the filtered oscillator jitter $J_{\rm rms,osc}$ [i.e., integration applied on the second and third terms of (22)]. Once $\beta > 0.2$, the output jitter $J_{\rm rms}$ is almost fully dominated by $J_{\rm rms,ref}$, while $J_{\rm rms,osc}$ is nearly completely filtered out. Specifically, at $\beta = 1$, the reference jitter is "copied" to the output of CSL, leading to $J_{\rm rms} \approx \sigma_{\Delta t,\rm ref}$ (i.e., 112.5 fs) without practically suppressing [also see Fig. 7(d)]. By decreasing β, the reference jitter is de-emphasized, while the oscillator jitter is emphasized. The (theoretically) minimum rms jitter could be as low as ~25 fs when $\beta = 0.06 - 0.1$, signifying that the reference and oscillator jitter contributions are in balance. However, the excessively small β could lead to an impractical locking range $f_{\rm LR}$ with the oscillator's PN dominating the output. To achieve the sub-100-fs jitter and reasonable lock range $f_{\rm LR}$, β could be chosen at 0.2–0.5. Further improvements targeting, for example, sub-50 fs performance, necessitate the reference source of higher purity while simultaneously reducing the PN contribution (albeit at higher power consumption) from the on-chip reference path.

IV. Frequency-Tracking Loop in CSL

The PVT variations can lead to the oscillator substantially misaligned with the desired frequency $Nf_{\rm ref}$. This causes reference spurs and an induced degradation in the rms jitter, thereby necessitating an FTL.

A. Ref. Spur and RMS Jitter Degradation by Frequency Offset

Assuming that PN contributions from the reference and oscillator are negligible, we quantitatively analyze the effect of oscillator's frequency offset on the reference spur performance. For an oscillator under the CSL regime (see Fig. 3), the average period of its timestamps is constrained to $T_{\rm ref}/N$, while the dynamic deviation of the timestamps are maximized at the $(N-1)$th cycle (from the full correction at Nth cycle) as $(T_{\rm osc} - T_{\rm ref}/N)(N-1)$, which is independent of β [see Fig. 3(b) and (c)]. Thus, the reference spur of CSL (and IL) can be derived as

$$\begin{aligned}\text{Spur}_{\rm ref} &= 20\ \log_{10}\left|\frac{(T_{\rm osc} - T_{\rm ref}/N)\cdot(N-1)}{T_{\rm ref}/N}\right| \\ &= 20\ \log_{10}\left|\frac{\Delta f_{\rm dev,norm}}{1+\Delta f_{\rm dev,norm}}\cdot(N-1)\right| \end{aligned} \tag{24}$$

which is almost proportional to the oscillator's normalized frequency offset $|\Delta f_{\rm dev,norm}|$ [see (9), $|\Delta f_{\rm dev,norm}| \ll 1$] and N.

For a high-performance (e.g., sub-100 fs) frequency synthesizer, the reference spurs alone can substantially degrade its jitter profile, which is typically not included in the integration range of rms jitter [16], [20]. The rms jitter considering both the integrated PN (i.e., $\text{IPN}_{\rm dBc}$) and reference spurs can be calculated as

$$J^2_{\rm rms,\ IPN\&spur} = J^2_{\rm rms} + \left(\frac{\sqrt{2\times 10^{\text{Spur}_{\rm ref}/10}}}{2\pi f_0}\right)^2. \tag{25}$$

Fig. 8 shows the calculated and simulated PN and reference spur, as well as its induced jitter degradation due to the frequency offset. It suggests that for a 10-GHz charge-sharing locked oscillator, the FTL should maintain $|\Delta f_{\rm dev,norm}| <$ 20 ppm [i.e., reference spur < 60 dBc for $N = 50$ per (24) and

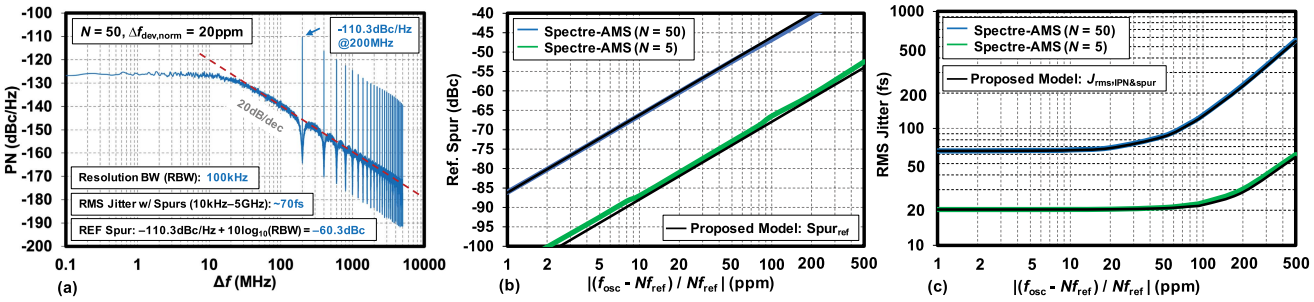


Fig. 8. (a) Simulated PN with normalized frequency offset $\Delta f_{\text{dev,norm}} = 20$ ppm and $N = 50$ [resolution bandwidth (RBW) set at 100 kHz]. Degradation of (b) reference spur and (c) rms jitter [including spur-induced jitter, see (25)] due to $\Delta f_{\text{dev,norm}}$. Conditions: $\beta = 0.5$, $f_{\text{osc}} = 10$ GHz, $\mathcal{L}_{\text{osc}}$ @10 MHz $= 10^{-140/10}$ rad^2/Hz, and $\mathcal{L}_{\text{ref}} = 10^{-160/10}$ rad^2/Hz.

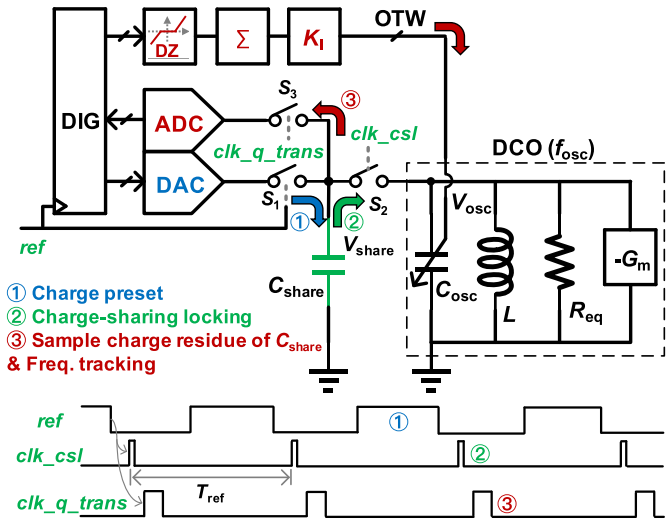


Fig. 9. CSL with FTL and its timing diagram.

Fig. 8(b)] to avoid any induced jitter degradation, as shown in Fig. 8(a) and (c).

B. Digital Frequency-Tracking Loop With Dead Zone

To ensure the robustness of CSL against PVT variations in maintaining the desired level of performance of rms jitter and reference spurs (see an example in Fig. 8), a successive-approximation-register (SAR)-ADC-based digital FTL is proposed to maintain $\Delta f_{\text{dev,norm}}$ within a specified range. By easily applying a dead zone (DZ) of $\Delta f_{\text{dev,norm}}$ in the digital FTL transfer function, we can avoid any conflict between the CSL and FTL operations.

As shown in Fig. 9, after the charge-sharing operation with the oscillator is completed, the charge residue leftover (i.e., ΔV_{share}) in the C_{share} will contain information of the frequency deviation $\Delta f_{\text{dev,norm}}$, as per (8). This voltage is digitized by a SAR-ADC [52] upon asserting *clk_q_trans*. The ADC output is passed through the DZ, accumulator, and attenuation factor K_{I} (controlling the convergence speed) to generate the oscillator tuning word (OTW). Note that there are two kinds of resolution existing in this FTL: the resolution of the frequency detector (i.e., combination of the ADC resolution and DZ) and the resolution of frequency tuning (i.e., the resolution of DCO fine bank). Aiming to maintain $|\Delta f_{\text{dev,norm}}| = 20$ ppm (i.e., the frequency detection resolution of 200 kHz for a 10-GHz oscillator), $N = 50$, $A_{\text{osc}} = 0.5$ V, $\beta = 0.5$, and $|\Delta V_{\text{share}}|$ can be calculated as 3.14 mV by (8), requiring an ADC with an LSB (i.e., least significant bit) of 3.14 mV. Consequently, upon settling to $|\Delta V_{\text{share}}| < 3.14$ mV, the output of DZ will be null, and so the FTL will not make any adjustment to the DCO frequency until the PVT variations exceed $|\Delta f_{\text{dev,norm}}| \sim 20$ ppm. On the other hand, as for the DCO resolution, it should be set at a fraction of $|\Delta f_{\text{dev,norm}}|$ (e.g., <10 ppm/bit or 100 kHz/bit) such that the frequency detection (rather than frequency tuning) resolution is the limiting factor. Otherwise, the FTL's OTW will never be settled but slowly toggling, worsening the CSL's in-band PN (i.e., conflicting with the CSL).

V. Circuit Implementation

A. Architecture

Detailed architecture of the 26-GHz quadrature frequency synthesizer[16] based on the proposed CSL technique is presented in Fig. 10. A fully differential operation is employed to effectively mitigate any common-mode (CM) noise (e.g., supply noise) or coupled interference. It consists of two single-ended 8-bit R-2R-ladder DACs [53], two sharing capacitors (C_{share}), a 9-bit differential SAR-ADC[17] [52], a timing controller, a digital loop filter, a quadrature DCO (Q-DCO), and its harmonic extractors (HEs). Resistors in the R-2R DACs are properly sized, enabling the sharing capacitors to be charged to the expected voltage during the high level of *ref*. The resolution of the differential SAR-ADC is chosen per discussion in Section IV-B, while the DAC's resolution could be set similar to ADC's. The two sharing capacitors C_{share} are set to 1.2 pF. This results in the simulated charge-sharing strength $\beta \approx 0.2$ for the nominal process corner, which helps to achieve an optimized rms jitter performance, as discussed in Section III. To lower the ON-resistance R_{ON} and

[16]Its system-level transient simulation with PN and spurious analysis flow is similar as in the timestamp-domain behavioral modeling in Section III-F but with capturing the behavior of the digital loop filter in Verilog, of the reference source, DAC, and ADC in Verilog-AMS, of the DCO in EMX S-parameter model by "bbspice" interpolation method, and of others in Spectre.

[17]Using a SAR-ADC with a lower number of output bits (e.g., 6-bit) would also be feasible as long as we can keep a similar step-size resolution with appropriate two reference voltages (e.g., 0.6 and 0.4 V).

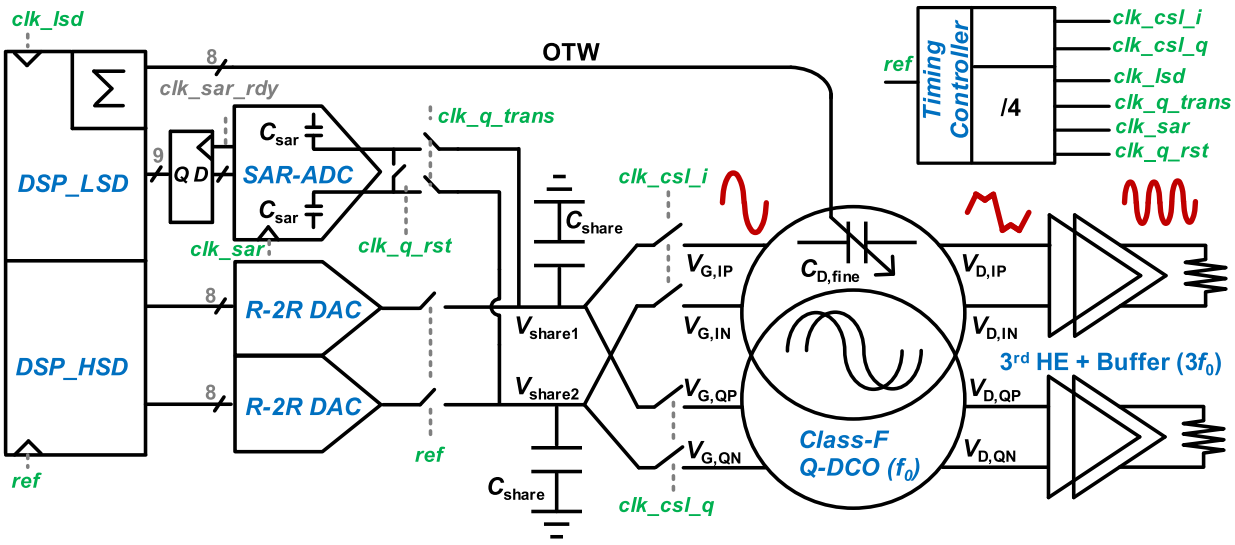


Fig. 10. Top-level schematic of the implemented CSL quadrature frequency synthesizer.

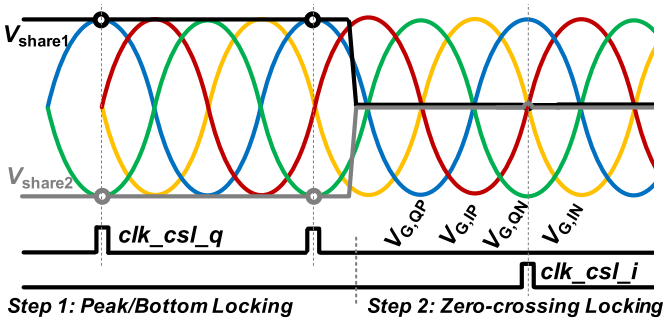


Fig. 11. Two-step locking scheme ensuring the lock at rising edges of $V_{G,IP}$.

improve its linearity, a bootstrap switch is employed for the charge-sharing switches and is controlled by *clk_csl_i/q*. On the other hand, the remaining switches are implemented as plain transmission gates. Four drain nodes $V_{D,IP/IN/QP/QN}$ of the class-F [54] Q-DCO with quasi-square waveforms are fed to the third-HE [44], [55], while its gate nodes $V_{G,IP/IN/QP/QN}$, featuring sinusoidal waveforms, are used for the CSL operation. To further reduce power, the SAR-ADC-based FTL runs at a quarter rate of the reference frequency, where all timing control signals are generated by the timing controller.

To ensure the proper timing alignment of the CSL operation at the rising zero-crossing point of $V_{G,IP}$ (set by a bias voltage V_B, as shown later in Fig. 14), a "two-step locking" is proposed. As shown in Fig. 11, assuming $N = 1$ for simplicity, the sharing switches controlled by *clk_csl_i* are initially turned OFF. In step 1, termed "peak-bottom locking" [56], V_{share1} and V_{share2} are preset to the peak (e.g., 1 V) and bottom (e.g., 0 V), respectively, of the expected single-ended sinusoid in preparation for the CSL with $V_{G,QP}$ and $V_{G,QN}$. This aligns the rising edge of $V_{G,IP}$ with the pulse of *clk_csl_i/q*. After ~0.5 μs (i.e., the required settling time per simulations), step 2 termed "zero-crossing locking" is triggered as previously discussed in conjunction with Figs. 2 and 9, in which $V_{share1/2}$ is preset to the dc offset of $V_{G,IP/IN}$ (i.e., V_B of Q-DCO at ~ 0.5 V). Without the assistance of the initial "peak-bottom locking" step, the oscillator would have a 50% probability of getting locked to the falling zero-crossing point, resulting in an overall positive feedback loop that can lead to a long locking time or even the loss of lock. It should be noted that the actual locking time for the CSL (frequency acquisition) mainly depends on an additional FLL or a coarse ADPLL (used briefly only once during the initialization; afterward, it is shut down), which was not implemented in our prototype of CSL.

B. Timing Control

Fig. 12 shows the schematic of the timing controller and its key timing diagram. The timing controller consists of a reference buffer, two adjustable pulse generators, a ÷4 frequency divider, and other pulse generators. The reference buffer should be sized large enough to make its intrinsic PN (or rms jitter) much lower than the PN of the off-chip reference clock. The falling edge of *ref* is used to generate an adjustable pulse (e.g., 5 bits covering 10–60 ps) for CSL, while DEMUX determines which part of Q-DCO is to be charge-shared. The chosen pulsewidth is an important parameter in both IL-PLLs and SS-PLLs. As a rule of thumb, the pulsewidth could be chosen as around 1/5 of the oscillating period with consideration of the limited R_{ON} of charge-sharing switches. The PVT robustness of pulse design was discussed in [57].

The timing-control signals for the FTL run at $f_{ref}/4$, which is generated by dividing the inverted reference signal (i.e., $\overline{ref}$) to obtain the low-speed clock *clk_lsd*. The rising edge of *clk_lsd* updates the Q-DCO's OTW per the last detected frequency error and triggers the pulse *clk_q_trans* of ~0.8 ns for transferring the differential charge residue on C_{share} (representing the current frequency error) to the input capacitance of SAR-ADC (C_{sar}) after the CSL event. If the differential charge residue on C_{share} is ΔV, the transferred charge on C_{sar}

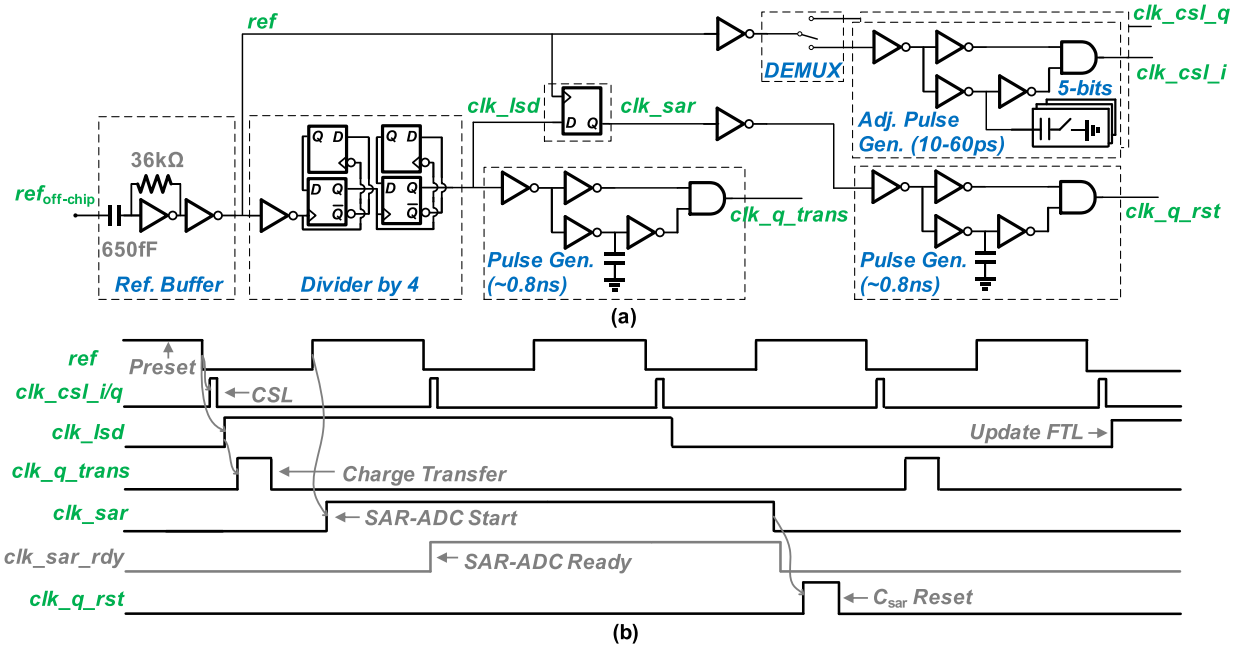


Fig. 12. Timing controller: (a) schematic and (b) timing diagram.

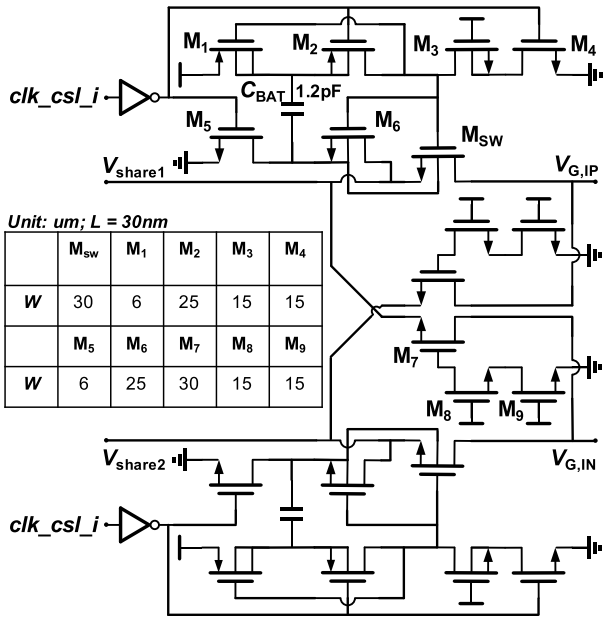
will be $\Delta V C_{\text{share}}/(C_{\text{share}}+C_{\text{sar}})$. Using *ref* to re-sample *clk_lsd* generates the SAR-ADC start signal *clk_sar*, which must come after the charge transfer. When the SAR-ADC finishes the evaluation, its internal "ready" signal *clk_sar_rdy* (triggered by *clk_sar*) loads its output into the flip-flops, while the falling edge of *clk_sar* generates the ∼0.8-ns pulse *clk_q_rst* for resetting $\Delta V C_{\text{share}}/(C_{\text{share}}+C_{\text{sar}})$ on C_{sar} to null, waiting for the next charge transfer. When the next rising edge of *clk_lsd* arrives, the SAR-ADC output will be used to update the FTL, as described in Section IV.

C. Charge-Sharing Switch With Adaptive Body-Biasing

A modified bootstrap switch [58], [59] combining the adaptive body-biasing concept [60] is introduced in Fig. 13, where M_{sw}, M_6, and M_3 are in deep N-wells. When *clk_csl_i* is low, $M_{1/5}$ preset C_{BAT} to V_{DD}, $M_{3/4}$ pull down, turning off M_{sw}, and the body of M_{sw} connects to the ground through M_5 for a better R_{OFF}. On the other hand, when *clk_csl_i* is high, $M_{2/6}$ turn on, connecting C_{BAT} (charged to V_{DD}) to the gate and source of M_{sw}. This fully turns on M_{sw}, with the body of M_{sw} connected to its source through M_6, further reducing its R_{ON}. M_7 works as a dummy for M_{sw} to cancel the differential-mode coupling from the oscillator to C_{share}. It should be noted that the unwanted clock feedthrough or charge injection due to the parasitics of the charge-sharing switch could lead to further spur degradation, which would require careful circuit redesign and/or finding a more resilient architecture.

D. Quadrature DCO

Quadrature mmW generation is another challenge for 5G communications. Directly running the oscillator at mmW frequencies [17], [61] would suffer from low quality



	M_{sw}	M_1	M_2	M_3	M_4
W	30	6	25	15	15
	M_5	M_6	M_7	M_8	M_9
W	6	25	30	15	15

Fig. 13. Proposed CSL bootstrap switch with adaptive body-biasing (shown I-path only).

(Q)-factor of switched-capacitor (sw-cap) banks. A quadrature third-harmonic extraction [44], [62] based on a source-coupling [63] quadrature class-F [54] oscillator is introduced, employing a 1:2:1 transformer [64], as shown in Fig. 14. The quadrature oscillator runs at a much lower fundamental frequency (e.g., 8.75 GHz), whose signals at the drain nodes with a strong third harmonic (e.g., 26.25 GHz) are extracted by two HEs [55]. The coupling phase delay ϕ could be used to avoid the well-known quadrature uncertainty (i.e., $+90°$ or $-90°$) [65].

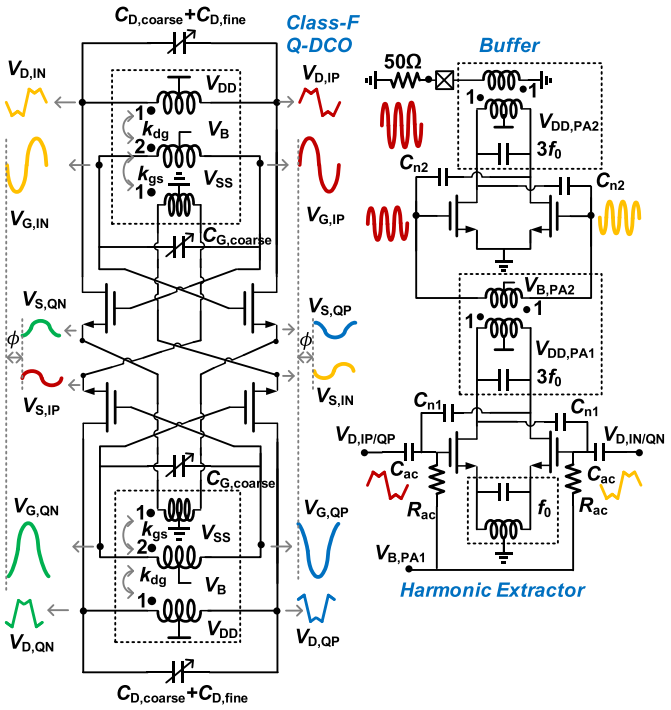
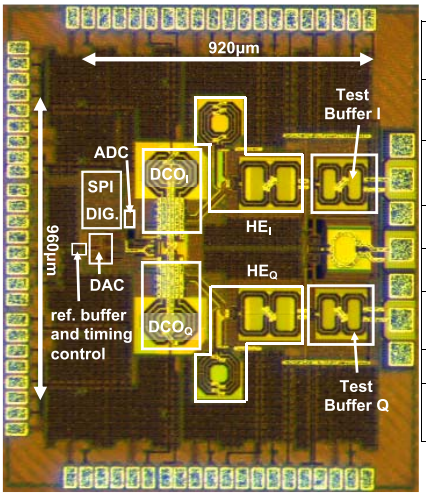


Fig. 14. Circuit diagram of the proposed 26-GHz quadrature generation comprising the quadrature class-F DCO and third-harmonic extractors.

The 7-bit coarse tuning banks (i.e., $C_{\mathrm{G,coarse}}$ and $C_{\mathrm{D,coarse}}$) based on conventional resistor-biasing sw-caps [44] are placed at the gate and drain nodes of Q-DCO, respectively. For the coarse frequency tuning, both $C_{\mathrm{G,coarse}}$ and $C_{\mathrm{D,coarse}}$ are tuned together to keep the class-F operation [44], [50]. An 8-bit fine-tuning bank (i.e., $C_{\mathrm{D,fine}}$), using a simple single-ended nMOS sw-cap architecture, appears only at the drain nodes for frequency tracking of FTL. The fine-tuning bank employs custom-made MOM caps, achieving a resolution of ~80 kHz with 40 aF, which is around 10 ppm for 8 GHz. Different supply domains are employed for the Q-DCO's core and its sw-caps to eliminate any singled-ended capacitance in the sw-caps being seen as a CM capacitance, which improves the CM impedance and reduces $4kTg_{\mathrm{ds}}$ noise [44], [46], [47]. The I/Q mismatch can be calibrated easily by providing a bit different tuning codes between $C_{\mathrm{D,fine}}$ in I and Q parts of the Q-DCO. The resolution is about ~1°/fF for the third harmonic, as per simulations. The transformer-based LC-tank was modeled and simulated using an S-parameter model ["linear" interpolation method for periodic steady-state (PSS) analysis while "bbspice" for transient simulation] with Cadence EMX.

VI. Experimental Results

The prototype of the proposed quadrature 26-GHz CSL frequency synthesizer was fabricated in TSMC 28-nm LP CMOS, as shown in Fig. 15. It occupies a total active area of 0.5 mm^2, including a small part of 0.0016 mm^2 for the SAR-ADC-based digital FTL. The reference buffer and the timing control circuit (operating at 1 V) consume 0.82 mW, while the FTL and the two R-2R DACs (operating at 1 V) consume 0.1 and 1.5 mW, respectively. The



Building Blocks	P_{DC} (mW)
QDCO (V_B=0.5V, V_{DD}=0.4V)	3.92
Harmonic Extractors (HE) (V_B=0.7V, V_{DD}=1V)	2×5
R-2R DACs	2×0.75
SAR-ADC	0.1
Ref. buf. + Timing logics + Others	0.82
SPI + Digital	0.14
Total	16.5

Fig. 15. Die micrograph and power breakdown of building blocks.

power consumption of Q-DCO (V_{DD} = 0.4 V) is 3.92 mW, while the two 3rd-harmonic extractors (HE) consume 10 mW. The total power consumption of the whole system is 16.5 mW.

The input reference was generated by an R&S SMA 100A signal generator. PN of the reference and CSL was characterized by an R&S 2-Hz–85-GHz FSW Signal and Spectrum Analyser, while Keysight E5052B was used to measure the PN at the Q-DCO output. The measured PN of the Q-DCO at a 26.46-GHz carrier is −42.26, −74.5, −102, and −126.5 dBc/Hz at 0.01-, 0.1-, 1-, and 10-MHz offsets, respectively, resulting in a $1/f^3$ PN corner of ~550 kHz. The FoM @10 MHz of the Q-DCO is calculated as −183.5 dB (with consideration of the HE's power of ~10 mW). As for the external 250-MHz reference source, its PN @100 kHz is around −145 dBc/Hz [see Fig. 16(a)] with ~81-fs rms jitter (integrated from 10 kHz to 30 MHz). The actual reference jitter seen by the CSL switch accounts for both the external reference source and its on-chip distribution path (i.e., from $ref_{\mathrm{off\text{-}chip}}$ to *clk_csl_i/q* in Fig. 12, simulated at ~79 fs), which is estimated at 113 fs ($=\sqrt{81^2+79^2}$ fs) in total.

Fig. 16(a)–(d) shows the measured rms jitter (integrated from 10 kHz to 30 MHz[18]) at 76–77 fs and reference spurs[19] at −45~−43 dBc from 26.25 to 21.75 GHz. To account for the third-harmonic extraction, the reference spur for the fundamental frequency of 8.75–7.25 GHz is around −53 dBc after subtracting 20 $\log_{10}(3)$ = 9.54 dB. Some visible sub-reference spurs (e.g., @$f_{\mathrm{ref}}/4$) originate from parasitic supply coupling from the divider in the timing control circuitry, which could be reduced by a better isolation of supplies. Across the whole ~19% tuning range (TR) [see Fig. 16(f)], the CSL frequency synthesizer's PN @1-MHz offset is around −110 dBc/Hz, while its in-band

[18]The PN plot in Fig. 16(a) shows the expected 20 dB/dec roll-off outside of the "loop" bandwidth cutoff of ~6 MHz. Thus, the jitter contribution above 30 MHz (5× the "loop" bandwidth) offset can be practically neglected.

[19]Per (25), the rms jitter considering both the measured integrated PN and reference spurs will be ~100 fs.

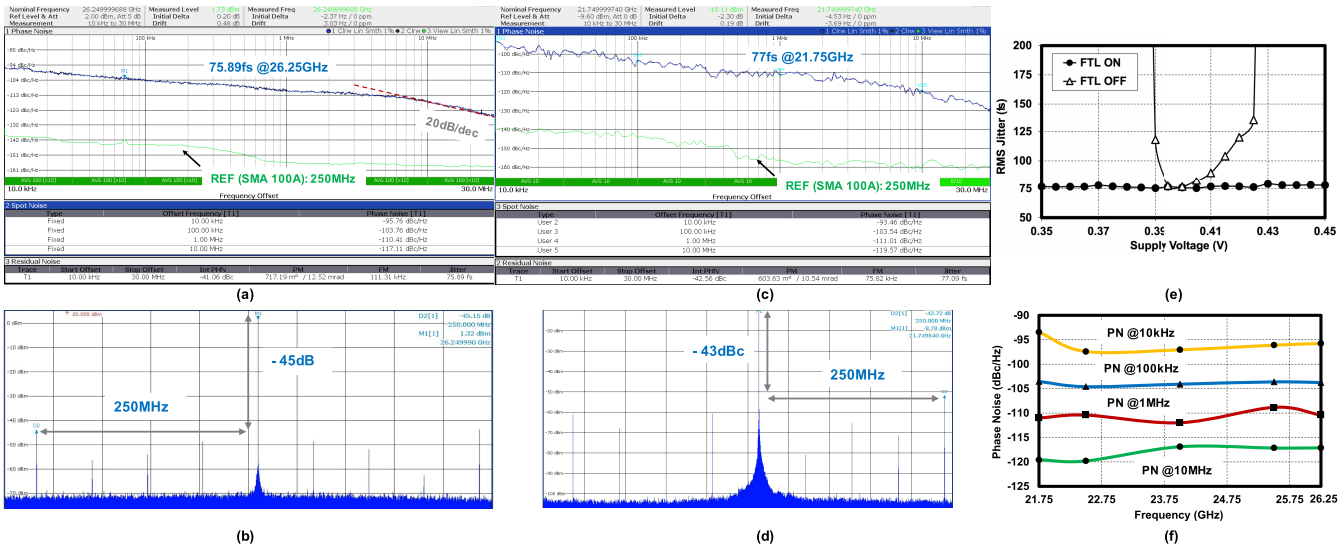


Fig. 16. Measurements: (a)–(d) PN, rms jitter, and spurs at 26.25 GHz (left) and 21.75 GHz (right). (e) Supply voltage effect on jitter with FTL ON/OFF. (f) PN over the TR.

TABLE I

PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RF AND mmW FREQUENCY SYNTHESIZERS

	This work	Kim, *ISSCC*'19 [20]	Siriburanon, *JSSC*'16 [18]	Yang, *ISSCC*'19 [6]	Szortyka, *JSSC*'15 [61]	Elkholy, *JSSC*'15 [16]
Tech. (nm)	28 LP	65	65	65	40	65
Architecture	Charge-Sharing Locking	Cascading 4GHz SS-DPLL + QILO	Cascading 20GHz SSPLL + QILO	Analog SSPLL	Analog SSPLL	Injection Locking
Freq. Tracking/Locking Loop	Digital FTL (SAR-ADC)	Analog Phase-Avg. FTL	ILFD + PFD/CP	High-speed Divider + PFD/CP	CML+ PFD/CP	Gated Pulse + BBPD
Quadrature	Yes	Yes	Yes	No	Yes	No
Approach	Class-F QDCO + 3rd Harm. Extraction	mmW QILO	mmW QILO	Direct mmW VCO	Direct mmW VCO	DCO
Output Freq. (GHz)	21.71 to 26.49 (19.3%)	28 to 31 (10.1%)	55.6 to 65.2 (15.8%)	25.4 to 29.5 (14.9%)	53.8 to 63.3 (16.2%)	6.75 to 8.25 (20%)
Ref. (MHz)	250	100	40	103	40	105 to 129
PN@1MHz (dBc/Hz)	-110.4	-105.84	-91	-112.8	-88.3	-112.3
Jitter (fs) (Integration range)	75.89 (10k to 30M)	76 (1k to 30M)	290 (NA)	71 (1k to 100M)	214 (1k to 100M)	179 (10k to 40M)
Ref. Spur (dB)	-45 – -43	-58@100MHz/ -40@2GHz	-73	-63	-40	-40
P_{DC} (mW)	16.5	41.8	32	15.3#	42	2.25
$P_{DC,FTL}$ (mW)	0.1	0.9	NA	NA	33	NA
FoM/FoM_p (dB)	-250.2/-253.2	-246/-249	-235.7/-238.7	-251.1#	-237/-240	-251
Active Area (mm^2)	0.5	0.32	N/A	0.24	0.16	0.25

FoM = $20\log_{10}$(Jitter/1s) + $10\log_{10}$(P_{DC}/1mW); FoM_p = FoM+$10\log_{10}$(2/#phase); #Include the power consumption of ref. buffer (5.1mW) from the ISSCC'19 Visuals

PN (e.g., PN @100-kHz offset) is about −104 dBc/Hz, which is dominated by the reference PN as expected from (22) (e.g., −145 dBc/Hz + 20 × $\log_{10}$(26.25 GHz/250 MHz) = −104.57 dBc/Hz). As illustrated in Fig. 16(e), with the proposed SAR-ADC-based FTL ON, the CSL can maintain the jitter performance when V_{DD} of the oscillator changes from 0.35 to 0.45 V, evidencing its robustness against supply variations.

Fig. 17 demonstrates the efficacy of the proposed theory. We calculate the PN at the CSL output (black curve) from (22) when feeding the measured PN of the reference source (thick blue curve) together with the simulated PN of the on-chip reference path (thin dark-blue curve) and the measured PN of the free-running DCO (thick red curve). It proves an excellent agreement (within 0.5 dB) with the measured PN at the CSL output (thick gray curve). It also shows the output PN is mainly

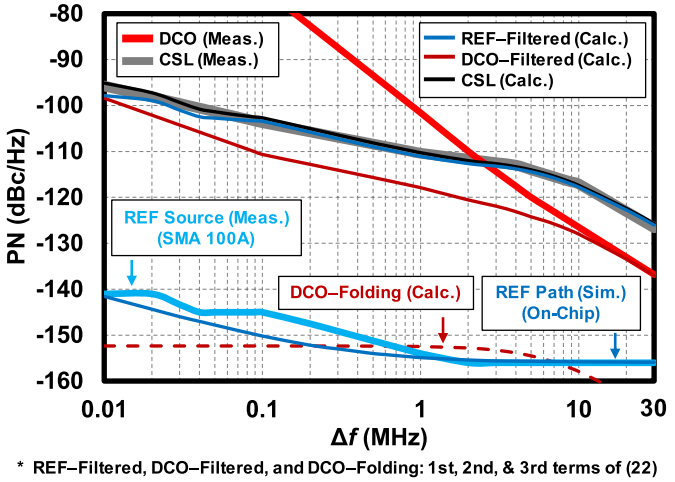


Fig. 17. Comparison of the measured PN versus calculated via (22) from measurements of composite sources with $\beta = 0.15$: oscillator and reference (adjusted by the simulated on-chip path, i.e., REF = "REF Source" + "REF Path").

dominated by the filtered reference PN (source + distribution path), while the DCO's PN is significantly suppressed (thin dark-red curve).

Table I compares this work with other state-of-the-art mmW (and one RF) PLLs. To the best of our knowledge, the proposed synthesizer shows the best FoM (−250 dB) for the mmW quadrature frequency generation, and if the beneficial quadrature output is disregarded, it is still only 1 dB worse than the analog SS-PLL in [6].

VII. Conclusion

A CSL frequency synthesizer with its *implicit* digital FTL is presented to support the sub-100-fs requirement for emerging high-speed communication applications, such as 5G/6G cellular. The proposed CSL mechanism solves the "loop"-bandwidth optimization issue in the conventional IL synthesizers and the timing-race problem with their FTL, thus achieving optimized rms jitter and robustness simultaneously. In addition, we propose a unified theory of PN for CSL (extending to IL) based on a *multirate* timestamp modeling technique, which can explain all PN phenomena, thus serving as a guide for its rms jitter optimization. The model could be extended to other wideband, low-jitter PLLs. As a newly developed fundamental phase-locking mechanism, the CSL has a high potential to be explored in other applications with other oscillator topologies.

Appendix
Proof of (21)

To derive the relationship between the z-transforms of $t_{\text{out}}[k]$ and $t_{\text{osc}}[k]$ & $t_{\text{ref}}[n]$, we start with an equation based on $\Delta t_{\text{corr}}[n]$ in Fig. 6 as

$$\beta(t_{\text{ref}}[n] - t_{\text{out,down,uncorr}}[n]) = t_{\text{corr}}[n] - t_{\text{corr}}[n-1]. \quad (26)$$

Substituting (20) into (26), we obtain its z-transform as

$$\beta(\widehat{T}_{\text{ref}}(z_{\text{ref}}) - z_{\text{ref}}^{-1}\widehat{T}_{\text{corr}}(z_{\text{ref}}) - \widehat{T}_{\text{osc,down}}(z_{\text{ref}})) = \widehat{T}_{\text{corr}}(z_{\text{ref}}) - z_{\text{ref}}^{-1}\widehat{T}_{\text{corr}}(z_{\text{ref}}) \quad (27)$$

and then

$$\widehat{T}_{\text{corr}}(z_{\text{ref}}) = \frac{\beta(\widehat{T}_{\text{ref}}(z_{\text{ref}}) - \widehat{T}_{\text{osc,down}}(z_{\text{ref}}))}{1-(1-\beta)z_{\text{ref}}^{-1}}. \quad (28)$$

On the other hand,

$$t_{\text{out}}[k] = t_{\text{corr,up-zoh}}[k] + t_{\text{osc}}[k] \quad (29)$$

and its z-transform is

$$\begin{aligned}\widehat{T}_{\text{out}}(z_{\text{osc}}) &= H_{\text{zoh}}(z_{\text{osc}}) \cdot \widehat{T}_{\text{corr,up}}(z_{\text{osc}}) + \widehat{T}_{\text{osc}}(z_{\text{osc}}) \\ &= H_{\text{zoh}}(z_{\text{osc}}) \cdot \widehat{T}_{\text{corr}}(z_{\text{ref}}) + \widehat{T}_{\text{osc}}(z_{\text{osc}}) \quad (30)\end{aligned}$$

where $\widehat{T}_{\text{corr,up}}(z_{\text{osc}}) = \widehat{T}_{\text{corr}}(z_{\text{osc}}^N) = \widehat{T}_{\text{corr}}(z_{\text{ref}})$. Substituting (13), (17), and (28) into (30), we get (21).

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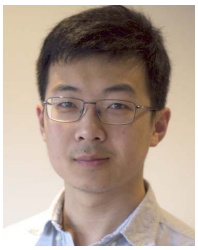

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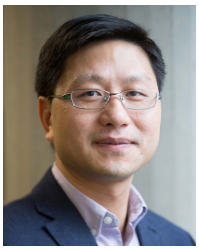

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