A Compact 0.2–0.3-V Inverse-Class-F_{23} Oscillator for Low $1/f^3$ Noise Over Wide Tuning Range

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***Abstract*— We introduce a new mode of oscillation in an *LC*-tank: an inverse class-F_{23}. In contrast to the conventional class-F oscillators, in which a high value of the real impedance (i.e., resistance) is presented to the third (in class-F_3) or/and to the second (in class-F_2/class-F_{23}) oscillator harmonics via an auxiliary resonance, here low resistive impedances (resembling a non-ideal short) are presented at both the second and third harmonics. This is made possible by tight magnetic coupling in the differential and common modes, respectively, afforded by a new compact 2:3 transformer. Being largely free from the harmonics in the voltage waveform and their possible deleterious phase shift effects on the flicker noise up-conversion, the phase noise performance in the flicker and thermal regions is further improved by narrowing the conduction angle. The 2:3 step-up transformer also provides a high passive gain to help with the startup in face of low supply. The switched-capacitor banks and cross-coupled transistor pair are carefully integrated under the transformer with a special arrangement of native (high-resistivity) substrate layer to mitigate their effect on the oscillation while reducing the area by 30%. The proposed digitally controlled oscillator (DCO) is implemented in 28-nm CMOS and achieves −95 dBc/Hz and −118 dBc/Hz at 100 kHz and 1 MHz offsets, respectively, while operating at a 0.3 V supply. The measured $1/f^3$ corner stays within 60 to 100 kHz over the 35% tuning range (TR) (from 2.02 to 2.87 GHz). This results in a figure-of-merit (FoM) with normalized TR (FoM_T) of −196 and −199 dB at 100 kHz and 1 MHz offsets, respectively, is a record in the space of ≤0.5 V and ≤1 mW.**

***Index Terms*— Class-C oscillator, digitally controlled oscillator (DCO), Internet-of-Things (IoT), low flicker phase noise (PN), low power, low voltage, narrow conduction angle, transformer, vertical integration.**

I. Introduction

IoT devices sustained by energy harvesters, such as photovoltaic cells, must support an ultralow-voltage (ULV) operation while minimizing power consumption and silicon area. This puts severe constraints on the performance of *LC*-tank oscillators. With the shrinking of transistor size in advanced CMOS, almost all of the oscillator's active area is now occupied by passive devices, i.e., inductors, which do not easily lend themselves to scaling. Furthermore, to achieve high power efficiency, the quality (Q) factor of the inductor needs to be maximized with an optimal coil radius of ∼120–180 μm [1], which unfortunately leads to a large area. On the other hand, switched-capacitor (sw-cap) banks for frequency tuning of digitally controlled oscillators (DCOs) consist of large arrays of sw-cap cells for wide tuning range (TR) and fine-tuning resolution together, at the cost of significant area increasing. To improve the area compactness, overlapping the inductor and sw-cap banks were proposed in [2] and [3], in which, a pattern ground shield (PGS) would typically be inserted to isolate electrically (not magnetically) the top layer inductor from the active circuits at the lower layers as well as from a lossy substrate. However, it only increases the Q-factor of the inductor by <3% but suffers from degradation in the passive devices' self-resonance frequency (SRF) and the oscillator's TR.

There are two main concerns in supporting the ULV operation of oscillators: phase noise (PN) degradation caused by the small oscillating amplitude and the difficulties in a startup. The thermal PN is inversely proportional to the square of the oscillating amplitude, which is normally limited by the supply voltage V_{DD}, indicated by the horizontal dashed line in Fig. 1(b). To increase the tank's oscillating amplitude, Kwok and Luong [4] exploited the passive gain (G) of a transformer to boost the voltage gain from the drain to the source of the cross-coupled pair; it can alternatively be implemented between the drain and gate as shown in Fig. 1(a) [5]. An independent control of the center-tap bias voltage V_B offers freedom to control the common-mode (CM) gate voltage helping with the startup in face of the low supply voltage. To implement this concept at ULV (i.e., $V_{DD} \approx 0.2$ V), a trifilar-coil transformer was used to further boost the passive voltage gain in [6], but at a cost of a narrow TR. Additionally, ULV limits the headroom of the cross-coupled pair which restricts the oscillators structure, i.e., tail current source/tail filter [8] cannot be used and class-C [1], [21] operation is difficult to be implemented due to its startup problem. However, the transformer impedance characteristic exhibits additional CM and differential-mode (DM) peaks (i.e., nondominant resonances) due to the magnetic coupling, k_{CM} and k_{DM}, respectively, as shown in Fig. 1(c). Class-F oscillators

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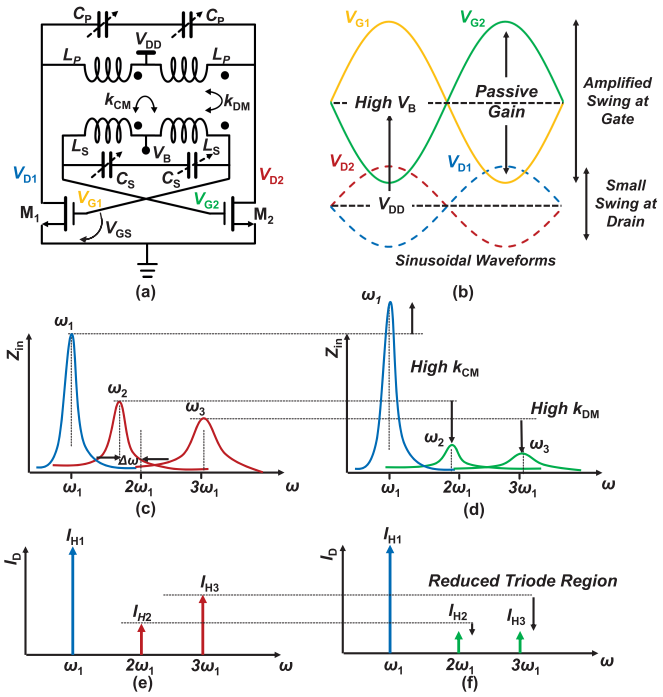

Fig. 1. Transformer-based oscillator operating at ULV: (a) schematic and (b) its waveforms. Transformer impedances in (c) conventional class-F oscillator with untuned harmonic resonances and (d) proposed inverse-class-F_{23} oscillator. Drain current harmonics in (e) class-F oscillator and (f) proposed oscillator with narrow conduction angle.

intentionally tune the CM or/and DM resonances to the second and third harmonics of the fundamental resonating frequency [5], [7], [10]. We emphasize that if the CM second and DM third harmonic resonance are not properly tuned, PN in the thermal ($1/f^2$) and flicker ($1/f^3$) noise regions will be deteriorated [9]–[19].

In this article, targeting the low supply voltage and compact area, we propose a DCO constructed on a 2:3 transformer with tight interwinding magnetic coupling and accommodating its switched-capacitor (sw-cap) banks right underneath [20]. Operating merely at 0.2–0.3 V, the proposed transformer featuring high k_{DM} and k_{CM} provides a large passive gain to enhance V_{GS}. This helps with the oscillation startup and with reducing the PN, as well as with lowering the tank impedances at higher frequencies which shunt the second and third harmonics, thereby introducing an "inverse-class-F_{23}" mode of operation. The weakened harmonics in the voltage waveform suppress the $1/f$ noise up-conversion across a wide TR that is also free from misalignment of the second and third harmonics resonances. Moreover, lowering V_B reduces the exposure of the cross-coupled pair to the sensitive triode region of distorted waveform arising from left-over harmonics. Thus, reduced conduction angle helps to maintain low flicker PN across the TR [13], [20].

Section II describes the proposed oscillator, the design and optimization of k_{DM} and k_{CM}, and the analysis of flicker noise up-conversion. The detailed considerations and implementation of vertically integrated sw-cap banks are revealed in Section III. The detailed circuit implementation is given in Section IV. The measurement results are discussed in Section V.

II. Proposed Inverse-Class-F_{23} Oscillator

As mentioned above, for supporting an ULV operation (i.e., 0.2–0.3 V), a step-up transformer is commonly employed [4], [6], [39]. This also helps with the $1/f^2$ PN, as the noise factor $F = 1 + \gamma/G$ can be reduced by a passive gain of G to compensate for the small oscillation amplitude. Other examples aiming to reduce the $1/f^2$ and $1/f^3$ PN in transformer-based oscillators are summarized as follows: Mazzanti and Andreani [21] and Tohidian *et al.* [22] utilize a transformer-based class-C oscillator which enhances the dc–RF current efficiency by lowering its gate bias voltage V_B. That prevents the cross-coupled pair from entering the triode region, which can also minimize the flicker noise up-conversion [13], [23], [24].

Multi-resonance tanks have been intensively studied in recent years for their ability to lower the PN up-conversion, resulting in various flavors of class-F operation, e.g., through an additional parallel resonance of the 3rd (in class-F_3 [5]) or/and second (in class-F_2 [7]/class-F_{23} [10], [11]) harmonic of the fundamental oscillation. Lim *et al.* [25] disclosed an interesting oscillator structure termed "inverse-class-F,"[1] which achieves low PN by means of a strong second harmonic resonance (i.e., enhanced class-F_2), but it suffers from a differential phase imbalance and is not suitable for an ULV operation due to its current-reuse structure [26], [27]. For the $1/f^3$ PN, according to [10], [14], the low-frequency $1/f$ fluctuations in voltage-biased oscillators are mainly up-converted by modulating the unbalanced waveform caused by misaligned harmonics (mainly the second and third).

In the proposed oscillator, the transformer is optimized with high coupling factor for both CM k_{CM} and DM k_{DM} to achieve higher passive gain and lower impedance of the tank harmonic resonances. Instead of relying on the precise CM/DM resonance of second and third harmonics in [10] and [11], this work achieves low $1/f$ noise up-conversion through another mechanism: improving symmetry of the oscillating waveform by lowering the effect of higher-order CM and DM harmonic impedances. This results in suppressing amplitude ratios of the harmonics: V_{H2}/V_{H1} and V_{H3}/V_{H1}, thus giving rise to the "inverse-class-F_{23}" operation [see Fig. 1(d) and (f)]. Consequently, a higher degree of freedom is allowed when optimizing the tank capacitance ratio to achieve a large TR.

A. Transformer Design for ULV and Low Flicker-PN Oscillation

To better understand the principle of inverse-class-F_{23} operation, the effect of the transformer's coupling factor on the oscillating waveform will be analyzed in detail. Fig. 2(a) shows the comprehensive two-port transformer model. In contrast to [5], where only the DM coupling factor between the primary and secondary coils are considered, in this work, we *also* examine the CM coupling factor between two sides of the primary coil inductor. This allows to accurately determine the impedance in both DM (Z_{DM}) and CM (Z_{CM}). Moreover, it also reveals the benefits of

[1]That definition stems from the field of RF power amplifiers: the waveform shapes of current and voltage: "square-like I_D and half-sinusoidal V_D," which is different from what we follow in our work.

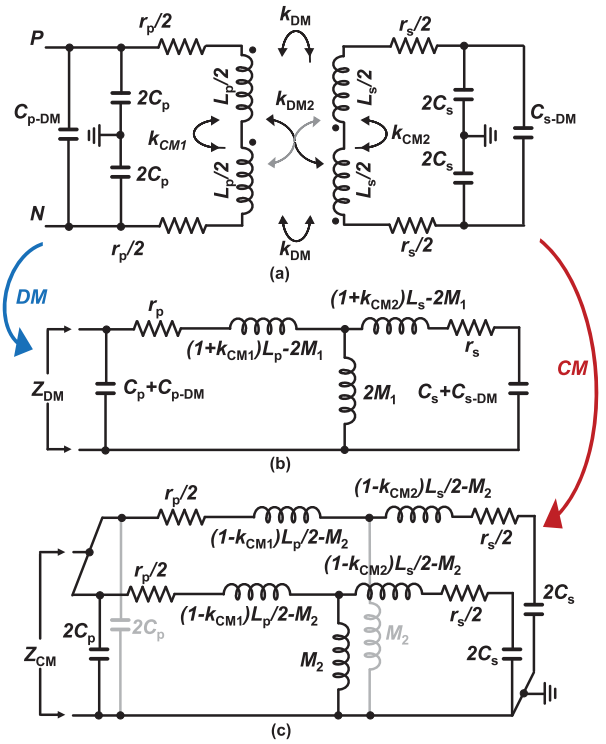

Fig. 2. (a) Two-port model of transformer considering both DM and CM coupling factors. Simplified equivalent T-model of (b) DM impedance and (c) CM impedance.

the proposed 2:3 transformer which leads to low resistive impedances (non-ideal short) near the second and third harmonics. The proposed simplified equivalent T-model which takes into account both CM and DM coupling factors is shown in Fig. 2(b) and (c). The mutual inductance is defined as $M_1 = k_{DM}((1+k_{CM1})L_p/2\cdot(1+k_{CM2})L_s/2)^{1/2}$ and $M_2 = k_{DM}((1-k_{CM1})L_p/2\cdot(1-k_{CM2})L_s/2)^{1/2}$. Note that k_{CM1} (k_{CM2}) refers to the primary (secondary) coil.

To maintain a low distortion of the oscillating waveform and consequently reduce the $1/f$ noise up-conversion, the transformer should exhibit high impedance for the fundamental frequency while suppressing (e.g., via short-circuiting) all other harmonics (i.e., second and third). In the differential mode, Z_{DM} can be derived based on the equivalent model shown in Fig. 2(b) as long (1) as shown at the bottom of this page, where $C'_p = C_p + C_{p-DM}$ and $C'_s = C_s + C_{s-DM}$. It can be expressed in a fraction format as (2) as shown at the bottom of this page, where $L'_p = (1+k_{CM1})L_p$ and $L'_s = (1+k_{CM2})L_s$. The fourth-order denominator can be solved by two conjugate-pole pairs to obtain two resonant frequencies: one is at the fundamental ω_1, and the other is at a much higher frequency, ω_3, which is $>2.5\omega_1$ when $k_{DM} > 0.7$ [5]. For $0.5 < k_{DM} < 1$, the main resonant frequency ω_{DM1} can be simplified and expressed as

$$\omega_{DM1}^2 = \frac{1}{(1+k_{CM1})L_pC'_p + (1+k_{CM2})L_sC'_s} \tag{3}$$

and the two resonant-peak impedances can be solved as

$$\begin{cases} Z_{DM1} = \dfrac{(1+k_{CM1})L_p + r_sr_pC'_s}{r_pC_p + r_sC'_s} \\ Z_{DM2} = \dfrac{(1+k_{CM1})(1+k_{CM2})L_pL_s(1-k_{DM}{}^2)}{C'_p\left[(1+k_{CM2})L_sr_p + (1+k_{CM1})L_pr_s\right]}. \end{cases} \tag{4}$$

When targeting ~2.4 GHz, L_p and L_s should be of several nH and so C'_p and C'_s will be at the ~pF level. By removing the nondominant factors in (4) and considering equal Q_p and Q_s ($Q_{DM} = (1+k_{CM})L\omega/r$), and equal k_{CM1} and k_{CM2}, Z_{DM} can be simplified as

$$\begin{cases} Z_{DM1} \approx \dfrac{(1+k_{CM})L_p}{r_pC'_p + r_sC'_s} \approx (1+k_{CM1})L_p\omega Q_{DM} \\ Z_{DM2} \approx \dfrac{Q_{DM}(1-k_{DM}{}^2)}{2C'_p\omega}. \end{cases} \tag{5}$$

With a fixed target frequency and optimized Q-factor, the impedance at the fundamental frequency is largely affected by k_{CM}. On the other hand, the impedance magnitude at higher harmonics can be reduced with an increase of k_{DM}.

To analyze the CM impedance, the equivalent T-model in Fig. 2(c) is analyzed. Following the above analysis for Z_{DM}, Z_{CM} exhibits a similar form as Z_{DM} but with the following differences: 1) $L'_p = (1-k_{CM1})L_p$ and $L'_s = (1-k_{CM2})L_s$. 2) Replacing r with $r/2$, L with $L/2$, and C with $2C$ (note, C_{p-DM} and C_{s-DM} cannot be seen in CM), as well as applying the 1/2 factor for the overall amplitude. Consequently, the CM resonant frequency can be expressed as

$$\omega_{CM1}^2 = \frac{1}{(1-k_{CM1})L_pC_p + (1-k_{CM2})L_sC_s}. \tag{6}$$

From the above equation, assuming $k_{CM1} = k_{CM2} \approx 0.3$ and $C_{p-DM} = C_p$; $C_{s-DM} = C_s$, the CM resonant frequency will be pushed higher to $2\omega_{DM1}$, which aligns precisely with the second harmonic. The peak magnitude of the CM impedance can be roughly estimated as

$$Z_{CM1} \approx \frac{1}{4}(1-k_{CM1})L_p\omega Q_{CM} \tag{7}$$

where $Q_{CM} = (1-k_{CM})L\omega/r$. Together with (5), it can be concluded that higher k_{CM1} can effectively reduce the second harmonic impedance, whereas higher k_{DM} can concurrently reduce the third harmonic impedance. To verify the above analysis, Fig. 3(a) shows the simulated amplitude ratio between the third harmonic and the fundamental of the drain voltage with the lowest achievable conduction angle of $\sim \pi/3$.

$$Z_{DM} = \frac{1}{sC'_p}\Bigg\| \left\{ r_p + s\left[(1+k_{CM1})L_p - 2M\right] + 2sM \Bigg\| \left\{ s[(1+k_{CM2})L_s - 2M] + r_s + \frac{1}{sC'_s} \right\} \right\} \tag{1}$$

$$Z_{DM} = \frac{s^3\left(L'_pL'_sC'_s\left(1-k_{DM}^2\right)\right) + s^2\left(C'_s\left(L'_sr_p + L'_pr_s\right)\right) + s\left(L'_p + r_sr_pC'_s\right) + r_p}{s^4\left(L'_pL'_sC'_pC'_s\left(1-k_{DM}{}^2\right)\right) + s^3\left(C'_pC'_s\left(L'_sr_p + L'_pr_s\right)\right) + s^2\left(L'_pC'_p + L'_sC'_s + r_pr_sC'_pC'_s\right) + s\left(r_pC'_p + r_sC'_s\right) + 1} \tag{2}$$

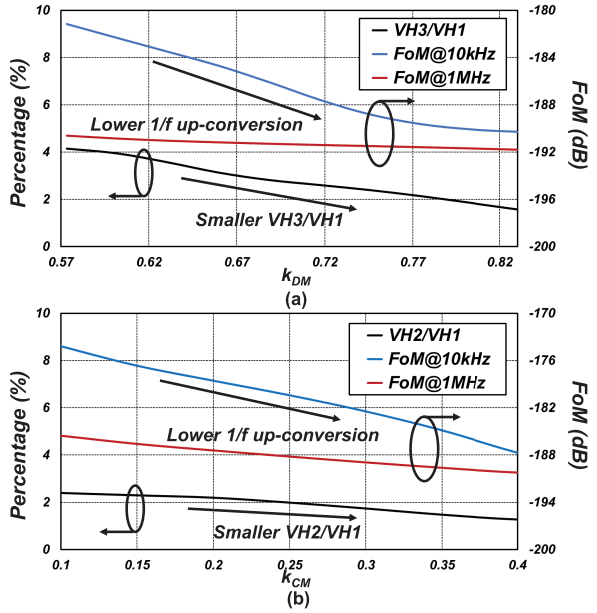

Fig. 3. Effect of (a) k_{DM}, and (b) k_{CM} on the third and second harmonic amplitude ratio to the fundamental, and the FoM@10 kHz and FoM@1 MHz.

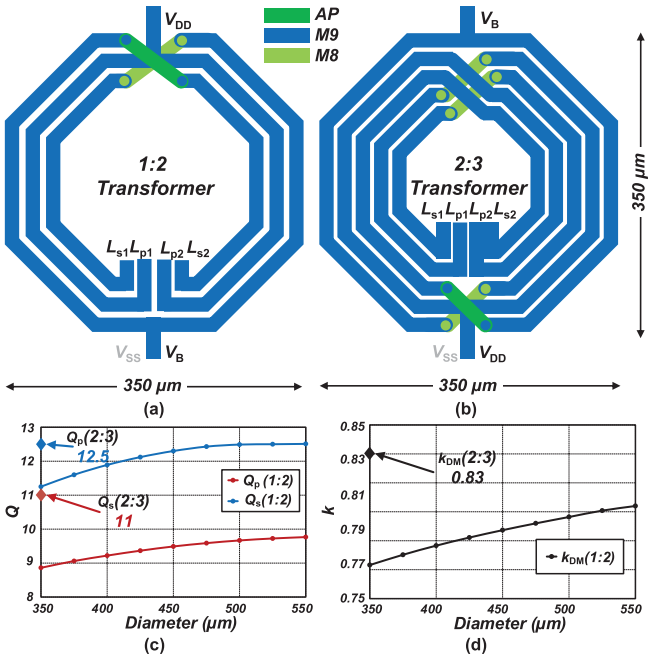

Fig. 4. Layout of (a) 1:2 and (b) 2:3 transformer for ~2.4 GHz resonance. One can visually discern tighter coupling through lower chances of magnetic field leakage between the coils in the 2:3 transformer. Simulated (c) Q_p, Q_s and (d) k_{DM} in the 1:2 transformer across different diameters and in the 2:3 transformer of 350 μm^2 diameter.

It can be observed that higher k_{DM} leads to a lower amplitude ratio, consequently resulting in better $1/f^3$ PN performance, thus better figure-of-merit (FoM)@10 kHz (located in the $1/f^3$ region). Similarly, higher k_{CM} reduces the second harmonic component in the drain voltage, causing weaker $1/f$ up-conversion, as shown in Fig. 3(b).

Obviously, the coupling factor can be increased by reducing the distance between the primary and secondary coils. This is, however, limited by the design rule check (DRC) rules of the CMOS process. Alternatively, the coupling factor can be further enhanced by increasing the coil turns ratio. Fig. 4(a) and (b) shows the commonly used 1:2 transformer and our 2:3 transformer, respectively. With the same size constraint of 350×350 μm^2, the 1:2 transformer achieves a smaller inductance than does the 2:3 transformer. Additionally, the higher turns ratio increases k_{CM} from 0.03 to 0.48 at 2.4 GHz. On the other hand, k_{DM} increases from 0.75 to 0.83. It can also be observed that larger k_{CM} can reduce the second harmonic CM resonance. The outer section of the two-turn primary coil L_p [see Fig. 4(b)] experiences the opposite direction of the CM current versus in the inner section of the coil. As it induces compensation between the inner and outer coils, the CM oscillation will be attenuated.

Fig. 5(a) and (b) shows a comparison between the theoretical and simulated DM and CM impedances, which includes: 1) EMX extracted S-parameter model; 2) EMX extracted complex circuit model; and 3) the simplified equivalent circuit model in Fig. 2(b) and (c). For the 2:3 transformer [Fig. 5(a) and (b)], the proposed model with an estimated tank capacitance shows a good correlation between the EMX circuit model and S-parameter model. Note that the S-parameter model includes the effect of the substrate parasitics and, thus, it results in a deteriorated, albeit more realistic, magnitude. Due to the higher number of turns, the 2:3 transformer benefits from the higher inductance and Q-factors at the constraint of same size. Q_p, Q_s, and k_{DM} are first simulated across different diameters of the 1:2 transformer in the range of 350–550μm, as shown in Fig. 4(c) and (d). With the diameter increase, Q_p and Q_s are slightly increasing but Q_p stays smaller than in the 2:3 transformer, while k_{DM} increases to 0.79 whereas k_{CM} maintains <0.05 because of the one coil turn. The effective transformer's Q is $(1 + X^2 + 2k_{DM})/(1/Q_p + X^2/Q_s)$, where $X = (L_sC_s)/(L_pC_p)$ [5]. Here, we use X ≈ 1, so that the $Q_{eff} \approx 2(1 + k_{DM})Q_pQ_s/(Q_p + Q_s)$. The higher k_{DM} in the 2:3 transformer increases the effective Q of the transformer to around 21.4, while in the 1:2 transformer it is 17.8.

To fairly compare the 1:2 and 2:3 transformers from the viewpoint of intrinsic impedance properties, in addition to the same-diameter (i.e., 350 μm) comparison, we also add a comparison point of the 1:2 transformer having the same L_p as does the 2:3 transformer (i.e., ~1.4 nH). The s-parameter model simulation results of these three transformers are shown in Fig. 5(c)–(e) where the tank's capacitance Q is set to 50 and the corresponding inductance and capacitance are shown in Table I. Each plot shows the fundamental, second, and third harmonic impedances over the TR of the fundamental peak at 2–2.8 GHz when the secondary tank capacitance is swept as shown in Table I. This is the range that matches with the real implementation of the coarse bank at the gate [see Fig. 10)]. With the same size, the 1:2 transformer has smaller k_{CM} and L_p which leads to a smaller fundamental impedance and higher CM impedance. For the similar L_p, the 1:2 transformer has ~2× smaller fundamental impedance and ~2× higher CM impedance due to k_{CM} of 0.03. For the second DM impedance, higher k_{DM} of 0.83 in the 2:3 transformer reduces it 1.2–1.5× compared to the 1:2 transformer with $k_{DM} = 0.79$. The

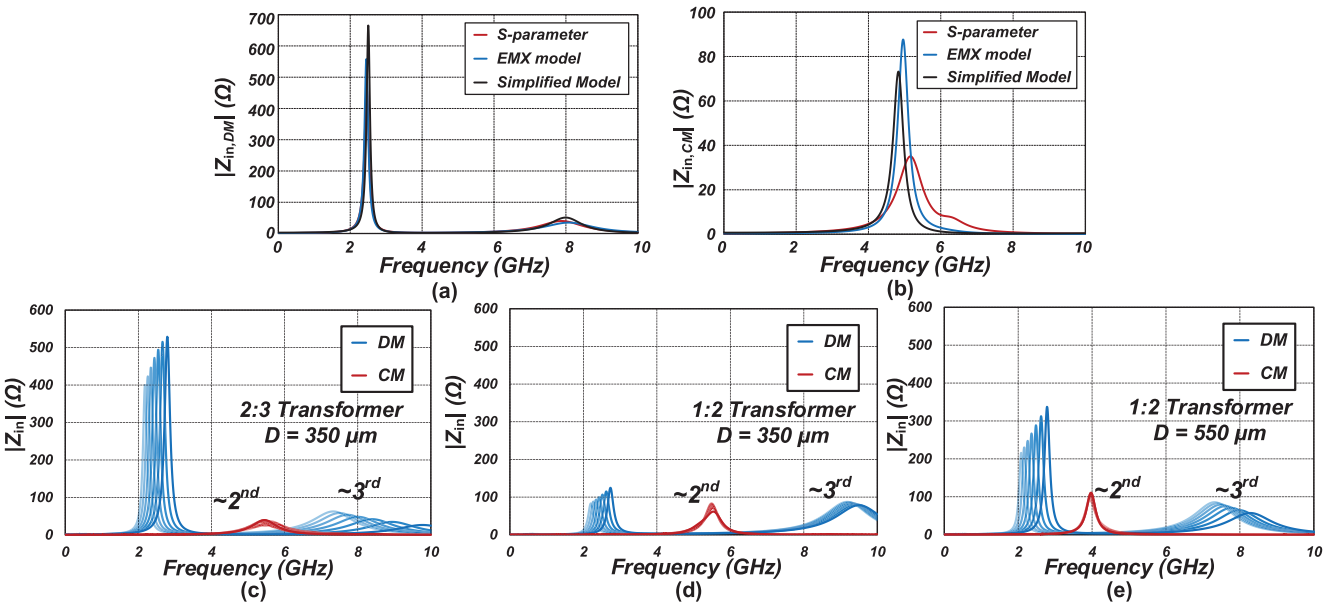

Fig. 5. Simulated Z_{in} with EMX-extracted S-parameter model, EMX circuit model, and proposed simplified model of the 2:3 transformer: (a) DM and (b) CM. (c)–(e) Comparison of Z_{in} between the 1:2 and 2:3 transformers at different diameters.

TABLE I
COMPARISON OF THE 1:2 AND 2:3 TRANSFORMER PARAMETERS

	2:3 Transformer (350μm)	1:2 Transformer (350μm)	1:2 Transformer (550μm)
L_p(nH)	1.44	0.75	1.47
L_s(nH)	2.65	1.59	3.24
C_p(pF)	1.1	1.1	1.1
C_s(pF)	0.2-0.9	1.6-2.0	0.8-1.6
Q_p	11	9.0	9.68
Q_s	12.5	11.2	11.57
k_{DM}	0.83	0.75	0.79
k_{CM}	0.48	0.03	0.03
SRF(GHz)	8.67	14.65	8.6

overall intrinsic second and third harmonics impedance ratio is, respectively, 4× and 2.4–3× smaller in the 2:3 transformer, which matches the impedance trend in (5) and (7) as discussed above.

B. Flicker Noise Up-Conversion in the Proposed Oscillator

The aforementioned 2:3 transformer is employed in the proposed oscillator operating at a 0.3 V supply. The simulated waveforms are shown in Fig. 6(a). Conduction angle of the drain current I_D is reduced to ∼1/3 when lowering the bias voltage V_B to 0.62 V. As compared with the higher V_B of 0.85 V in Fig. 6(b), the drain current shows smaller second and third harmonics. As shown in Fig. 6(c), the sinusoidal drain voltage V_D is of high spectral purity. Combined with the proposed transformer featuring low harmonic impedances, the second and third voltage harmonics are only 2.3% and 1.5% of the fundamental, respectively, which is instrumental in reducing the $1/f$ noise up-conversion caused by the modulation of these harmonics.

Following the study of flicker noise upconversion framework in [11], [13], [14], and [28], $1/f^3$ PN can be derived as:

$$\mathcal{L}_{1/f^3}(\Delta\omega) = \left(\frac{\sqrt{2}}{2\Delta\omega T_1}\int_0^{T_1} h_{DS}(t)\cdot I_{1/f,\mathrm{rms}}(t)dt\right)^2 \quad (8)$$

where $T_1 = 2\pi/\omega_1$ is the oscillator period, $h_{DS}(t)$ is the non-normalized impulse sensitivity function (ISF), and $I_{1/f,\mathrm{rms}}(t)$ is the periodically modulated rms value of flicker current noise. The $I_{1/f,\mathrm{rms}}(t)$ can be simulated through a NOISE simulation engine by setting the corresponding oscillation waveform [13], [14]; the results are shown in Fig. 6(d). Lower V_B narrows the conduction angle of $1/f$ current noise from approximately $T_1/2$ to $T_1/3$. The simulated h_{DS} reflects the phase response of V_{DS} against current impulse perturbations, as shown in Fig. 6(e). Thanks to the transformer with low harmonic impedance together with the reduction of the conduction angle of the cross-coupled pair when V_B is optimized at a lower value (e.g., $V_B = 0.62$ V), h_{DS} exhibits a near-sinusoidal response composed of balanced positive and negative regions. It can be observed that the highlighted "red" area in the middle shows a highly symmetric response, whereas the highlighted "blue" region near the peak/trough shows a relatively less symmetric shape. It can be observed from Fig. 6(d) that this is because the narrower conduction angle consequently limits the region where the $1/f$ current can inject. On the other hand, when higher V_B is applied, the cross-coupled pair is pushed into the triode region over a larger portion of about 1/3 of the period. This results in a distorted shape of h_{DS}. To elucidate the flicker noise conversion, the effective ISF ($h_{DS}\times I_{1/f,\mathrm{rms}}(t)$) is plotted in Fig. 6(f). From (8), it can be shown that when V_B is lowered to 0.62 V, the integrated effective ISF will be smaller, reflecting the reduced $1/f$ noise up-conversion. When V_B

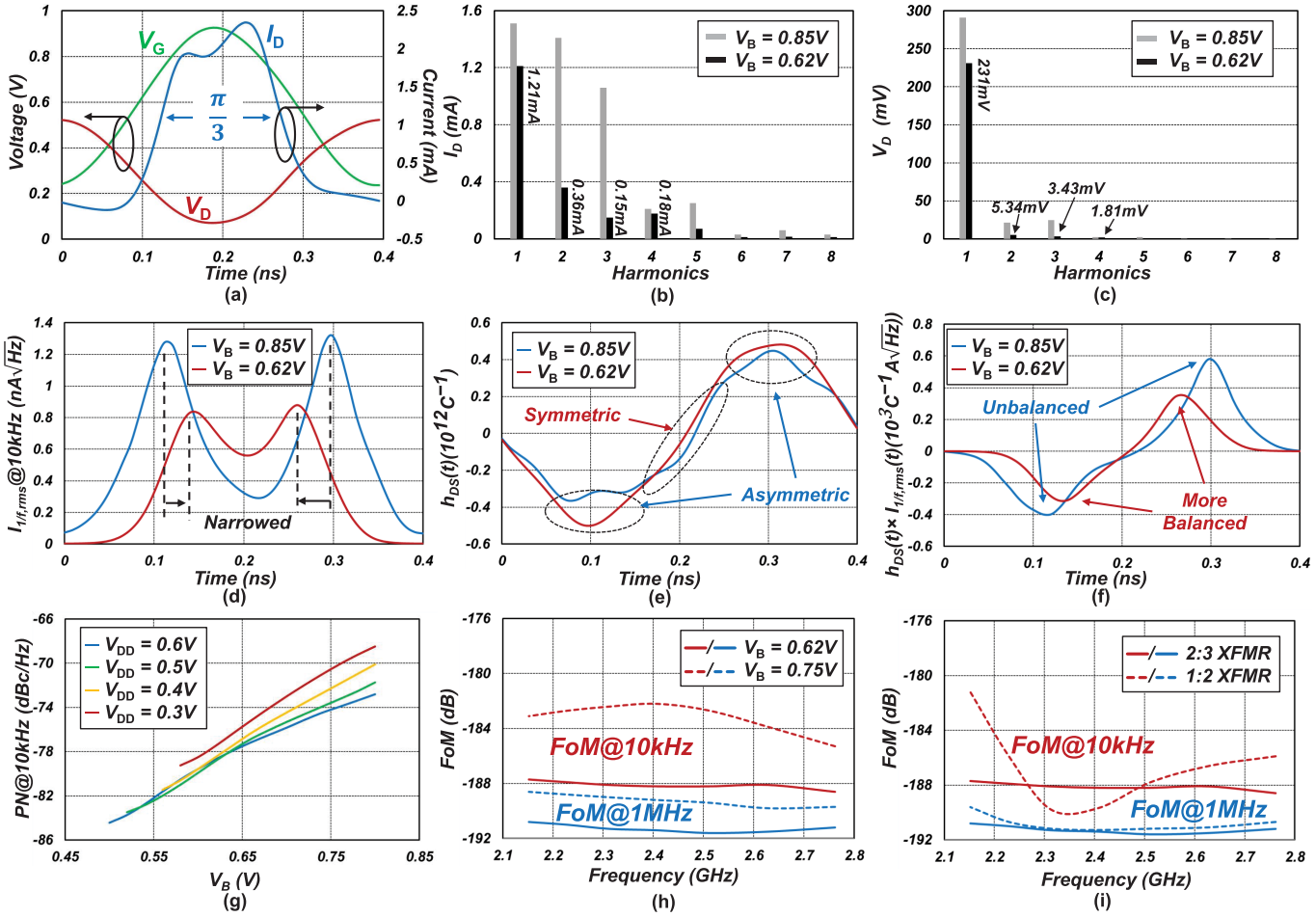

Fig. 6. (a) Simulated waveforms of V_G, V_D, and I_D when V_B=0.62 V. Spectral harmonics of (b) I_D and (c) V_D at different V_B. Time evolution plots of: (d) $1/f$ noise current intensity ($i_{1/f,\mathrm{rms}}$@10 kHz), (e) ISF transfer function h_{DS}, and (f) effective ISF ($h_{DS}\times i_{1/f,\mathrm{rms}}$@10 kHz) at different V_B at 0.3 V supply. (g) Simulated PN plots at 10 kHz versus V_B at different supply levels. (h) FoM@10 kHz and FoM@1 MHz versus carrier frequency when $V_B = 0.62$ V and $V_B = 0.75$ V and (i) comparison of FoM of 2:3 and 1:2 transformers versus carrier frequency, when V_B of 1:2 transformer is 0.62 V and V_B of 2:3 transformer is 0.65 V.

increases, the positive portion gets larger than the negative portion, which results in a higher $1/f$ up-conversion.

Fig. 6(g) shows the simulated PN at a 10 kHz offset, which represents the $1/f^3$ PN region. It can be observed that the proposed oscillator can operate at a low supply voltage of 0.3 V. In the $1/f^3$ region, as discussed in Section II, the $1/f$ noise up-conversion is mostly through the noise modulating into the unbalanced waveform. Additionally, by optimally lowering V_B, the $1/f^3$ PN at 10 kHz can get reduced (~8 dB), which further confirms the beneficial effects of narrowing the conduction angle. Fig. 6(h) shows the simulated FoM at 10 kHz and 1 MHz across the frequency TR when only changing the drain tank capacitance. With V_B set low at 0.62 V, FoM@10 kHz and FoM@1 MHz vary less than 2 dB across an entire >500 MHz TR. When V_B is increased to 0.75 V, both FoMs degrade and FoM@10 kHz varies 4 dB in the whole range.

To further quantify the benefits of the proposed 2:3 transformer in the targeted oscillator in Fig. 1, we compare its performance with that using the aforementioned 1:2 transformer of the 550×550 μm^2 size. Due to the lower Q_p, Q_s and k_{DM} of the latter, V_B needs to be raised from 0.62 to 0.65 V under the same 0.3 V supply, which increases the power consumption around 2×. Fig. 6(i) shows the FoM at 10 kHz and 1 MHz for both designs across the TR. FoM@1 MHz for the conventional transformer is slightly worse but FoM@10 kHz shows a large variation of as much as ~8 dB. This re-confirms the sensitivity of $1/f^3$ PN to the tank's capacitor ratio matching in the prior-art structures, such as [10], [11]. However, the proposed 2:3 transformer-based oscillator shows a much lower variation (<1.5 dB) of FoM@10 kHz with the tank's capacitance ratio. That proves that the proposed $1/f^3$ PN reduction technique offers more degrees of freedom and allows the tank's capacitance to be optimized for a larger TR.

III. Vertically Integrated Switched-Capacitor Banks and Special Arrangement for Native Layer

For Bluetooth applications, an LC-based oscillator usually occupies a large silicon area. Note that in the frequency region of 2.4 GHz, it is the passive components (inductors and sw-cap banks) that dominate the area. A 2.4 GHz oscillator designed in 28 nm CMOS requires at least 350 × 350 μm^2 to accommodate the 2:3 transformer used in this design with Q > 12. On the other hand, an additional significant area

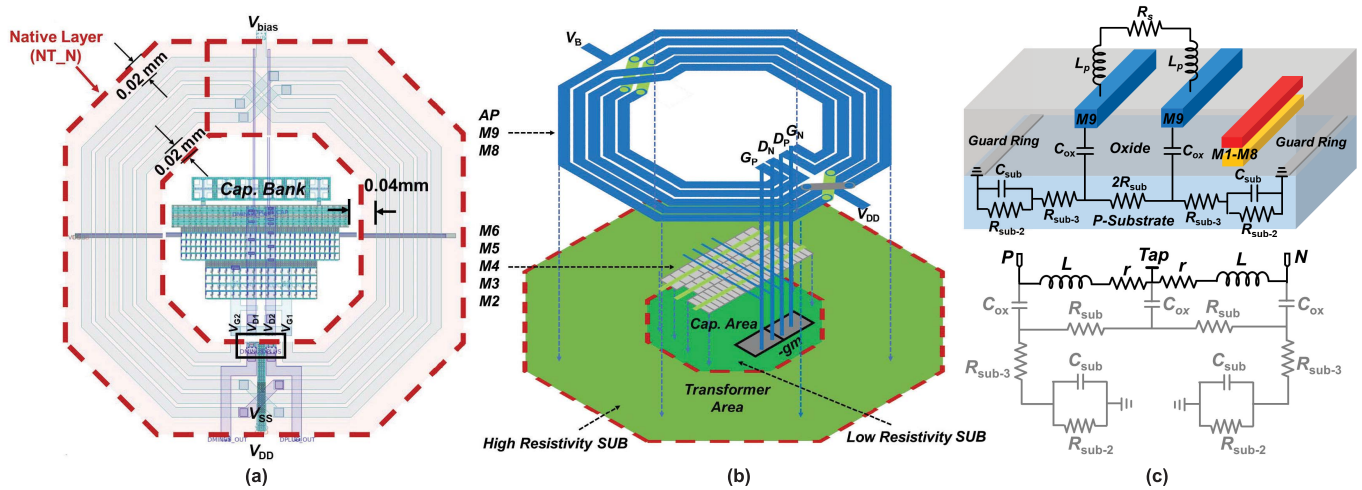

Fig. 7. Proposed ULV oscillator with vertically integrated sw-cap banks: (a) layout and (b) side view of the transformer and placement of the sw-cap banks. (c) Equivalent model of the transformer and substrate considering all parasitics.

must also be spent on the digitally controlled capacitor banks which can provide wide TR (e.g., 39%) with fine resolution (e.g., <10 kHz). The aforementioned capacitor banks would occupy an additional area of $100 \times 80\ \mu m^2$.

A. Vertically Integration of Sw-Cap Banks

To save the area of sw-caps, we propose that all the sw-cap banks and the cross-coupled pair are vertically integrated under the transformer coils. Therefore, the total area is kept at the aforementioned $350 \times 350\ \mu m^2$. However, the transformer carries a large ac current (several milliamp), generating strong electromagnetic (EM) fields around it. Any sensitive circuit located nearby could induce eddy currents, disturbing the operation of sensitive circuits, while the transformer's Q-factor itself will degrade due to large metal fragments near the coil [29]. Thus, in the proposed oscillator, the sw-cap banks are located in the center of the transformer with a gap up to 40 μm against the coils [see Fig. 7(a)], avoiding their direct electrical coupling to the utmost extent. The sw-cap banks are composed of nMOS switches and metal-oxide-metal (MOM) capacitors which are implemented by lower M2–M6 metal layers, while the layout is carefully considered, e.g., metal wires are made with the minimum width to reduce the degradation of the transformer Q-factor. Fig. 8(c) and (d) shows the simulated Q_p and Q_s of the transformer. The Q-factor drop is less than 1 when the sw-cap banks are placed in the middle of the transformer. This amount of Q degradation would be similar to the case when dummy metal pieces are placed inside the coil to meet the DRC rules. Since the sw-cap banks are mostly passive with a tiny switching current (~20 μA), the electric field induced by sw-cap banks is much weaker compared to that from the transformer.

B. Special Arrangement of Native Layer and Its EM Analysis

Fig. 7(a) and (b) shows the top view and the 3-D view of the proposed oscillator, respectively, where the sw-cap banks and active circuits are placed within the confines of the 2:3 transformer. In contrast to [2], the substrate underneath the transformer [highlighted as the light-green region in Fig. 7(b)] is covered by a native non-doping layer (i.e., "NT_N-layer), exhibiting high substrate resistivity of $>10\ \Omega \cdot cm$ [2] to reduce

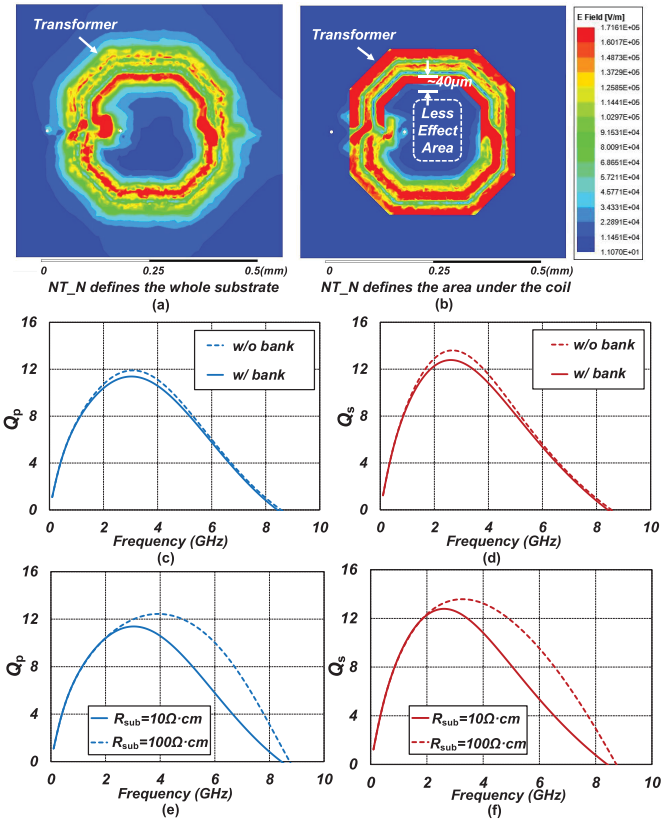

Fig. 8. Simulated electric field distribution with (a) NT_N-layer covering the whole substrate and (b) NT_N-layer covering the area underneath the transformer. Simulated Q-factor of the (c) primary and (d) secondary coils of the transformer with/without the sw-cap bank metal layers and (e) and (f) with different substrate resistivity.

[2]For a given CMOS technology, the resistivity of the non-doping substrate can be roughly estimated by comparing the simulated "Q-factors versus frequency" of a process design kit (PDK)'s inductor (covered by NT_N-layer) based on its Spectre model with that based on its EM extraction.

the eddy currents and to ultimately improve the transformer's Q factor. The area inside the transformer (not enveloped by the NT_N-layer, highlighted as the dark-green region) is defined as a normal substrate of low-resistivity (<10 Ω·cm, preventing latch-up [41]), accommodating the sw-cap banks and the cross-coupled pair for area savings. Specifically, the area of the special NT_N-layer is arranged with a 20 μm extension away from the coil, which can reduce the transformer coupling effect on the inner circuits by constraining the electric field within a specific region. The supplies to these banks are routed horizontally and fed in from both sides using a lower-level metal (M5). In the case of toggling the sw-cap banks in the targeted all-digital phase-locked loop (ADPLL), the simulated peak current of the entire sw-cap driver stage is only 50 μA, thus inducing a negligible electrical/magnetic field from such a thin metal to the transformer. As an example, the proposed oscillator has already been implemented as part of an ADPLL [30]. The measured reference spur is −60 dBc, which is still relatively low when compared with state-of-the-art without the use of vertical integration [31].

To verify the above explanation, simulations of the 3-D electric field distribution have been performed in Ansys HFSS, as shown in Fig. 8(a) and (b). We observe that the induced electric field is strong underneath the transformer region and gradually spreads outward through the substrate. Specifically, with the special "NT_N-layer definition, the substrate resistivity gap between the undoped and the doped regions confines the electric field propagation within the specified area. It becomes vanishing for the inner normal substrate region (i.e., ∼40 μm away from the coils), having little influence on the vertically-integrated sw-cap banks and the cross-coupled pair.

To further evaluate the effect of the substrate resistance on the Q-factor of the transformer, a simplified equivalent circuit model shown in Fig. 7(c) [32] is used.[3] The substrate resistance $2R_{\text{sub}}$ pertains to the area underneath the coils. Through the thick-oxide capacitance C_{ox}, it is connected in parallel with the inductors between the two ports P and N. The substrate under these two ports is connected to the ground tap through the ground guard ring located outside of the transformer. Hence, an $R-RC$ network is used to model the ground connection. The extra impedance Z_{par} caused by these parasitics (components highlighted in gray) between the two ports P and N can be calculated by the long (9) as shown at the bottom of this page. For simplicity, we assume $R_{\text{sub}-3}$ is much smaller than $R_{\text{sub}-2}$ and so we transfer Z_{par} in (9) into a form of $(1/(j\omega C_{\text{p}}+1/R_{\text{p}}))$, in which R_{p} and C_{p} represent the parallel equivalent resistance and capacitance. According to [32], [33], the Q-factor that considers the substrate effects can be derived as

$$Q=\frac{\omega L}{r}\cdot\frac{R_{\text{p}}}{R_{\text{p}}+\left[\left(\frac{\omega L}{r}\right)^2+1\right]r} \tag{10}$$

where R_{p} can be calculated from (9)

$$R_{\text{p}}=\frac{2(R_{\text{sub}-2}+R_{\text{sub}})}{\omega^2 R_{\text{sub}-2}R_{\text{sub}}C_{\text{ox}}^2}+\frac{2R_{\text{sub}-2}R_{\text{sub}}(C_{\text{sub}}+C_{\text{ox}})^2}{(R_{\text{sub}-2}+R_{\text{sub}})C_{\text{ox}}^2}. \tag{11}$$

We use $R_{\text{sub}}=kR_{\text{sub}-2}$ to simplify (11) as

$$R_{\text{p}}=\frac{2(1+k)}{\omega^2 kR_{\text{sub}-2}C_{\text{ox}}^2}+\frac{2kR_{\text{sub}-2}(C_{\text{sub}}+C_{\text{ox}})^2}{(1+k)C_{\text{ox}}^2}. \tag{12}$$

To improve the Q-factor in (10), R_{p} should be increased. From (12), R_{p} is composed of two parts, in which the first term is inversely proportional to $R_{\text{sub}-2}$ and the second term is proportional to $R_{\text{sub}-2}$. The demarcation point lies at

$$R'_{\text{sub}-2}=\frac{(1+k)}{\omega k(C_{\text{sub}}+C_{\text{ox}})}. \tag{13}$$

However, with an estimated $k=10$ at $\omega=2\pi\cdot 2.4\times$ GHz, C_{sub} should be much smaller than C_{ox} which is around 10 aF/μm^2. The transformer's metal area is around 20 000 μm^2 leading to C_{ox} of 200 fF, so the estimated value of $R'_{\text{sub}-2}$ should be ∼300 Ω. With several hundreds of micrometer across the transformer dimension, the substrate resistance is around several kiloohm so that R_{p} is dominated by the second term, which is in the region of being proportional to $R_{\text{sub}-2}$, as shown in Fig. 9. By using the NT_N high resistance doping layer, the increased $R_{\text{sub}-2}$ can improve the Q-factor of the transformer. Fig. 8(e) and (f) shows the simulated transformer's Q_{p} and Q_{s} with different substrate resistance. The 10× of resistance increase can improve the Q-factor by

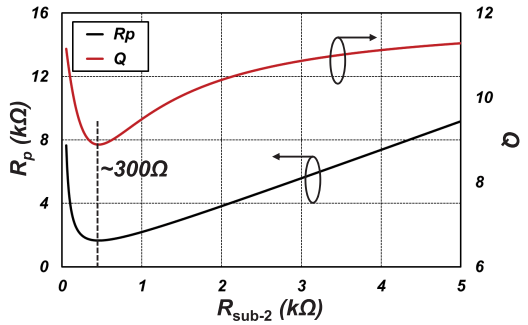

Fig. 9. Calculated R_{p} and Q versus the $R_{\text{sub}-2}$.

[3]The substrate resistive energy loss due to the magnetic coupling between the coils and substrate is neglected due to the high-resistivity of NT_N-defined substrate (i.e., by avoiding the eddy currents). Thus, the Q-degradation of the coils in the high-frequency range is mainly caused by the positive imaginary energy (magnetic energy) loss in capacitive parasitics (i.e., limited SRF of the coils, see Table I) and the substrate resistive energy loss by electrical coupling [41].

$$\begin{aligned}Z_{\text{par}}&=\frac{2}{j\omega C_{\text{ox}}}+(2R_{\text{sub}})\|\left[2\left(\frac{1}{j\omega C_{\text{sub}}}||R_{\text{sub}-2}\right)\right]\approx 2\frac{(R_{\text{sub}-2}+R_{\text{sub}})+j\omega R_{\text{sub}-2}R_{\text{sub}}(C_{\text{ox}}+C_{\text{sub}})}{j\omega(R_{\text{sub}-2}+R_{\text{sub}})C_{\text{ox}}-\omega^2 R_{\text{sub}-2}R_{\text{sub}}C_{\text{sub}}C_{\text{ox}}}\\&=2\frac{(R_{\text{sub}-2}+R_{\text{sub}})^2+\omega^2 {R_{\text{sub}-2}}^2{R_{\text{sub}}}^2(C_{\text{sub}}+C_{\text{ox}})^2}{\omega^2 R_{\text{sub}-2}R_{\text{sub}}(R_{\text{sub}-2}+R_{\text{sub}})C_{\text{ox}}^2+j\omega C_{\text{ox}}\left[(R_{\text{sub}-2}+R_{\text{sub}})^2+R_{\text{sub}-2}^2R_{\text{sub}}^2C_{\text{sub}}(C_{\text{sub}}+C_{\text{ox}})\right]}\end{aligned} \tag{9}$$

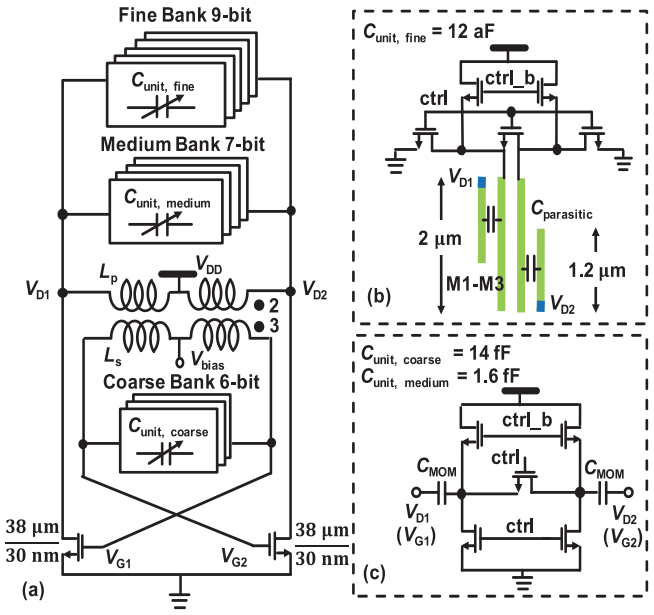

Fig. 10. Schematics of: (a) proposed DCO, (b) fine-bank cell, and (c) medium- and coarse-bank cell.

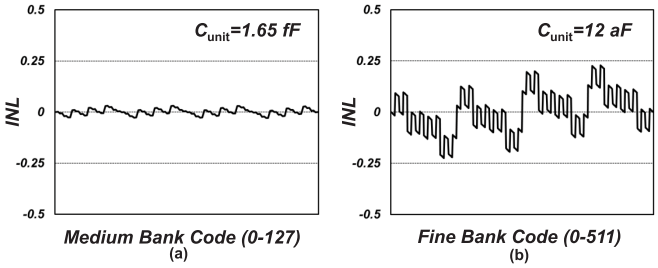

Fig. 11. Simulated INL of (a) medium bank and (b) fine bank.

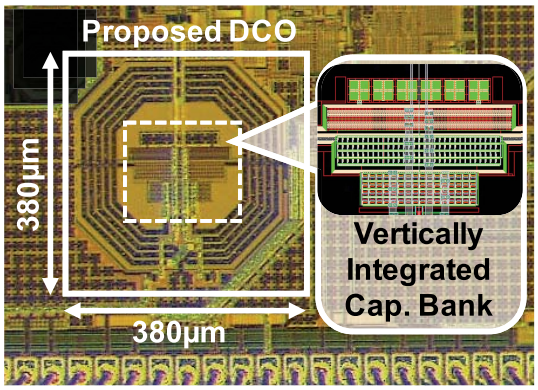

Fig. 12. Chip micrograph with zoomed-in layout of the sw-cap bank.

0.5–1 (i.e., 4%–8%). Note that in [2] and [3], PGS is adopted in which additional ground metal layers are placed to replace the high silicon resistance R_{sub-2} by the metal resistance R_m. Then, R_p is dominated by the first term which can increase by lowering R_m. However, the PGS induces an additional parallel capacitance, increasing C_{ox} to more than 500 fF, which will limit the tank TR. The increased C_{ox} also decreases R_p quadratically in the first term in (12), so that the reported improvement of Q-factor due to the PGS in [2] was only about 3%.

IV. Detailed Circuit Implementation

Fig. 10 shows a detailed schematic of the proposed DCO. It comprises the nMOS cross-coupled pair, the newly introduced high k_m 2:3 transformer, and three digital tuning capacitor banks. The 2:3 transformer is configured with its primary coil connected to the transistor drains and the secondary coil cross-connected to the gates. The 2:3 transformer provides a passive gain of ∼1.5 to boost up the resonating gate voltage, which helps with the oscillation startup at the ultralow supply voltage of 0.3 V. To allow integration in digital phase-locked loops (PLLs), the digitally controlled capacitor banks need to cover a wide range with fine resolution. To this effect, there are three switched-capacitor (sw-cap) banks composed of the coarse, medium, and fine banks. A 6-bit coarse sw-cap bank is placed at the gate tank, which magnifies the capacitance-to-frequency conversion ratio. On the other hand, the medium and fine sw-cap banks are connected to the drain tank. To avoid any dead zone in frequency tuning, the range of the 7-bit medium bank is set wider than two LSBs of the coarse bank, whereas the range of the 9-bit fine bank is wider than two LSBs of the medium bank. The capacitor cells in all banks are implemented with nMOS pull-up and pull-down devices as shown in Fig. 10(c) [34]. The binary medium and coarse banks are both using a MOM capacitor available from the PDK with an LSB capacitance of 1.6 and 14 fF, respectively. To avoid the PN limited by the quantization noise of the DCO in an ADPLL, an 8 kHz resolution of the fine bank is targeted. This corresponds to approximately tens of aF for an LSB unit cell. To support such high resolution, a custom-designed metal fringe capacitor (as MOM) is adopted in the binary fine bank. Taking advantage of the CMOS scaling in this 28-nm technology, M1–M3 metal strings of minimum width are used to constitute a capacitor with a unit capacitance of 12 aF. Each unit cell is surrounded by a ground guard ring to isolate it from the rest. The post-simulations with $R+C+CC$ extraction show $\Delta C = C_{on} - C_{off} = 12$ aF. The simulated integral nonlinearity (INL) of the medium and fine banks are less than +0.05/−0.05 LSB and +0.25/−0.25 LSB, respectively, as summarized in Fig. 11. Since the design of the sw-cap banks is fully passive, it consumes less than 50 μA. Therefore, an ultralow-power dc-dc converter can readily boost the 0.2–0.3 V supply to the desired (i.e., sufficiently above V_{th}) level with a minimal effect on the overall FoM (less than 1 percent change) [6], [35].

V. Measurement Results

The proposed DCO, which was designed for ULV, wide TR, low area, and low $1/f^3$ PN operation, is implemented in TSMC 28-nm low-power (LP) CMOS. Fig. 12 shows its chip microphotograph. The whole DCO has been squeezed in a compact area of 0.38×0.38 mm^2. This includes three sw-cap banks, decoupling capacitors for the sw-cap bank supply, and the cross-coupled pair, which are all vertically integrated within the confines of the transformer.

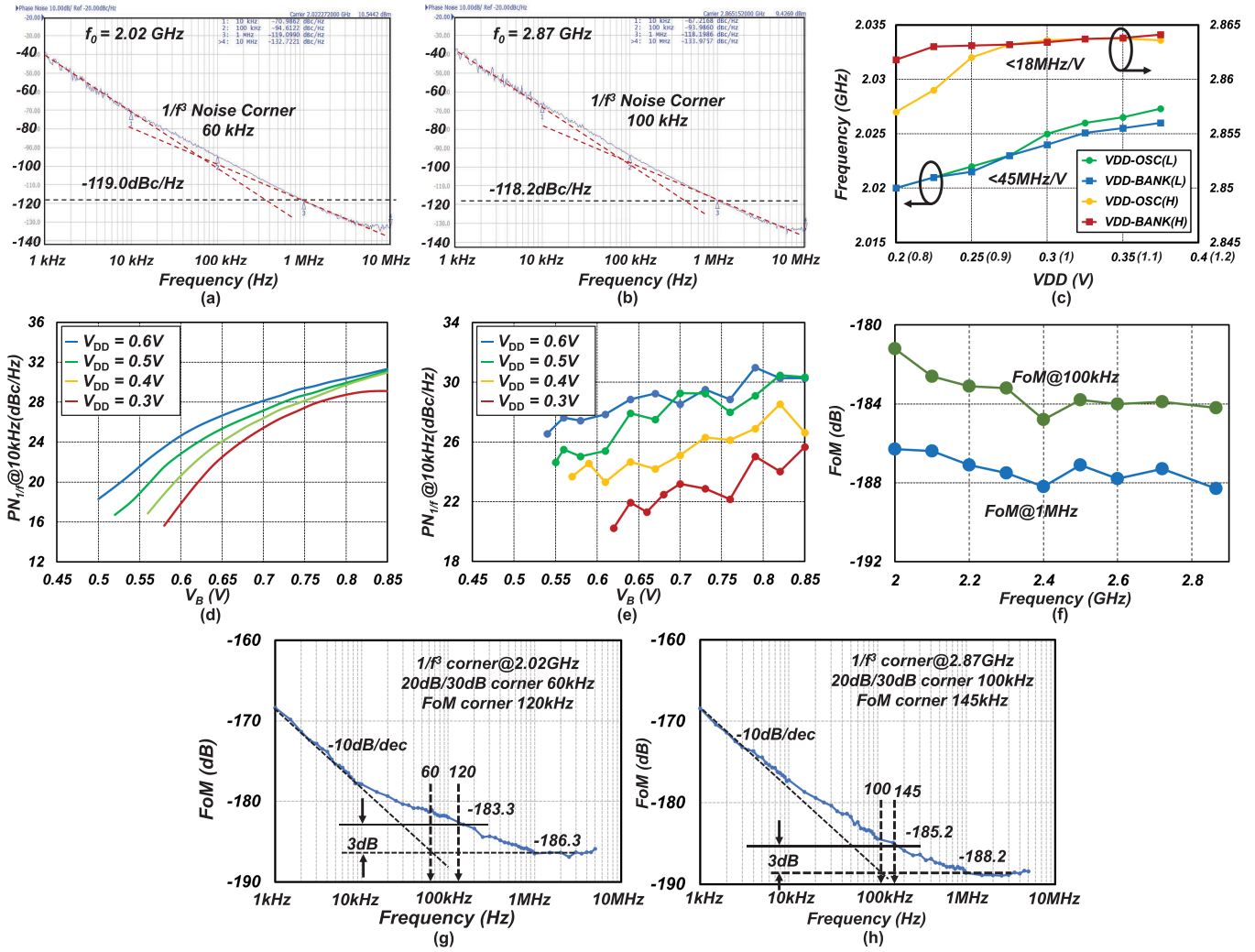

Fig. 13. Measured PN plots at (a) 2.02 GHz and (b) 2.87 GHz. (c) Measured frequency pushing characteristic of the oscillator/capacitor bank supply. (d) Post-layout simulated $\mathrm{PN}_{1/f}$@10 kHz and (e) measured $\mathrm{PN}_{1/f}$@10 kHz. (f) Measured FoM@100 kHz and FoM@10 MHz in the entire frequency TR. FoM versus offset frequency when oscillating at (g) 2.02 GHz and (h) 2.87 GHz.

The PN was measured by Keysight E5052B Signal Source Analyzer. At a 0.3 V supply, the measured PN is plotted in Fig. 13(a) and (b) at two extremes of the measured TR of 35% (2.02–2.87 GHz). The PN at a 1 MHz frequency offset achieves −119 dBc/Hz at 2.02 GHz and −118 dBc/Hz at 2.87 GHz. The measured frequency TR of the coarse and medium banks are 760 and 90 MHz, respectively. On the other hand, the 9-bit fine bank achieves 8 kHz resolution. At the carrier frequency of 2.4 GHz, the DCO achieves −95.9 dBc/Hz and −119.3 dBc/Hz PN at 100 kHz and 1 MHz offsets, respectively, while consuming 0.75 mW under the 0.3 V supply. Fig. 13(c) shows the effect of supply voltage variation on the generated frequency. Within the 0.25–0.35 V supply voltage sweep, the DCO frequency is pushed by <18 MHz/V at the lowest frequency and <45 MHz at the highest frequency when changing the oscillator supply (0.25–0.35 V) or the sw-cap bank supply (0.9–1.1 V), which is comparable to the best-in-class [6] and [38] and suitable for integration with energy harvesters.

To benchmark the oscillator flicker PN performance, one of the most popular methods is to compare the $1/f^3$ PN corner, which is a frequency at the intersection point of the −30 and −20 dB/dec regions. Unfortunately, the ease and accuracy of the $1/f^3$ corner estimation is limited as it is usually derived from a graphical PN plot. To evaluate the $1/f$ noise up-conversion effect more quantitatively [11], here we use the following PN excess metric:

$$\mathrm{PN}_{1/f}@10\ \mathrm{kHz} = \mathrm{PN}@10\ \mathrm{kHz} - \mathrm{PN}@10\ \mathrm{MHz} - 60\ \mathrm{dB} \tag{14}$$

to reflect only the $1/f$ noise up-conversion while removing the thermal noise up-conversion in the $1/f^3$ region.

Fig. 13(d) shows the simulated $\mathrm{PN}_{1/f}$@10 kHz versus V_B under different supply voltages, V_DD. It can be ascertained that lower V_B reduces the conduction angle which limits the exposure to the asymmetric ISF region, leading to a weaker $1/f$ noise up-conversion and thus smaller $\mathrm{PN}_{1/f}$@10 kHz. This trend is confirmed by the measured $\mathrm{PN}_{1/f}$@10 kHz shown in Fig. 13(e). With a reduction of V_B from 0.85 to 0.62 V, $\mathrm{PN}_{1/f}$@10 kHz can be reduced by 4 dB, which matches with the simulation results. Consequently, both the simula-

TABLE II
COMPARISON TABLE OF STATE-OF-THE-ART OSCILLATORS WITH SUPPLY VOLTAGE $\leq$0.6 V

	This Work	ISSCC'19 [36]	ISSCC'18 [37]	ISSCC'17 [6]	VLSI'09 [39]	RFIC'19 [40]	JSSC'05 [4]	RFIC'15 [38]	JSSC'18 [25]
Technology	28nm	22nm	28nm	16nm	180nm	22nm	180nm	40nm	65nm
Topology	Inverse-Class-CF_{23}	Folded, 4-Winding Transformer	Gate-to-Source Transformer	Trifilar-Coil	Dual Class-C	4-port resonator	Drain-to-Source Transformer	Switching Current Source	Inverse Class-F
V_{DD} (V)	0.2/0.3	0.1/0.2	0.2	0.2	0.2/0.3	0.35	0.5	0.5	0.6
Power (mW)	0.44/0.75	0.54/2.28	0.67	0.6	0.114/0.16	0.44	0.57	0.48	1.2
Frequency(GHz) (TR%)	2.02-2.86 **(35%)**	4.15-4.97 (18%)	2.24-2.6 (14.9%)	3.2-4.0 (22%)	4.5 (N/A)	4.06-4.96 (20%)	3.8 (8.4%)	4.0 (22%)	3.49-4.51 (25.5%)
PN@100kHz (dBc/Hz)	-92/-95.9	-92.3/-96.1	-95	-88	-79/-84	-93.1/-91.6	N/A	-89	-102.4/-98.5
PN@1MHz (dBc/Hz)	-115.1/-119.3	-113/121.9	-119	-114	-104/-109	-115.6/-116.6	-119	-114	-125.6/-123.7
FoM@100kHz (dB)	-183.3/-184.8	-188/-188.3	-184	-182	-182/-185	-189/-189.2	NA	-184	-192.5/-191
FoM@1MHz (dB)	-186.3/-188.1	-190.8/-193.4	-188	-188	-187/-190	-192/-195.5	-193	-189	-195.6/-196.2
FoM_T@100kHz (dB)	**-194.2/-195.6**	-193.1/-193.4	-186	-186	NA	-195/-195.2	NA	-190	-200.6/-199
FoM_T@1MHz (dB)	**-197.1/-199**	-195.9/-198.5	-190	-195	NA	-198/-201.2	-191	-195	-203.7/-204.3
$1/f^3$ Corner (kHz)	**60-100**	50-700	150	100-150	400	100-250	NA	400	100-300
Area (mm^2)	0.14	0.27	0.15	0.11	0.29	0.19	0.76	0.14	0.14
Freq. Pushing (MHz/V)	**18/45**	40	29.7	38.2	NA	80	NA	17	15

FoM=PN-20log($f_0/\Delta f$)+10log(P_{DC}(mW)), FoM_T=PN-20log(($f_0/\Delta f$)(TR/10))+10log(P_{DC}(mW))

tions and measurements quantitatively prove that reducing the conduction angle is beneficial for mitigating the $1/f$ noise up-conversion. Moreover, thanks to the new 2:3 transformer, the proposed ULV DCO achieves an FoM of -185 dB at a 100 kHz offset and -188.1 dB at a 1 MHz offset while this performance can be maintained within 3 dB across the entire TR without resorting to any other tuning mechanism [see Fig. 13(f)]. The FoM versus offset frequency is plotted in Fig. 13(g) and (h) at the lowest and highest frequencies. By graphically finding the point on the PN plot that is 3 dB worse than FoM@1 MHz, thus defined as "FoM $1/f^3$ corner" [it is higher than the conventionally defined "20-dB/30-dB $1/f^3$ corner" frequency which is 60–100 kHz shown in Fig. 13(a) and (b)], it achieves a leading number of 120–145 kHz when compared with [4], [6], [25], [36]–[40] in Table II, which also shows the leading FoM_T@100 kHz. The proposed DCO also has the ability to operate under a 0.2 V supply while consuming 42% less power but at a cost of only $<$2 dB degradation in FoM_T.

VI. CONCLUSION

In this article, we introduced a new class of oscillators, inverse-class-F_{23}, designed for an ULV operation at 0.2–0.3 V with a wide TR of 35%. The second and third harmonic voltages are significantly suppressed by the proposed 2:3 transformer with a high-coupling factor in both common and differential modes, improving the waveform symmetry and suppressing the flicker PN without requiring precise tuning of harmonic resonances. At the same time, the passive gain of the proposed 2:3 transformer helps with the startup in the ULV regime. Its area of 0.14 mm^2 is very compact by means of vertically integrating all active devices underneath its transformer windings, with judicious use of the native non-doping layer to mitigate its impact on performance. The PN figure-of-merit (FoM) is among the best-in-class among low-supply oscillators, while its FoM normalized to the TR (FoM_T) of -195.6 dB is the best reported for the ULV oscillators operating at a supply voltage $<$0.5 V. Together with the reduced current conduction angle, the proposed inverse-class-F_{23} DCO achieves a low $1/f^3$ noise corner of 60 kHz. The low $1/f^3$ corner can be maintained within 100 kHz over the whole TR without any tuning mechanism.

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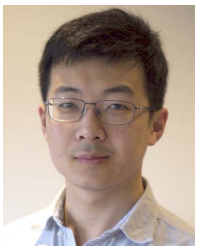

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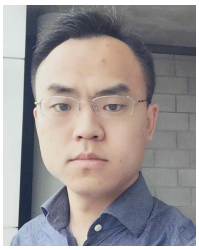

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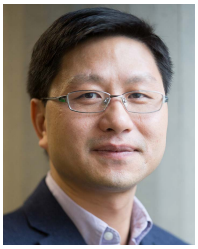

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