Introduction to the Special Section on the 2021 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS Special Section of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to a collection of the best articles selected from the 2021 IEEE International Solid-State Circuits Conference (ISSCC) that took place on February 13–22, 2021, in San Francisco, CA, USA. This Special Section covers articles from the Wireline, Digital Circuits, Digital Architectures and Systems (DASs), Machine Learning and AI, and Memory Committees.

II. Wireline Articles

Our wireline selection includes a mix of industry and university papers on transmitters and receivers that push the state of the art in speed and power efficiency. On the transmit side, the trend of doubling the link data rates continued at ISSCC 2021 by the introduction of the first 224-Gb/s PAM4 transmitter in 10-nm FinFET and a 200-Gb/s PAM4 transmitter in 28 nm. This Special Section includes an extended version of both papers with more details on implementation and measurement data. The 224-Gb/s transmitter, designed by Intel, incorporates a digital-to-analog converter, an 8-tap feed-forward equalizer (FFE), and a quarter-rate output driver. The 200-Gb/s transmitter designed at the University of California at Berkeley, on the other hand, deploys a segmented driver architecture with reconfigurable FFE taps.

On the receive side, this section includes a complete 112-Gb/s PAM4 receiver, designed in a 7-nm FinFET by Huawei, and a 100-Gb/s PAM4 optical receiver in 28-nm CMOS by Intel. While the former implementation is an analog to digital converter (ADC)/digital signal processing (DSP)-based system, the latter design deploys sample-and-hold circuits, analog FFE, and direct decision feedback equalizer (DFE) to achieve the desired performance. The 112-Gb/s paper, in particular, pushes the state of the art in DFE design for ADC-based systems by demonstrating a 9-tap sliding DFE.

Finally, this section includes a 56-Gb/s NRZ receiver in a 28-nm process. The receiver, designed at the University of California at Los Angeles, deploys a number of feed-forward and feedback loops in the front-end to extend front-end bandwidth and equalization capabilities, and achieve a very good power efficiency in a relatively slow process.

III. Digital Circuits Articles

Four articles have been selected from digital circuits sessions. The first article by Yoon *et al.* presents a 64-Kb compute-in-memory (CIM) macro testchip fabricated in 40-nm CMOS and RRAM process. It achieves a peak energy efficiency of 56.67 TOPS/W while demonstrating the 8-bitline hybrid CIM/digital MAC operation with 1–8 b inputs and weights, and 20 b outputs without quantization. The second article by Zhang *et al.* presents a fractional-N digital multiplying delay-locked loop (MDLL) that employs a digital-to-time converter to control the reference injection for the fractional-N operation. The MDLL prototype fabricated in 65-nm CMOS achieves −60 dBc fractional spur and 1.67-ps rms jitter at around 20-MHz offset. The third article by Huang *et al.* presents a single inductor multiple output (SIMO) converter with dynamic droop allocation and adaptive clocking. These techniques implemented on an integrated 4-domain SIMO System on Chip (SoC) in 65-nm CMOS show total system power reduction of 31%. The fourth article by Liu *et al.* proposes a dynamic voltage-stacking scheme, which supports two operating modes: a flat mode in the normal state and a stack mode in the sleep state. The measurements show that compared with the conventional flat architecture, the dynamic voltage-stacking scheme reduces the sleep current by 32.3% under the same circumstances, and it also improves ULPMark-CP score by 23.6%, which is higher than the top1 in the ULPMark score list.

IV. Digital Architectures and Systems Articles

In the DAS category, five articles from two sessions have been selected. The first article by Matsubara *et al.* presents a 12-nm autonomous driving SoC featuring a convolutional neural network achieving 60.4 TOPS at 13.8 TOPS/W, combined with task-separated Automotive Safety Integration Level D (ASIL-D) control. The second article by Rossi *et al.* showcases a wide-dynamic-range IoT SoC, achieving a combination of 1.7 μW state-retentive sleep power and a peak-performance of 32 GOPS at 1.3 TOPS/W efficiency. The third article by Schmidt *et al.* presents an 8-core RISC-V-based SoC designed entirely using an agile design methodology where a generator-based design-flow enables a small-design team to achieve silicon success with a complex 1.44 GHz, multi-core 1.125 M-gate mixed-signal SoC. The fourth article by Taneja *et al.* describes a novel unified true random number generator (TRNG) and physically unclonable function (PUF) architecture using a 16-Kb SRAM achieving 3.6-Mb/s TRNG throughput and 1.78%–3.84% PUF BER in 28-nm CMOS. The fifth article by Ghosh *et al.* describes an AES256 architecture with a digital signal attenuation circuit and a time-varying transfer function, improving security by 25% over existing work.

V. Machine Learning Articles

Two articles from the machine learning sessions of ISSCC 2021 have been selected. The first article by Lee *et al.* presents a 7-nm 4-core AI chip that offers four types of mixed

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precision computation to support diverse application demands for training and inference. Workload-aware clock throttling is used to maximize performance within a given power budget. The AI chip demonstrates up to 3.5 TFLOPS/W and up to 25.6 TFLOPS for hybrid-FP8 iso-accuracy training, and up to 16 TOPS/W and 102 TOPS for INT4 iso-accuracy inference. The second article by Jia *et al.* describes a scalable neural-network inference accelerator with a 4 × 4 array of programmable cores combining precise mixed-signal capacitor-based in-memory computing with digital single instruction multiple data (SIMD) near-memory computing. The accelerator is fabricated in 16-nm CMOS technology and achieves peak MAC-level throughput of 3 TOPS and peak MAC-level energy efficiency of 30 TOPS/W, both for 8-b operations. An 11-layer CNN and ResNet-50 are executed on the accelerator, achieving accuracy, throughput, and energy efficiency of 91.51% and 73.33%, 7815 and 581 image/s, 51.5 and 3.0 K image/s/W, with 4-b weights and activations, respectively.

VI. Memory Articles

From memory sessions, three cutting-edge articles have been selected for this Special Section. The first article by Kang *et al.* presents a GDDR6 DRAM with a half-rate daisy-chain-based write clock (WCK) tree. An 8-Gb chip fabricated in 1y-nm DRAM process achieves 24-Gb/s/pin bandwidth. Second, an article by Hollis *et al.* demonstrates an 8-Gb GDDR6X DRAM that features a PAM-4 encoded, single-ended memory interface to double the per-pin bandwidth for a given data-clock and delivers 22 Gb/s/pin. The third article by Song *et al.* describes a 3-nm GAA SRAM array design that increases transistor sizing flexibility compared to a FinFET technology which improves read margin. Write assist techniques are also introduced and improve V_{min} by 230 mV.

Amir Amirkhany
Samsung Display America Lab
San Jose, CA 95134 USA

Tanay Karnik
Intel Labs, Intel Corporation
Hillsboro, OR 97124 USA

Shidhartha Das
Arm Ltd.
Cambridge CB1 9NJ, U.K.

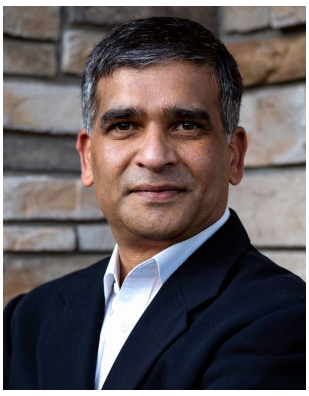
Jun Deguchi
Institute of Memory Research and Development
Kioxia Corporation
Kawasaki 212-0013, Japan

Yasuhiko Taito
Memory IP Technology Department 1
Renesas Electronics Corporation
Kodaira 187-8588, Japan

Amir Amirkhany (Senior Member, IEEE) received the B.S. degree from the Sharif University of Technology, Tehran, Iran, in 1995, the M.Sc. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2001, and the Ph.D. degree from Stanford University, Stanford, CA, USA, all in electrical engineering, in 2008.

He is the Head of Samsung Display America Laboratory, San Jose, CA, USA. In this capacity, he manages all research and development work for Samsung Display Company (SDC), Bay Area, CA, USA. Prior to Samsung, he was with Rambus Inc., Sunnyvale, CA, USA, where he led the development of proprietary high-speed memory interfaces. He has authored or coauthored over 25 IEEE publications. He holds over 50 issued patents.

Dr. Amirkhany was a recipient of several IEEE and Samsung Best Paper Awards.



Tanay Karnik (Fellow, IEEE) received the Ph.D. degree in computer engineering from the University of Illinois at Urbana–Champaign (UIUC), Urbana, IL, USA, in 1995.

He joined Intel, Hillsboro, OR, USA, in 1995. He was the Director of Intel's University Research Office, Hillsboro. He is a Senior Principal Engineer and the Director of the Heterogeneous Platforms Laboratory at Intel Laboratories. His research interests are in the areas of heterogeneous integration, small form factor systems, 3-D architectures, variation tolerance, power delivery, and architectures for novel devices.

Dr. Karnik was a member of the IEEE International Solid-State Circuits Conference (ISSCC), Design Automation Conference (DAC), International Conference on Computer Aided Design (ICCAD), International Conference on Integrated Circuit Design and Technology (ICICDT), International Symposium on Very Large Scale Integration (ISVLSI), International Symposium on Circuits and Systems (ISCAS), 3-D Integrated Circuits (3DIC), and International Symposium on Quality Electronic Design (ISQED) program committees and IEEE Journal of Solid-State Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, and IEEE Transactions on Circuits and

SYSTEMS review committees. He is an ISQED Fellow. He received an Intel Achievement Award for the pioneering work on integrated power delivery. He has presented several keynotes, invited talks, and tutorials, and has served on seven Ph.D. students' committees. He was the General Chair of International Symposium on Low Power Electronic Design (ISLPED) in 2014, Asian Symposium on Quality Electronic Design (ASQED) in 2010, ISQED in 2009, ISQED in 2008, and ICICDT in 2008. He is an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, a Senior Advisory Board Member of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, and a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Shidhartha Das received the M.Sc. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 2003 and 2009, respectively.

He is currently a Distinguished Engineer with Arm Ltd., Cambridge, U.K., where he conducts research on high-performance CPU design, focusing on circuits/micro-architectural techniques for power delivery and variation mitigation. He holds 58 granted U.S. patents and several more that are pending.

Dr. Das has received multiple best paper awards and his research has been featured in *IEEE Spectrum*. In the past, he has contributed to multiple areas of technology development, including mixed-signal architectures for machine-learning acceleration and emerging nonvolatile memories for which he received the Arm Inventor of the Year Award in 2016.

Jun Deguchi (Member, IEEE) received the B.E. and M.E. degrees in machine intelligence and systems engineering and the Ph.D. degree in bioengineering and robotics from Tohoku University, Sendai, Japan, in 2001, 2003, and 2006, respectively.

In 2004, he was a Visiting Scholar at the University of California at Santa Cruz, Santa Cruz, CA, USA. In 2006, he joined Toshiba Corporation, Kawasaki, Japan, where he was involved in the design of analog/RF circuits for wireless communications, CMOS image sensors, high-speed I/O, and accelerators for deep learning. From 2014 to 2015, he was a Visiting Scientist at the MIT Media Laboratory, Cambridge, MA, USA, and was involved in research on brain/neuroscience. In 2017, he moved to Kioxia Corporation (formerly Toshiba Memory Corporation), Kawasaki, and has been a Research Lead of an Advanced Circuit Design Team working on high-speed I/O and deep learning/in-memory accelerators.

Dr. Deguchi has been a member of the International Technical Program Committee (TPC) of IEEE International Solid-State Circuits Conference (ISSCC) since 2016, and IEEE Asian Solid-State Circuits Conference (A-SSCC) since 2017. He has served as a TPC Vice-Chair of IEEE A-SSCC in 2019 and a Review Committee Member of the IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS) 2020.

Yasuhiko Taito received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 1991 and 1993, respectively.

In 1993, he joined Mitsubishi Electric Corporation, Itami, Japan, and was engaged in the design of NOR and DINOR flash memories. He was also involved in commodity and embedded DRAM design. He developed embedded DRAM macros for System on Chip (SoC) with a high-speed SRAM interface. After transferring to Renesas Technology Corporation, Itami, in 2003 and Renesas Electronics Corporation, Tokyo, in 2010, he had been actively working on the development of embedded NOR and SG-MONOS (split-gate MONOS) flash macro development mainly for high-end automotive MCUs. He is currently a Principal Engineer with the Memory IP Technology Department 1, Renesas Electronics Corporation, and heading the projects of advanced embedded nonvolatile memories for automotive and IoT/consumer MCU products.

Mr. Taito has been serving as a Technical Program Committee Member for the IEEE International Solid-State Circuits Conference (ISSCC) since 2018. He served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2021.